Preparation of slab production in Japan

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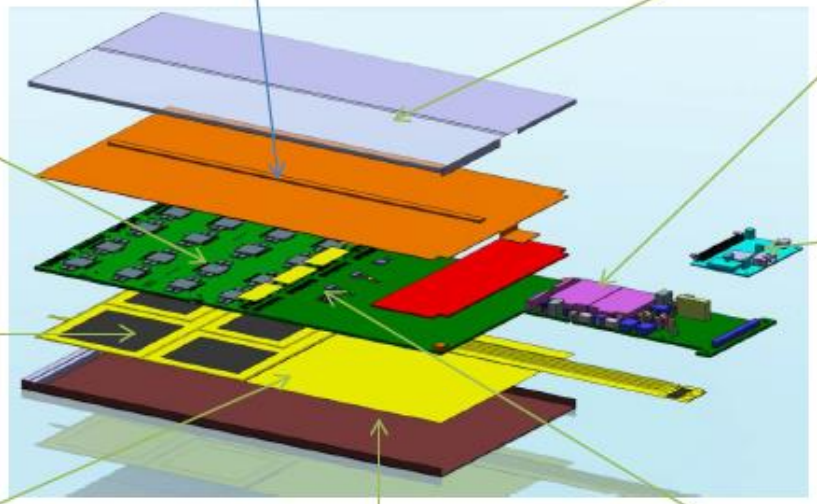
Production in Japan - Targets

- Optimization of production/test method
  - Benefits from Japanese industry
    - PCB, FPC, dispenser, …
    - We have close connections to design companies
      - (instead of work by in-house engineers in Europe)
- Quick studies in Japan by having more slabs
  - Firmware development
  - Development of test stands
    (ASIC, slab with RI, cosmic, …)
- Get more slabs by production at multi-sites
- Investigate optimal price

Breakup of a short slab



Coper sheet for cooling

Cover (EMI shielding)

Power pulsing circuitry (400 mF)

PCB 1024 chn. 16x **SKIROC2**

Detector Interface (DIF)

Si PIN diodes

Front-end, DAQ, TFC Not shown

HV kapton

A "short SLAB"

FCC Interconnects

Stiffener, Absorber Carbon fiber + W

Single layer, 'U' stiffener

KYUSHU UNIVERSITY

tokyo

LPNHE

LPSC Grenoble

Breakup of a short slab (cont.)

- Sensors by HPK
- FEV with SKIROC2(A)
- Gluing sensor to FEV
- SMB board (adapter to DIF) and interconnection
- FPC (Kapton) for bias (and gluing them)
- Copper sheet and cover
- Stiffener
- DIF

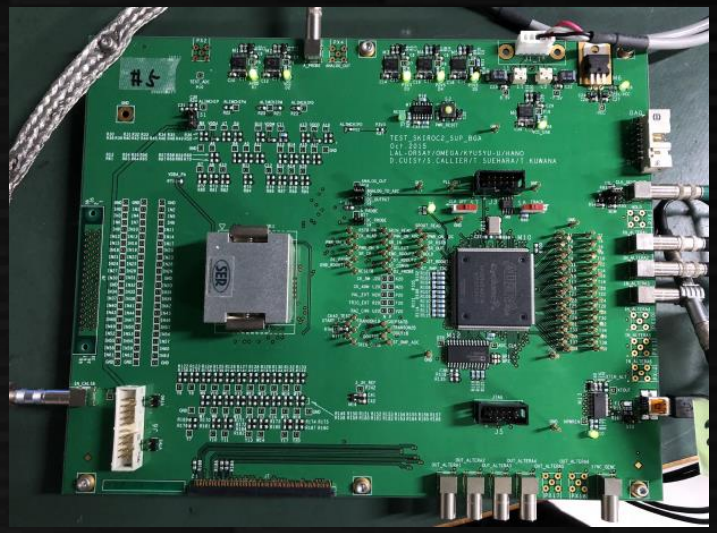
Sensor production

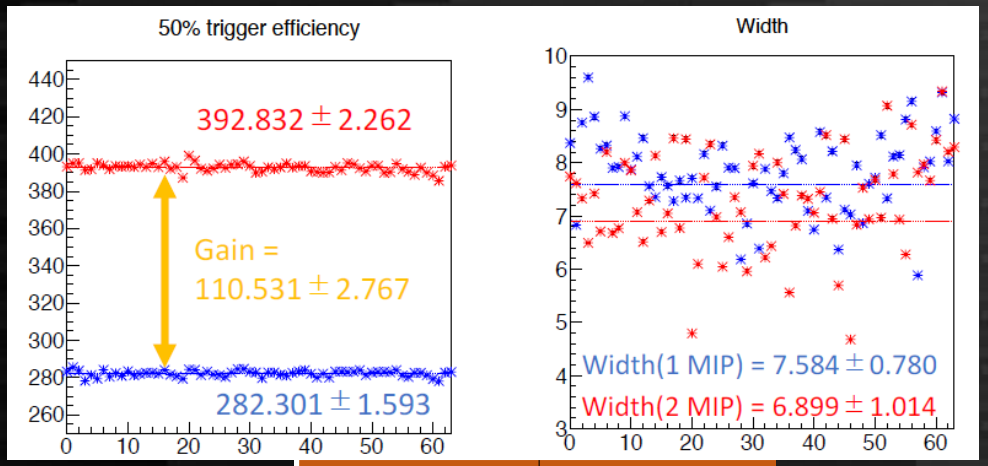
- An order of 24 sensors has been placed
  - Delivery estimation: mid March
  - 650 μm, expected full depletion at ~ 120 V
  - 5 to LLR, 19 kept in Kyushu
    (16 for slabs, 3 for backup & sensor studies)
  - Cost: 108 kJPY (~800 EUR)/sensor
    (special price, for order 20- in Japan)

Exchange of material

- LLR – Kyushu
  - 1st exchange
    - 8 wafers (320 μm, 0GR) to LLR in 2015
    - 1 slab/DIF to Kyushu in 2017
    - 4 DIF (without cabling) to Kyushu in 2016
  - 2nd exchange
    - 5 wafers (650 μm) to LLR (4 kEUR)
    - Packaged chips (80?) to Kyushu (2 kEUR)
    - 1 GDCC to Kyushu (2 kEUR?)
    - ~ 7 SMBv5 (without cabling?) to LLR
    - 2 FEV12 (without cabling?) to Kyushu
- LAL – Kyushu
  - 2 wafers (320 or 500) from Kyushu
  - TLU from LAL?

SKIROC2A – Test stand

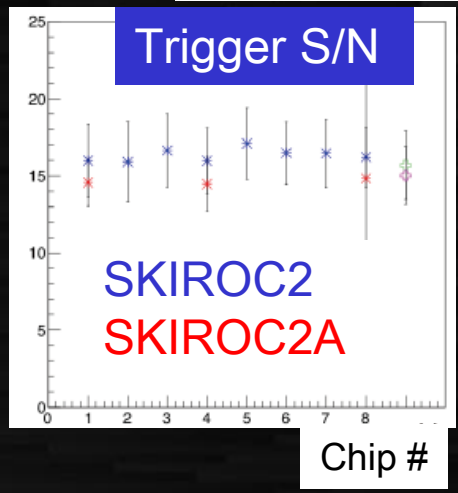


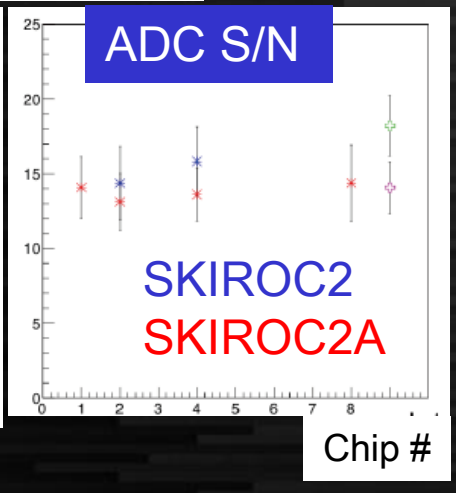


SK2A	1
Gain	110.531 ± 2.767
Width (1 MIP)	7.584 ± 0.780
S/N	14.574 ± 1.543

Omega testboard (BGA ver.)
Control by C++ software

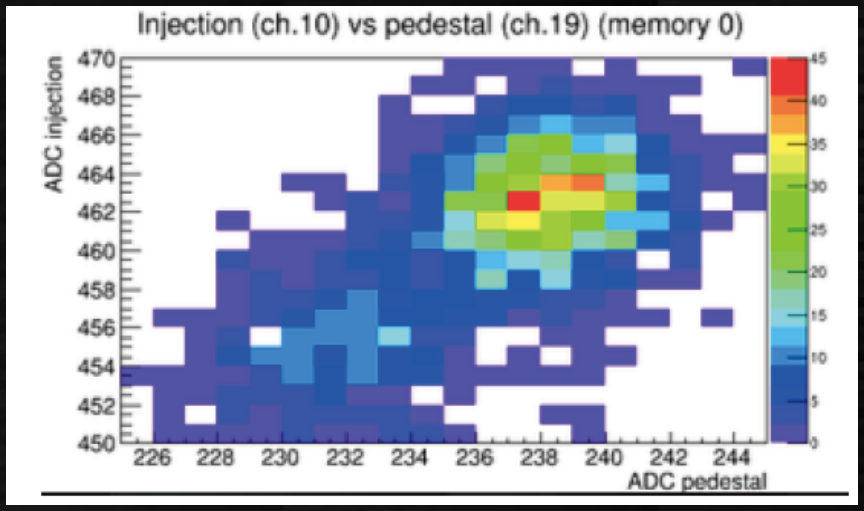
- Automatic scan w/ slow control
  - Channels, thresholds, etc.
- Automatic DAQ
- Automatic control of pulser
  - Linearity, S-curve etc.
- 10+10 chips tested → 89 more



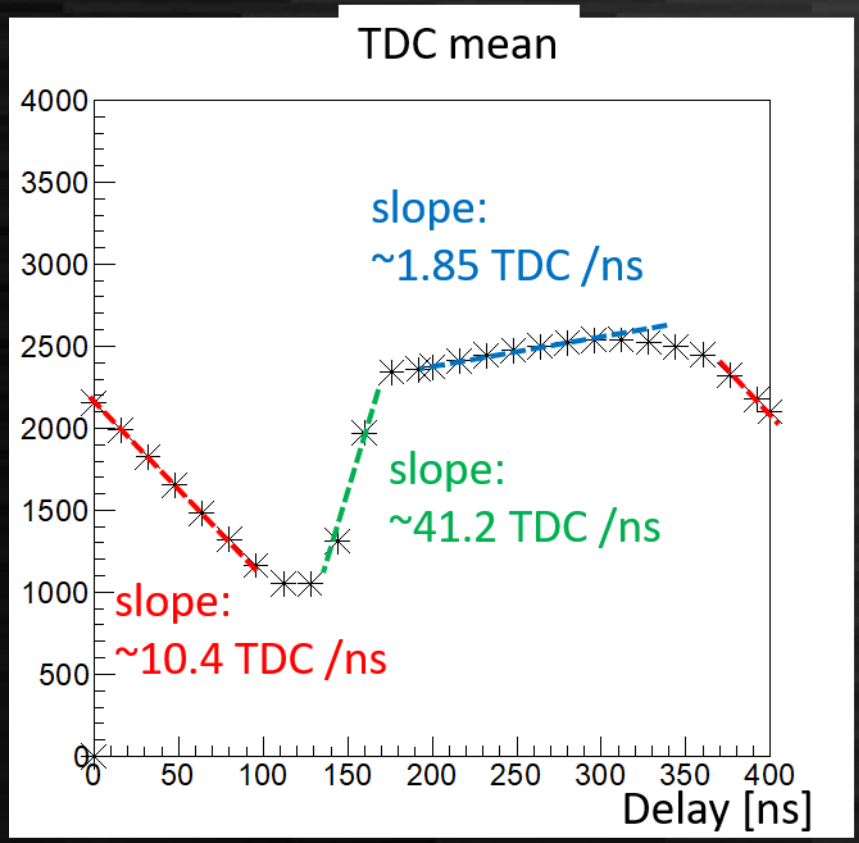


Detailed report will be in Mainz

SKIROC2A - issues



Double pedestal observed
degrading pedestal width
Relation to retriggering
should be checked



No-good TDC shape on
Soldered board (OK with socket
but worse resolution

Individual threshold control
is not good with socket board
and SKIROC2A
(big shift on trigger threshold
even with 4-bit DAC=0)

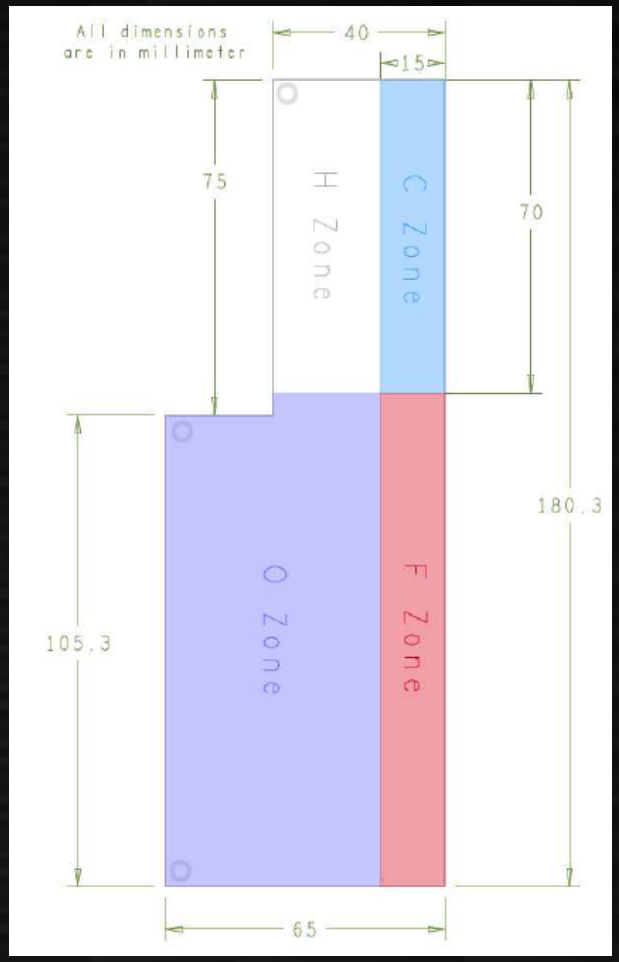
SKIROC2A test plan

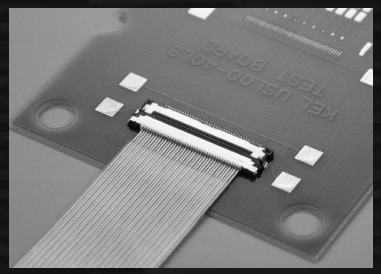
- Target: 1 hour / chip (89 chips in 2 weeks)
  - Installation
  - S-Curve of trigger
    - With 1 and 2 MIP injection
      - All channel at once – gain and S/N ratio
      - Even and odd channels - crosstalk
    - Without injection (which we need some kind of online analysis, which can be implemented only in April)
  - Slow shaper
    - Pedestal calibration
    - Linearity, crosstalk and S/N ratio
      - Injection at all channels and even/odd channels
  - TDC calibration?

FEV production

- FEV13 designed by LLR
- We planned to produce it in Japan, but due to budget reason this delayed to next FY (after April)
- We'll receive 2 (or 3) boards from LLR in end of March
- Will be cabled and tested in April

SMB (adapter board)





- Designed in Japan
  - Schematic in Kyushu (myself) finished
  - Layout by Japanese company ongoing
- Major changes
  - TINY footprint
    - Components in 70 x 40 mm (C/H zone) (except LEMO and PP-capacitors)
    - All chips are changed to small/thin
      - Power regulators
      - Buffer chips
  - Change of FEV connection
    - Flex cables (40 pins) x 3
    - Pin assignment reconsidered (by LLR)
  - Power supply to preamp (AVDD_PA) separated from AVDD

SMB (cont)

- Schedule
  - First schematic – 22 Dec. 2017
  - Final schematic and BOM – 15 Feb. 2017
  - Meeting with layout designer – 8 Feb. 2017
  - First layout – hopefully 23 Feb. 2017
  - Final layout – 2 Mar. 2017 (production due date)
  - Start production – 5 Mar. 2017
  - Delivery of un-cabled boards – 14 Mar. 2017
  - Start of cabling – 15 Mar. 2017
  - Delivery of cabled board – 28 Mar. 2017
- Price (7 + 1 build-up board)
  - Layout: 3.8 kEUR (allegro engineers are hard to find in Japan)
  - Board production: 3 kEUR initial + 140 EUR / board (for 5-20)
  - Cabling: 650 EUR initial + (110 + 400) EUR / board (for 2)

Gluing sensors and alignment

- We bought a glue dispenser with a 3-D stage in Kyushu
  - 20 kEUR
  - Multi-project facility (ILC, ATLAS, muon g-2)
- Glue: EPO-TEK E4110-LV (low viscosity version)
  - Will be optimized later
- Alignment: we will develop a jig to pick-and-place the sensors on to FEV by this robot

3 pads will be used to hold sensors

Misc.

- Kapton (FPC)
  - We can produce, but budget is unclear in this FY
- Carbon fiber
  - ?
- Copper plate
  - Possible next FY
- Others?

Schedule of assembly/test

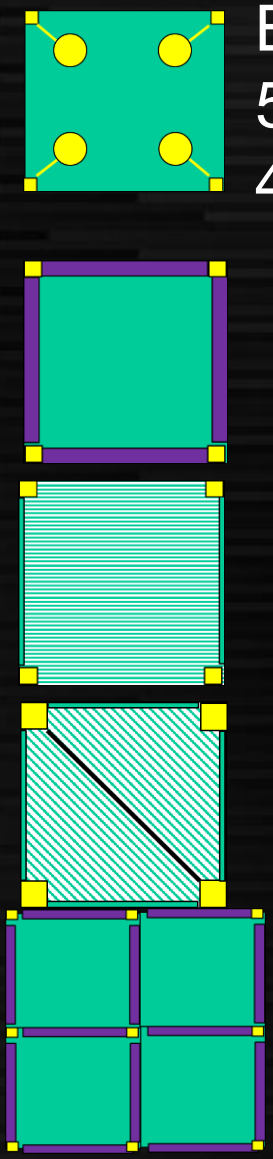
- First (1?) FEV available in end of April
- First (2?) SMBs available in end of March (out of 15 boards)
- FEV-SMB-DIF test wo sensor in early May
- Gluing preparation: March – April
- First gluing: late May
- Test with sensor: May - June
- Will see if we can send it to test beam in end of June
  - Single slab maximum
- (5) FEV production in Japan: maybe June
- Pure-Japanese slabs will be produced in July-August
- Can be sent to test beam if we have in Autumn

Other activities

Position sensitive detector

Wafer pattern
Delivery: end March

Two options included
- Resistive P+ (1kΩ/cm^2)
- Dedicated R layer (10k)



Basic pattern
5.5 x 5.5 mm, 4 pads/cell
4 x 4 cells → 64 ch

Low-resistance edges
to reduce distortion

Resistive 1-D strips
to reduce distortion

45 degree strips
to separate to 2 zones

Shared pads
to reduce readout ch.

Timing detector

- LGAD
  - Try to produce next FY (we have dedicated budget)
    - 50-60k EUR needed!!
    - Delivery: end of this year (?)
  - Timing layer
    - Should be small to minimize capacitance
      - Should try several sizes of pads and strips
    - Thin – active thickness of 50-100 μm
      - Due to mostly technical difficulty in HPK
      - They're still developing – possible thickness not clear
    - Inverse-type LGAD (gain layer at the bottom)
  - PSD layer
    - To increase S/N ratio – should try