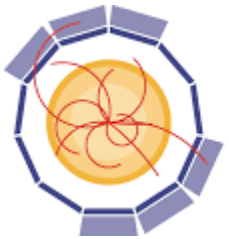
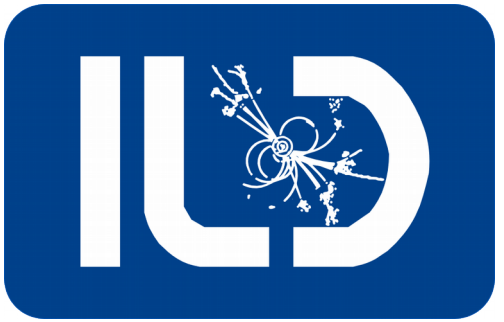
Status of R&D at LLR

Frédéric Magniette
On behalf of the SiW-Ecal Team at LLR

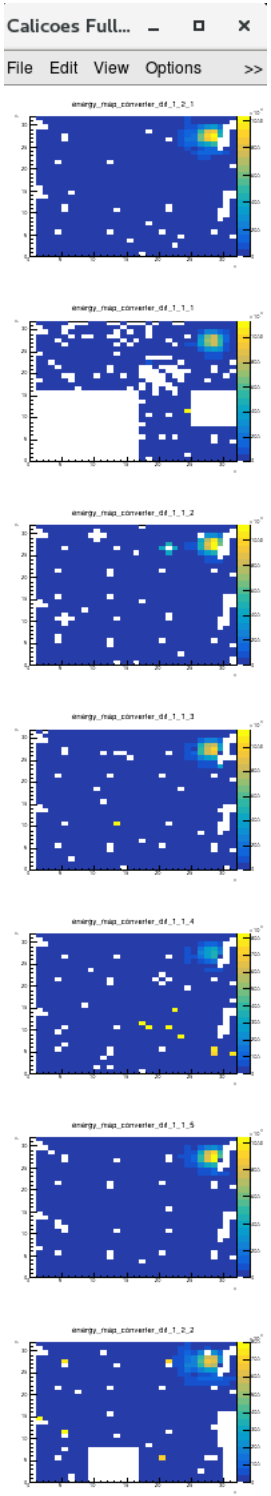


AIDA 2020



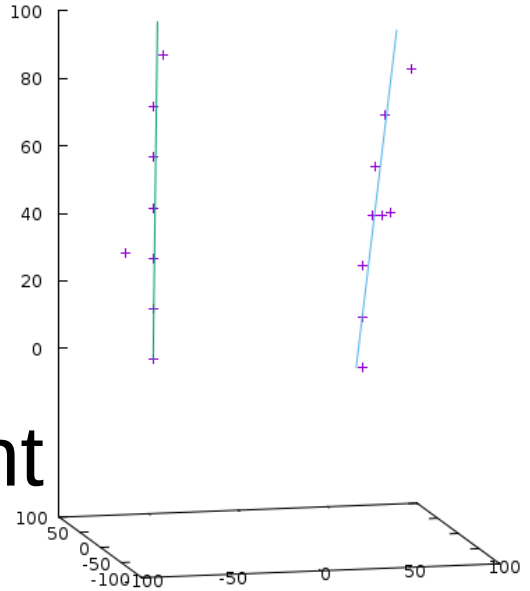
Short slab prototype

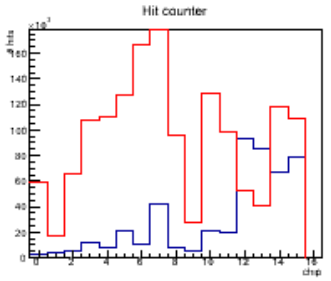
- 7 layers with ILD level of integration (1024 channels per ASU)
- Single ASU slabs

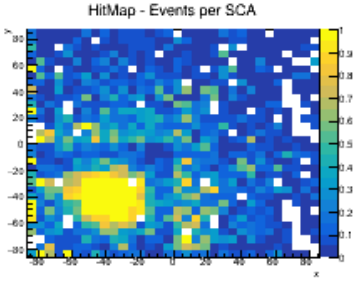


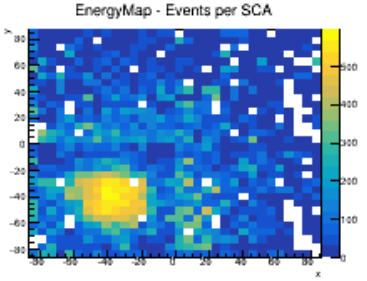
DAQ improvements

- Online data treatment system (Presented at CHEF'17)
- New monitoring system
- New script system integrating movement table (no more night shift)
- Linear tracks reconstruction (online)



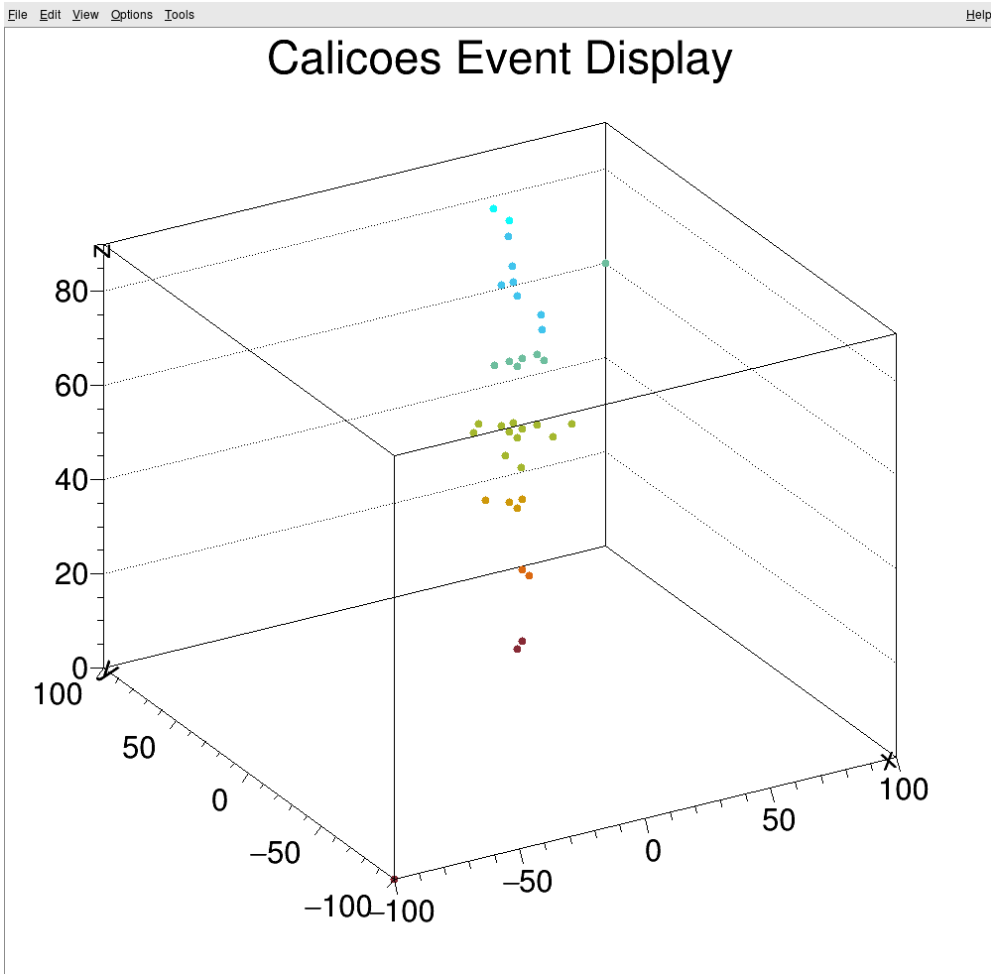




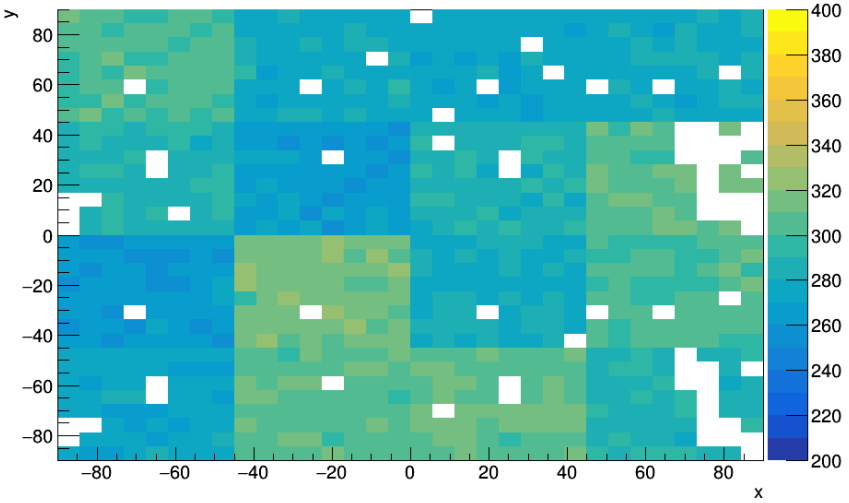


Beam-test 2017 @DESY

- Good results (All details in A. Irles talk)
- Full validation of the technical concept
- Some minor drawbacks
- Time to grow
  - Development of a new SMB/FEV adapted to long slab
  - Development of an electrical long slab prototype



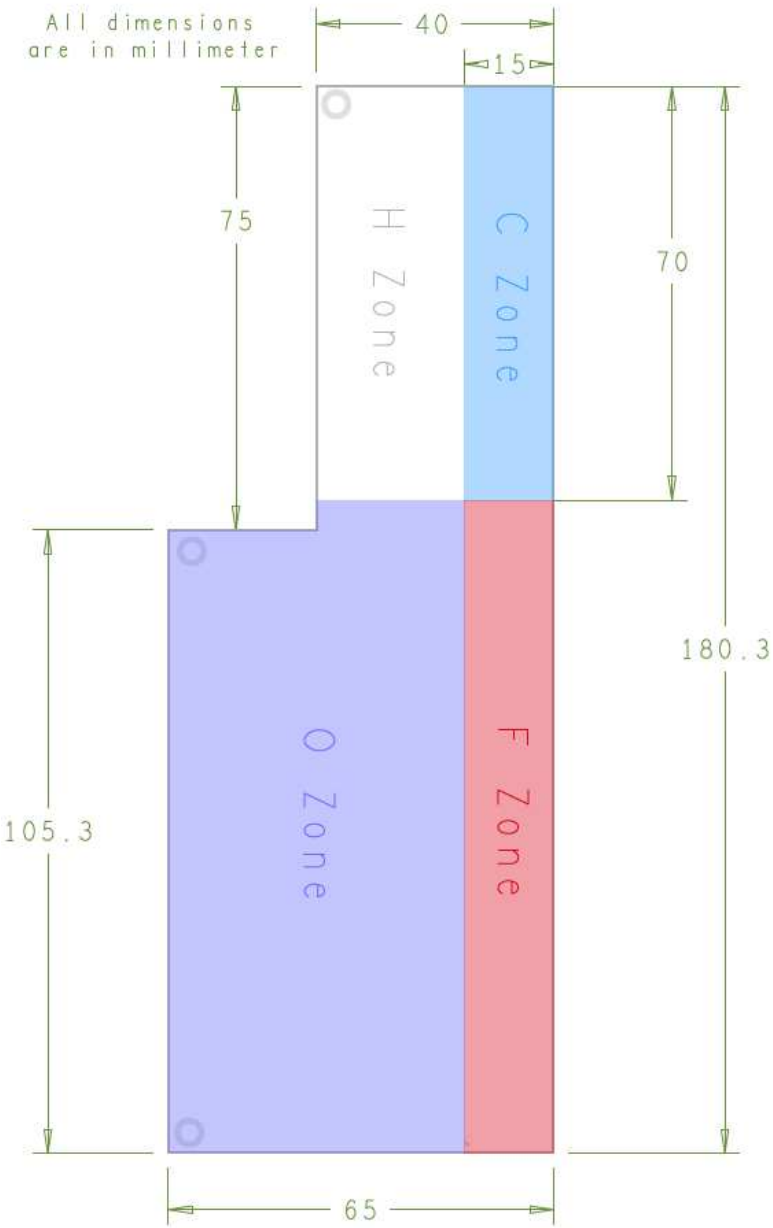
Short slab prototype limitations



- Masked channels
- HV noise sensitivity
- Long slab chaining problem
- Fast clock limitations (frequency and cut)
- No hardware identification
- No way to input an outside spill number
- Using Skiroc2 instead of Skiroc2a

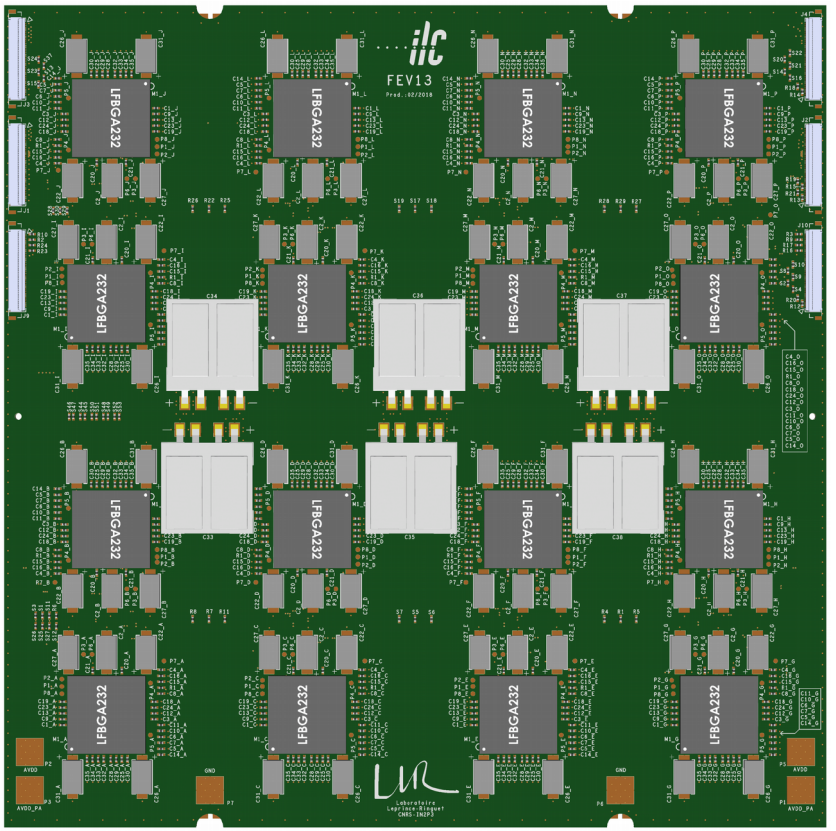
New SMB

- Developed with Kyushu University
- Cope with ILD geometry
- All necessary components on the 70x40 zone
- Only debugging feature are out of bounds
- New connector imprint compatible with connectors and kapton
- High level of integration



New FEV

- Very low noise design
- Reducing masked channels
- Adapted to Skiroc2a
- ILD compliant connection (70mm)
- Data rerouting to avoid long path from end of slab to SMB (U path)
- Includes capacitance for power pulsing
- New power supply decoupling
- Cope with ILD width
- Status : first batch delivery mid-march

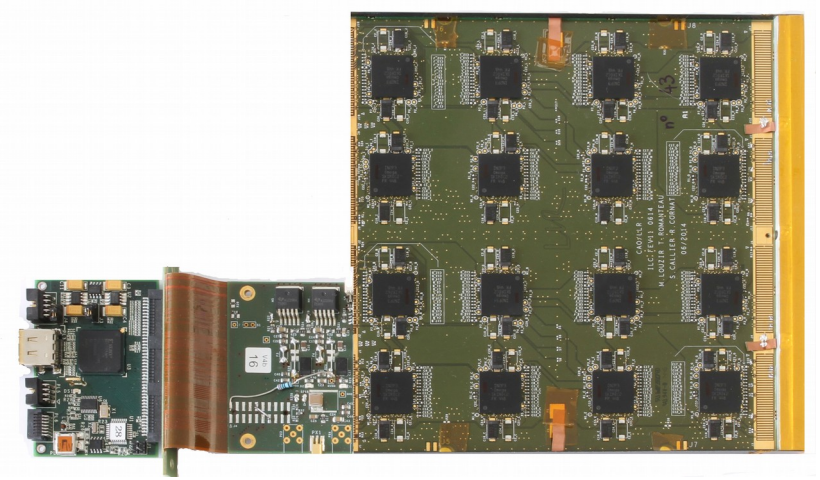


DAQ improvements

- Fast Clock
  - adjustable at 40 or 50MHz
  - off during acquisition
- Hardware identification (See Yu Miura Talk)
- Spill number injection from outside
- Eudaq module (in collaboration with Adrian)

New slabs

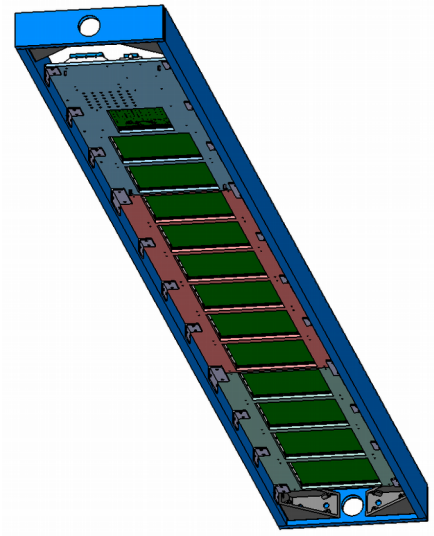
- Planned production of 5 new short slabs
  - Kyushu & LLR
  - Wafer 650 µm & 525 µm
  - New SMB/FEV
  - Skiroc2a

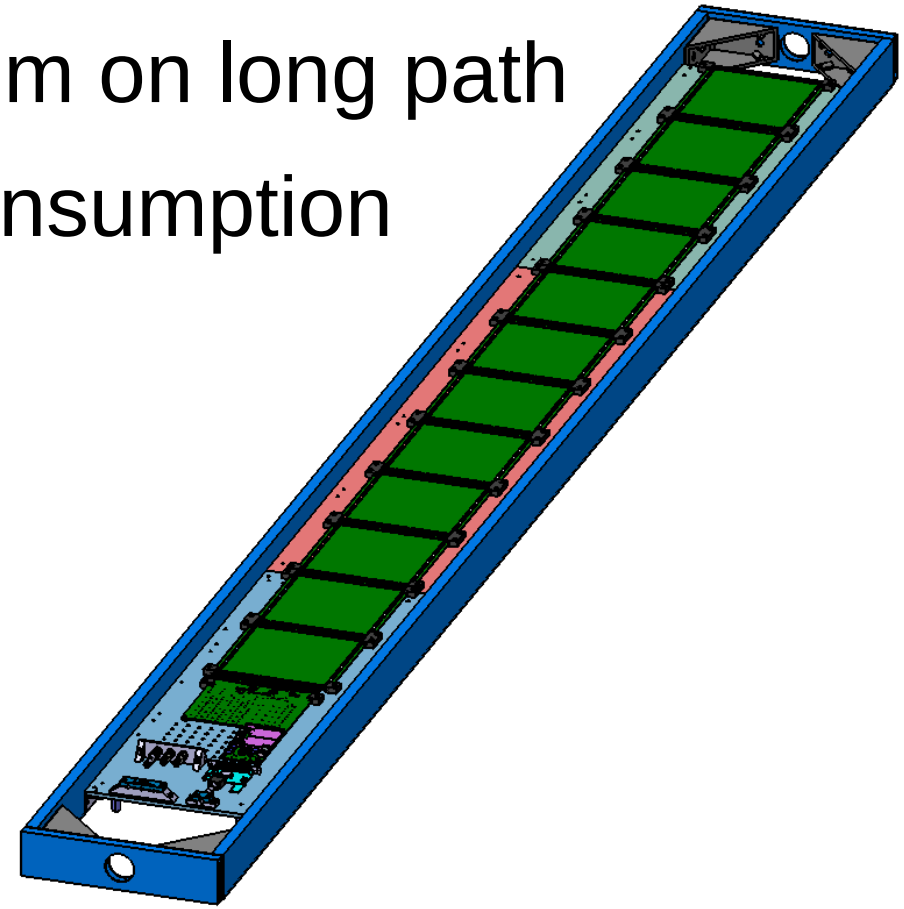


- Expect better behavior (masked channel…) with same performance (S/N)
- Planned production of long slab in future

Long slab electrical prototype

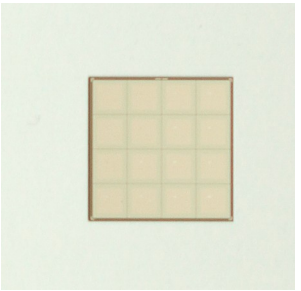
- To test electric signal popagation and clock properties
- To debug read-out system on long path
- To evaluate electrical consumption



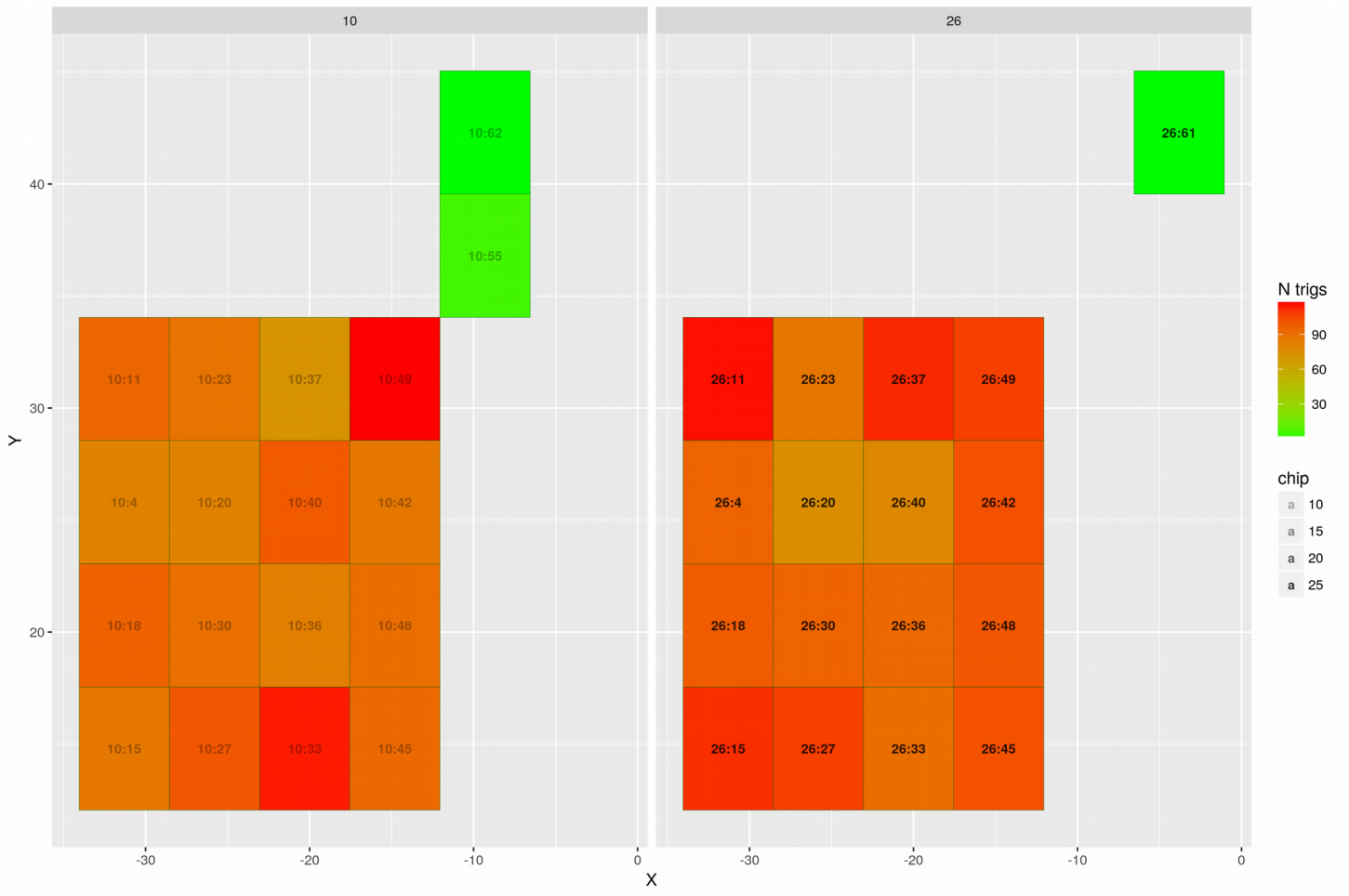


Long Slab Status

- 2 ASUs mounted – up to 12 expected
- One by one mounting strategy
- Equiped with baby-wafer (4x4)
- Hood for light protection
- Handling structure for beam-tests
- Satisfying level of noise



Cosmic Runs


10
26
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N trigs
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chip
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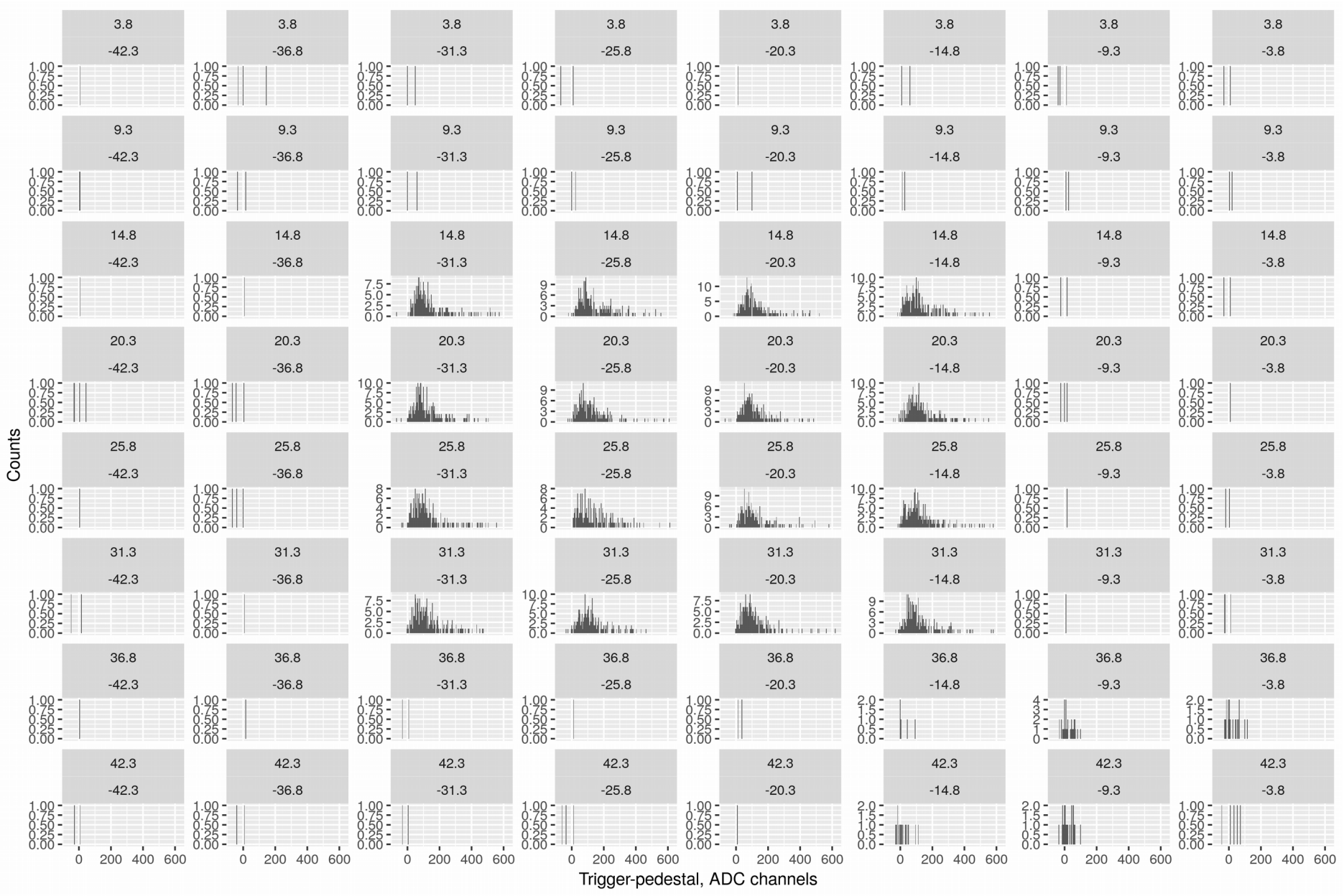
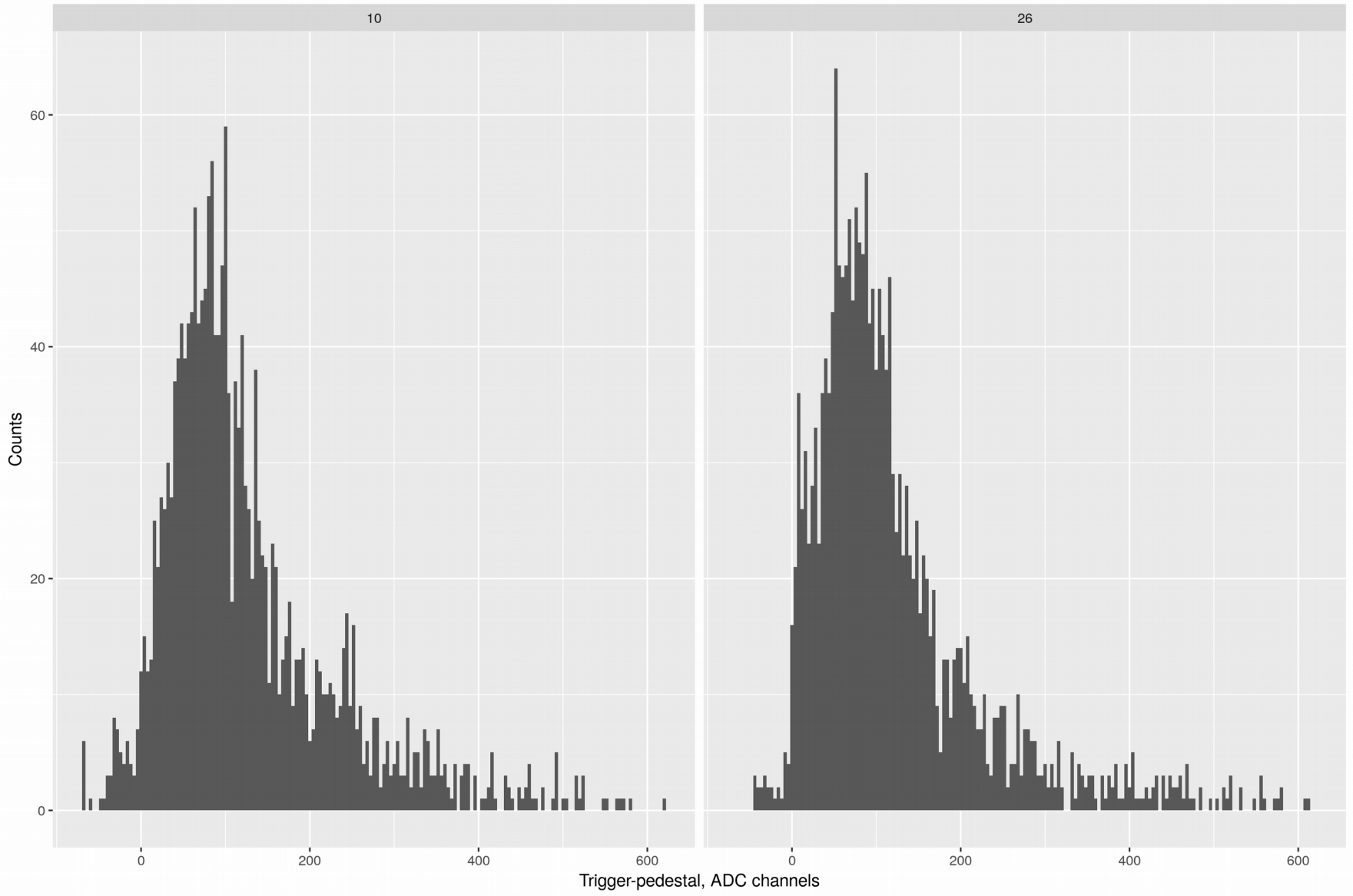
a 20
a 25

Cosmic Runs (2)



Cosmic Runs (3)

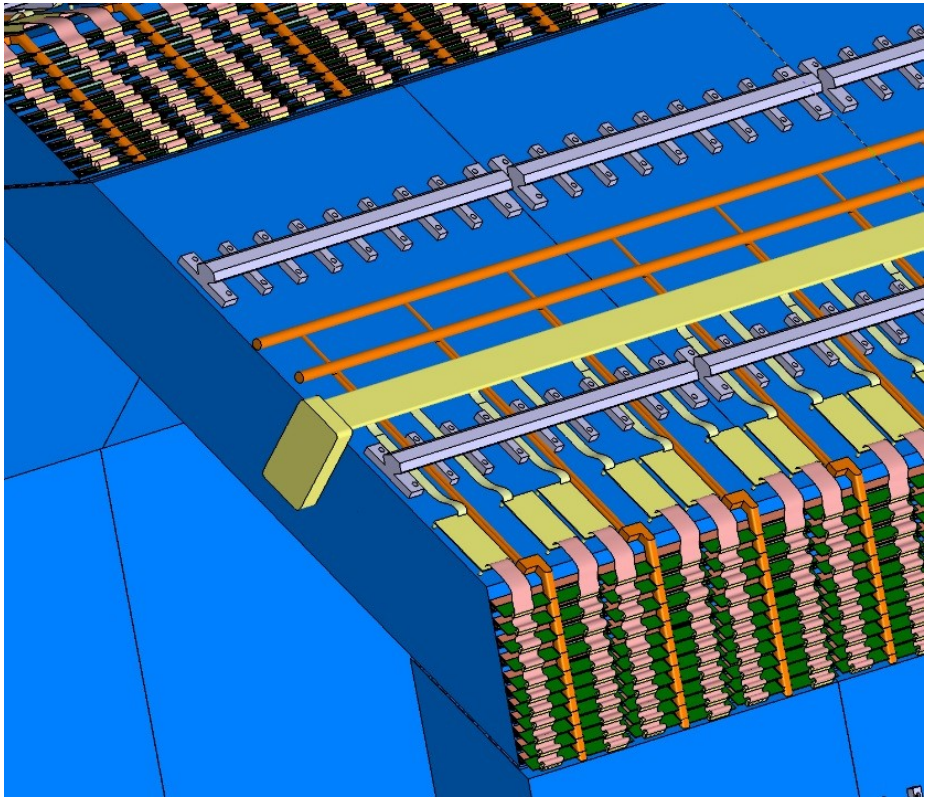


Mechanical structure

- Adapted for
  - Beam-tests
  - cosmic-tests
  - radioactive source tests
- 360° rotation
- Adjustable height
- Wheels for long move
- Fine adjustment in both directions

Compact DAQ study for ILD

- Adaptation of the prototype DAQ to ILD constraint
- DIF suppression
- Redesign of the GDCC
- Reducing wires by buses or combined protocols
- HV generation inside GDCC



Scheduling

- Waiting for a good news in August
- In the meantime
  - Finishing the electrical long slab prototype
  - Finishing a new SMB/FEV short slab prototype
  - Finishing the options study for the compact DAQ
  - Beam-test @DESY in July 2018