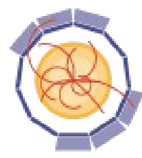

AIDA2020

Progress at LAL

Assembly and digital readout system

Roman Pöschl

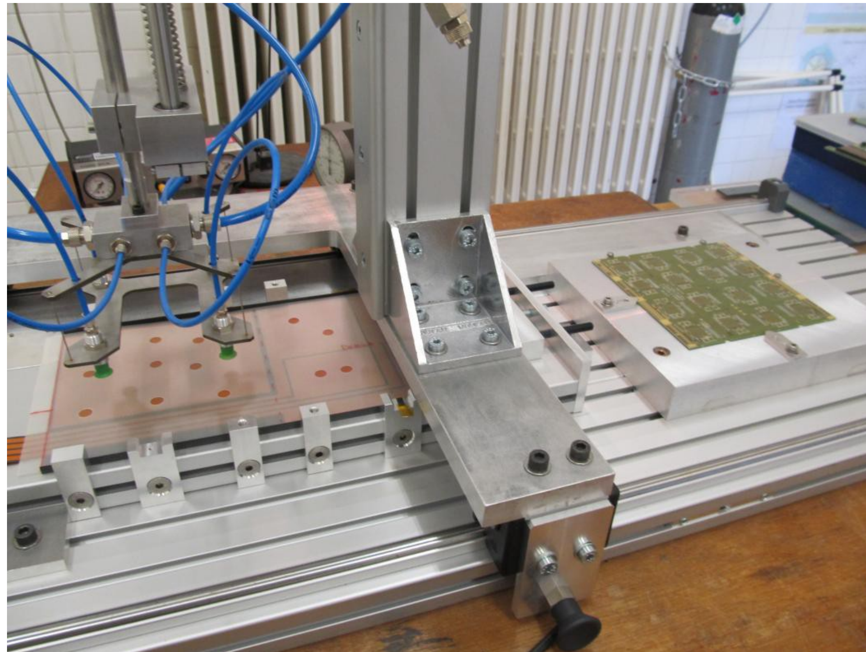
On behalf of
Alice Thiebault, Julien Bonis, Denis Douillet, Alexandre Gallas,
Christian Bourgeois, Dominique Breton, Jihane Maalmi, Jimmy Jeglot*,
Dirk Zerwas, Adrian Irles
+
Stephane Callier and SKKU Group

Ecal Meeting KEK/Japan – February 2018

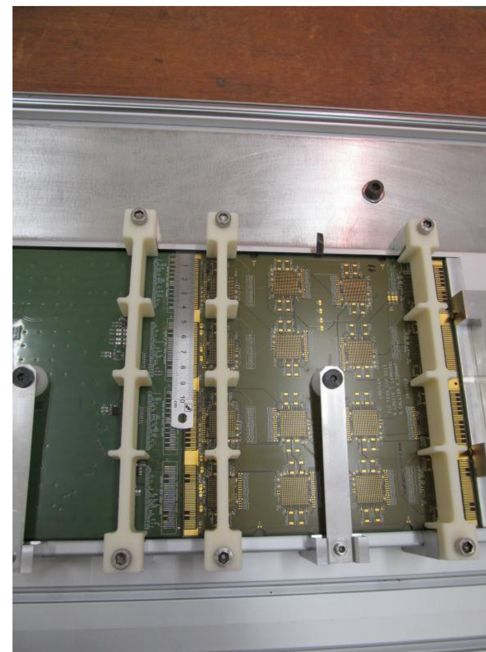
*Most slides from Jimmy's talk at AIDA-2020 Meeting

SiW ECAL Assembly

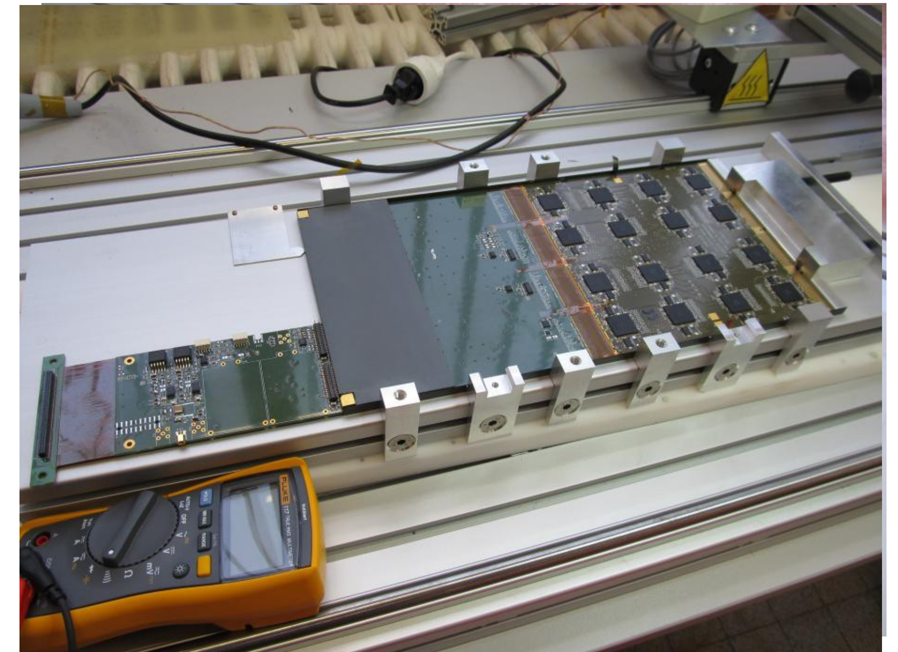
Pick and place



Precise alignment



Ready for test



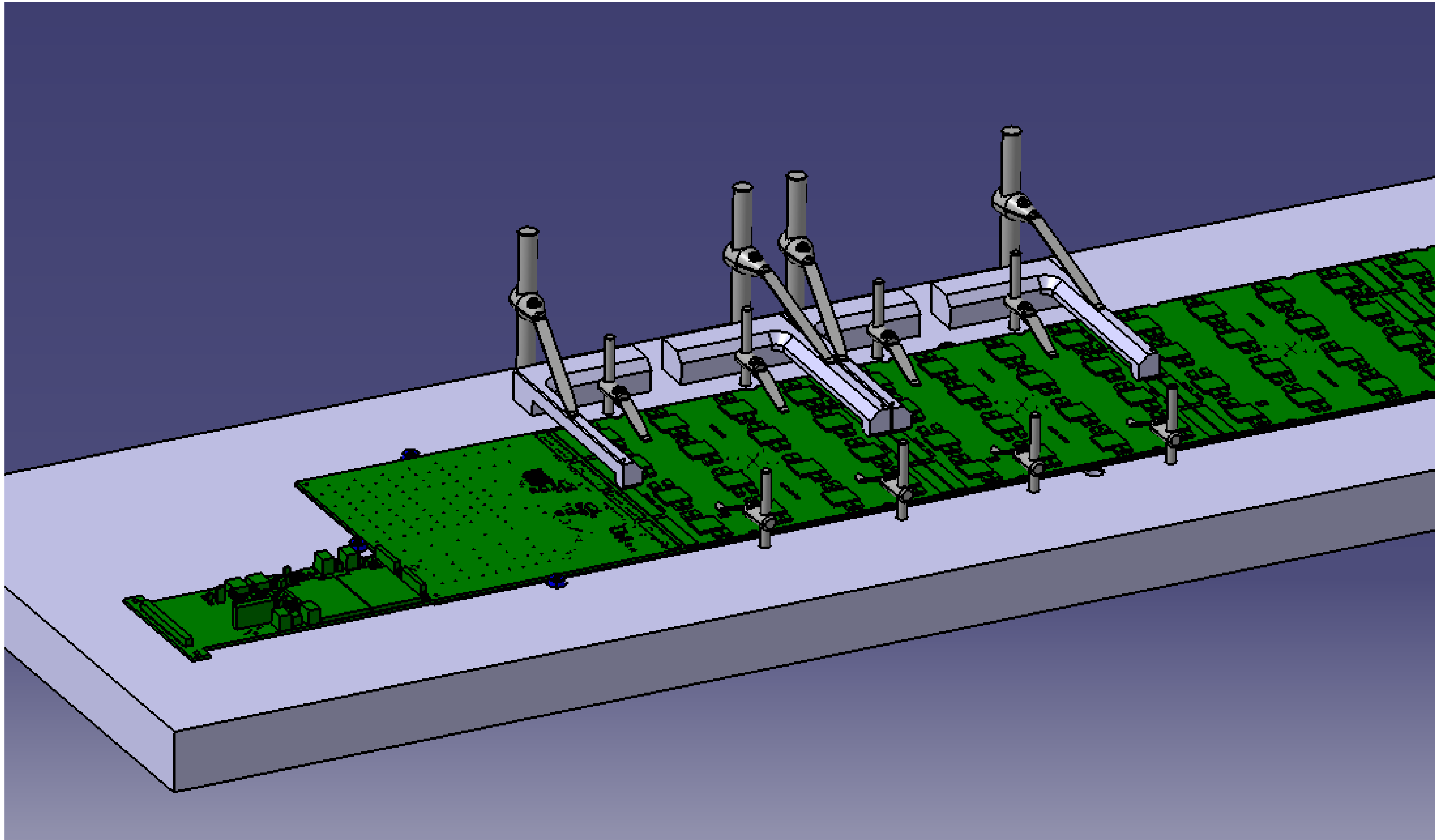
- Assembly steps are validated with **short layers** (13 assembly steps)

- Need big step towards **long layer** to assure high quality product
  - Automated pick-and-place and alignment
  - Interplay of many different working steps
    a) Assembly proper
    b) Continuous control of up to 8 (14) ASUs during assembly

- Successful product requires a lot of testing and exercising of well trained technical staff!!!

Thiebault/Bonis/Gallas

SiW ECAL – Assembly bench drawing

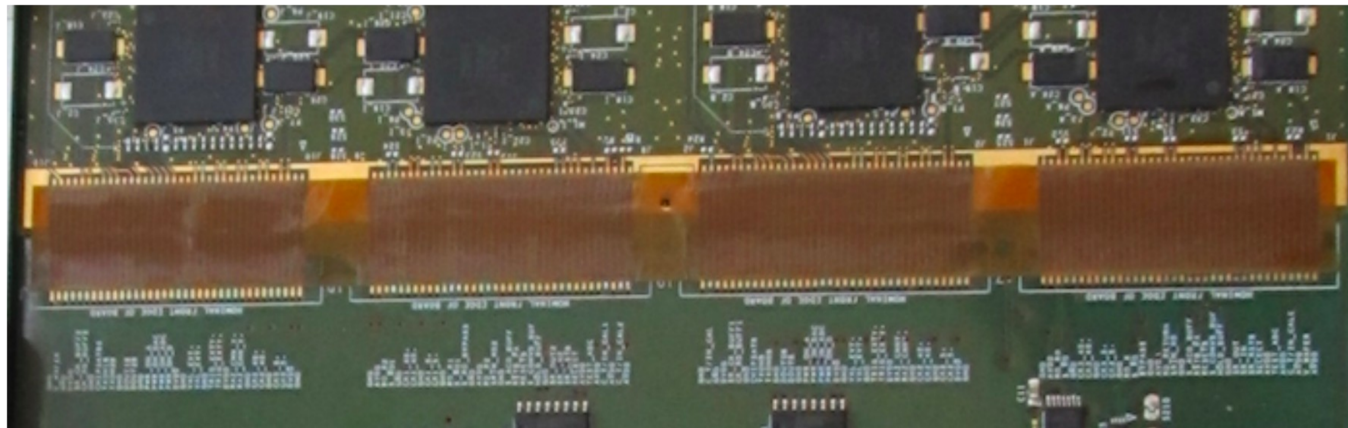


- Preparation of upgraded testbench
- First pieces have been delivered
- Special care for precise ASU alignment

Thiebault/Bonis/Gallas

On interconnection

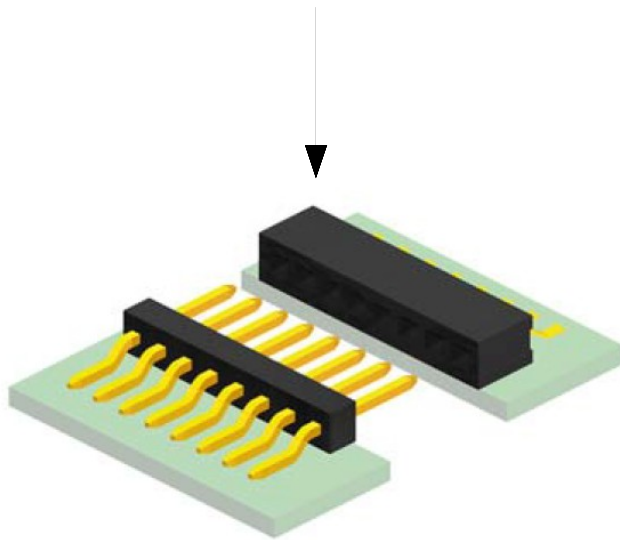
Interconnection is maybe the most involved piece of the assembly



Solution with Flat Kapton **works**

- Proven for short slabs
- Interconnection so far made by hand
- Delicate work

Had difficulties to find supplier for (semi) industrial procedure

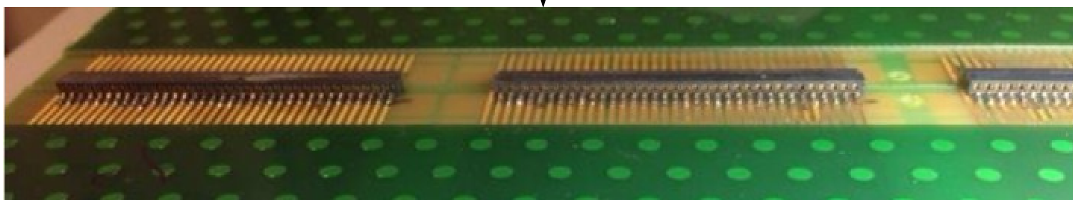


Alternative with 'real' connector identifies

- Take advantage of mobile phone technology
- 1.27 – 1.5 mm height

May enable to realise individual ASUs

Compatible with BGA type PCBs
Not a penalty for COB type PCBs



ASUs interconnection: New connector based proposal

The following interconnection proposal is meant for the ASU with the SKIROC-BGA option.

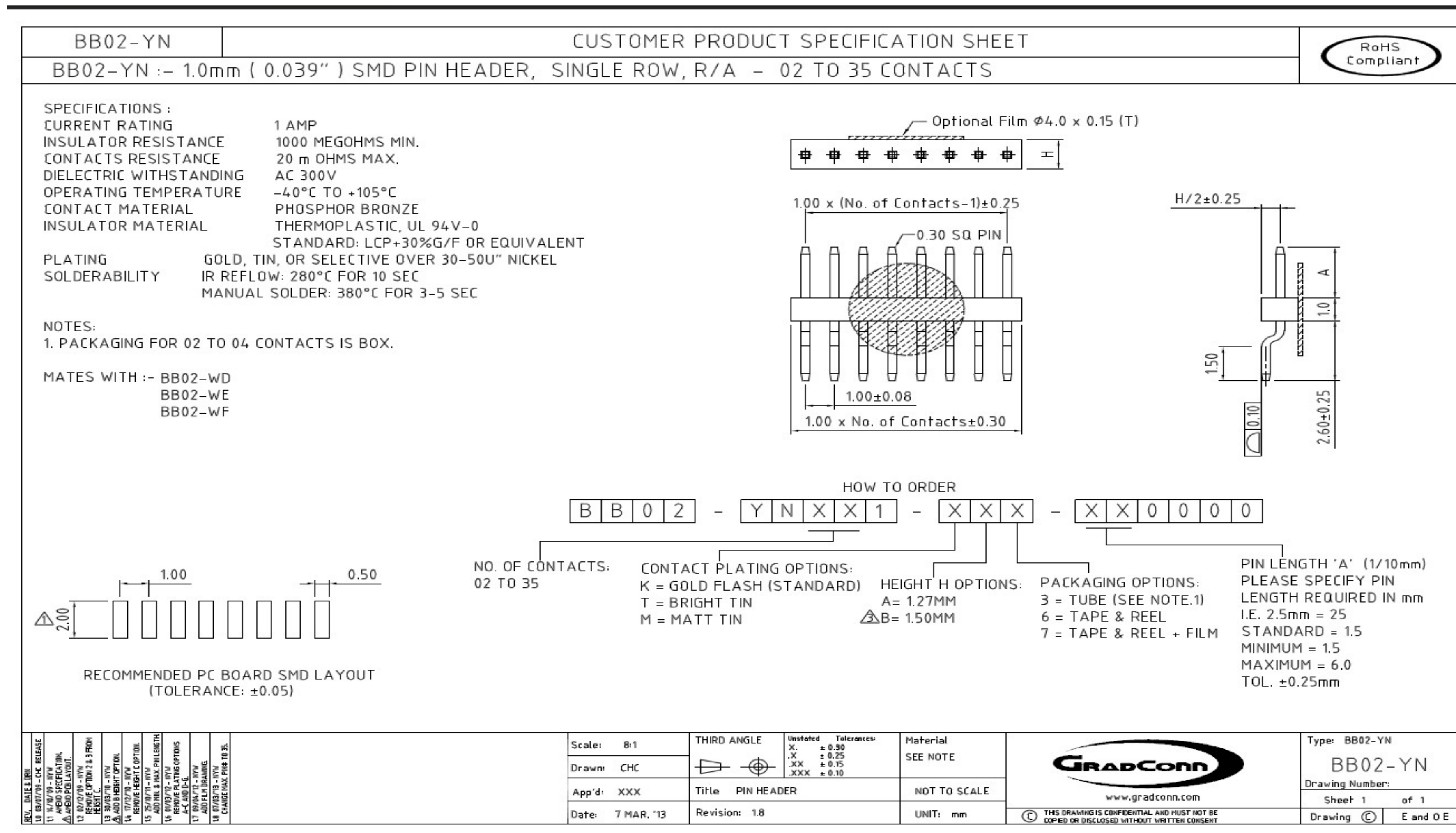
We propose Gradconn connector BB02-YN

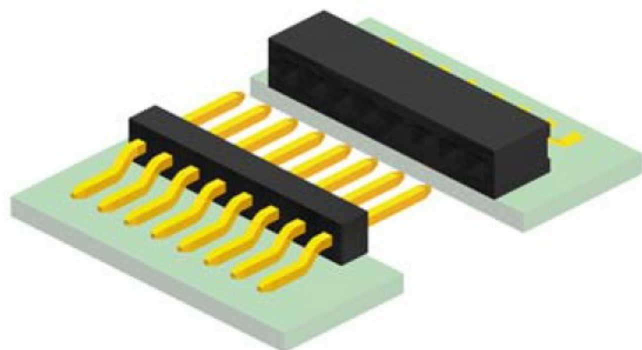
Specifications:

- 35 pins
- Height : **1,5 mm** possibly **1,27 mm.**
- **Pitch 1mm compatible with existing ASUs**
- Current rating : 1 A.
- AC 300 Volts

For the 1,27 mm height option :
It costs : **5000 $ (**tooling) + **1,4 $ x 10 000** units !

Maybe not as robust as the 1.5 mm high version.

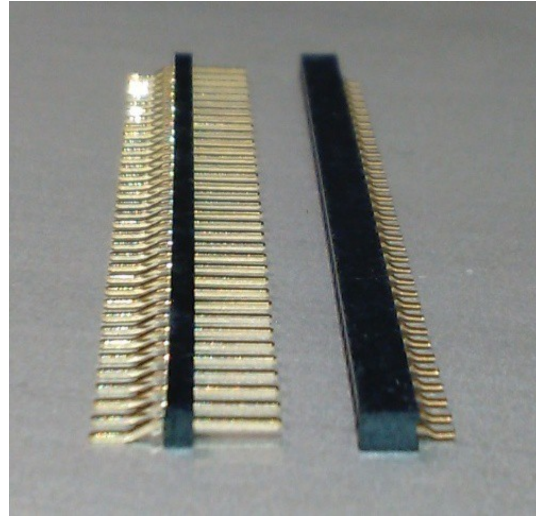


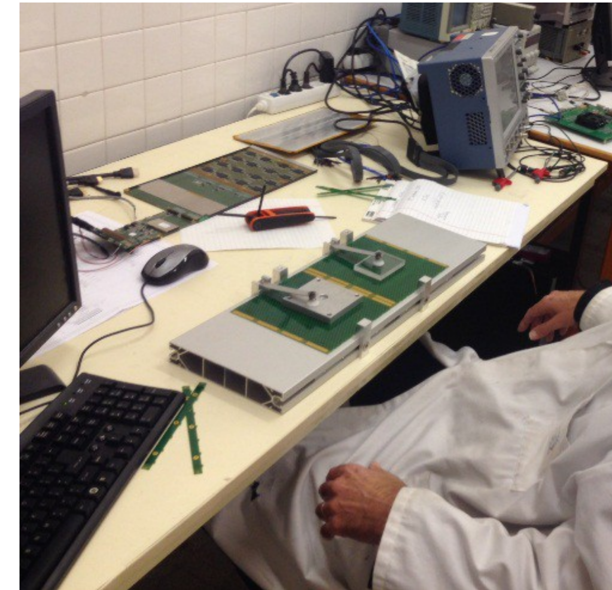


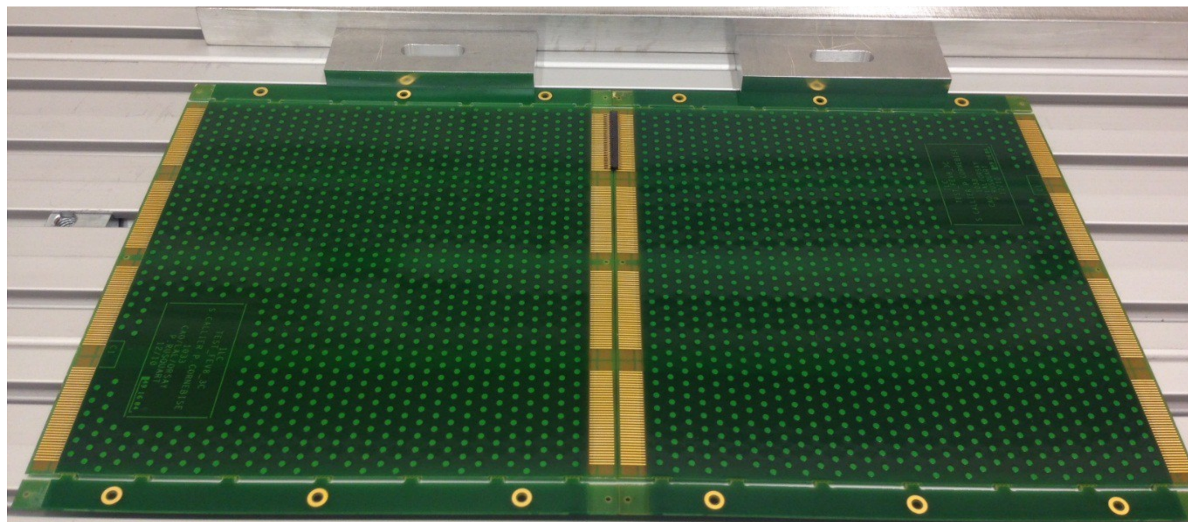
https://www.gradconn.com/Products/BoardToBoard/MatingHalves/BB02-YN/BB02-WF

Interconnection with Flat Connector

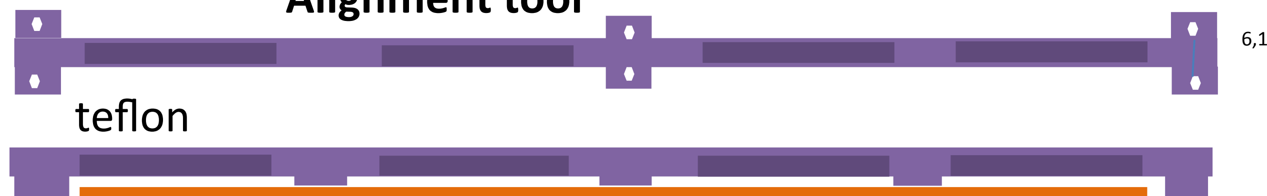
First impressions:
- Good mechanical stability
- Easy to mount and solder

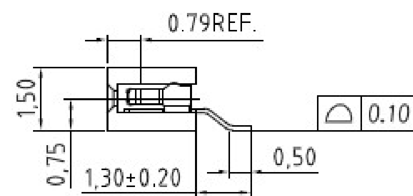


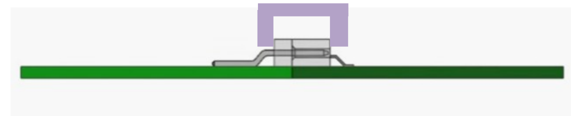


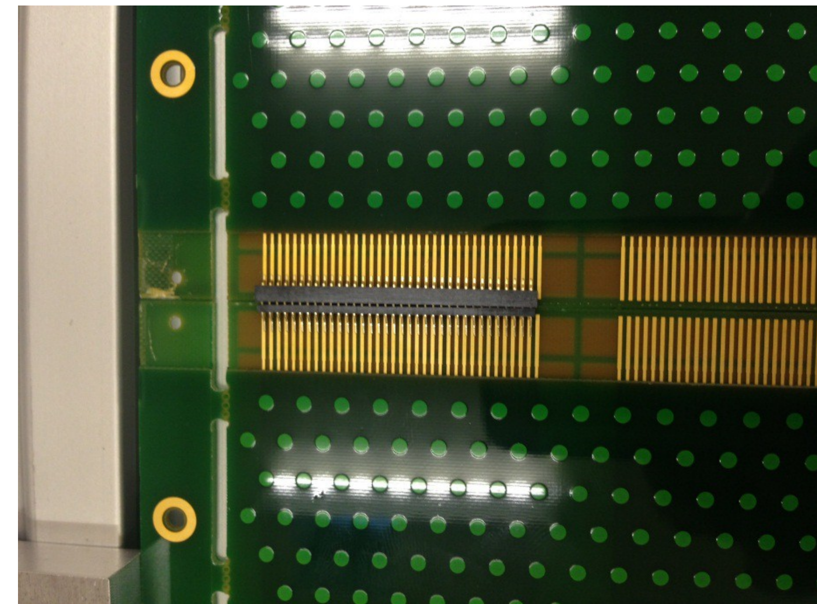


Alignment tool





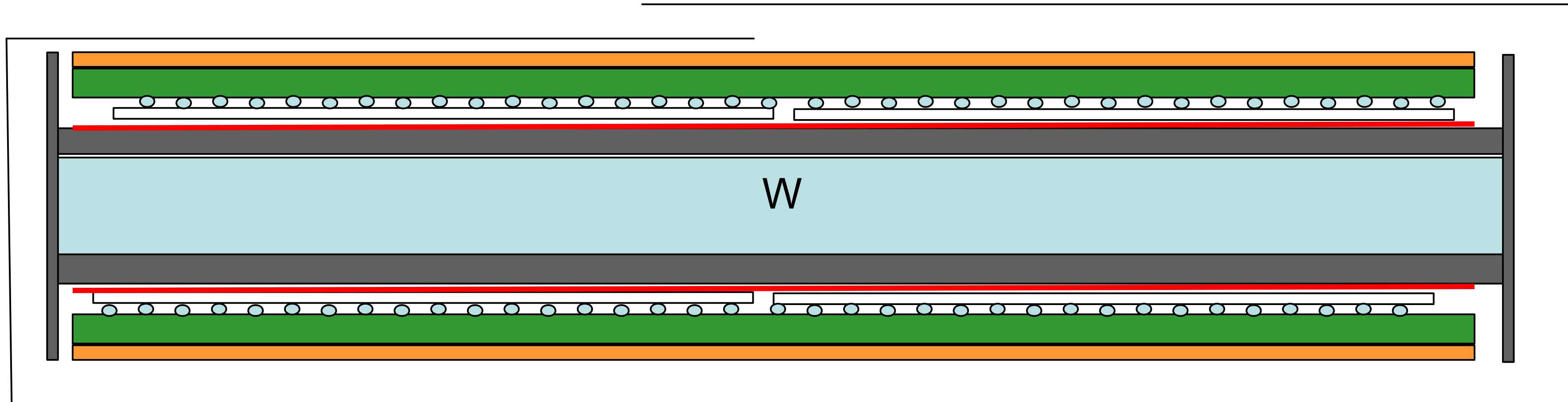




ASU assembly procedure revisited
To be further validated in coming weeks

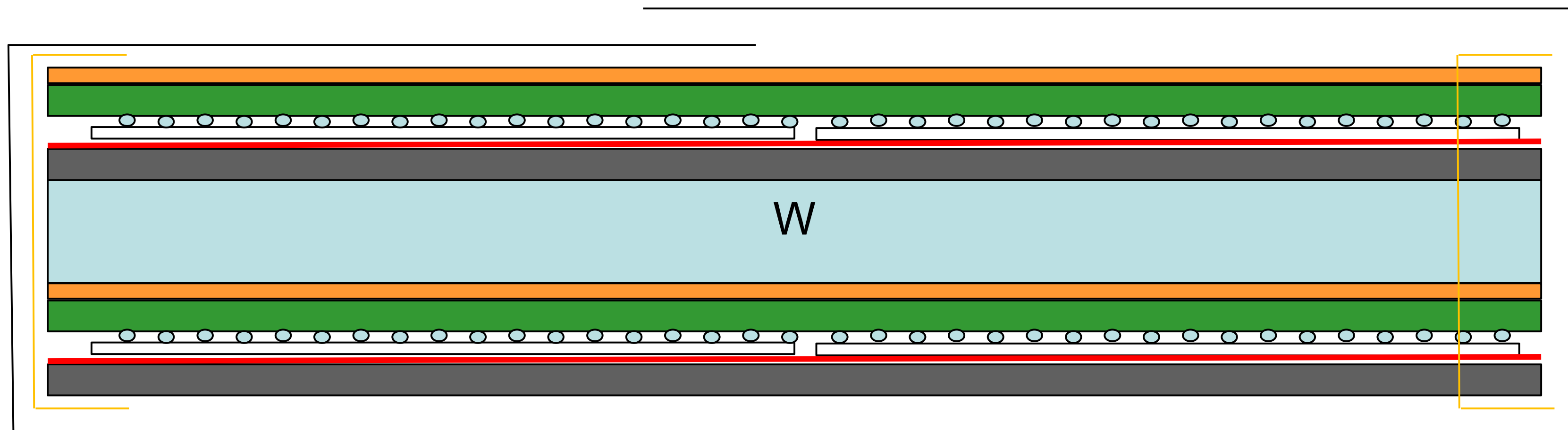
SiW ECAL – Long layer – Options

Current default solution



With thin side walls
Requires to master geometry of side walls
Some concerns for recent production of short slabs
May render assembly more involved

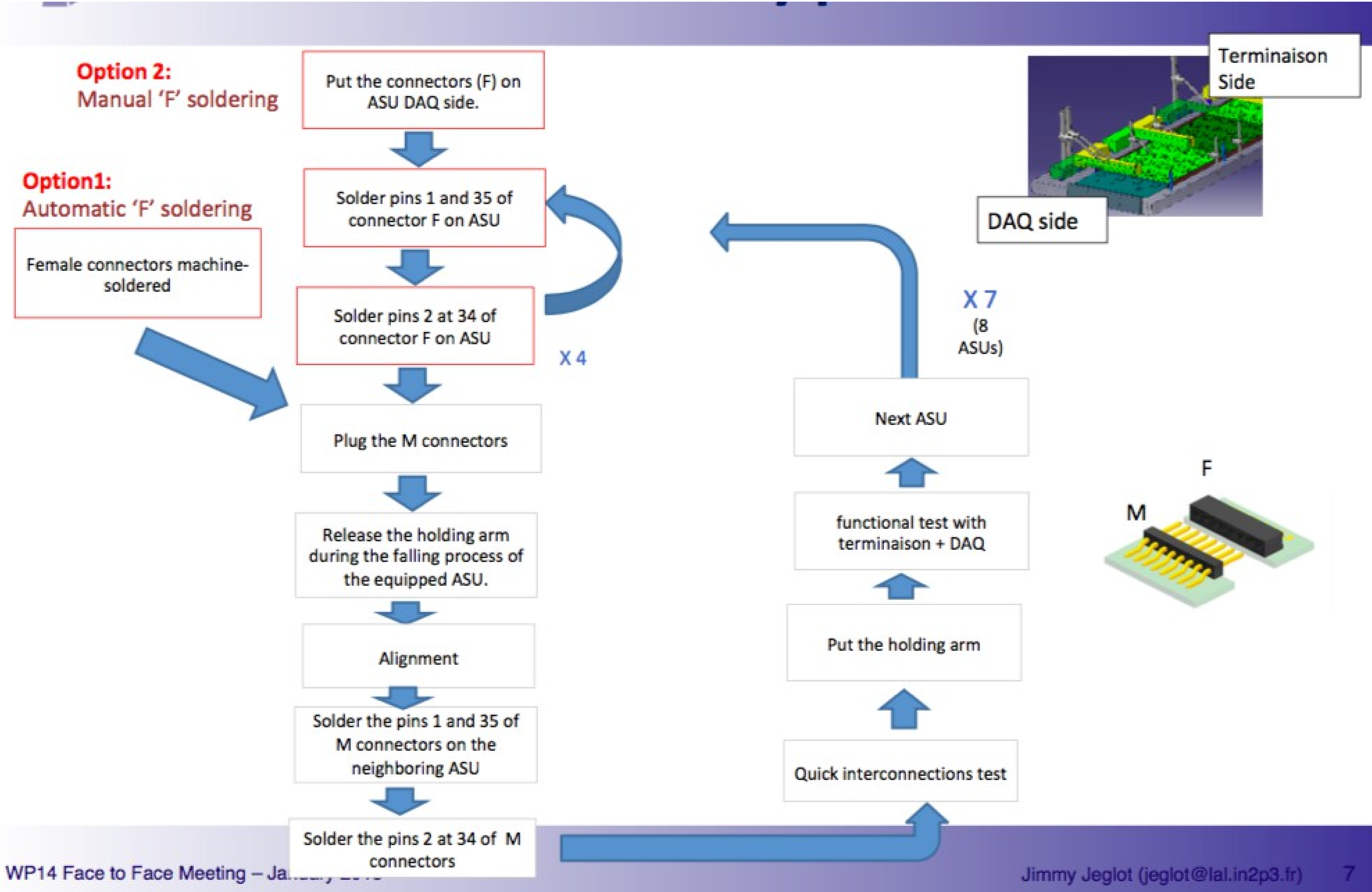
Alternative option



Without thin side walls
Assembly much easier
May need additional protection on sides
Weight poses on wafers (may be minor issue)
Will be initially followed up for assembly (while waiting for production of carrier structures)

- First test with short plate back in 2016
- New (long) carbon plate is available for assembly procedure

ASU Assembly Procedure



- Expect first compilation of bench during March 2018
- Updated assembly bench is AIDA-2020 deliverable due in April 2018

Ongoing tests of connectivity

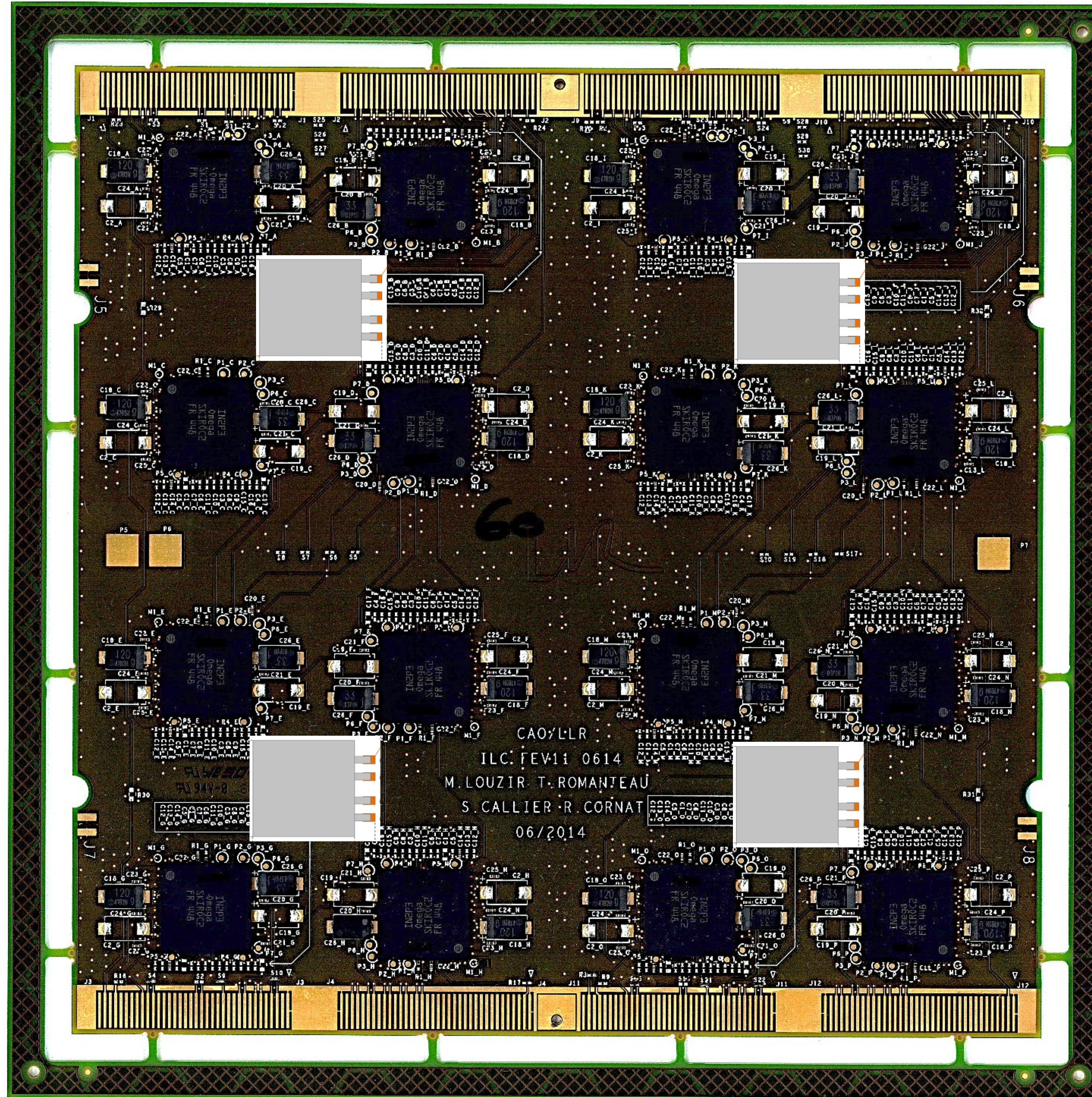
Still ongoing tests to perform:

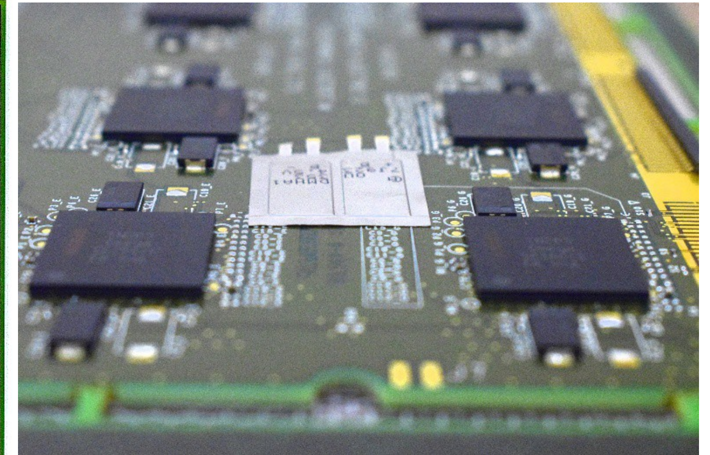
- Connectors resistivity measurement
- Further tests with long slabs.
- Emulate power-pulsing and measure the effect on the AVDD power supply on the ASUs all along the slab.
- Signal integrity along the slab: we may need to add buffers on the ASUs
- Mechanical stress test
- Check ASU alignment over a long sab.

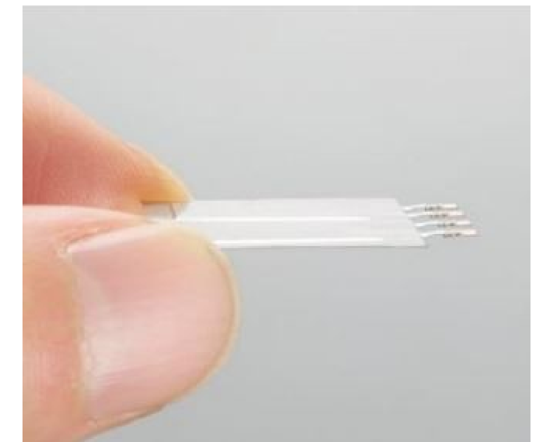
Ultra Flat Capacitors

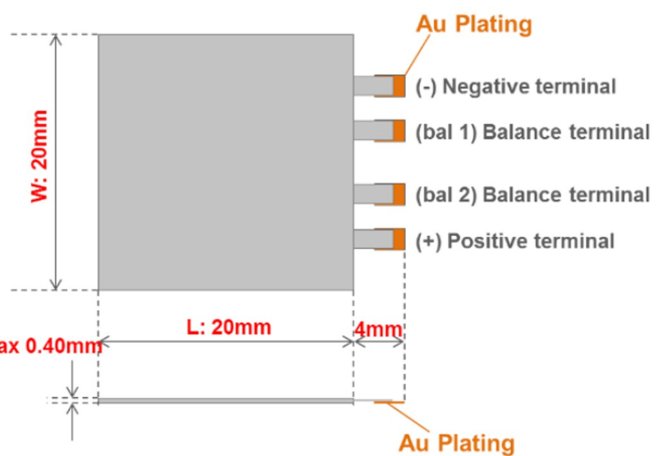
See e.g. CALICE Meeting 2017 in Japan and AIDA-2020 WP14 Meeting 2018 at CERN

Ultra-Thin Supercapacitor
DMH series
DMHA14R5V353M4ATA0
35 mF / 4.5 V









Integrated capacitors allow for **reducing peak currents from 12A to 1.2 A** during power pulsing

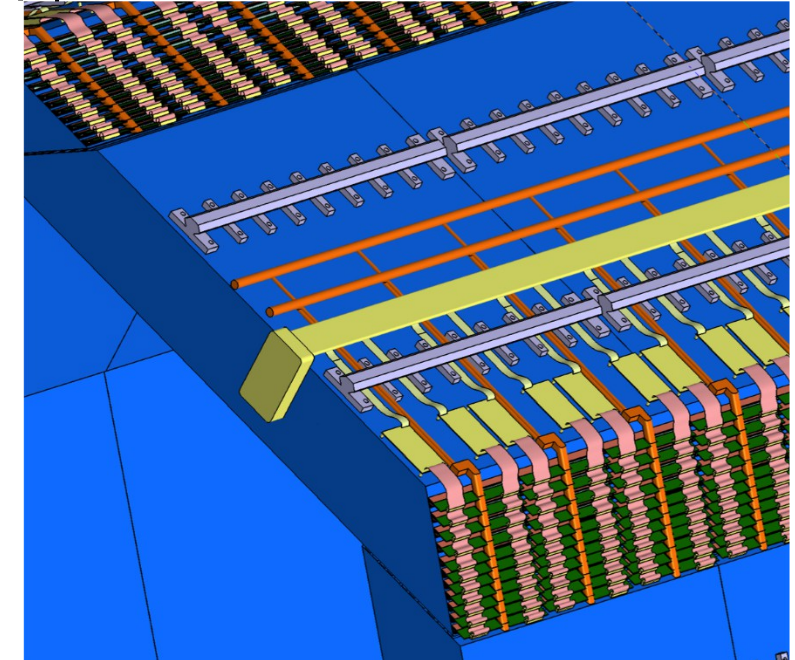
Raised Question! Life time has to be checked, depends on voltage and temperature…

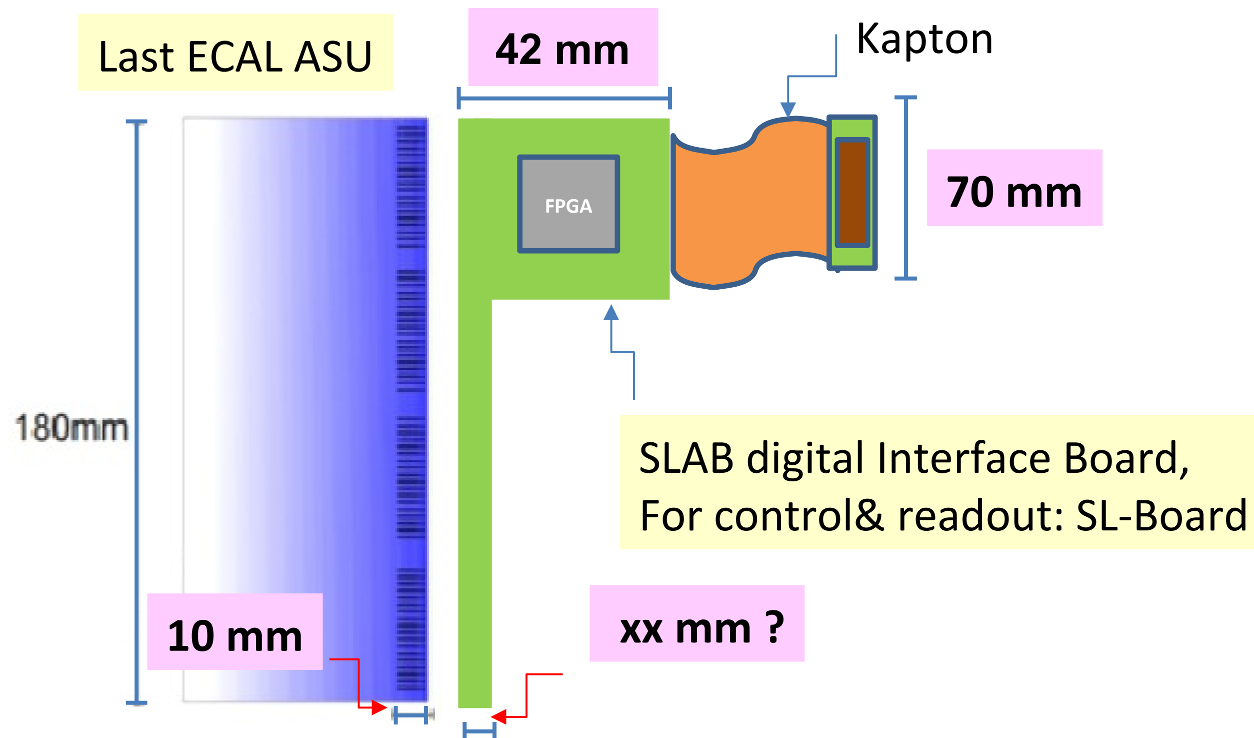
Ecal Electronics Space Constraints

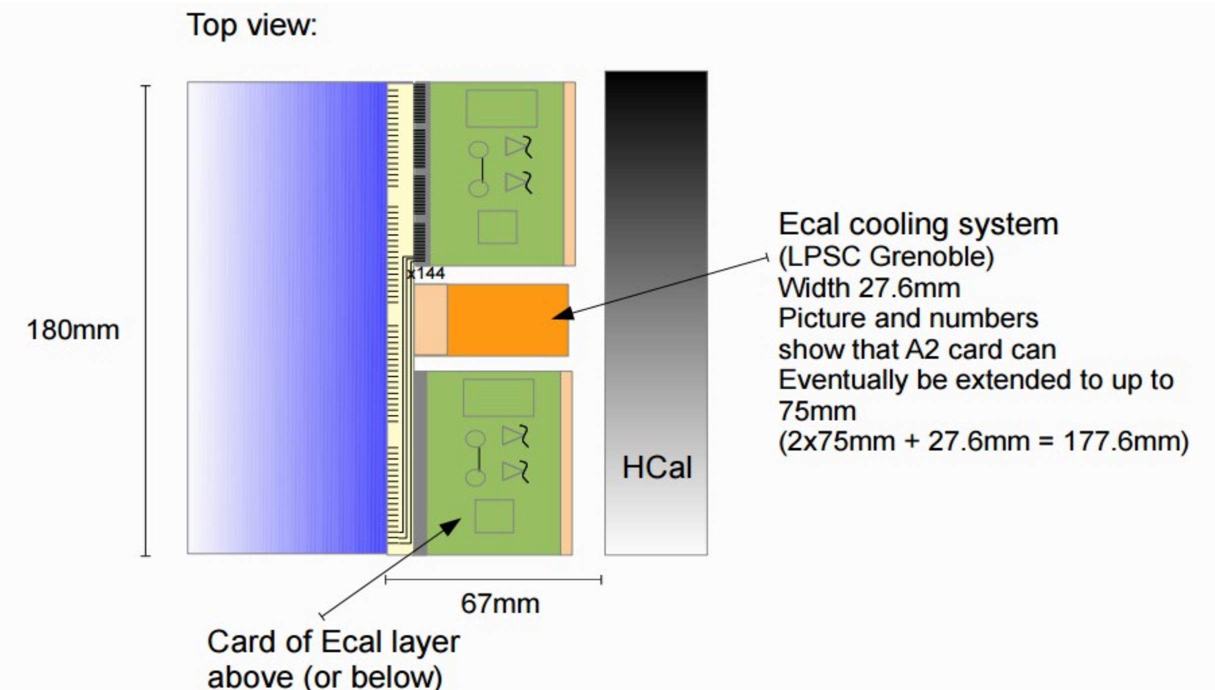
Space constraints for the Active Sensor Units (ASUs):
Maximum Height for Electronics (including PCB): depends on number of layers (20-30?)
For final design: x.x mm ?
For prototype: (PCB + components for the **SKIROC-2 BGA option**) : **~ 3mm**
Current ASU Electronic board design:
Last PCB Height (FEV 11**): 1.6 mm** , FEV12 : xx mm??
SKIROC BGA height: **1.4 mm**
Total : 3 mm

Space constraints for the Slab Intercace Board (SL-Board):
L-shape (even and odd ASUs) Dimensions: see below.
Maximum Height: **~ 12 mm**

ECAL Services

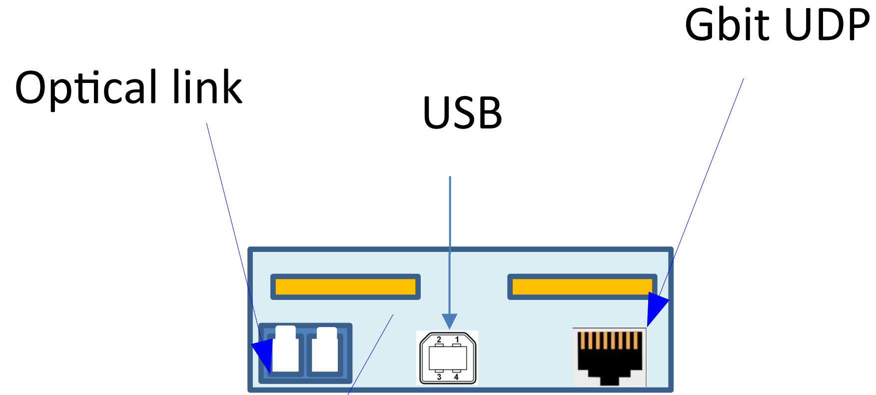






Maalmi/Jeglot/Breton

Control and readout electronics



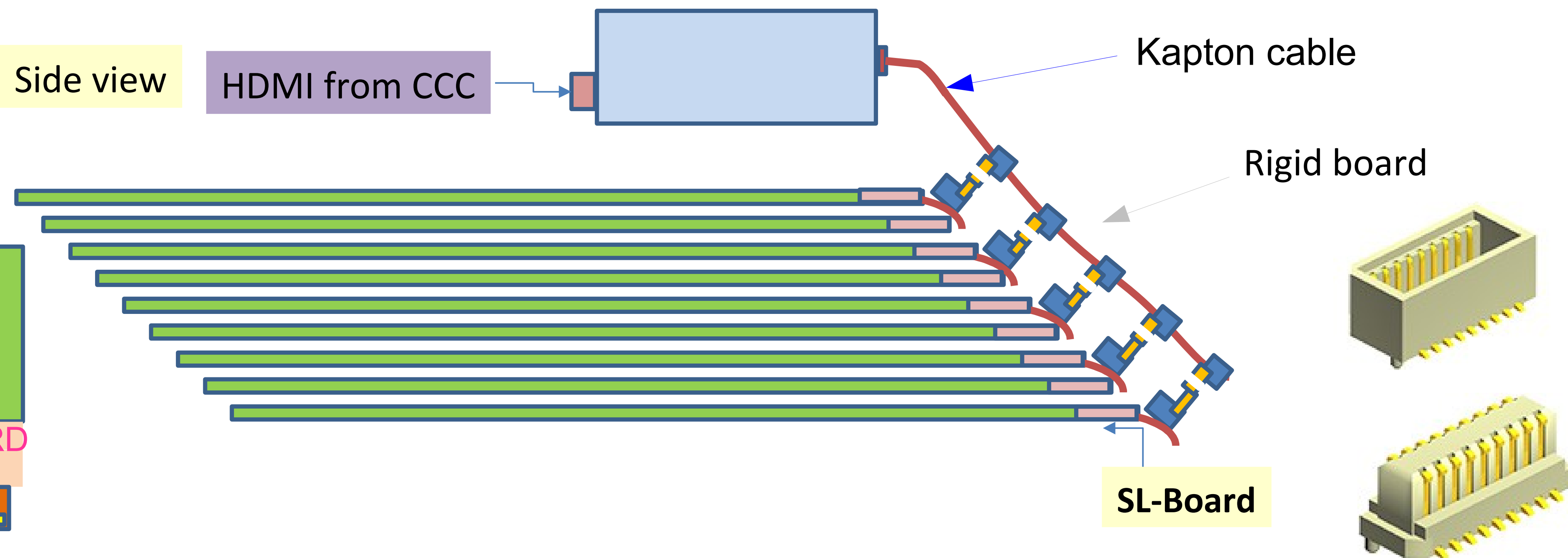
CORE Module : Control & Readout Module

Hirose FX18- 100 pin, 0.8 pitch

The development for the control and readout electronics are based on :

SL-Board :
It's the digital interface board situated at the extremity of the Slab, based on a MAX10 FPGA, which handles:
- Control & readout of the chained ASUs (SKIROC interface)
- Interface to the CORE acquisition module through a kapton cable in order to have flexibility for the connection inside the detector (45° angle constraint)

CORE-Module : Control & Readout module that handles a column of Slabs, for the prototype phase.



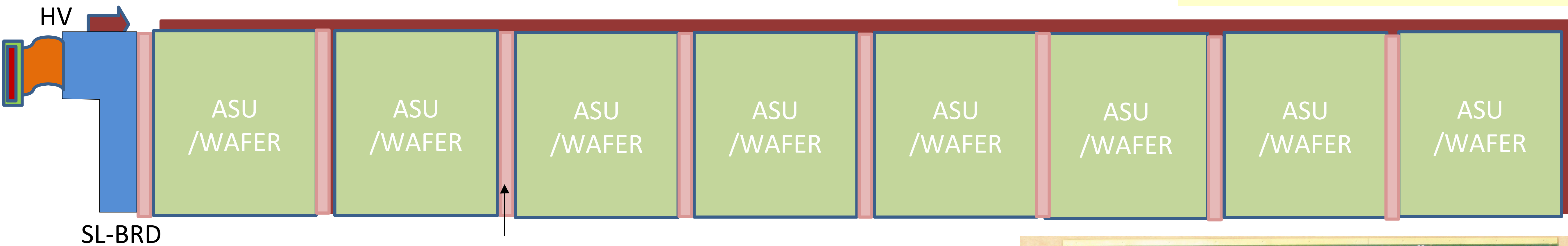
SLAB extremity

The Acquistion Module

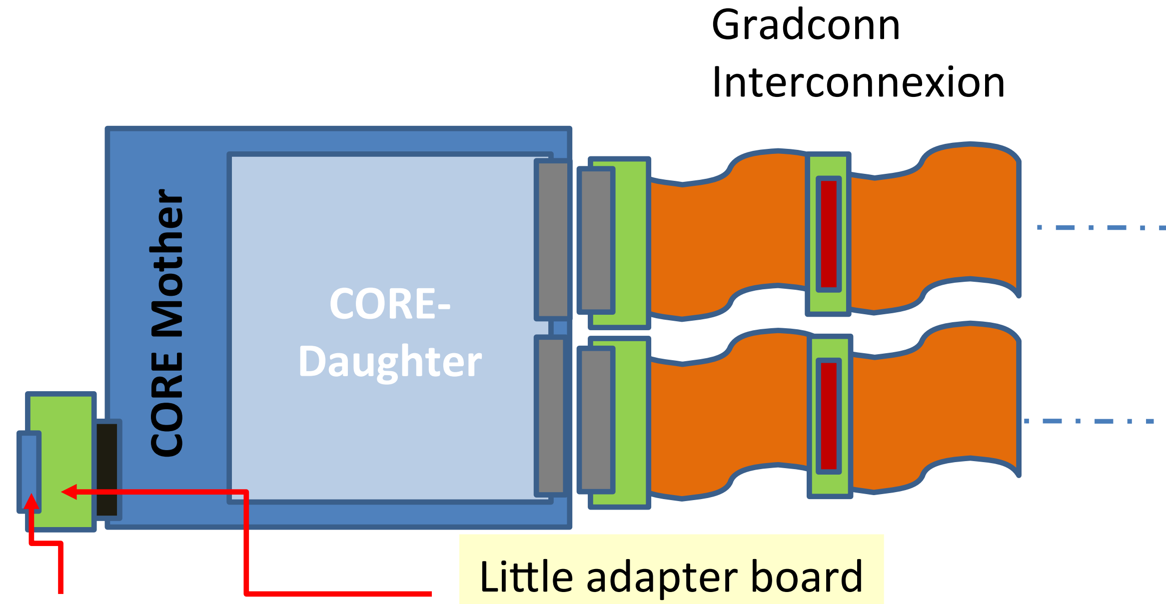
The Control & Readout Acquisition system will be based on an **existing mother board** that handles:

- Control & Readout through **USB/Ethernet/ Optical fiber**
- Distribution of clock and fast commands

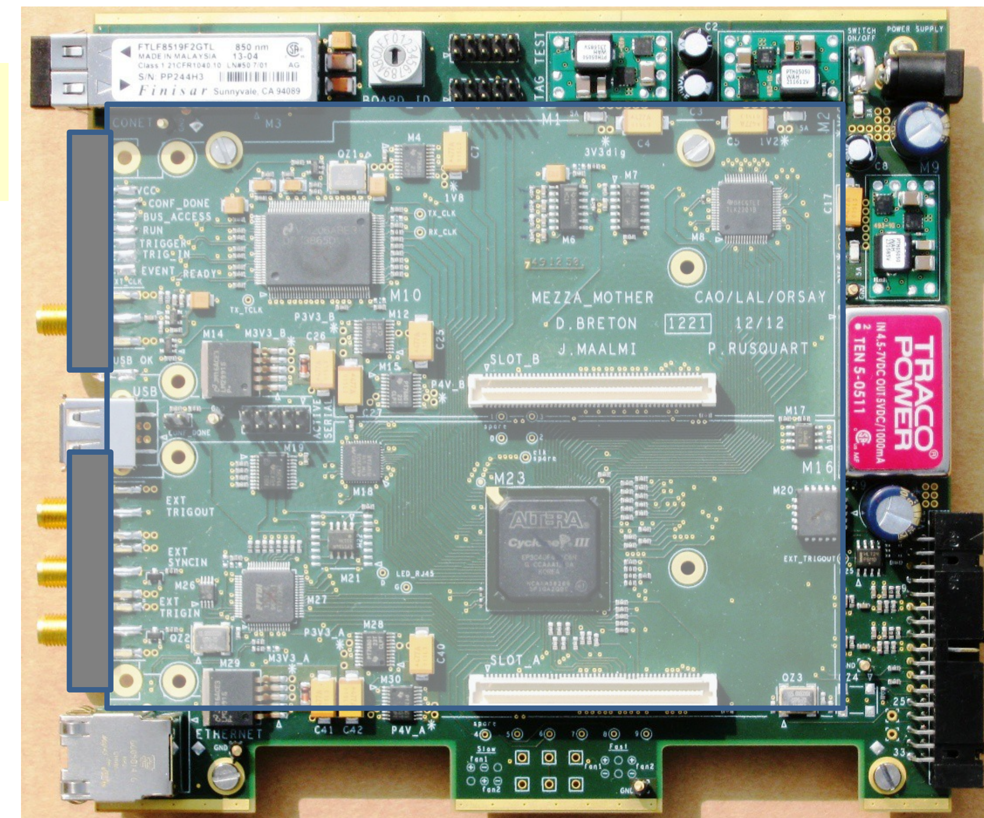
- There are existing low level **C-libraries**. (LAL-ML protocol)
- This LAL development is already used for other experiments.
- The **Detector specific CORE Daughter board is under developement** as well as the rigid **board**



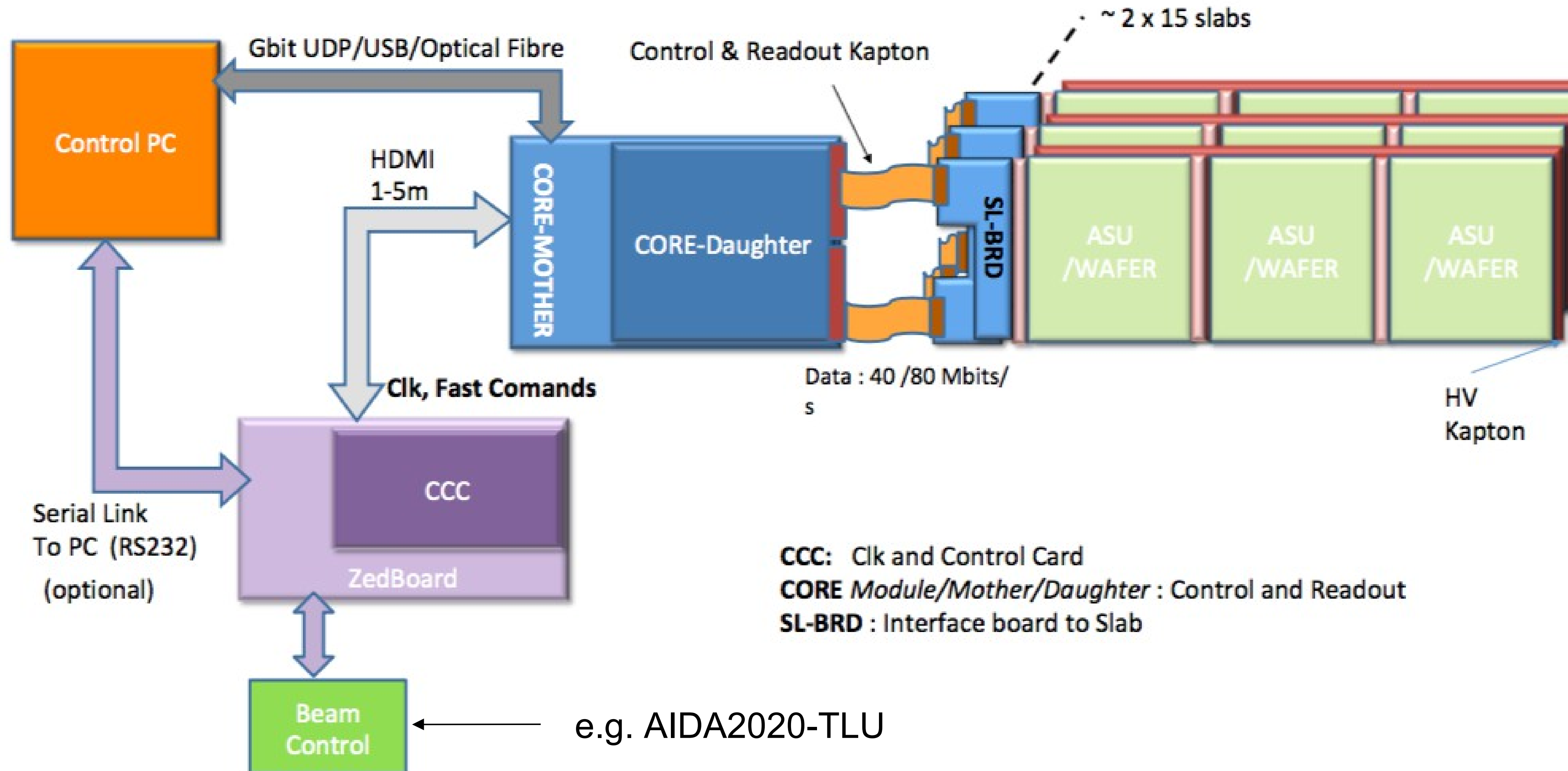
Gradconn Interconnexion



Existing CORE MOTHER



Global Architecture Scheme



e.g. AIDA2020-TLU

- Overall design
- .... compatible with ILD constraints
  - Little space consumption for connection between slabs and CORE Modules
  - CORE Mother can be placed at e.g. forefront of barrel, Daughter between Ecal and Hcal

- ... assures compatibility with other AIDA2020 developments

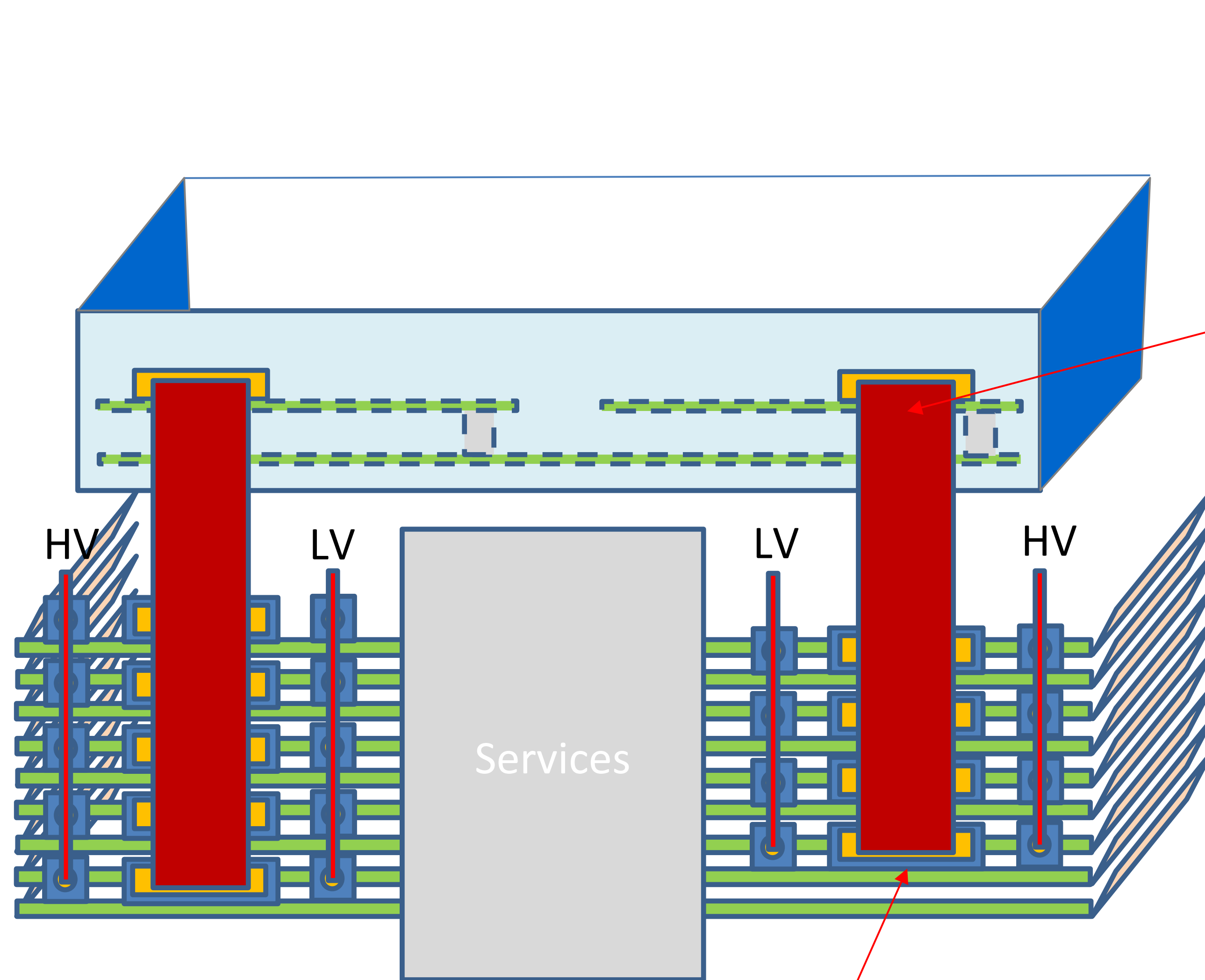
=> Paves way for combined beam tests (other calos,trackers etc.)

- Expect first version of system to be in place for Spring 2018

- SL-Board is delivery for AIDA2020 and P2IO/HIGHTEC

Control and readout signals

Core Module connector:
7 common differential pairs for sensitive signald, *30 individual pairs* for control and readout, 14 common lines, GND



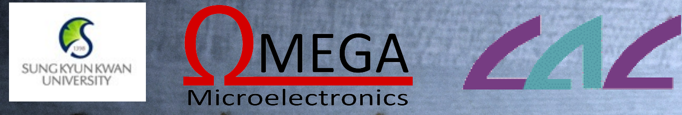
SL-Board Connector
7 differential pairs for sensitive signals, 2 individual pairs for control and readout, 14 common lines, GND

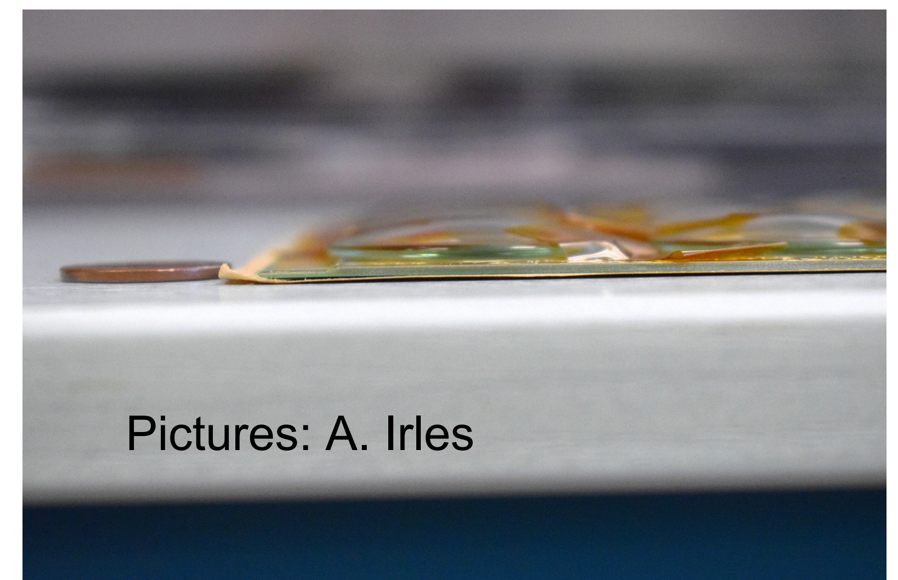
Group	Signals
	Clk
	Trigger
	Start/Stop
	Busy
JTAG	Control
JTAG	TCK
JTAG	TMS
JTAG	TDI
	TDO
SPI	SCK
SPI	SDI
SPI	SDO

Signals
Rx_i
Tx_i
Spare …
GND …
ADD[0]
ADD[1]
ADD[2]
ADD[3]

Full design of ILD compatible electronic services started that includes parts described above

News from FEV_COB





- Metrology of "mechanical" boards
  - Planarity < 0.5mm: 1 out of 3 slightly of specs
- 10 PCBs ready since beginning of December 2017 (SKKU/EOS)
- 4 PCBs delivered to LAL in January 2018
- 2 PCBs bonded at CERN at beginning of February 2018
  - Contact with local platform in Paris region
- Some quick (non-conclusive) tests before departure to Asia
  - Debugging starts after ILD Meeting
- First COB Version that should be equipped with Si Wafers

Summary and conclusions

- Progress towards assembly chain for Ecal and compact digital readout
- Both are deliverables for European project AIDA-2020 and P2IO project HIGHTEC
- Main change in assembly procedure w.r.t previous scheme:
  Exchange of interconnection Kaptons by flat connectors
  First tests will address long slabs with simplified ASUs
- All proposed solutions are applicable to existing hardware and to ILD
  ... designed with system aspects in mind
  ... r/o electronics will fit into tight space between end of slabs and Hcal
  ... first exchange to take into account constraints of cooling system
  ... next step: different ASU sizes may allow for even a higher level integration
- Design phase finished and heading for production of components
- Expect upgraded assembly bench to be in place in March
- First version of compact readout electronics during Spring 2018
- Integration of components developed within AIDA-2020 will allow for smooth integration with other detector prototypes
- New version of FEV11_COB to be equipped with Si wafers for validation of technology
  (Reminder still the only PCB design that could cope with current ILD constraints)

Backup

Power-Pulsing:
New ultra-flat Capacitors!

We propose to use new ultra-flat capacitors to distribute over the ASUs, this will permit:

Peak current reduction: especially through the connectors
No more voltage drop along the slab
Homogeneous peak power dissipation during power pulsing.

We go from the 400 mF capacitor/ 12A (peak Current) for the whole SLAB to 140 mF / 1.2 A per ASU.

Reminder of power consumption values :

- DVVD (3.3V) 11 mA / Chip, Total 300 mA
- AVDD (3.3V) / Chip : 77 mA during ACQ, 20 mA during Conversion, 0.01 mA idle

- Distributing the capacitors along the slab permits reducing current between ASUs with a factor ~50-100.
- The current peak is local.
- The current delivered for charge reloading of the capacitors will be limited at the extremity of the Slab