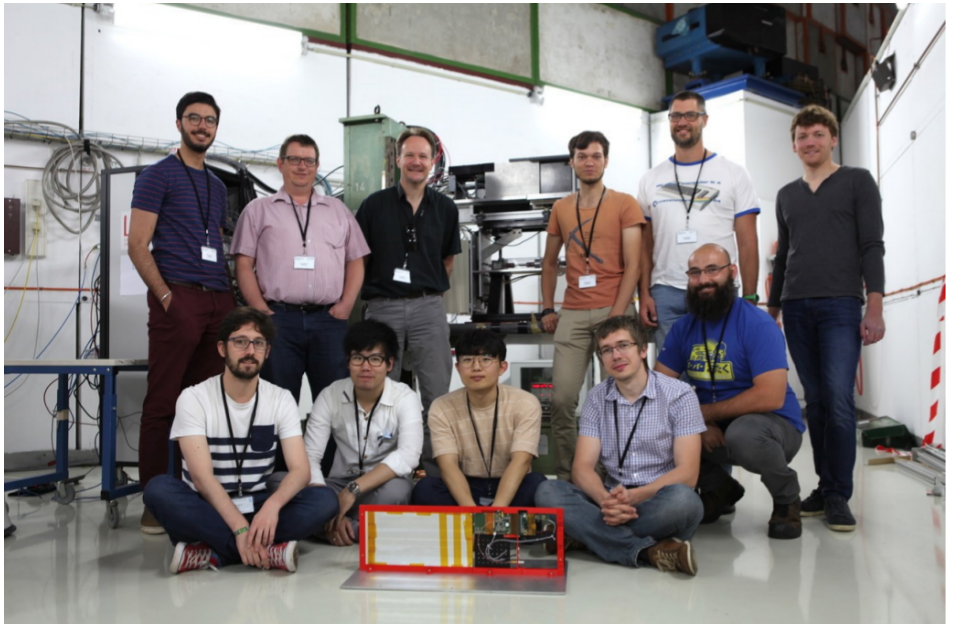
Si-W ECAL Test Beam 2017 analysis

A. Irles, LAL

19th February 2018, ILD ECAL pre-meeting

Outline

- Commissioning summary and new procedure
- Beam Test performance
  - Retriggers
  - SiW-ECAL → Si-tracker performance
  - Pedestal evaluation in electromagnetic shower events.
  - SiW-ECAL: first look to energy measurements.
- Summary

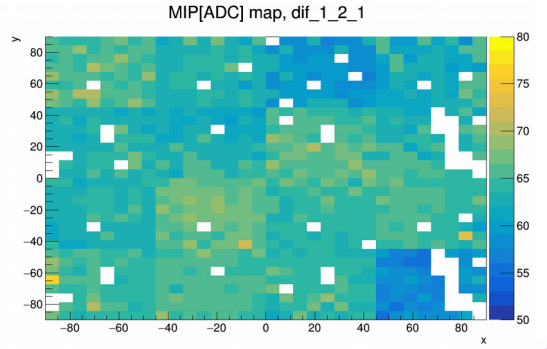


Commissioning: passport delivery

- We had defined a commissioning procedure and passport delivery system for the beam test to:
  - Find, understand and isolate noise sources.
  - Define the set of **optimal working parameters** (trigger threshold, spill, gain, etc…)

Two different noise sources have been found:

- Noise “bursts”
  - Affecting all the slabs
  - at the end of long spills due to grounding loops when two slabs where in electrical contact through the structure
  - **solved by improving the single slab electrical isolation** (and, in addition, by using short spills in beam test)
- Noise “sparks” (or ADC=4 – underflow - channels)
  - associated with cross shape events, double pedestals
  - **solved by an agressive masking procedure** (**all** number **37 plus** an common list of **5%** of the channels)
  - After beam test observations: these channels present some issues in the routing (pad to PCB)

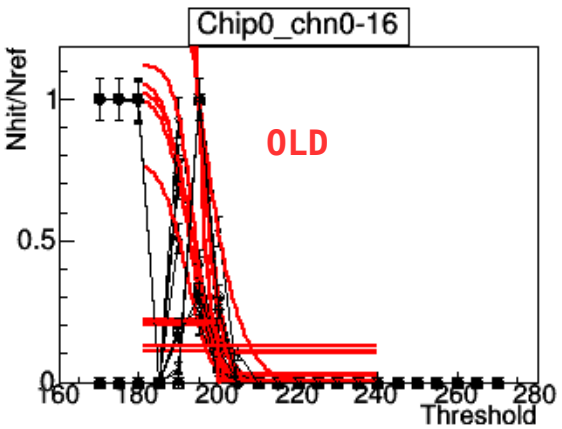


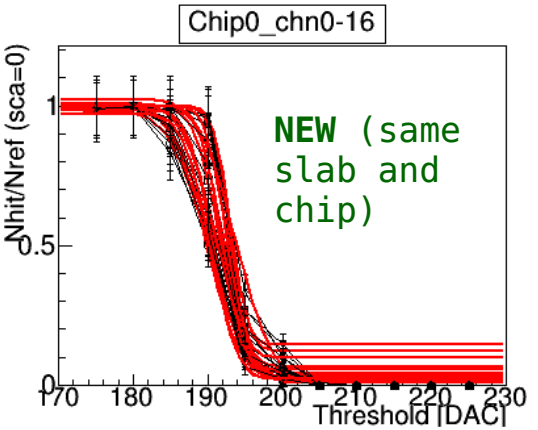
Settings and statu of the slabs for the TB2017

- 7/10 slabs passed the passport control.
- Layer 1, Slab 21 → 43.4% **(one wafer+1 chip)**
- Layer 2 – 6 , slabs 16,-21 **~6-8%**
- Layer 7, slab 22, **~ 16% (one chip)**
- 5% are masked manually just before starting the commissioning → same patter in all slabs:
  - Chn 37 in all chips; Chn 41-53, chips 1,9; Chn 5, chips 0 and 8; Chn 3, 9, 10, chip 7 and 15;
  - Conservative selection!
- Total # of channels available: 6204 (87%)
- Once the noise was under control, the next step is the choice of the working settings. Most of them taken from Omega or previous test beams:
  - Spill settings: 5 Hz, 3.7 ms width (0.9 start acq + 0.5 val evt + 2.3 ms)
  - Gain: PA = 1.2pF, CC=6pF (cc does not afect to the gain)
  - Threshold >= 225/230 DAC (chip based)

Improved commissioning procedure

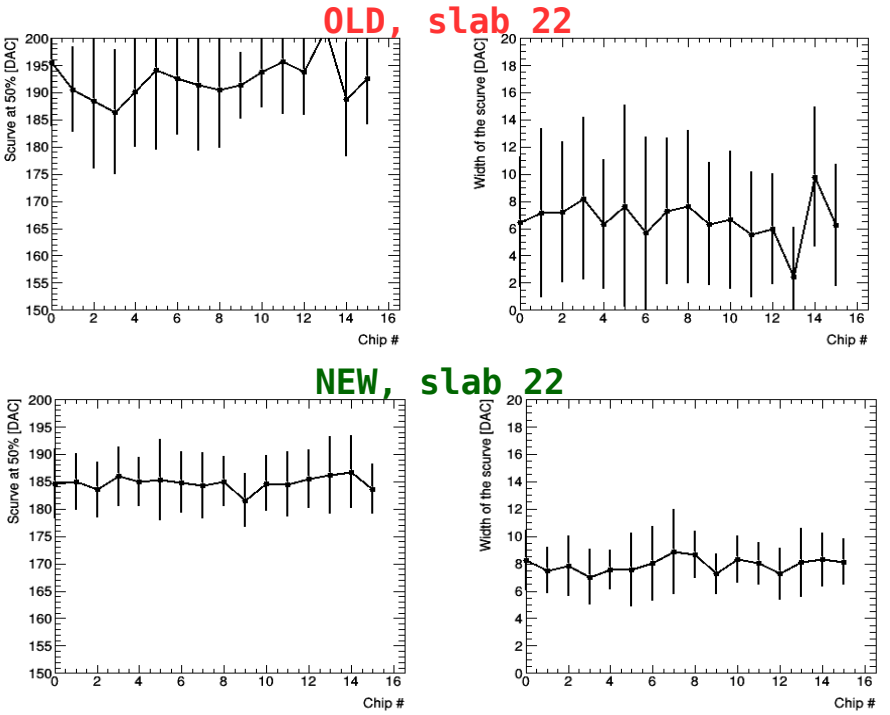
- A lot of debugging (data integrity, data conversion, etc)
- Understanding of the noise sources: specific search of spark sensitive channels (ADC=4 channels).
- Optimize algorithm and timing criteria (spill width is very important when looking for noise sources). Recursive method:
  - Relatively high trigger threshold: mask the most noisy ADC=4 channels, then the "super noisy" channels (1 per mill or less!), then perform fine search using cosmic rates.
  - Perform the scurve analysis and select the optimal threshold
  - Repeat with chip wise trigger threshold: most of the steps of the first iteration with the optimal thresholds.





Improved commissioning procedure

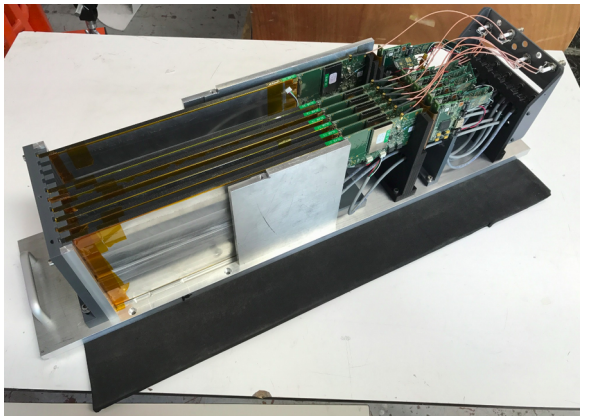
- Improvement for
  - Slab 18: from 75 to 45 noisy channels masked
  - Slab 19: from 72 to 33 noisy channels masked
  - Slab 22: from 173 to 48 noisy channels masked
  - From ~8% to ~4%
- It is better established (and tested)
- It will make easier the channel-wise threshold optimization (sk2a)
- It is generic and flexible
  - usable for short and long slab
- Includes calibration and pedestal analysis!
  - With cosmics or source
- Between 0.5-2 h in total
- Already in pyrame3: features/calicoes3_commissionings
- Twiki (work in progress!) https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY201706Commissioning

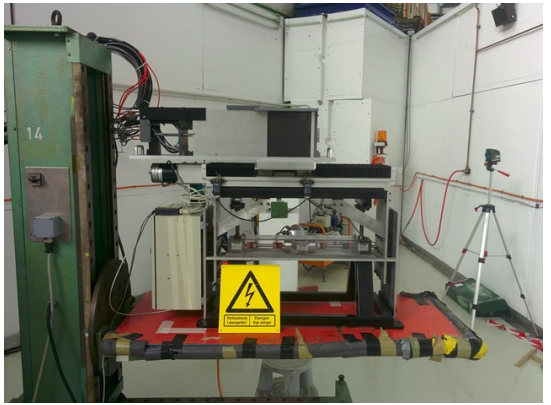


Test Beam at DESY

- **Setup** :
  - 7 short slabs (over 10): 6 FEV11, 1 FeV10 each equipped with 4 325um Si wafers and 16 Skiroc2
  - Power pulsing and ILC mode (emulated ILC spill conditions)
- **Physics program:**
  - Calibration run with 3 GeV positrons perpendicular beam without tungsten absorber plates
  - Calibration run with 3 GeV positrons in ~45 degrees (6 slabs)
  - Magnetic field tests with 1 slab (up to 1 T) in the PCMag
  - Electromagnetic showers program.

    Scan of energies with different W repartititions





~~SiW-ECAL~~ → Si-”tracker”

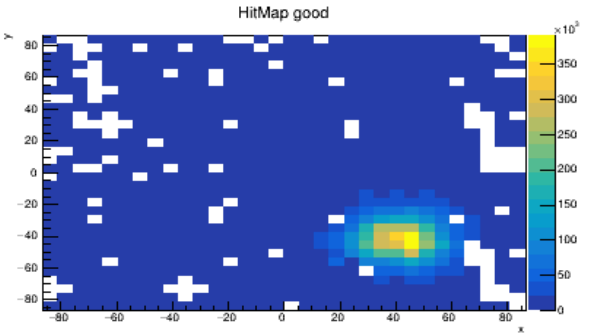
- Results for the SiW-ECAL acting as a tracker (w/o W)
  - Retriggers
  - Pedestal studies
  - MIP calibration and S/N results
  - Tracking MIP efficiency

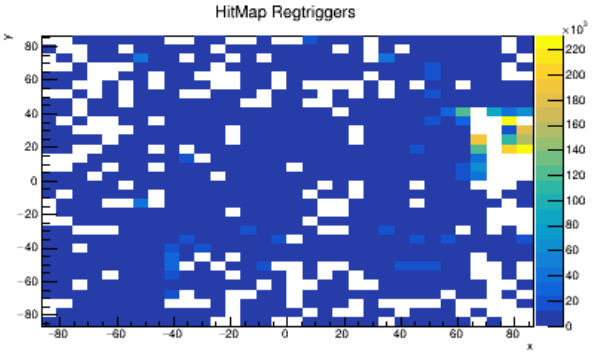
SiW-ECAL

- Results for the SiW-ECAL
  - Pedestal stability in shower-like events
  - First look to shower energy (not to be included in the technical paper)

Retriggers in beam test

- We observed during beam test and commissioning the appearance of retriggers:
  - Fake triggers filling several SCAs with consecutive bcids
- They are located in areas of the PCB **far from the beam spot** (also in **different BCID than real events**)
  - Retriggers rates in chips in the beamspot ~1.5 % or lower which are easliy filtered. No impact in the mip reconstruction efficiency (slide 16)
  - Retriggers rates in chips far from the beamspot ~ 30-40%
- Collective/cross talk effects in the PCB ? Baselines shifts ?
- Hints that skiroc is not the origin of this:
  - FEV10/11 performs better than FEV8
  - Retriggers are not observed in skiroc testboards.
  - Not related to preamp power supply





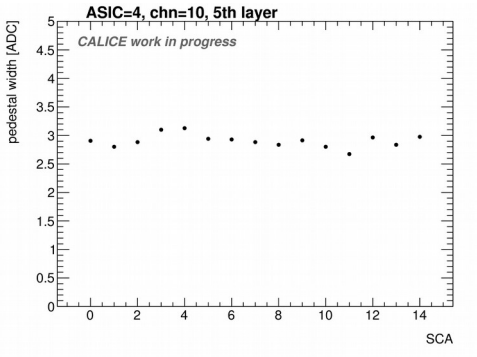
- The **retrigger issue is not problematic for BT** (well isolated & fitlered).

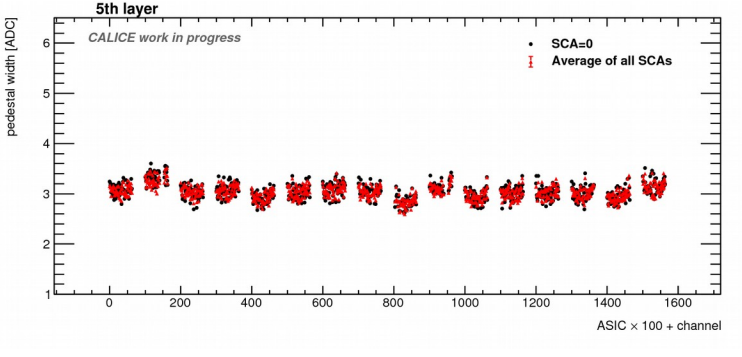
Pedestal calculation

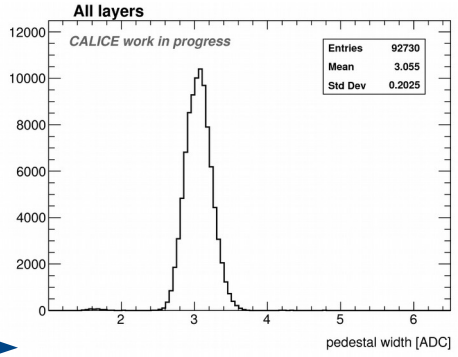
- Pedestal and noise (pedestal distribution width) calculation for all layers using the calibration run

One channel | **One layer** | **Full prototype**

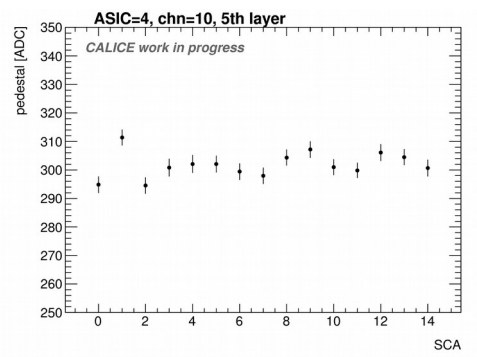
noise

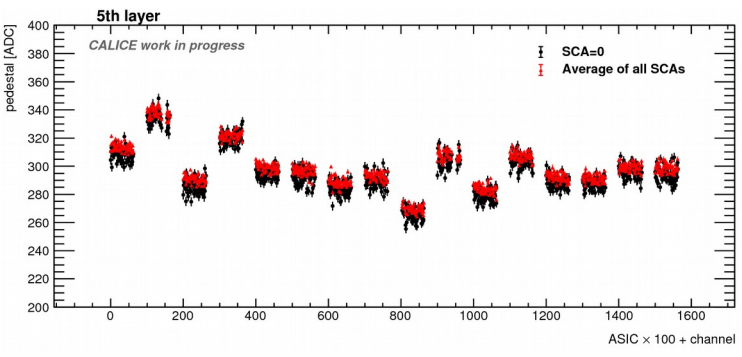


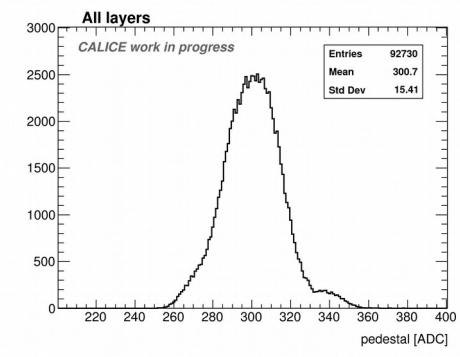




pedestal



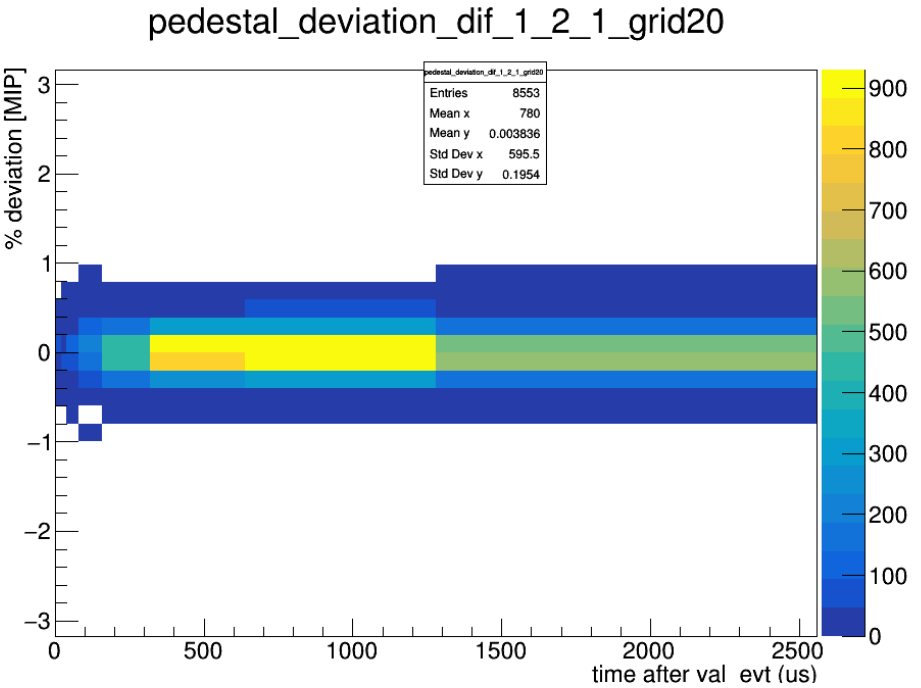




- Very **homogeneous noise response** (3 ADC ± 6.6%)

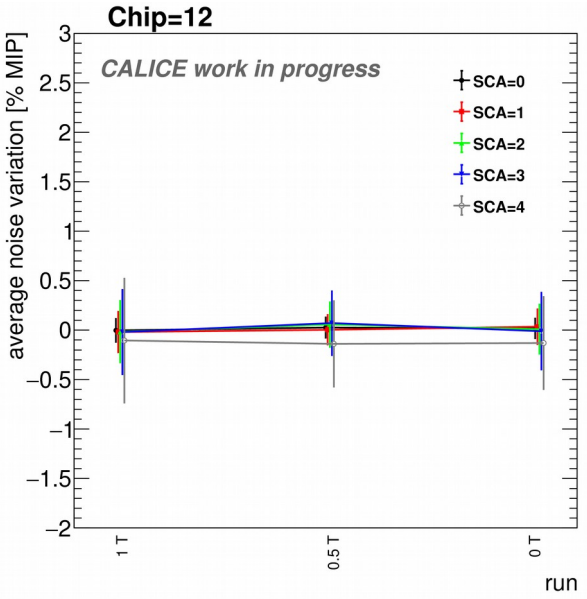
Pedestal mean position for different times within a spill

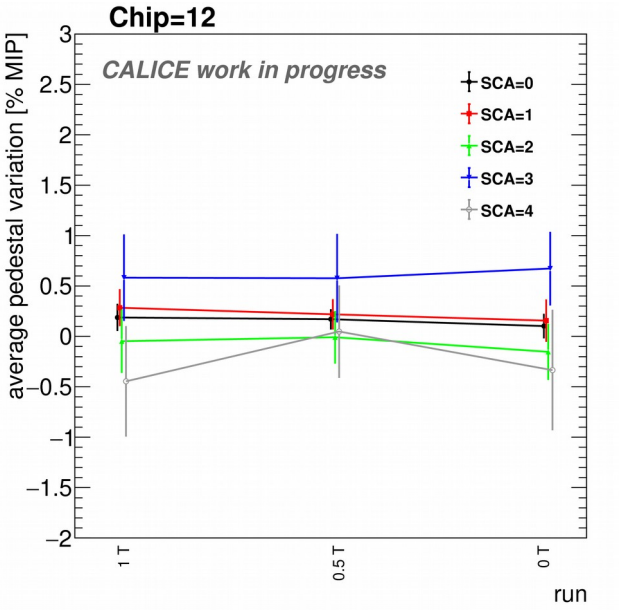
- Pedestal distributions are built in different bins of time (using BCID value) within the spill.
- Deviation is shown in units of ~MIP
  - assuming MIP at ~65 ADC
  - Reference calculated using all bcid ranges together
  - In the plot: one entry per channel and SCA.
- Pedestal value remains constant within 0.2%MIPs
  - Similar results for all slabs/grid points



Pedestal & noise stability in magnetic fields

- Test of layer1 (slab 21) in the PCMag. Beam pointing to chip 12.





Ref. Run with beam, B=0T: (50 min)

- *B=1T: (13h)*
- *B=0.5T (3h)*
- *B=0 T (1h)*

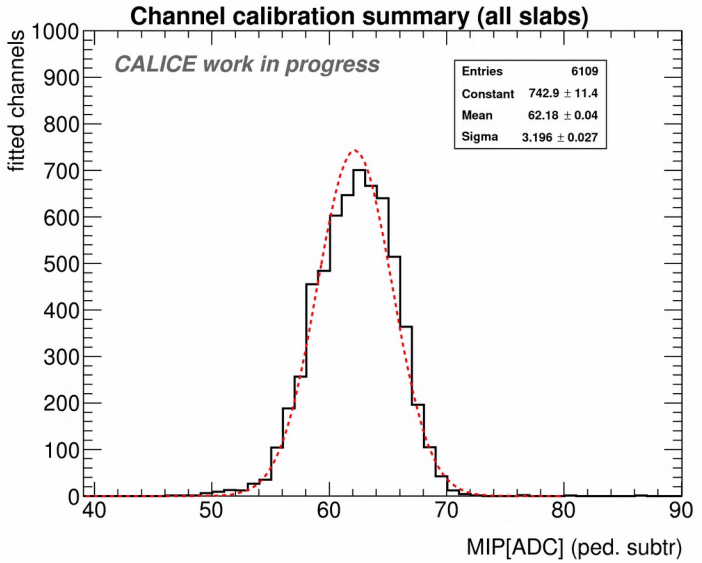
Reminder: 1% of MIP ~ 0.6 ADC

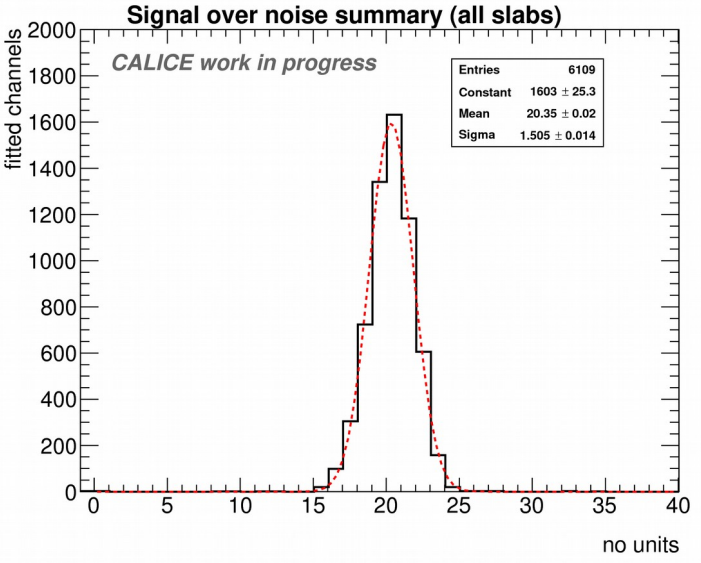
- The pedestal position & noise levels is stable for operation in 1 and 0.5 T after ~20h of run in PowerPulsing mode.

Calibration

- MIP calibration: **fit** the **98%** of available channels
- **MPV** = 62.2 ADC, sigma= 3.2 ADC **(dispersion of 5.1 %)**
- **S/N = 20.3,** sigma = 1.5 (7.4 % dispersion)

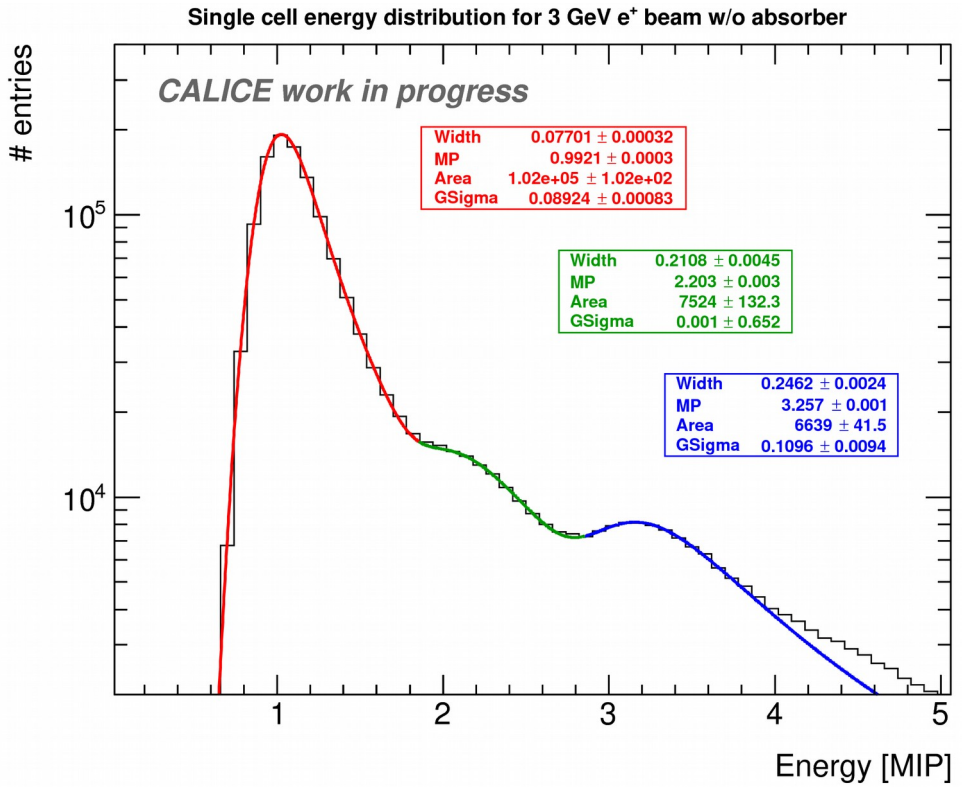
(MIP position – pedestal position) / pedestal width





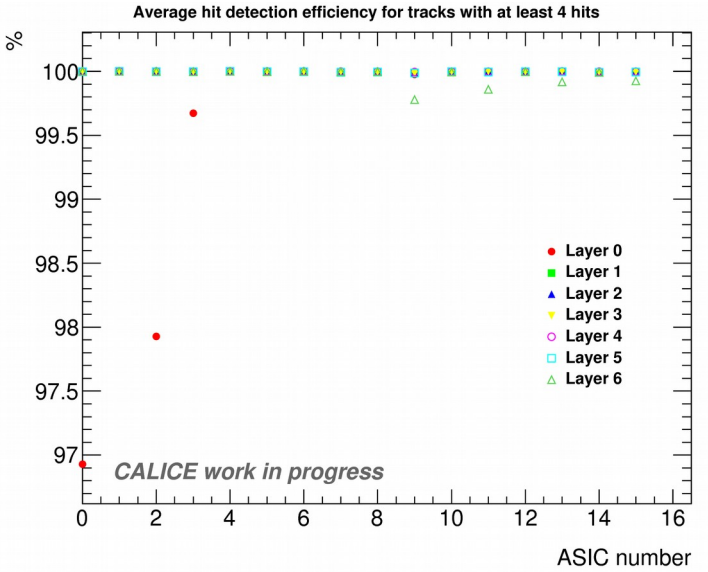
Calibration

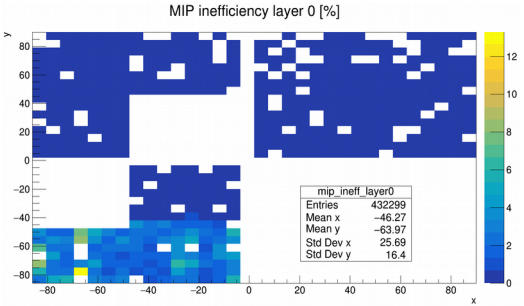
- Using these calibration values and enhancing the stats putting all cells together in one histogram we can fit the 2&3 MIP peaks (2 or 3 electrons crossing together)

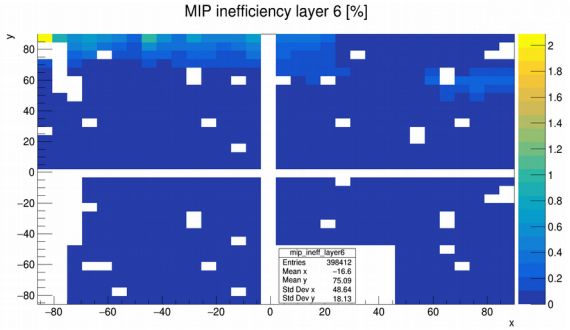


Tracking efficiency

- Assume “perpendicular” track events with at least 4 hits and check every layer if it has a trigger or not in the track path
  - Only small differences if 3 or >4 minimum hits
  - “perpendicularity” definition allows for ± 1 channel of margin
  - Masked channels / chips excluded from the analysis
- Inneficiency definition includes the pure trigger inneficiency and the blindness of the detector due to saturated memory.
- “Perfect” efficiency for most of the chips
  - Few “inefficient” chips in the first layer –> retriggering not under control in these chips ?
  - Small innefficiency in the last layer for outlier channels.







Pedestal study for electromagnetic shower events

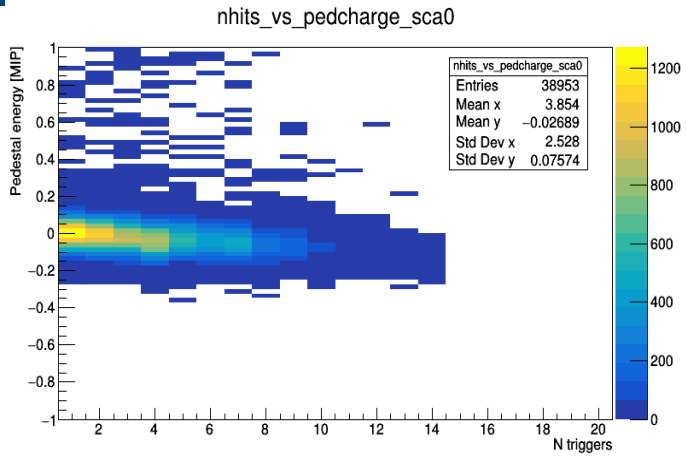
- We study data files from the Tungsten program → high charge deposition events
  - For simplicity, we use the second tungsten configuration files and only one chip in the beam spot (the 12)
- We use “reconstructed” data files:
  - Pedestals calculated from calibration data are subtracted.
  - MIP calibration is applied.
- We recalculate the pedestals for shower-like events:
  - At least 6 slabs with hits with E>0.5 MIP and bcid< 2850.
  - With these events, we recalculate the pedestal (should = 0) for all channels and SCA with enough statistics (at least 50 entries)

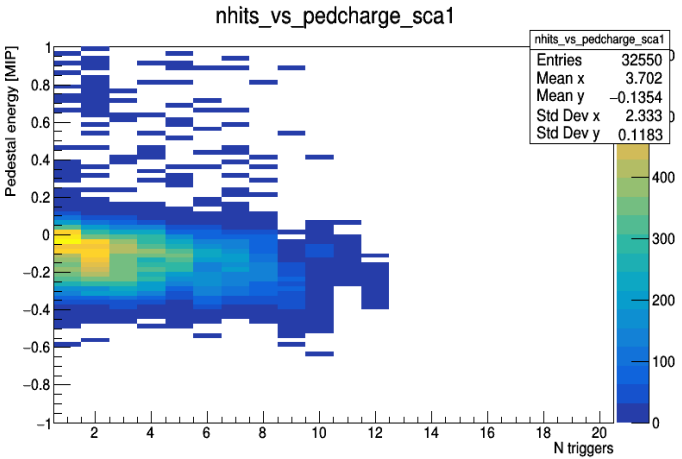
    Not fit to gauss, only using Mean and RMS of the histogram.

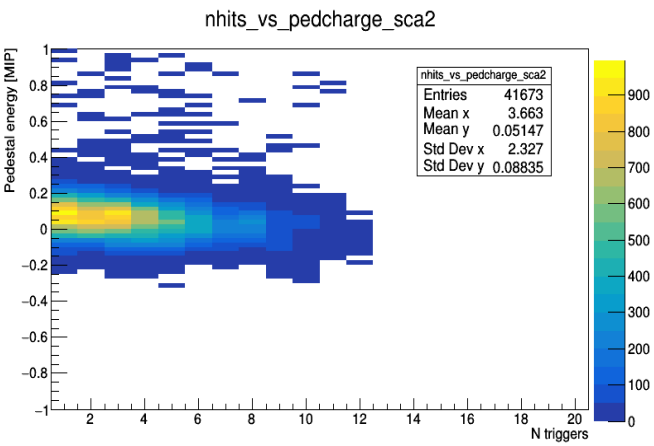
- Then we apply the new values to the data → “resubtraction”. All deviations of pedestals will, therefore, measured in MIP units.
  - If not pedestal is recalculated, we use the calculated in the original calibration run.

Pedestal vs number of triggers

- Relation between total charge collected by the chip and the pedestal position?
- I study the correlations between the pedestal “hits” in [MIP] and the total number of triggers in the event (ONLY CHIP 12, third layer)



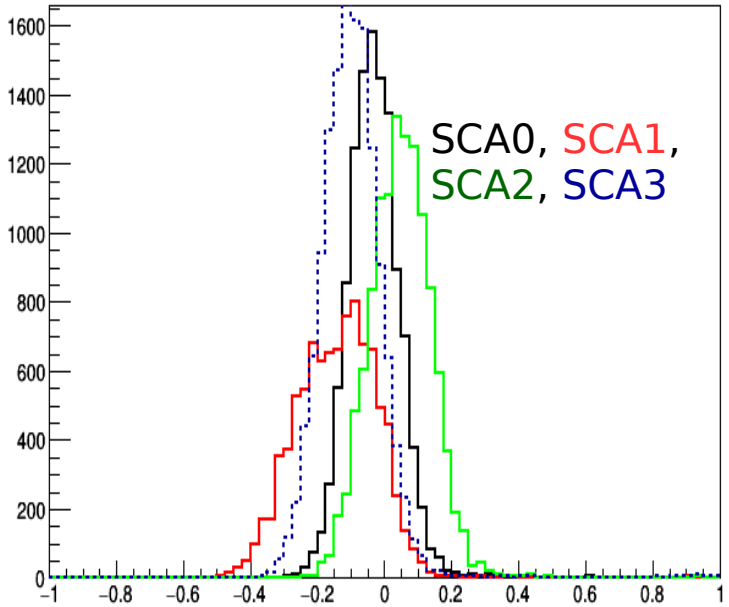


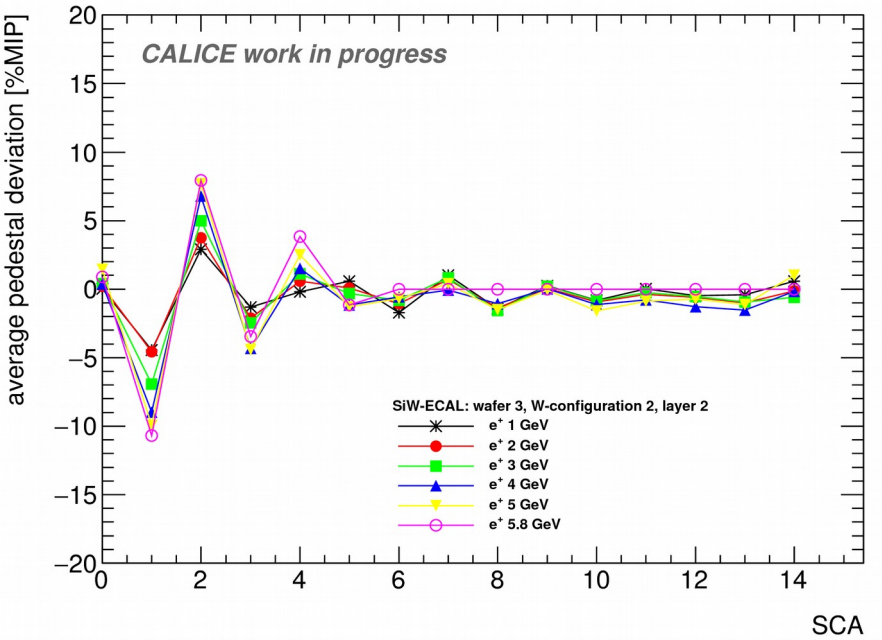


- **Correlation** between number of hits in the event and pedestal value: **more hits, lower pedestal values**
  - Expected (Stephane dixit) Coming directly from the preamp power supply.

Pedestal shift

- Repeating same kind of study but SCA based.
  - Conf2, 4 GeV electrons, chip 12
- Left: Pedestal distribution of one channel for different SCAs
- Right: Average of the pedestal deviation for all channels in chip12, third layer

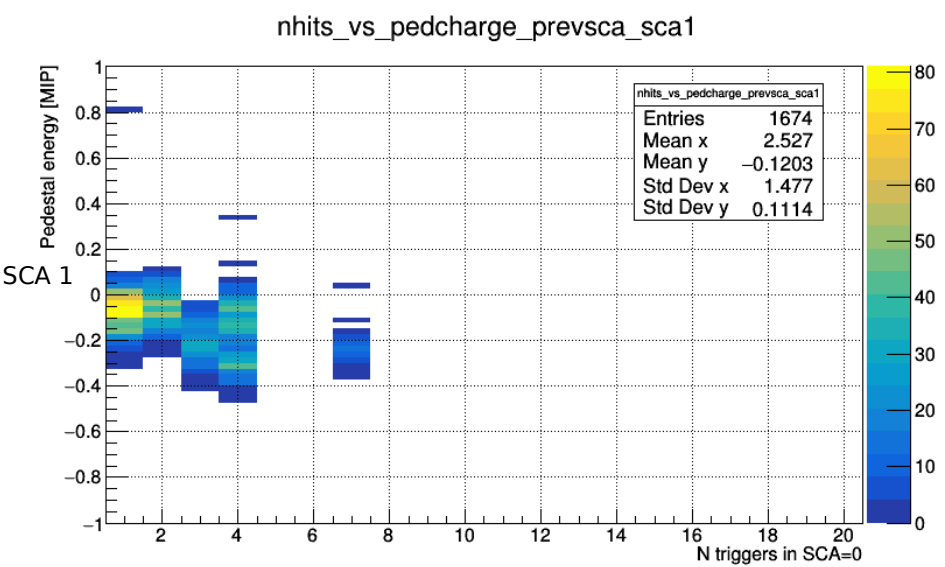


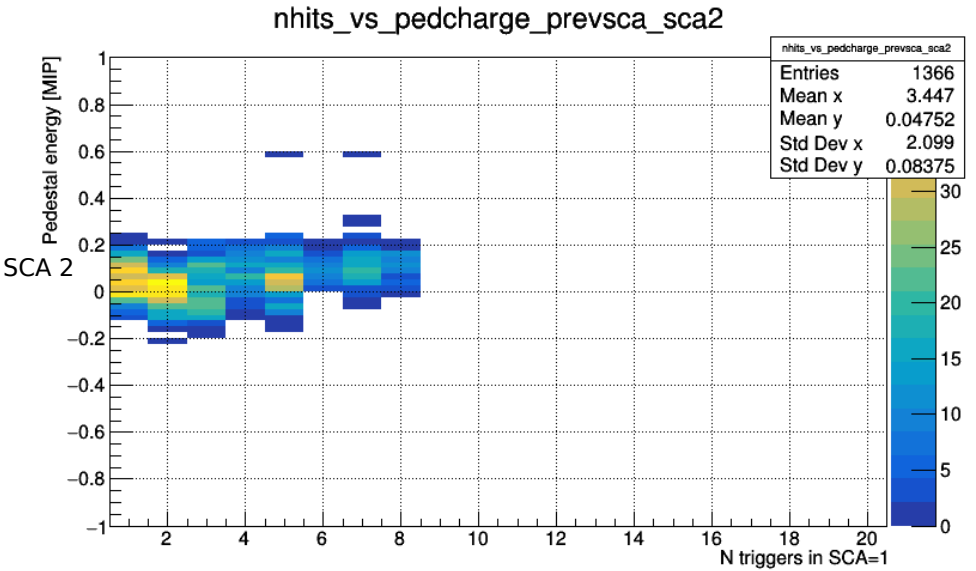


Reminder: 10% of MIP ~ 6-7 ADC

Pedestal vs number of triggers

- Relation between total charge collected by the chip in SCA X-1 and the pedestal in SCA X ? (ONLY CHIP 12, fourth layer)



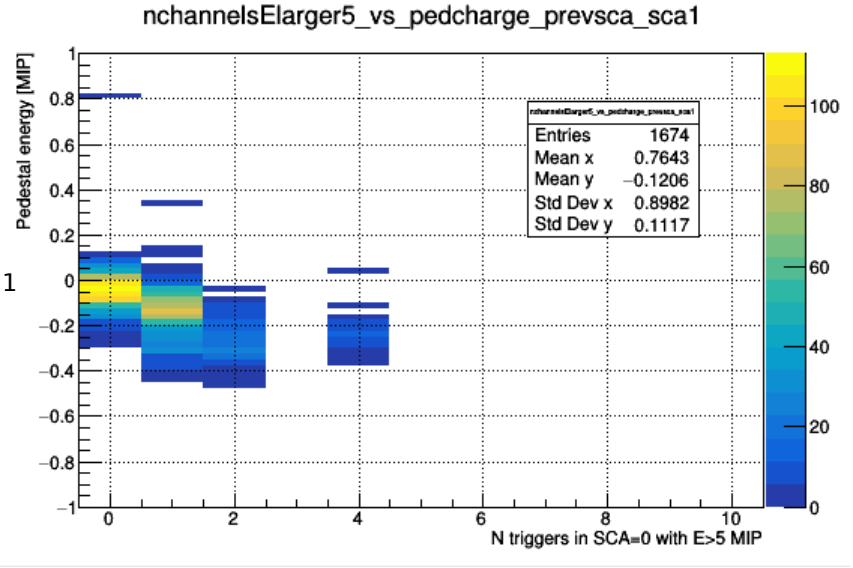


- The **global shift in pedestal for alternate shifts** seems to be **correlated with the amount of charge in the previous SCA:**
  - the more charge in SCA0, the lowest pedestal value in SCA 1
  - the more charge in SCA1, the larger pedestal value in SCA 2

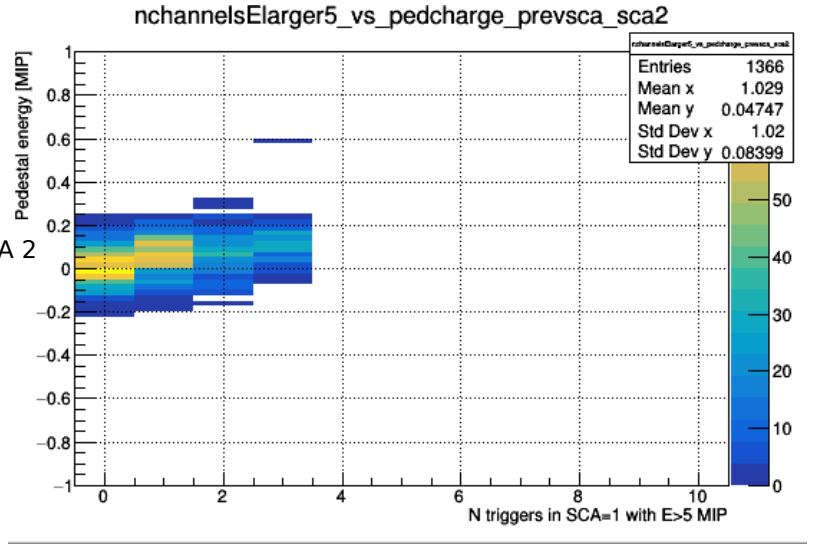
Pedestal vs number of triggers with high load

- This correlation is better seen if we plot the pedestal valu**e vs the number of channels that were triggered and collected “a lot” of charge (E> 5 MIP)**

SCA 1



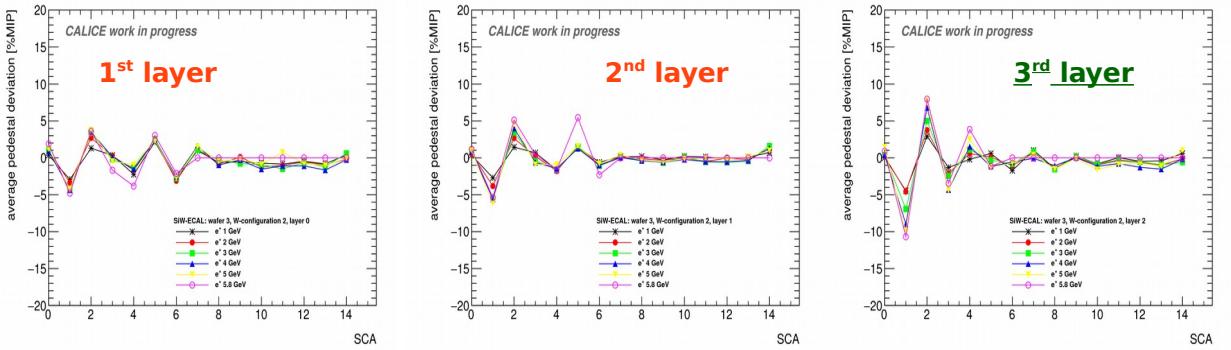
SCA 2

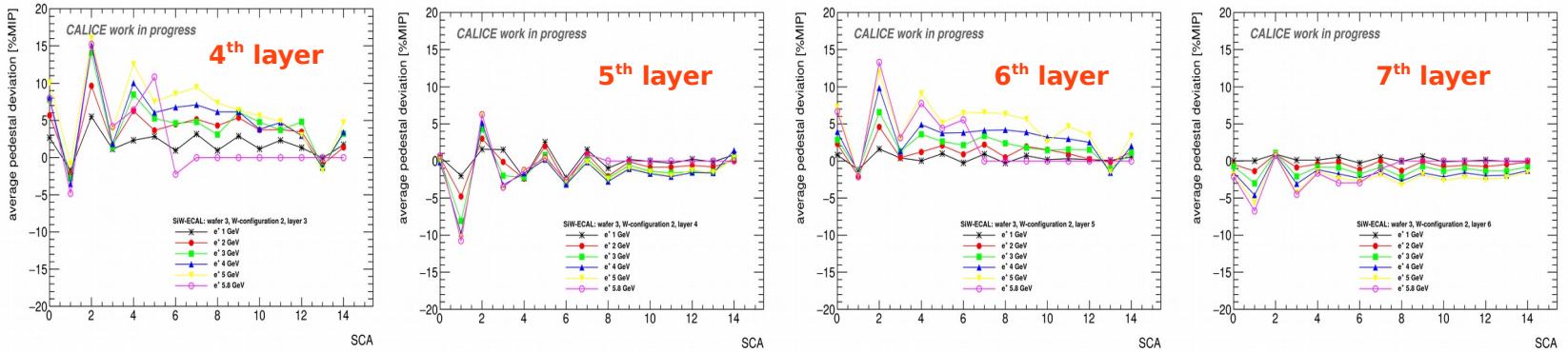


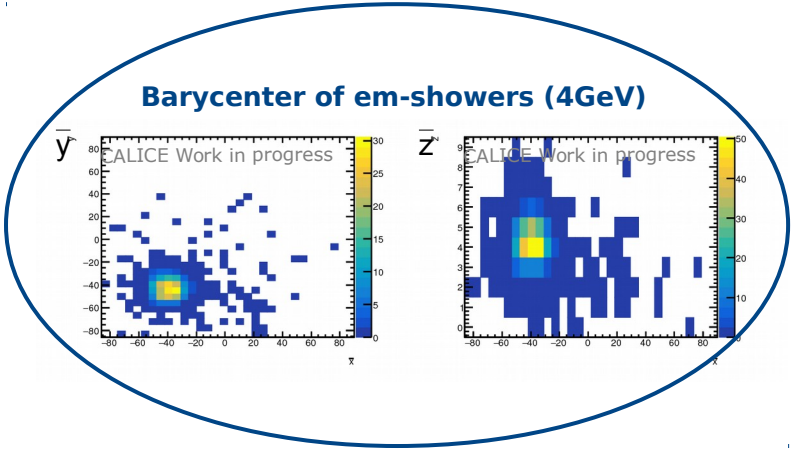
- The **global shift in pedestal for alternate shifts** seems to be **correlated with the amount of charge in the previous SCA. Specifically, with the concentration of high loads.**

Pedestal shift for all layers

- Similar energy dependence is present in mostly all layers
- Some layers have also shift in SCA0

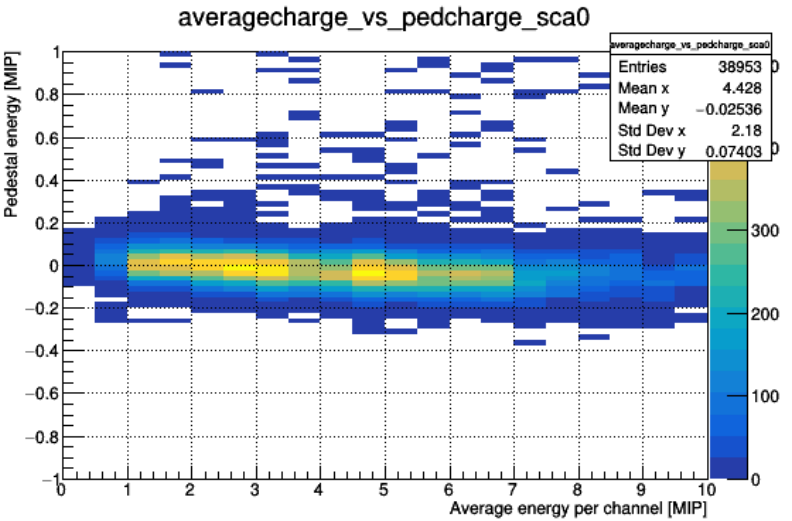




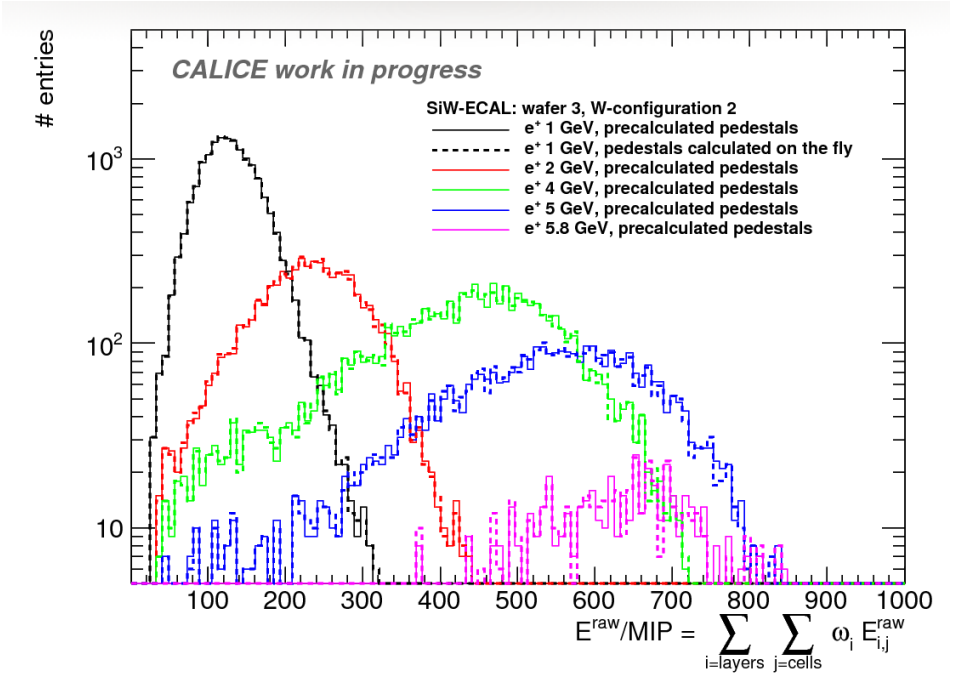


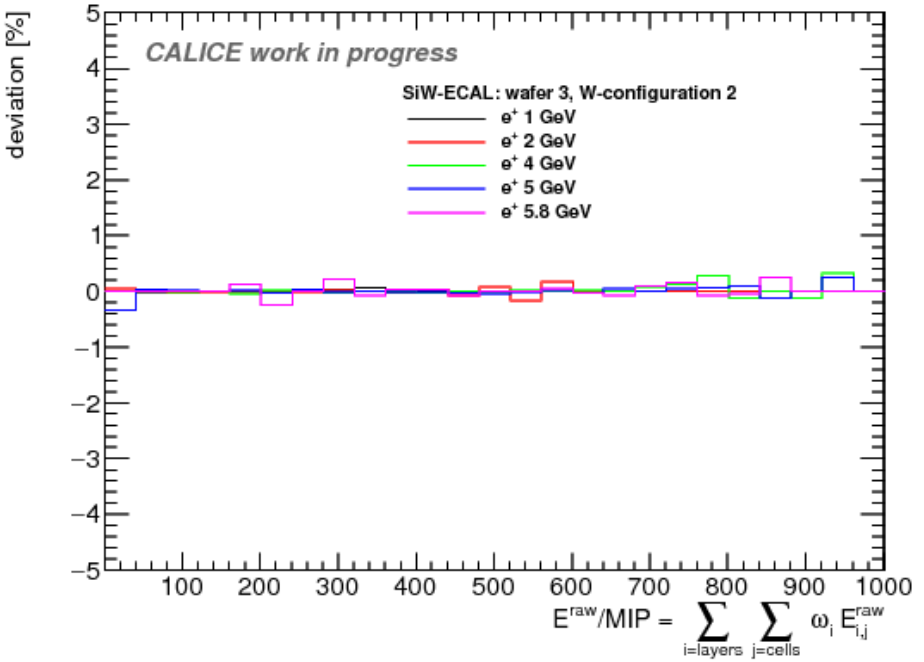
Energy reconstruction and pedestal shift

- How does the measured pedestal shifts affect to the Energy reconstruction ?
- We don’t expect large effects since:
  - The effect is different in every layer (following shower profile)
  - Shifts maximum of ~0.1 MIP and average deposition charge (for 4 GeV) ~> 3-5 MIP
  - The shift is alternated and slightly different in all layers (shift in SCA is compensated by shift in SCA+1, etc)



Energy reconstruction and pedestal shift





- **Energy reconstruction: the impact seems to be minimum** & compatible with statistical fluctuations

Pedestal stability on electromagnetic shower events: summary

- We know that a 5-10% [MIP] pedestal shift for high charge load events is expected due to the architecture of the chip itself.
- We don’t understand why there is, in addition to this, a global shift from SCA to SCA+1.
  - We see this happening also in channels with disable preamps.
  - Power supply issues… from other chips? → to be tested in beam by enabling only one chip.
  - Ongoing tests with charge injection.
  - More data checks in the back-up slides.
- The impact for energy calibration analysis in beam test is small.

Summary

- Principal noise sources are understood and a reliable commissioning procedure is available
- The results of the studies of pedestal + noise are excellent in terms of homogeneity and stability
- We have very good performance on B-field with unchanged pedestal and noise conditions.
- Very homogeneous calibration constants (5%) and a high S/N (20)
- Some issues still not understood on the pedestal evaluation in high charge load events –> not affecting the energy measurements for beam test.
  - Ongoing tests & more tests with beam (?)

- A technical paper about technollogical prototype cconstruction + performance on beam test is ongoing.
  - We have a meeting the 1st of March where I expect to circulate a first draft to be discussed with some sections (construction, DAQ, etc) to completed by the different parts.
  - https://indico.in2p3.fr/event/17025/

Back-up slides

Retriggering summary

of events (Grid 41, dif 1_1_2)

	All events	SCA = 0	Chip 3 or 10 (on beam)	Other chips (not on beam)
Empty event (0 hits)	20509 (9.5%)	10	13824 (11.7%)	6685 (6.8%)
Normal event (1-4 hits)	157589 (72.8%)	33595	102152 (86.8%)	55437 (56.1%)
Retriggering (>= 5 hits)	38517 (17.8%)	20	1756 (1.5%)	36761 (37.2%)
Total	**216615**	**33625**	**117732**	**98883**

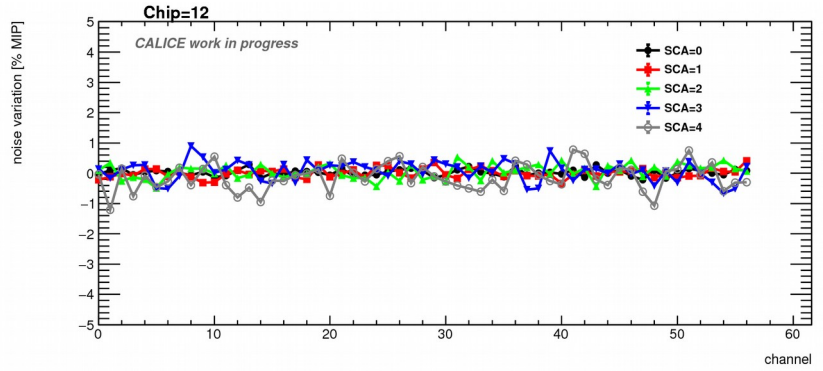
Chip 3/10 are full at around 1 - 1.5 cycle (4000-6000 bx)
Normal : Empty around 8:1 (not dependent on beam)
Retriggering occurs more in no-beam chips
(probably due to longer live time)

Taikan Suehara et al., SiW-ECAL TB analysis meeting, 14 Sep. 2017 page 3

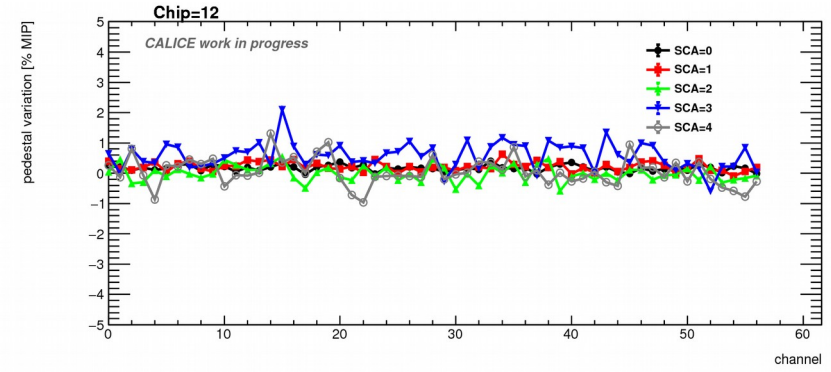
Pedestal & noise stability in magnetic fields

- Test of layer1 (slab 21) in the PCMag. Beam pointing to chip 12.
- Compare the pedestal & noise for the 1 T run with a reference run

noise



pedestal

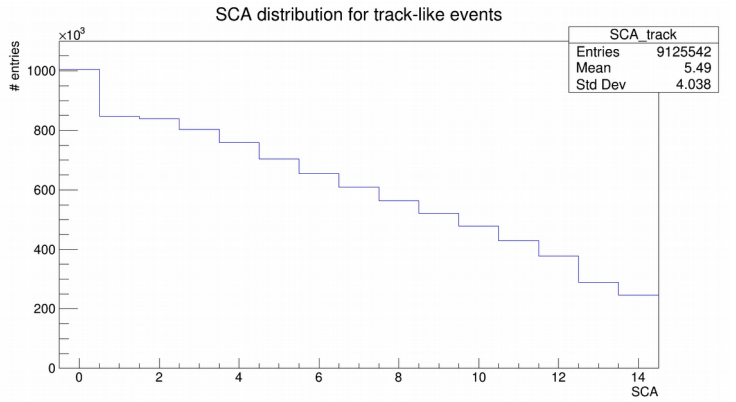


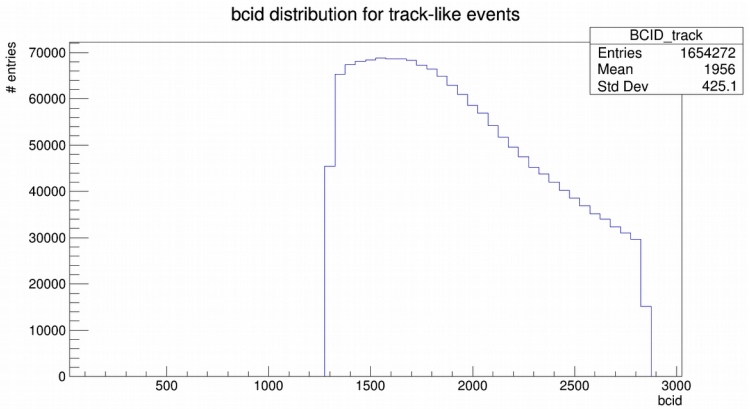
Ref. Run with beam, B=0T: (50 min)

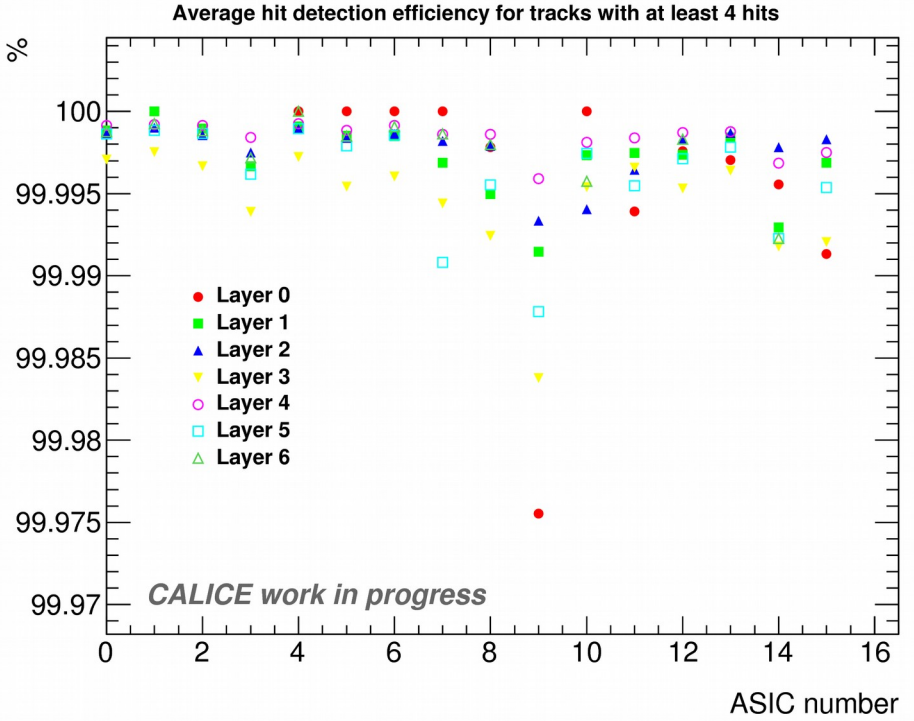
- *B=1T: (13h)*
- *B=0.5T (3h)*
- *B=0 T (1h)*

Reminder: 1% of MIP ~ 0.6 ADC

Tracking efficiency



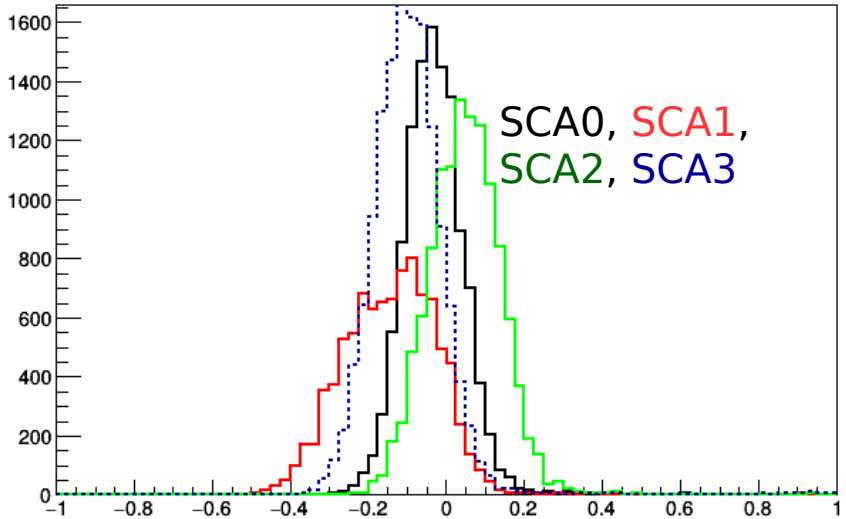




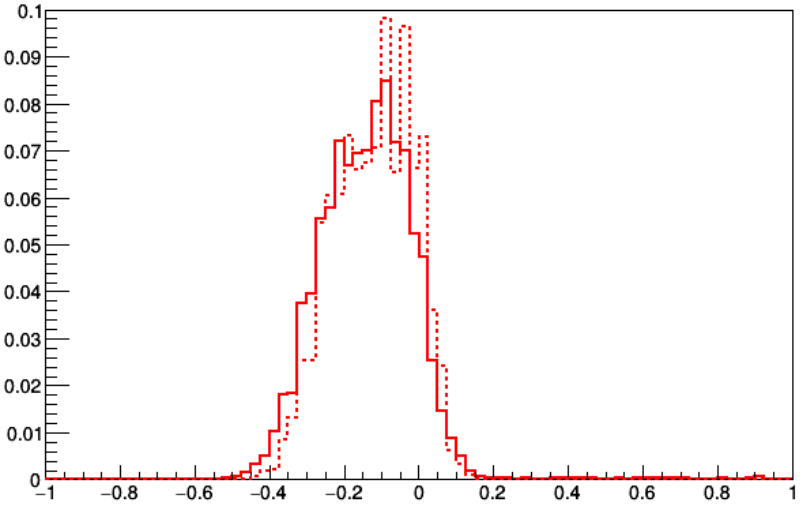
Pedestal recalculation for chips in the beam spot

- Conf2, 4 GeV electrons, beam hits chips 12-15. Pedestal shift related to the distance to the triggered channel? → no

Pedestal distribution for all channels (chip 12-15),

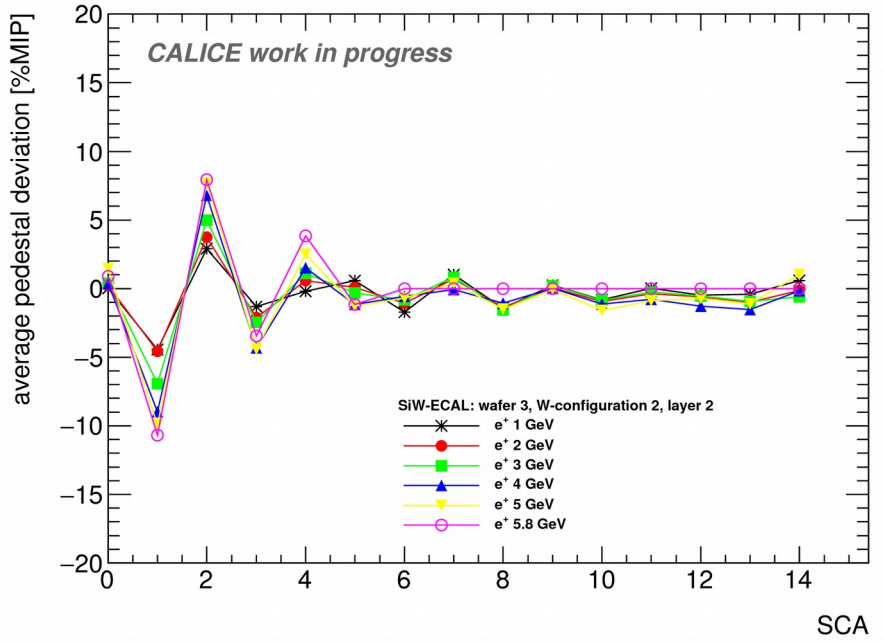


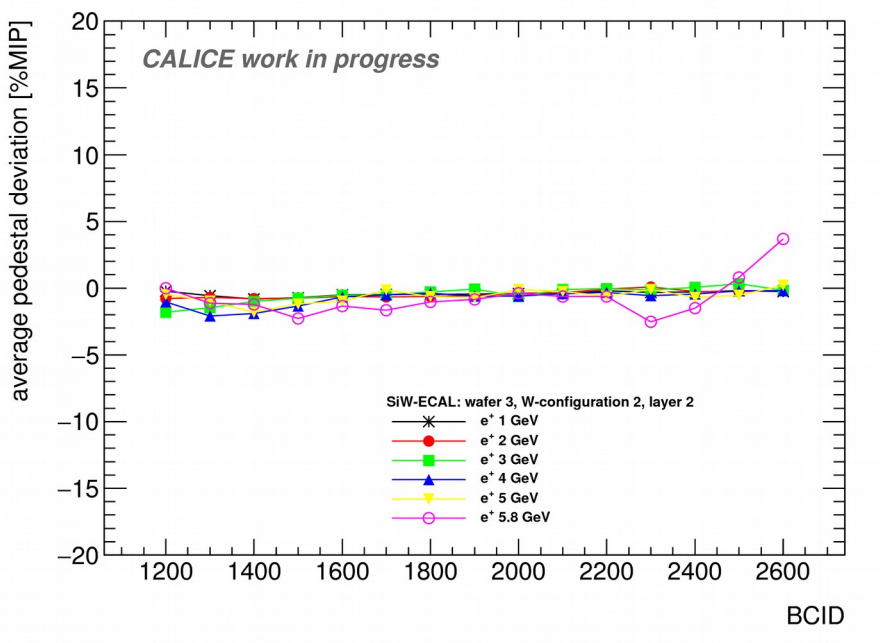
Comparison of pedestal distribution (normalized) for SCA 1 for channels with a hit in the neighborhood (continuous line) and channels far from hits, d>5 cells, in the event (dotted line)



Pedestal shift

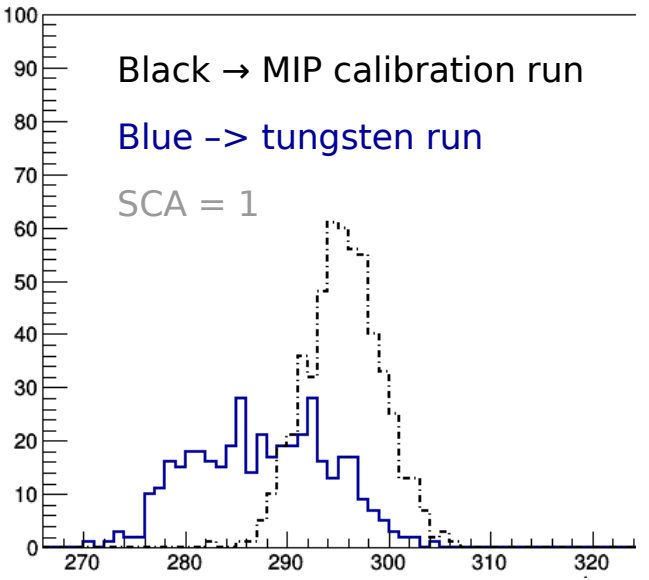
- Same, but vs bcid
  - The effect is diluted (SCA 1 compensated by SCA2, etc)
  - It is not a "timing" issue



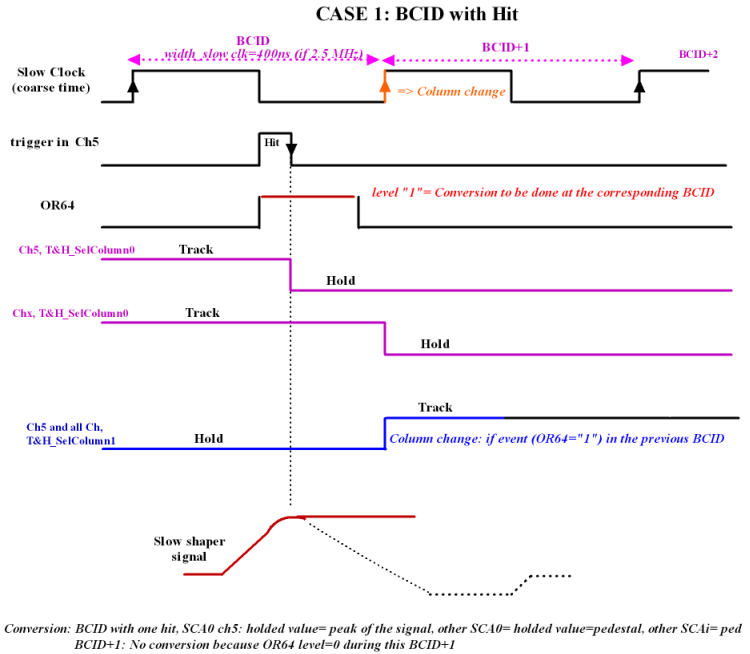


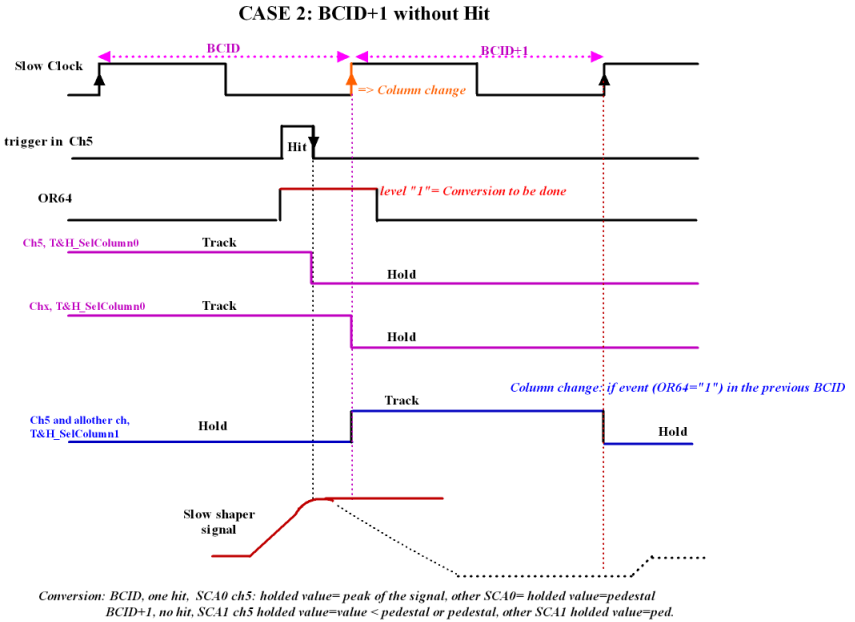
Pedestal shift for channels with disabled preamps

- We study the pedestal shift for channels with preamps switched off:
  - Chip 12, channel 50 (trigger masked and preamps switched off) for a mip run and a a run with absorber (4 GeV, conf2)
  - This channel is classified as masked, therefore is not included in the reconstructed data. We use “raw data” → very simple event selection
- The pedestal shift is also observed for the tungsten run, and not observed in the calibration run.



BCID+1 events (aka empty events)





- Next SCA (NSCA+1) is filled with a zero, but SCA=NSCA is usable → not remove from analysis !
- ~ 15% of chances of happening (reduced to ~1-3% in skiroc2a)