FONT Meeting

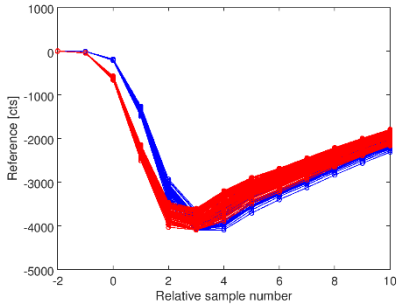
Friday 16th February 2018

Diode processor, sample jumps and IQ phase

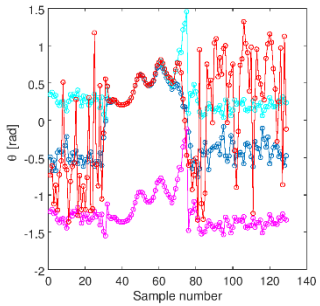
Douglas BETT

Contents

- Diode processor
  - setup and commissioning
  - stability, dynamic range measurements

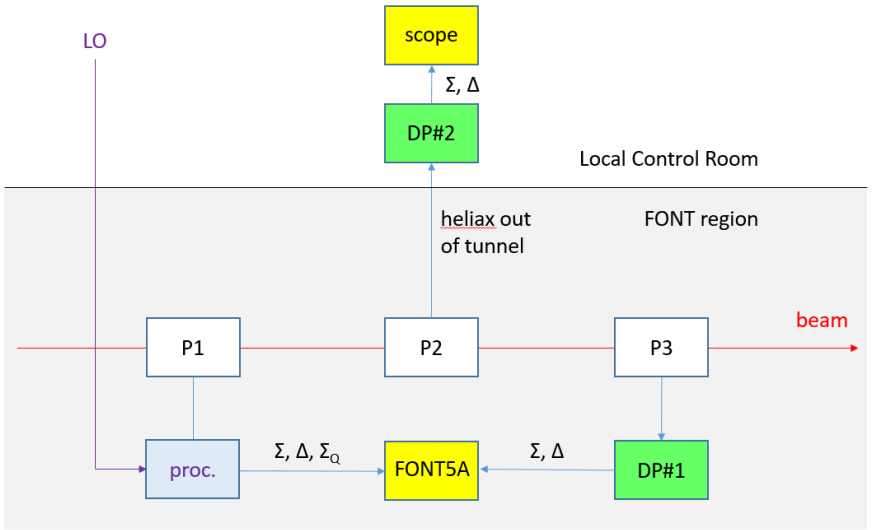


- Sample jumps
  - review and timing signal study
  - amplitude and frequency analysis

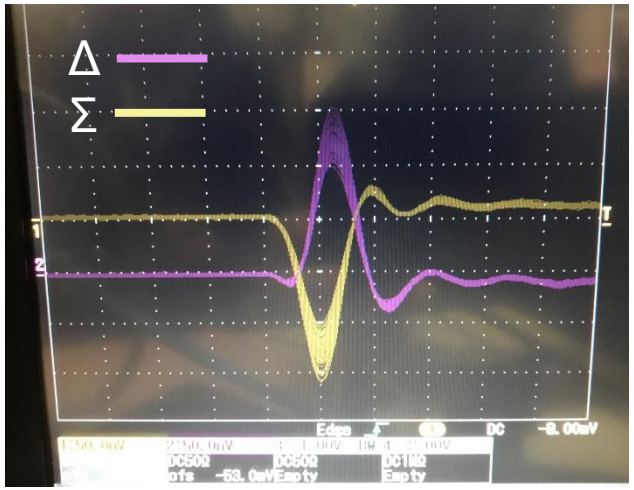


- Bonus: IQ phase
  - historically random before signal arrived

Diode processor commissioning



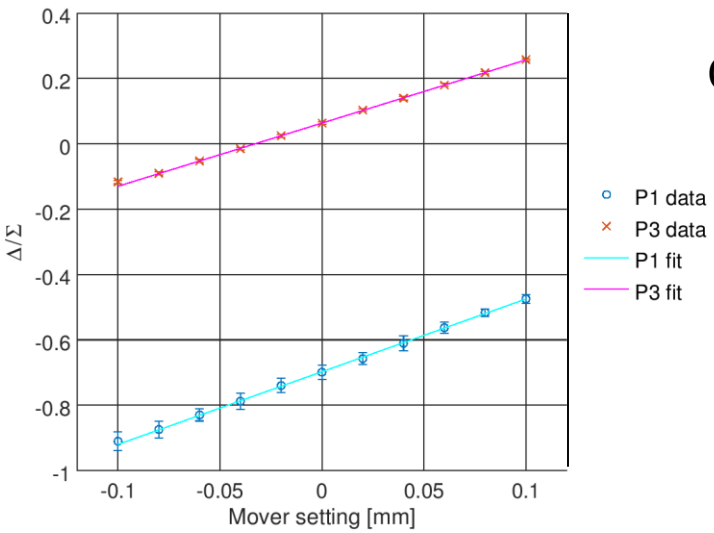
- Matched pair of heliax required to transport raw stripline signals;
  B1, B2 available in P2 region
- Heliax 4 replaced B1 as fast clock input of upstream FONT5A board
- 6 dB attenuators installed on P3 and DP1 instrumented in situ (phase shifter removed from signal path due to cabling issues)
- Initial processor tests performed in Local Control Room using scope



- DP2 instrumented with P2 signals with 6 dB attenuation on inputs and no filters on outputs
- Δ signal responded as expected to changes in P2 BPM mover setting but beam orbit sufficiently offset that Δ could not be reduced to zero
- From crude calibration estimated jitter to be tens of microns
- With attenuation removed |Σ| = 350 mV

Initial in situ measurements

180206_owl



mCal1

Calibration using BPM movers

$k = y/(\Delta/\Sigma)$

449.4 (P1)

517.3 (P3)

jitRun2

Measured beam jitter

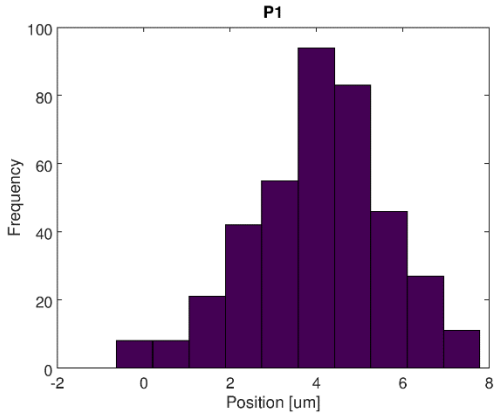
1.59 um (P1)

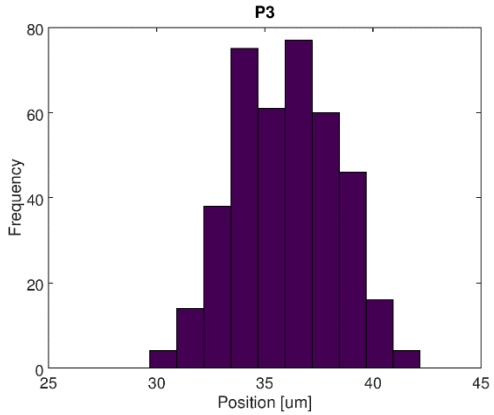
2.37 um (P3)

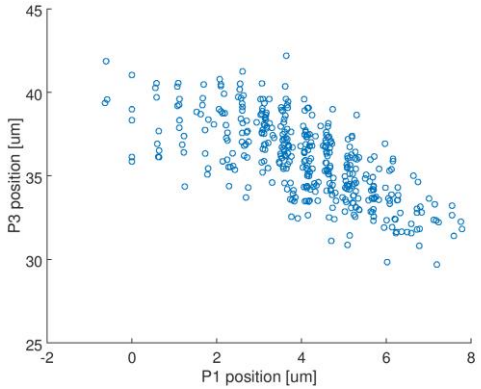
P1-P3 correlation = -0.70

LATENCY
P3 sum signal peak occurs three samples after that of P1 (formerly 5 samples)
→ can infer a reduction in latency of > 5 ns compared to conventional processor

caveats
- significant P3 offset
- couldn't change LO phase; Σ_Q used instead of Σ for P1
- charge unstable: σ(Σ) doubled during latter half of jitter run
- no phase compensation for P1
- no drift removal

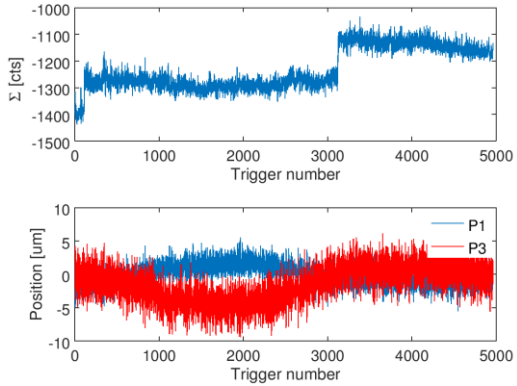


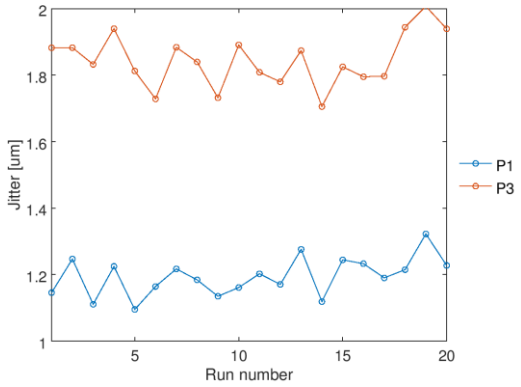


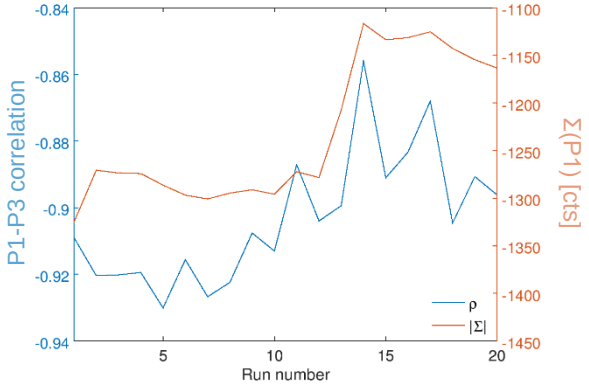


Stability

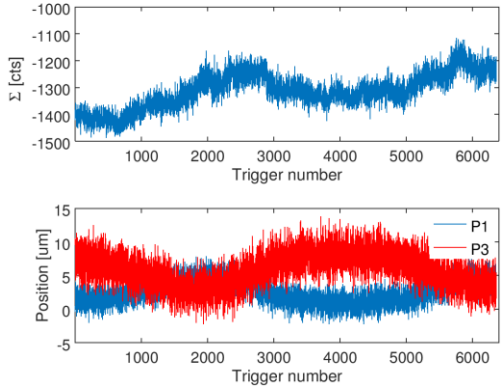
[14:07:29] diodeProcessor: 5,000 trigger data run. Charge modified twice during run.

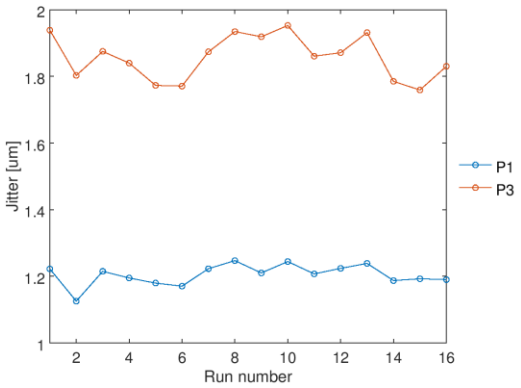


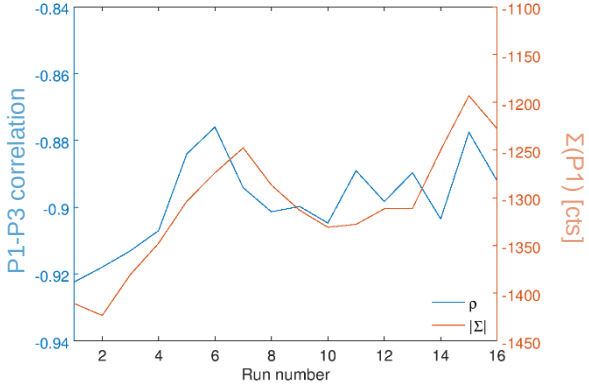




[15:40:21] jitRun: 16 × 400 trigger data runs. Charge varied by itself.



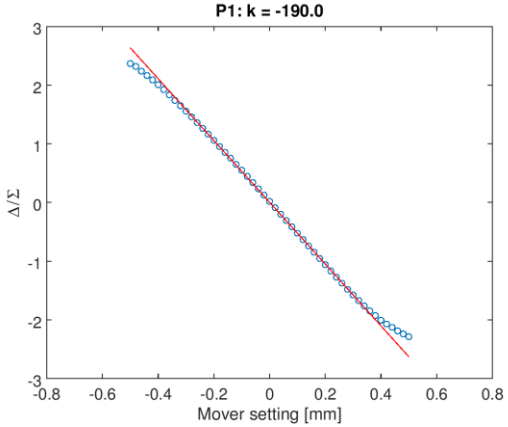




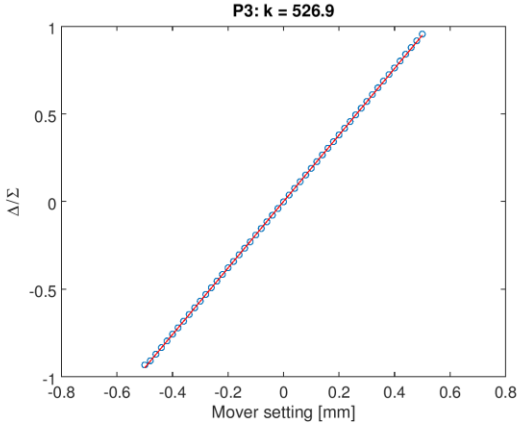
Dynamic range

Mover scan over range ± 500 μm with a 20 μm step size.

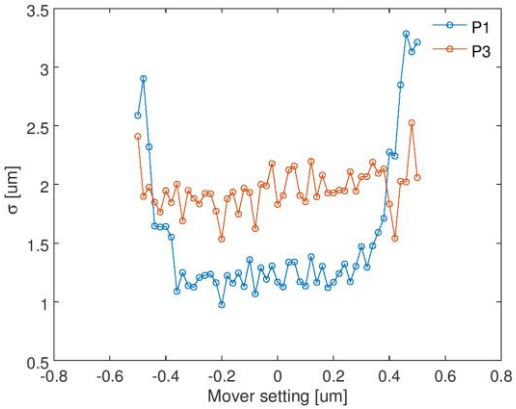
P1 mean position



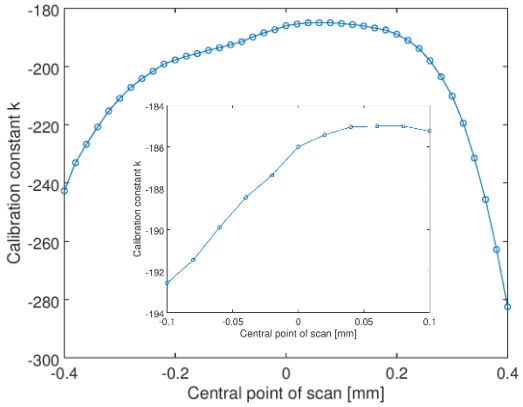
P3 mean position

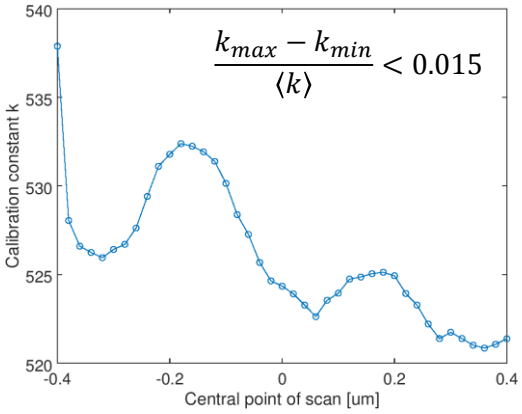


Position jitter

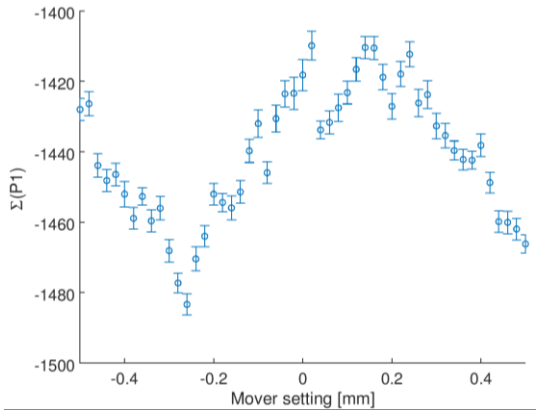


Calibration constant for each BPM as a function of central point of scan.



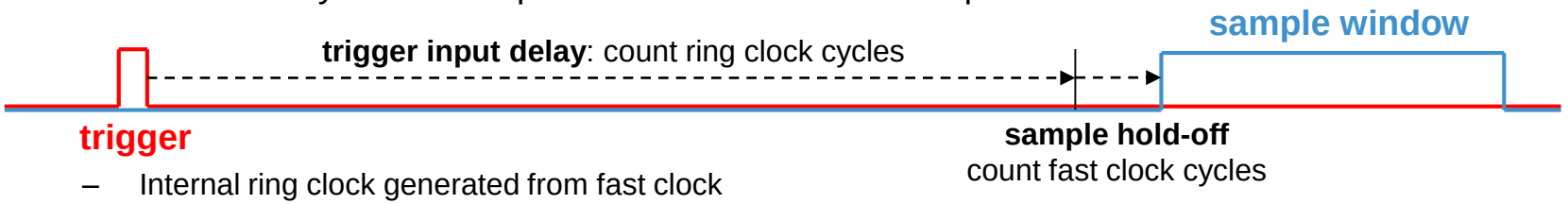


charge



Sample jumps: a review

- Refers to recently observed spontaneous shifts in the sample window of the FONT5A board



  - Internal ring clock generated from fast clock
  - Board starts counting ring clock cycles after trigger rising edge detected
  - Input trigger delay defines number of ring clock cycles to wait before sampling
  - Sample hold-off allows sample window to be further delayed by up to 127 fast clock cycles
- Problem intermittent: possible to go an entire shift without observing it once but if it does happen, the board sample timing will tend to jump repeatedly
- Frequently the sample window shifts by such a large amount that it no longer includes both bunches
- For feedback and analysis purposes the signals should remain stationary; depending on the size of the jump and initial value of sample hold-off, it may not be possible to trivially recover the initial state

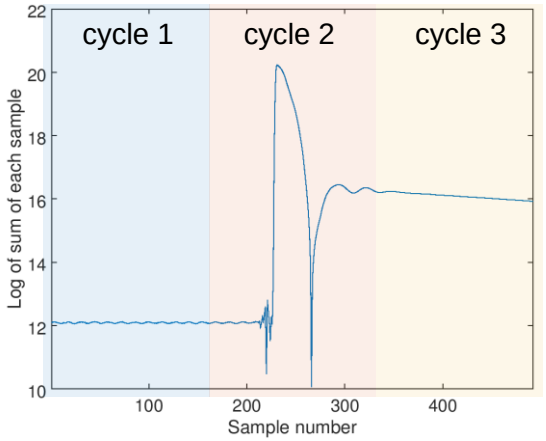
TIMING SIGNAL STABILITY STUDY

- Trigger, ring clock and beam (represented by sum output of diode processor) all found to be stable with respect to each other
- Fast clock and ring clock left on scope. After sample jump, fast clock phase found to have flipped
- Fast clocks are outputs of Mikey's LO distribution box i.e. generated from the DR 714 MHz

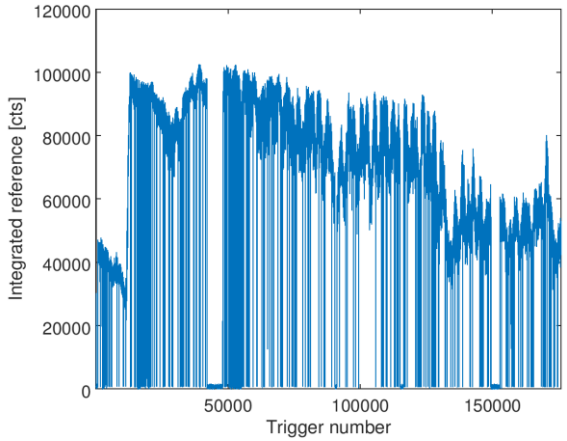
Sample jumps: overnight

- In an attempt to gather some data about this phenomenon, at the end of Wednesday day shift the sample window was increased to 492 samples (three ring clock cycles) and the board left to repeatedly take data runs until deactivated next morning
- 440 runs × 400 triggers / run = 176,000 triggers ~ 15h40m
- **Not a single sample jump**
- Hard to demonstrate due to large size of data set, but came up with a few metrics

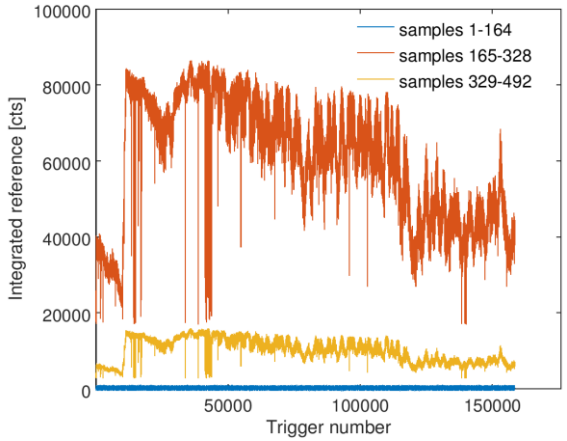
Sum of waveforms on a sample-by-sample basis.



Sum of waveforms on a trigger-by-trigger basis.

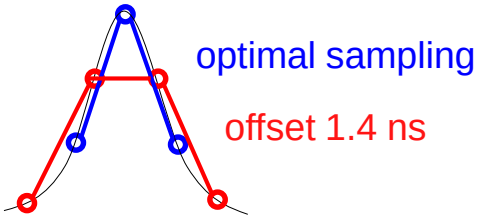


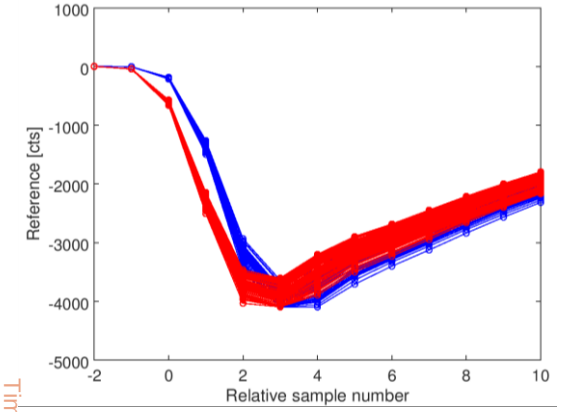
Same as previous but separated by ring clock cycle.



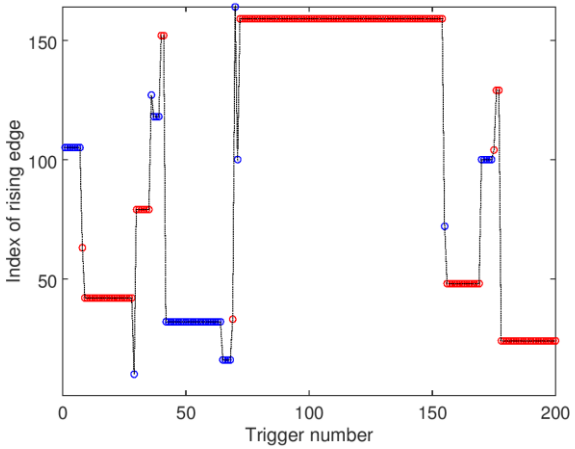
Sample jumps: jump3

- Fortunately plenty of jumping during the Friday day shift – took data (downstream board only) as soon as it happened, but noted that the upstream board was affected too
- Sample window can jump by a non-integer number of fast clock cycles
  - Particularly obvious upstream: as the scan delays are typically used to shift the ADC clocks in order to catch the peaks of the Σ signals, a 1.4 ns shift completely changes the shape of the sampled signal
  - Also visible in the shape of the reference diode
    - For each trigger, locate the rising edge of the reference signal
    - By superimposing the rising edges, it is immediately evident that there are two distinct populations
    - The red lines correspond to a sample clock lagging by 1.4 ns relative to the blue lines

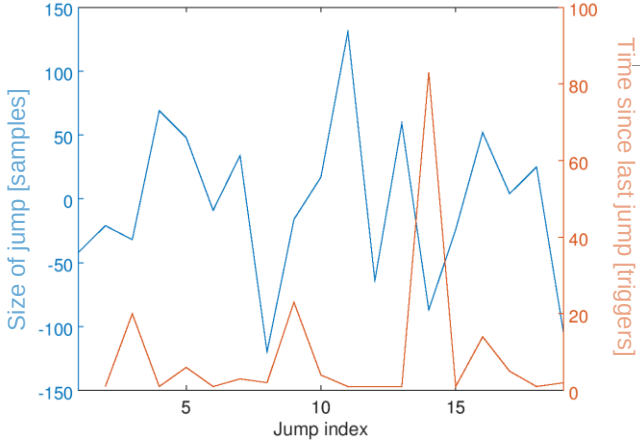




Index of rising edge

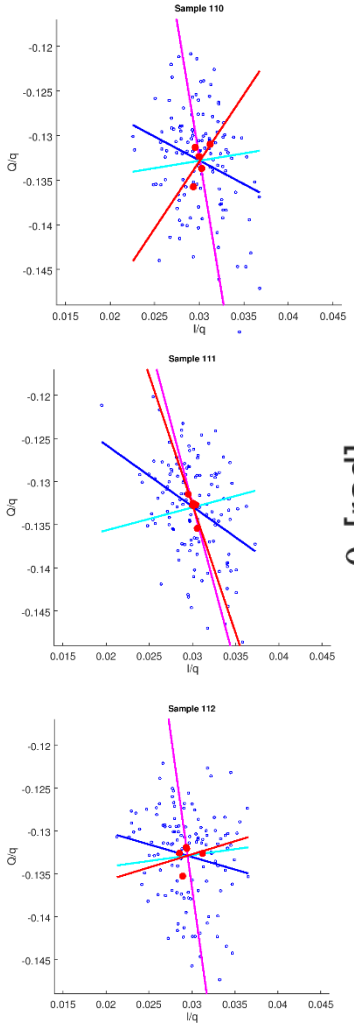


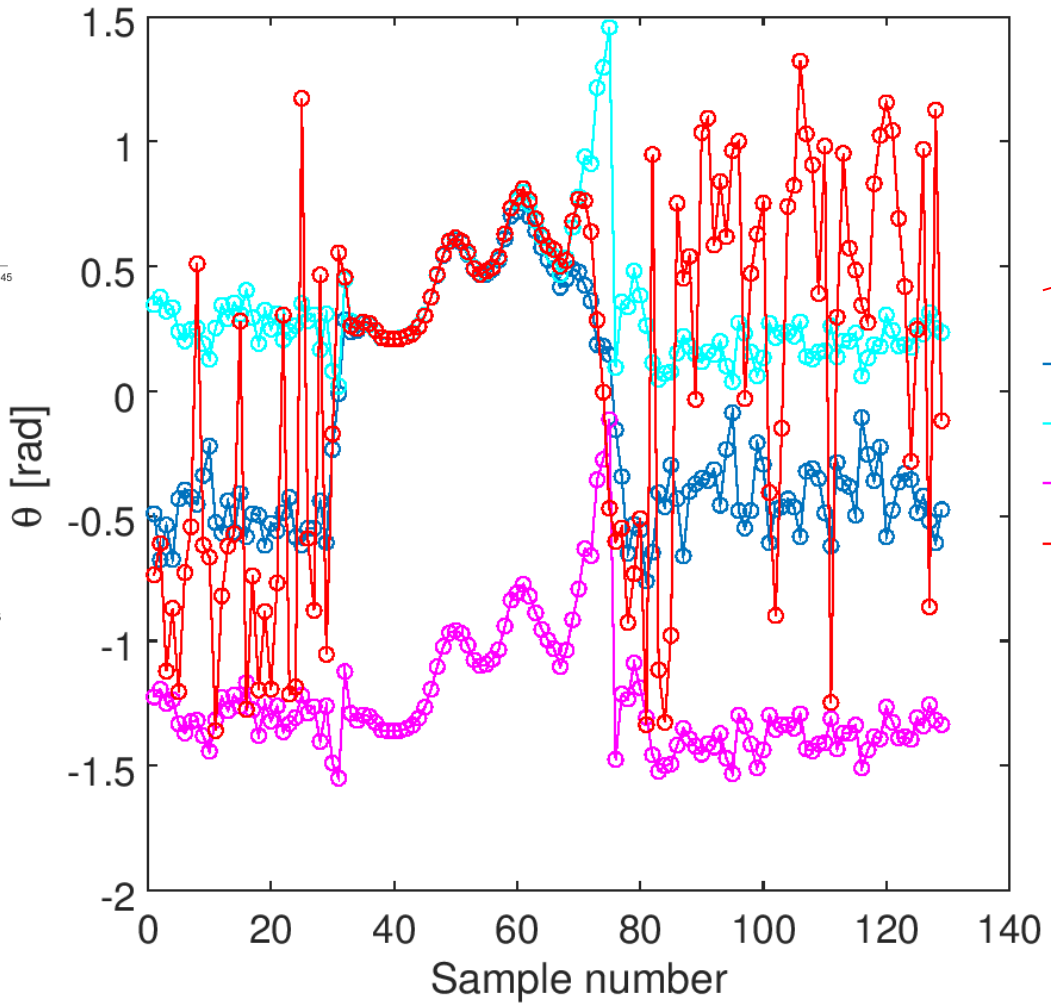
Size and frequency of jumps



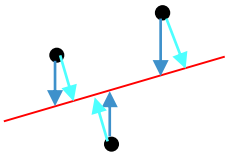
Too small a data set to make any definitive conclusions about the size and frequency of sample jumps

Bonus: IQ phase





Single-sample IQ phase rotation angle as a function of waveform sample index.



lsq = least squares
perp-lsq = perpendicular least squares

lsq
perp-lsq(+)
perp-lsq(-)
lsq(bin)

Random phase found in absence of signal only when fit performed to the data once binned by quad mover setting.
This amounts to fitting to just 5 data points and accounts for the loss of consistency compared to fitting to all data points.

Conclusions

- Diode processor successfully commissioned. Not able to demonstrate performance limit but have shown that it exceeds requirement.
- Based on the available evidence, the most likely cause of the sample jumping is the fast clock.
- Apparent random IQ phase before arrival of signal simply a consequence of performing a fit with a very small number of data points.