LCWS 2018

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Design and test of a very low-latency BPM signal processor for use in the CLIC IP FB system

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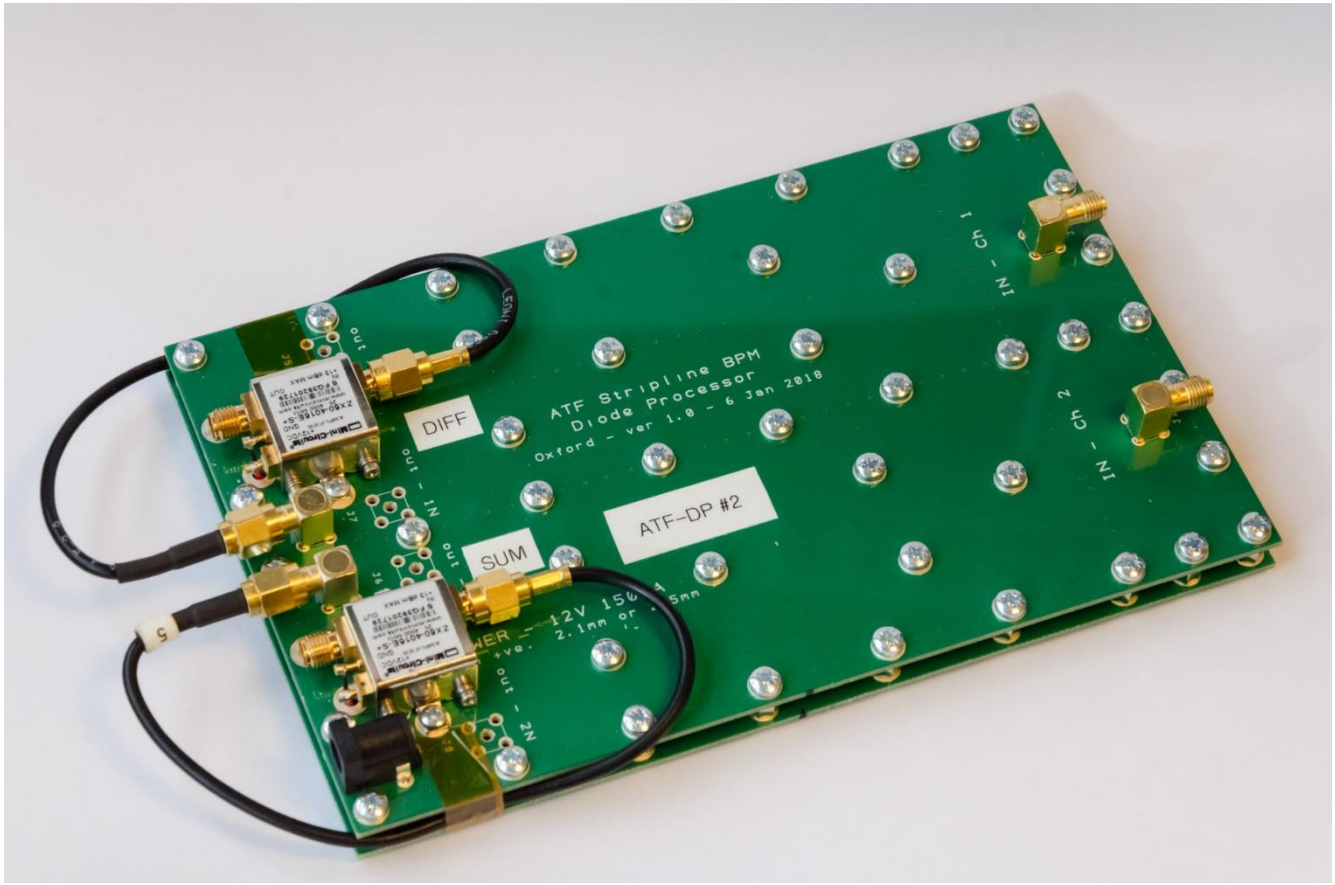


Background: Motivation

- The Compact Linear Collider (CLIC) will require a beam position feedback system at the interaction point (IP)
- This will require a beam position monitor (BPM) with the following characteristics:
  - Low latency
  - Simple, reliable
  - Rad-hard, tolerant of high magnetic field (no ferrites!)
  - Resolution not critical

- These requirements are met by a stripline BPM used with the simplest possible processor: a diode detector on each strip

- …but would resolution of such a processor be adequate?

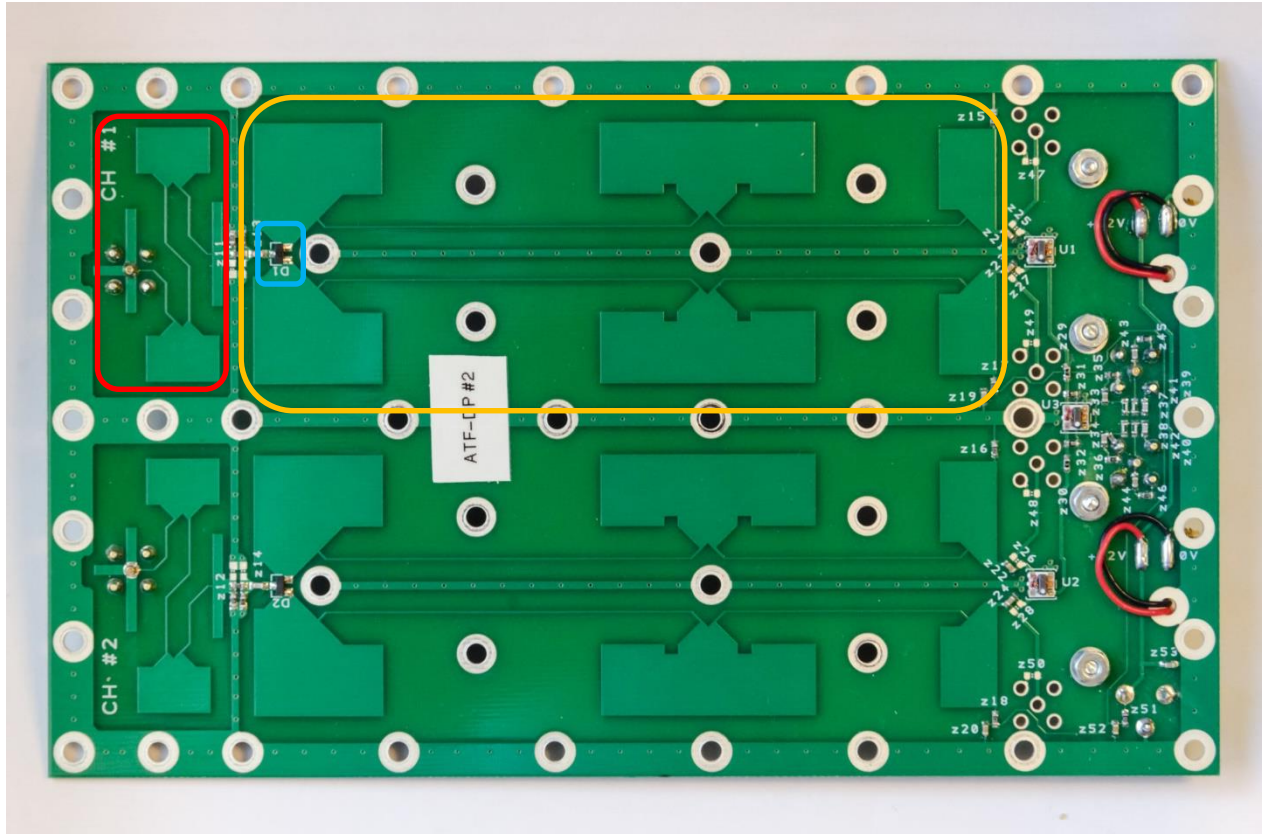
Background: Design

- A prototype was constructed for testing at the KEK Accelerator Test Facility (ATF)
  - Harder: single bunch beam rather than a train (comparable bunch charge)
  - Easier: BPM output peaks around 700 MHz versus 2 GHz bunch frequency for CLIC
- Processor designed to scale up in frequency
  - Filters would scale down in size by a factor ~2, using 0.8 mm RF substrate instead of 1.6 mm FR4*
  - Replace silicon Schottky diodes in large packages (SOT23) with GaAs diodes in smaller packages
- At CLIC processor outputs would be input to differential amplifiers on custom GaAs MMIC**
  - FONT5 digitizer at ATF unable to handle pulses this narrow due to 357 MHz ADCs, so supplement diode processor with an additional stage to condition signals

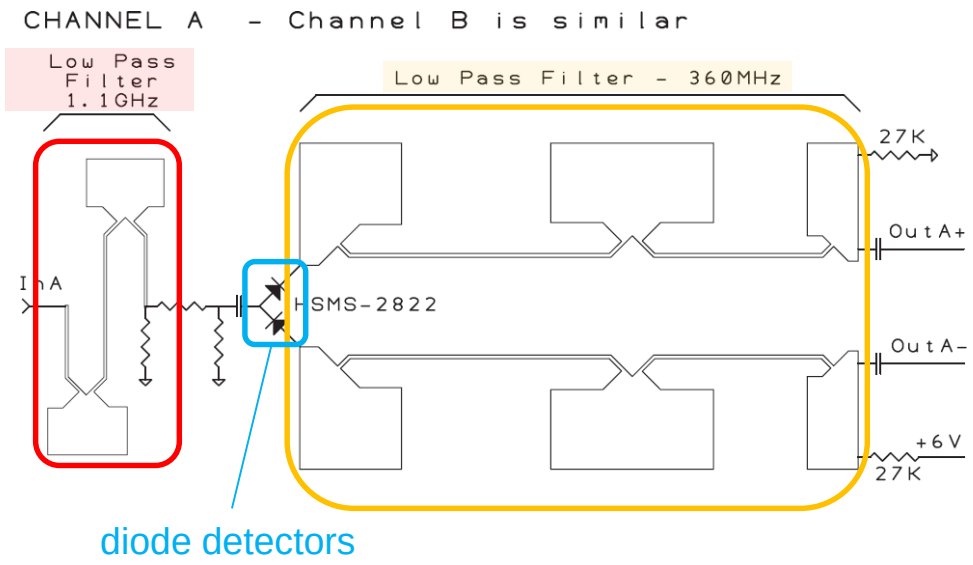
*FR4: glass-reinforced epoxy laminate material

**MMIC: Monolithic Microwave Integrated Circuit

Diode processor: Schematic

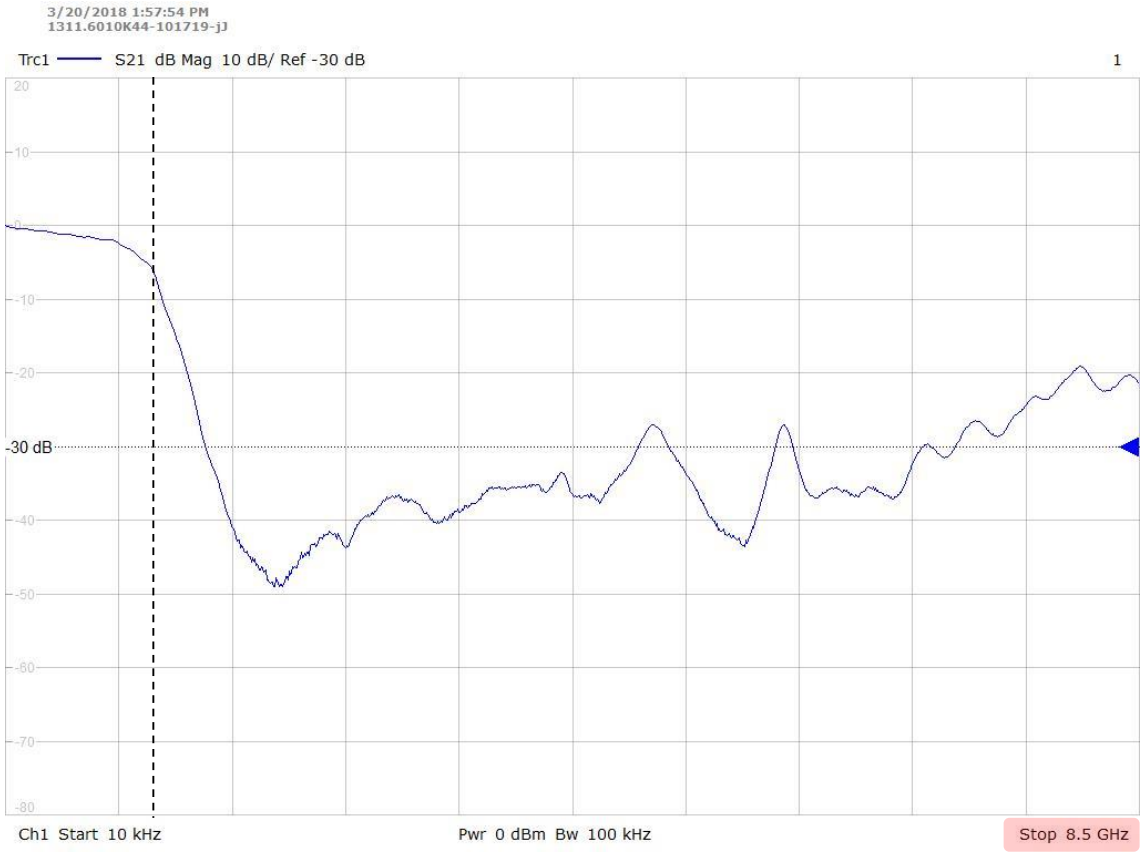


- First microstrip LPF (1.1 GHz)
- Diode detectors
- Second microstrip LPF (360 MHz)

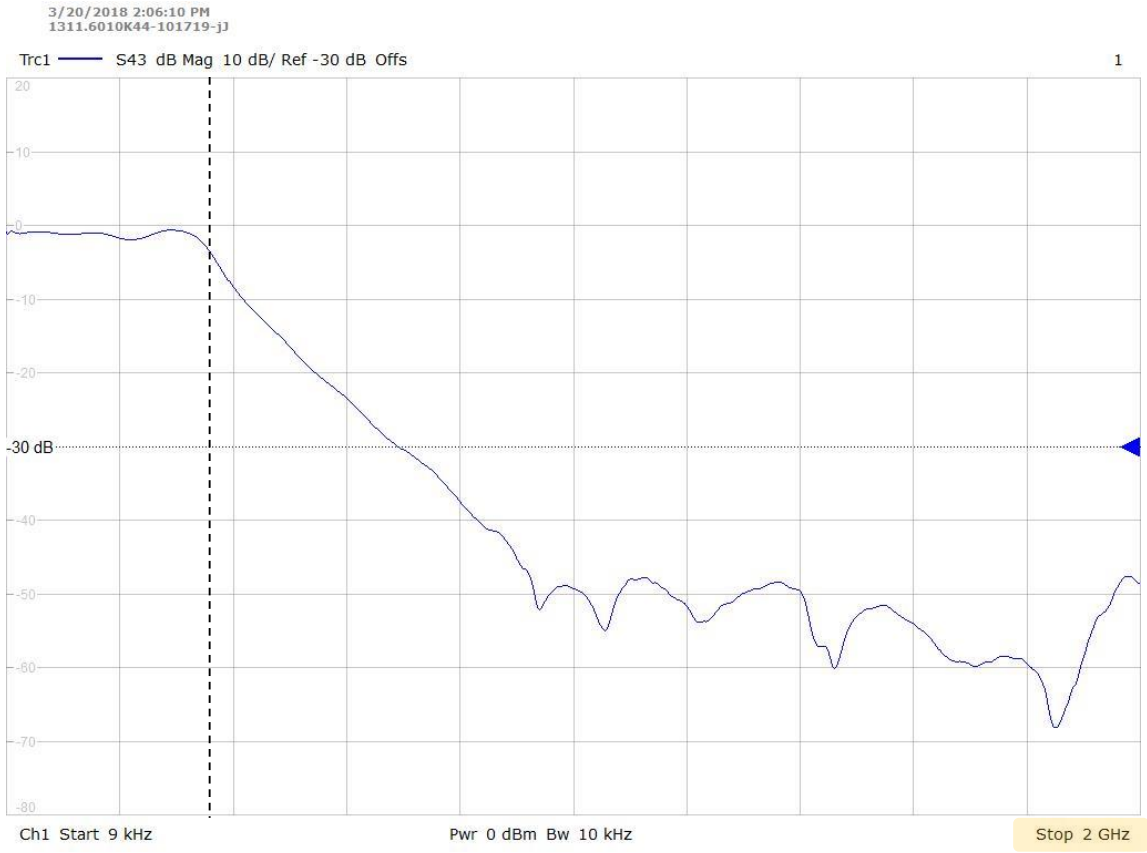


Diode processor: Filtering

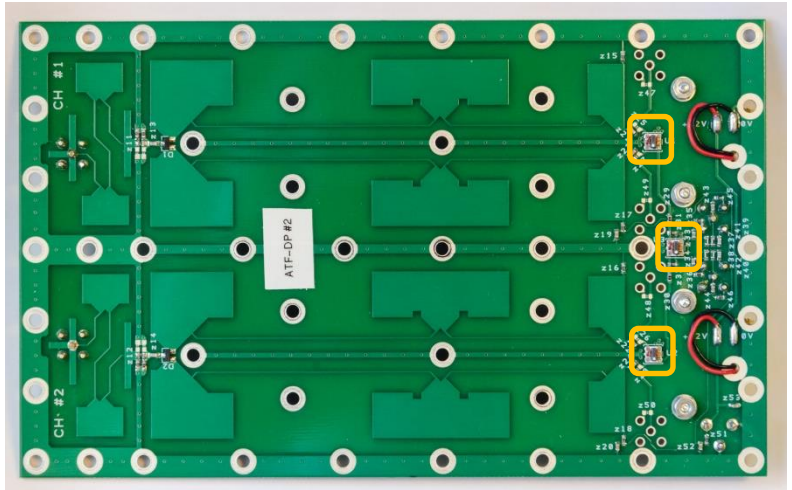
First filter: 1.1 GHz low-pass



Second filter: 360 MHz low-pass

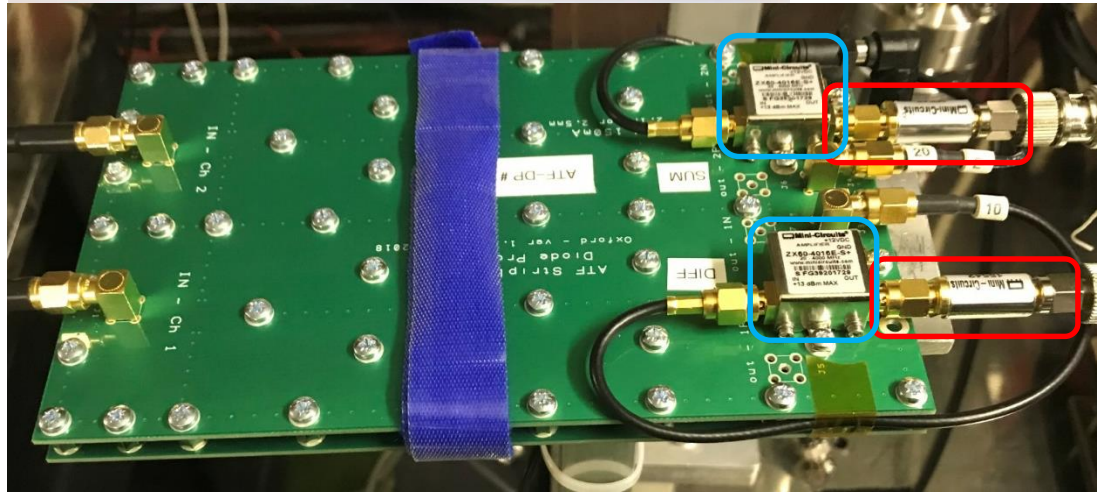


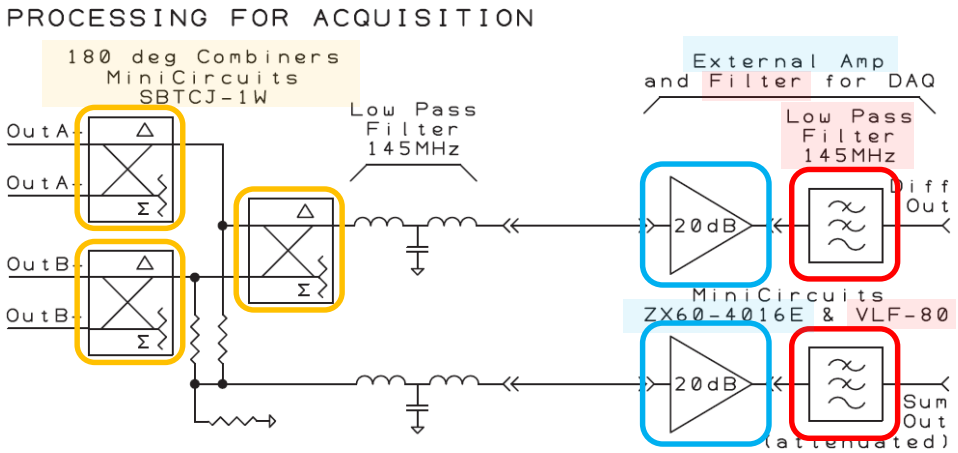
Supplemental stage: Schematic



- 180° combiners to form the difference of the two inputs
- Narrow LPF (145 MHz) to broaden the pulse
- External amplifier to suit digitizer sensitivity
- External LPF (145 MHz) to reduce amplifier noise

Reduced bandwidth widens output pulse but should not otherwise improve performance (for single bunch case at ATF)

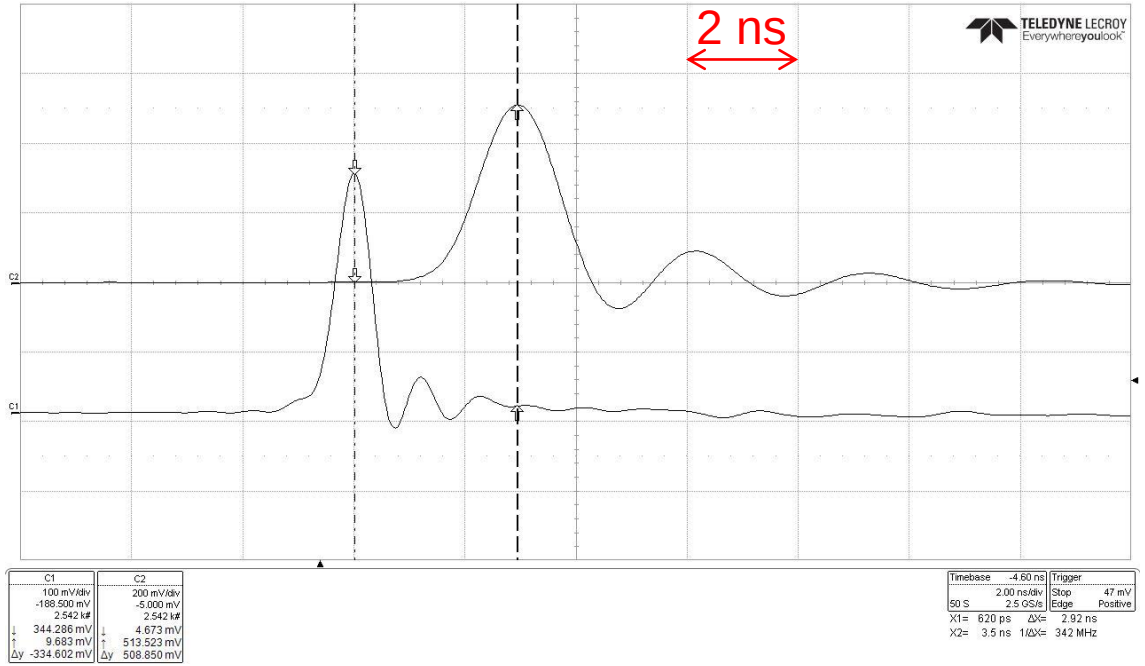




Diode processor: Latency

Extra processing adds a lot of latency

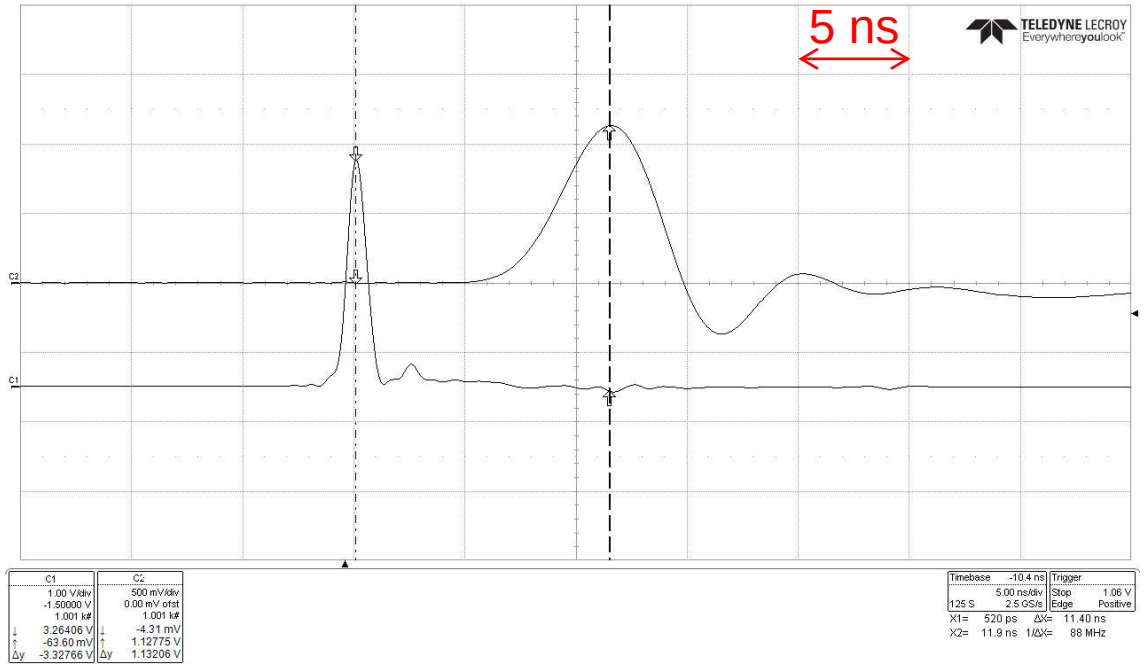
Pulse response after **diode processor**



Measured latency: **2.9 ns**

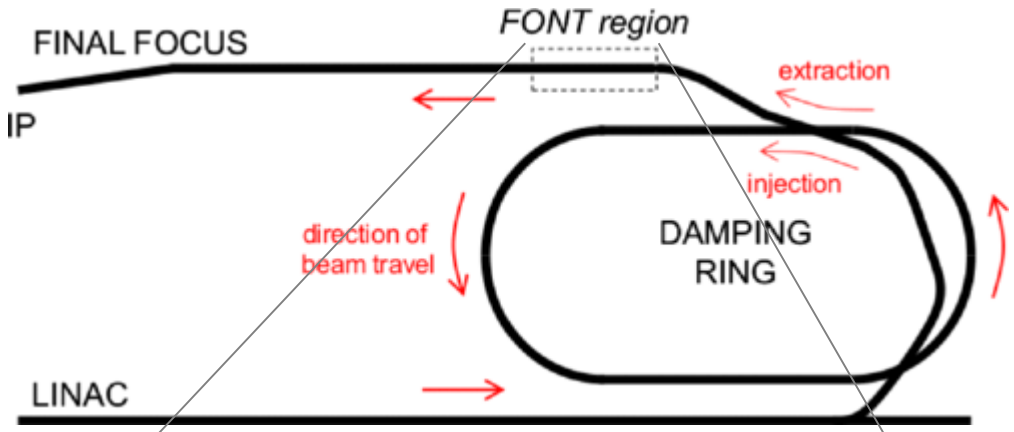
(would scale to ~1.0 ns for CLIC)

Pulse response after **supplemental stage**

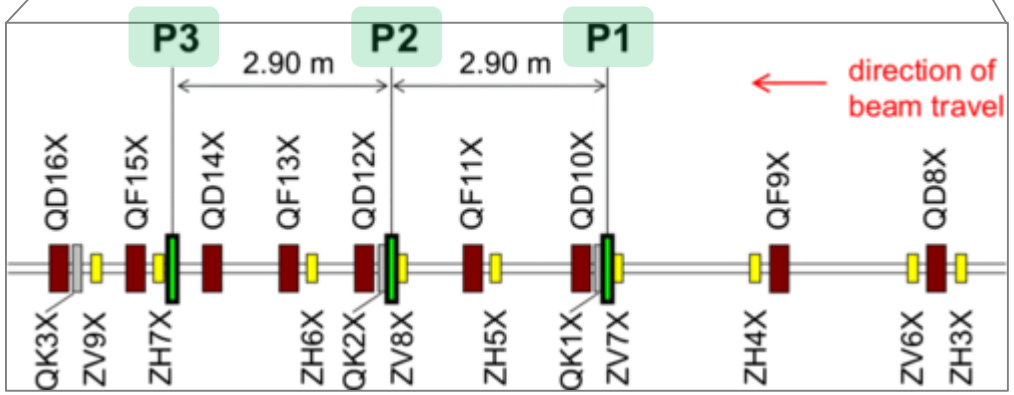


Measured latency: **10.4 ns**

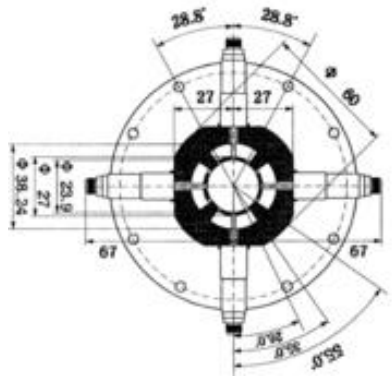
ATF: Stripline BPMs

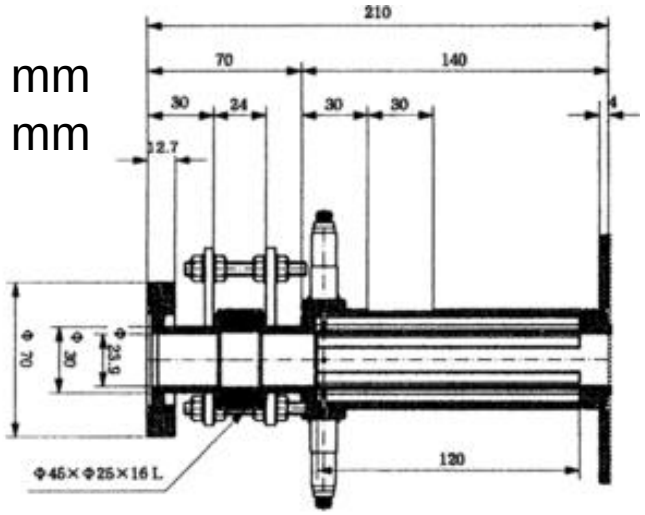


set of three stripline BPMs

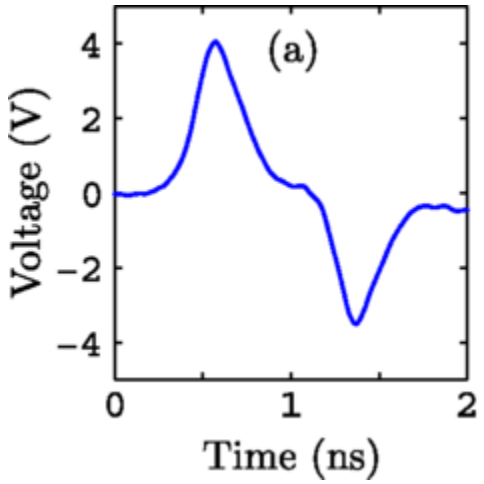


length: 120 mm
diameter: 24 mm

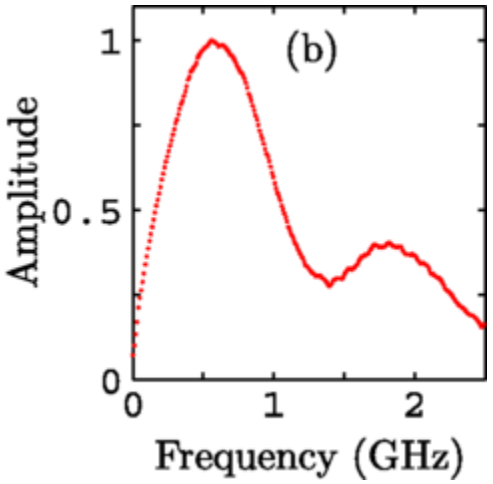




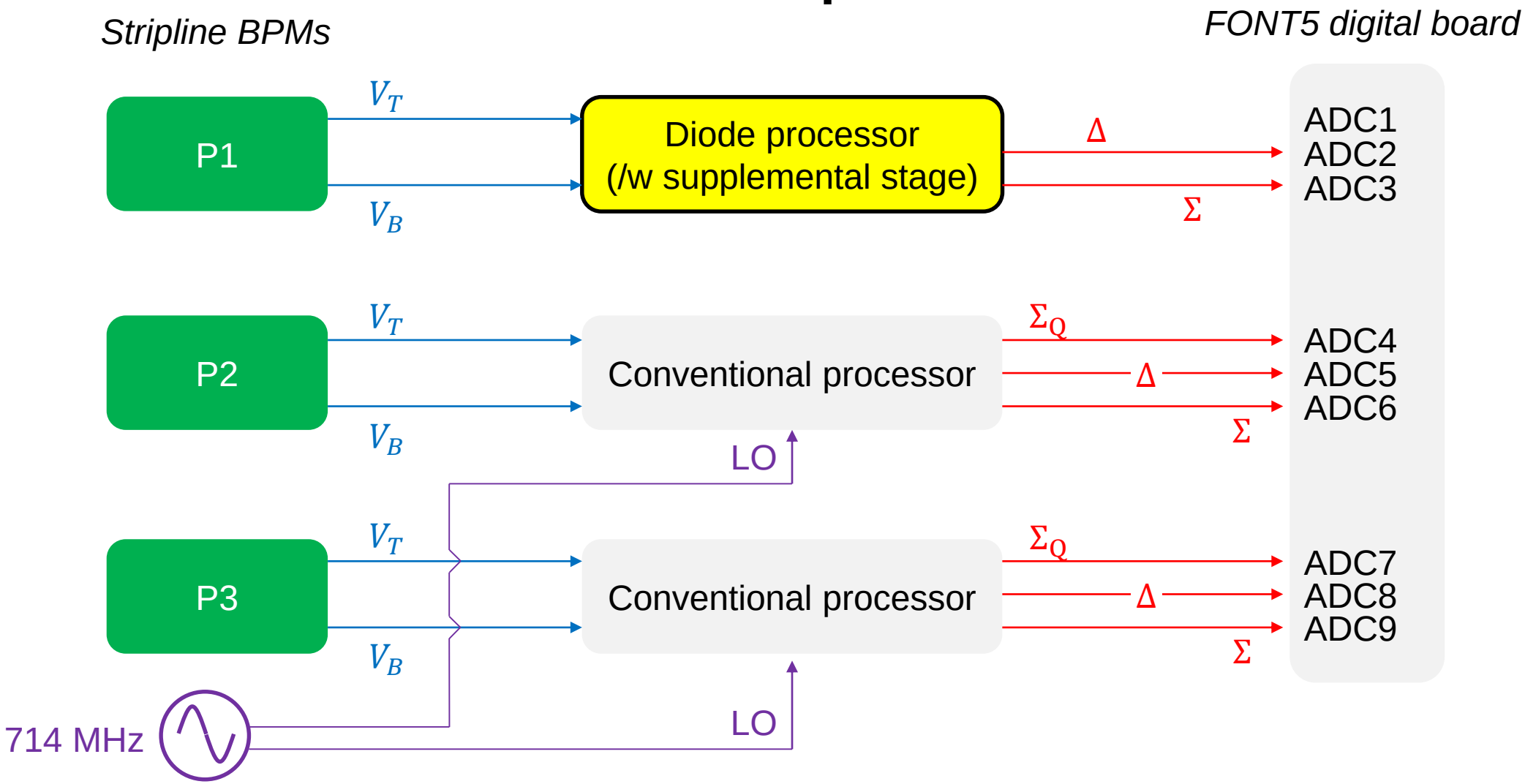
Time domain



Frequency domain

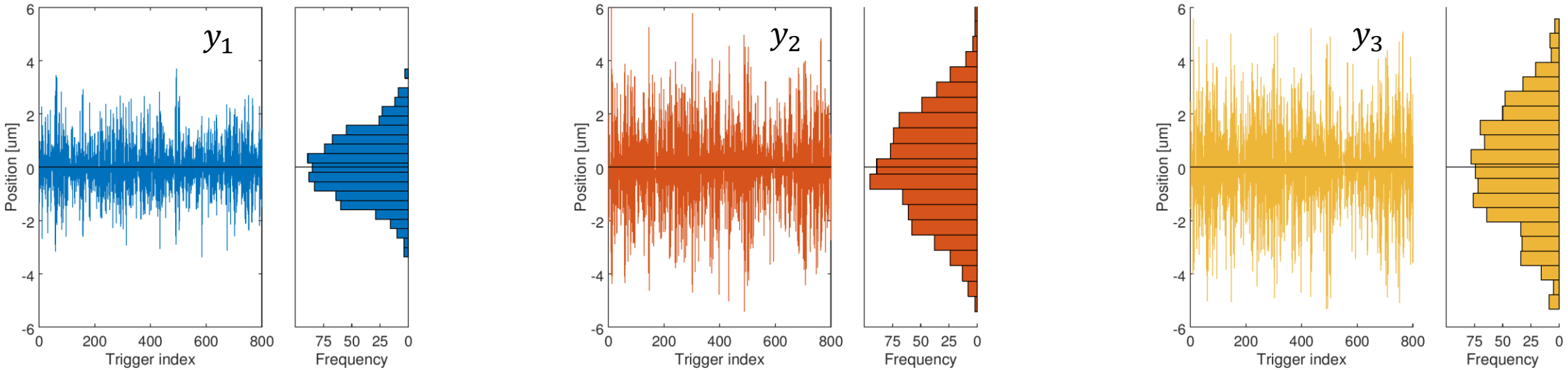


ATF: Acquisition



Conventional processors described in Phys. Rev. ST Accel Beams **18**, 032803 (2015)

ATF: Results



- Define residual position at P1: $y_{res} = y_1 - (C_{12}y_2 + C_{13}y_3)$ (where C_{12}, C_{13} are geometric coefficients)
- Variance of residual given by weighted sum in quadrature of BPM resolutions: $\sigma_{res}^2 = \delta_1^2 + C_{12}^2\delta_2^2 + C_{13}^2\delta_3^2$
- Assume conventional processors have equal resolution ~ 200 nm* at relevant beam charge (0.65×10^{10})
- Estimated resolution of diode processor (with supplemental stage) is then ~325 nm

FONT stripline BPM resolution* (N. Blaskovic) ATF Operation Meeting **2 Dec 2016

Conclusion

- Proof-of-concept **diode processor** designed for the CLIC IP feedback system
- Prototype tested on stripline BPMs at KEK ATF, but design scalable to CLIC requirements

- Latency of **2.9 ns** measured in lab (scaling to **1.0 ns** for CLIC design)
- Supplemental processor stage necessary at ATF to condition diode processor outputs for use with existing digitizer and results in an overall latency of **10.4 ns**

- Resolution of diode processor (with supplemental stage) estimated at **325 nm**