

# CALICE/ILD SiW-ECAL a 26 Layer Model and 1<sup>st</sup> Tests of a Long Slab

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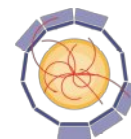
**École polytechnique, Palaiseau**

*LMR*

**LCWS 2018**

**23.11.2018, Arlington (TX)**

TNA support + WP14



**AIDA** 2020

# Introduction

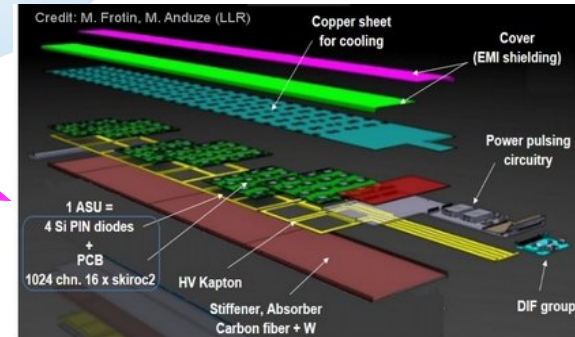
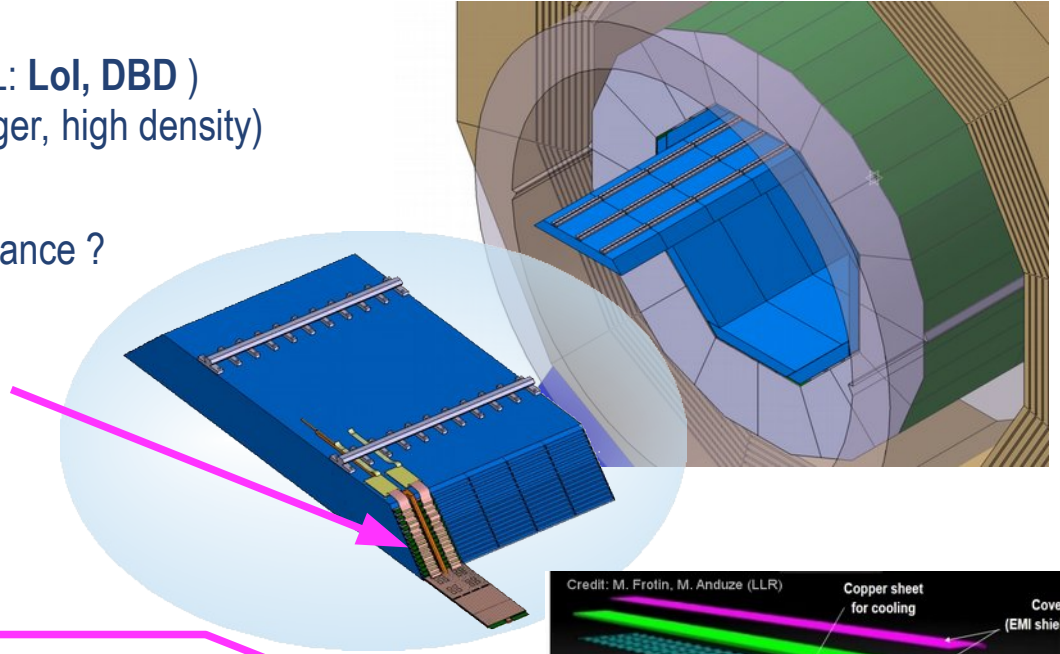
**SiW-ECAL ~ 30% of ILD costs** (ILD Models of SiW-ECAL: LoI, DBD )  
and most sensitive calorimeter (1/3 – 2500 mips, auto-trigger, high density)

1 ) How to reduce costs without impact (too much) performance ?

- $R_{\text{INNER}}^{\text{ECAL}} = 1842\text{mm} \rightarrow 1462\text{mm}$ : in simulations
- **30** → **26 layers**
  - 8", 725 $\mu\text{m}$  wafers

2) Recent progress in feasibility studies:

- **Base unit «ASU» ~ validated**
  - almost validated (see Adrián's talk): on beam test data: uniformity, noise, auto-trigger perf. Response low E and high E to be assessed
  - Updated version → **FEV13 design by Taikan**
- **1<sup>st</sup> prototype of a long slab (this presentation)**



# Redefinition of dimensions

2 designs to be looked at:

- a “**baseline**” (or “large”) with inner ECal radius at  $R_{\text{ECal}} = 1804\text{mm}$ , (model close to the DBD)
- a “**small ILD**” model  $R_{\text{ECal}} \sim 1500\text{ mm}$  (all related quantities adapted  $\leftrightarrow R_{\text{outer}}[\text{Endcaps}]$ )
  - Plus a model with slightly reduced number of layers = 26 layers (wrt 30).

Under work version of **ECal Technical Design Document** (TDD, 96 pages)

by Henri Videau (LLR), Marc Anduze (LLR) and Denis Grondin (LPSC) (+ ed. Daniel Jeans & Roman Poeschl) available on

<https://lirbox.in2p3.fr/owncloud/index.php/s/eeVeAlyv8o27VRF>

Small ILD with 26 layers → §5 of TDD.

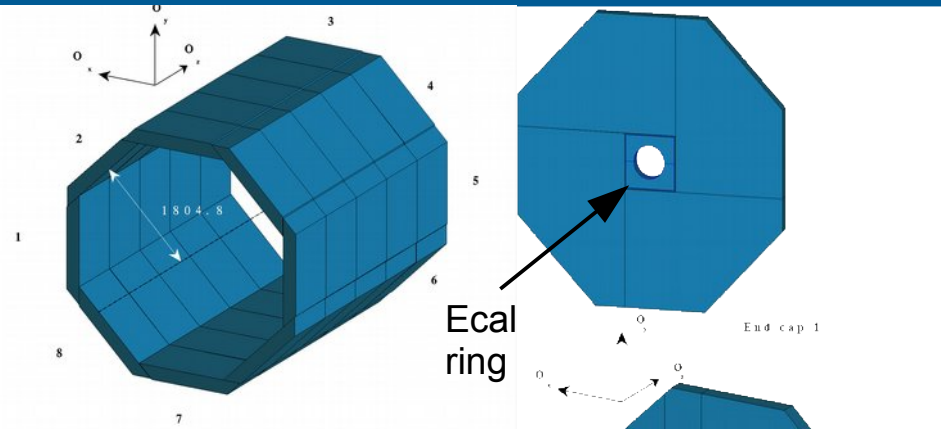
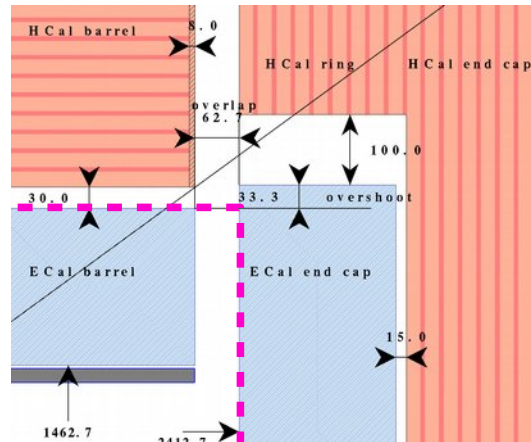
# Dimension constructions (reminder)

Barrel length fixed at **4700mm** in all models, same as HCal or TPC

- 8 staves  $\supset$  5 CF/W modules  $\supset$  5 alveoli columns
- 1 alveoli width =  $\sim 2 \times$  wafers width + walls + clearance  $\sim$  **187.4mm**

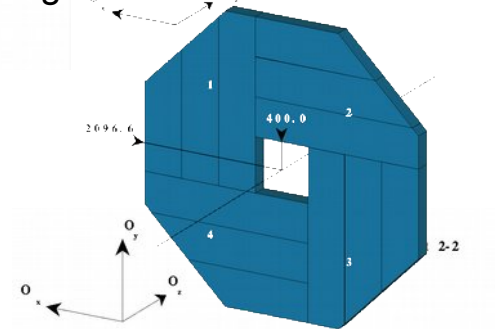
## Endcaps

- $Z_{\text{front}}^{\text{EndCaps}} = Z_{\text{outer}}^{\text{Barrel}} + \text{overlap (62mm for Services + Security)}$
- $R_{\text{INNER}}^{\text{EndCaps}}$  fixed at 400mm  $\Rightarrow$  ECal ring
- $R_{\text{OUTER}}^{\text{EndCaps}} = R_{\text{INNER}}^{\text{EndCaps}} + n \text{ alveoli (+ wall, clearance)}$
- $R_{\text{OUTER}}^{\text{Barrel}} = R_{\text{OUTER}}^{\text{EndCaps}} - \text{overshoot}$



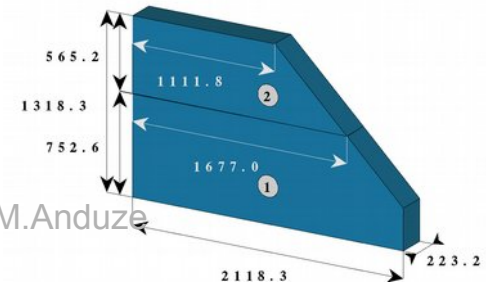
## Baseline

- Endcap quadrant with 3 modules of 3 alveoli



## Small

- Endcap quadrant with 2 modules of 4 and 3 alveoli

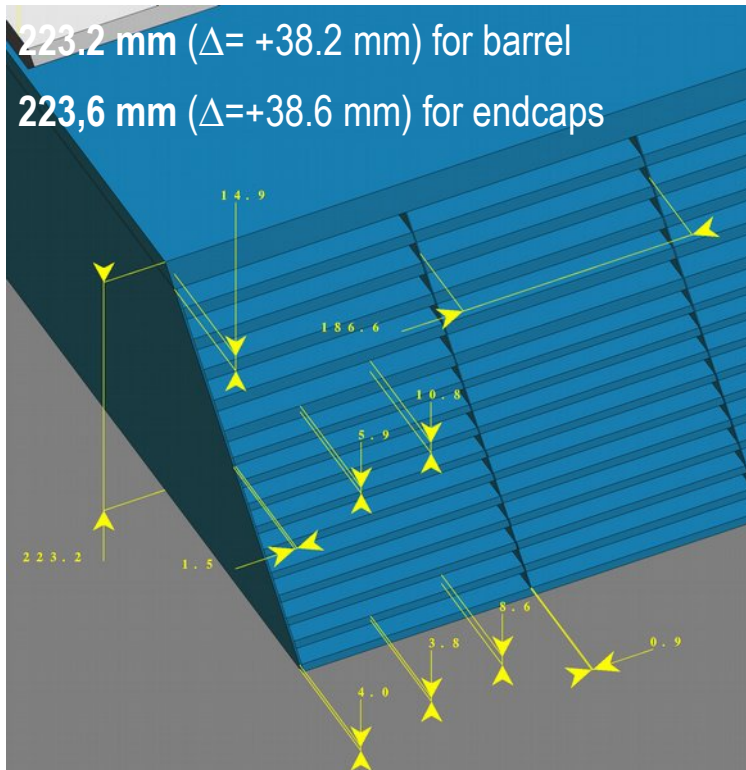
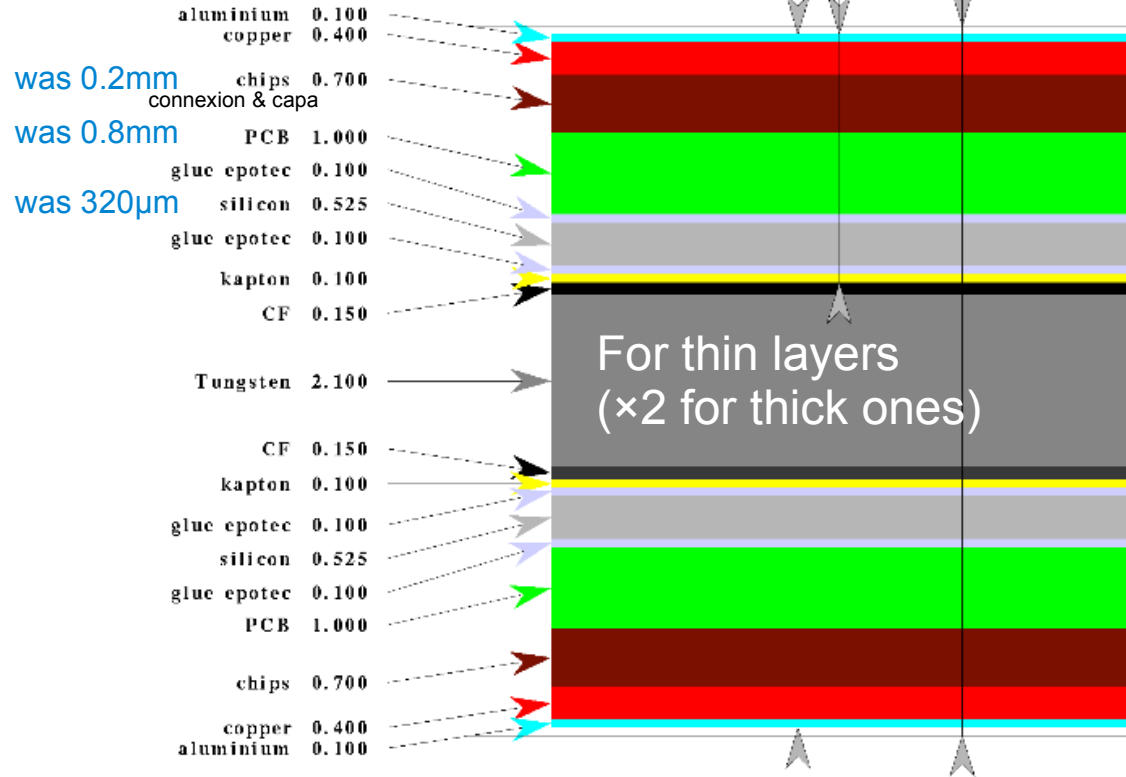
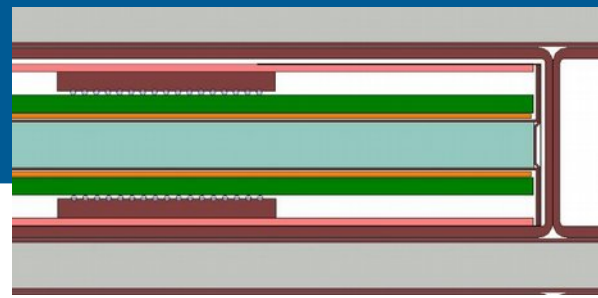


# ECal thickness

DBD thickness: 185 mm, "hopelessly aggressive"

More realistic calculations

- 223.2 mm ( $\Delta = +38.2$  mm) for barrel
- 223,6 mm ( $\Delta = +38.6$  mm) for endcaps





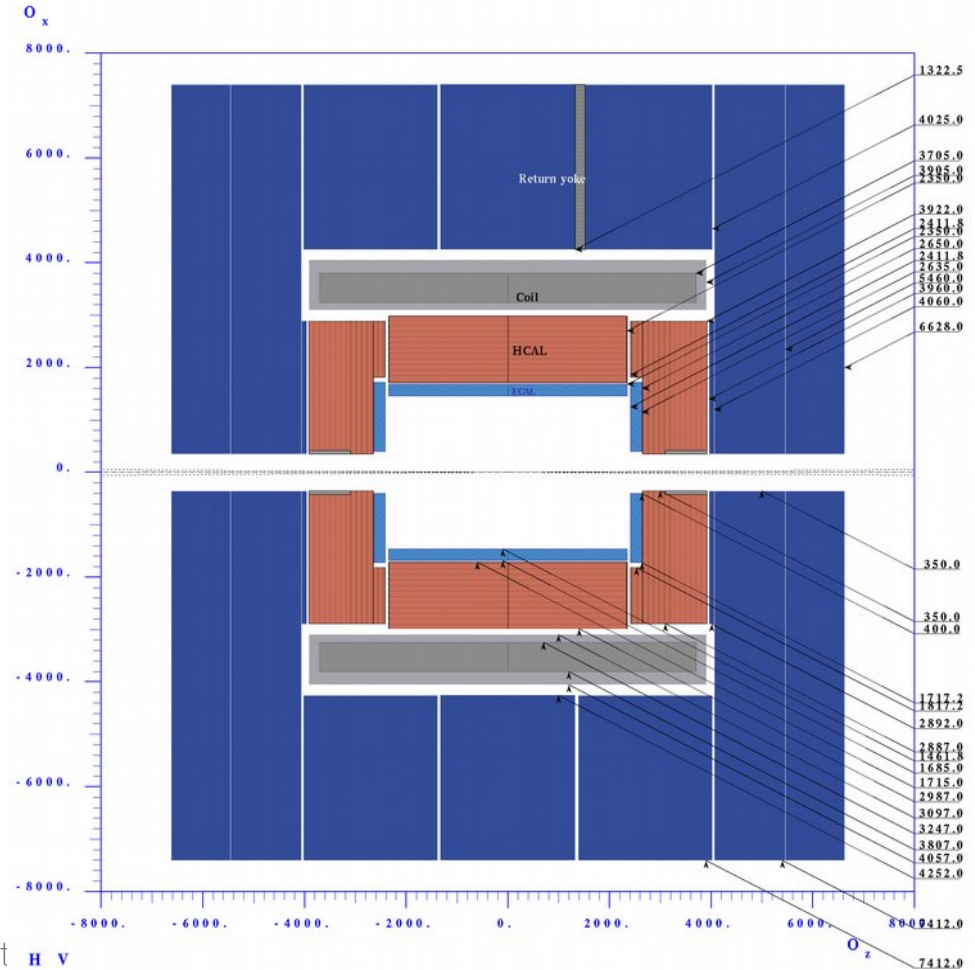
# Small ILD

Same recommendations as for baseline:

- recalculated  $R_{\text{INNER}}^{\text{HCAL, BARREL}}$  as  $1500 + 185 + 30 = 1715\text{mm}$

Small ILD ECal dimensions:

- $R_{\text{INNER}}^{\text{ECal, BARREL}} = R_{\text{INNER}}^{\text{HCAL, BARREL}} - 30\text{mm} - 223.2\text{mm} = 1461.8\text{mm}$
- $Z_{\text{FRONT}}^{\text{ECal, EndCaps}} = 2411.8\text{mm}$  (unchanged from baseline)
- $R_{\text{OUTER}}^{\text{ECal, EndCaps}} = 1717.2\text{mm}$ 
  - 2 modules per quadrant of 4 (inner) and 3 (outer) alveoli
  - The overshoot of the end-cap to the barrel is then 32mm



# Going to 26 Layers: performances

Going from 30 to 26 layers

- Reduction of cost; increase of Energy resolution
  - keep  $24X_0$  (84mm) of Tungsten

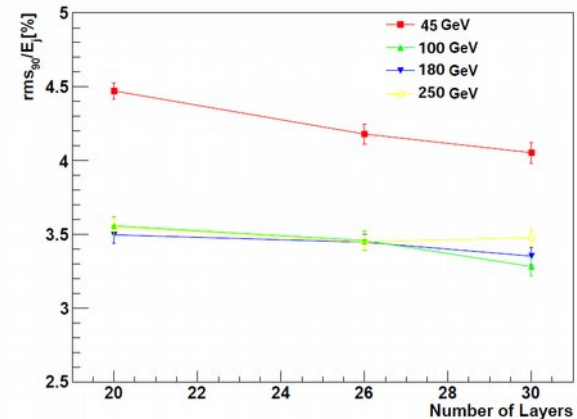
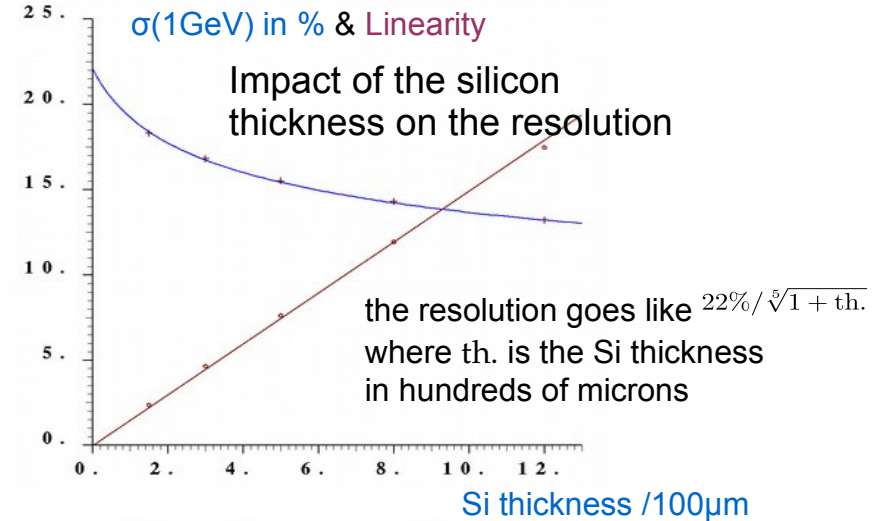
Increasing the Si thickness to 725 $\mu$ m

Energy resolution  $\sigma(E)/E$ :

- for 26 layers w.r.t. 30:  $\nearrow$  +8.5%
  - with 725 $\mu$ m w.r.t 500 $\mu$ m :  $\searrow$  -6.6%  
(-8.7% wrt to DBD 300 $\mu$ m)
- } *near compensation*

Study needed on dead zones (larger GR...), separation, resolution and efficiency performances at low energy.

- eg: JER :  $\sigma(E_J)/E_J$  +6% for 26 layers (500  $\mu$ m) to be redone...  
Shown @ 6<sup>th</sup> ILD Optim meeting (16/07/2014) [[link](#)]

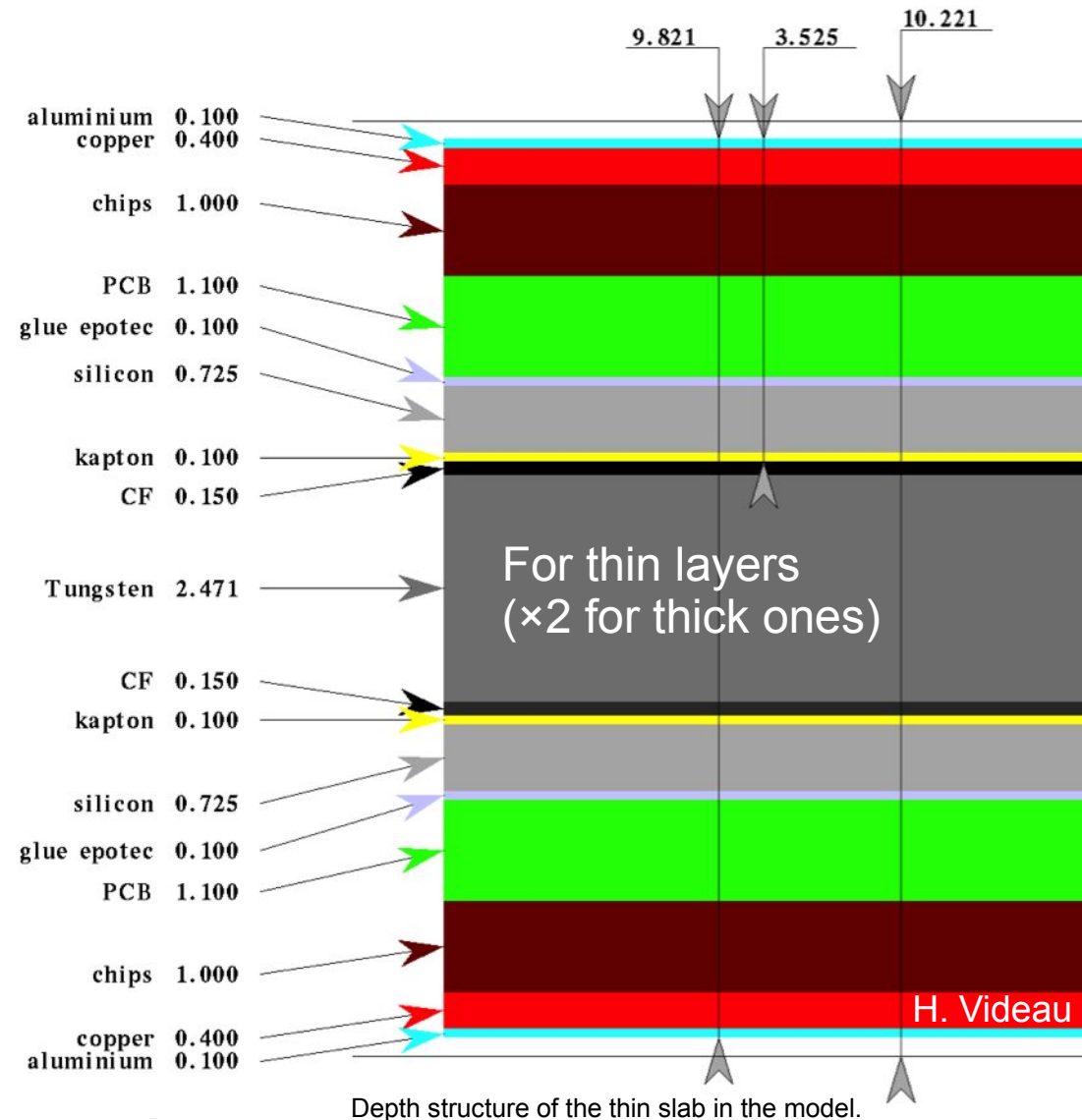


# 26 layers: dimensions

## ECal thickness:

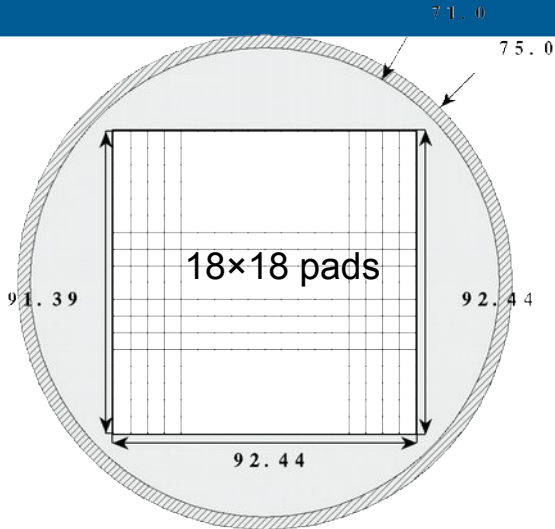
- 26 layers = 18 'simple' layers with 2.47mm of W  
+ 8 'double' layers with 5.6mm  
shared between structure and slabs (4.94mm of W)
  - → 211.9 mm (wrt to 223.9 for 30 layer model)
- → relaxed constraints on
  - clearance margin inside alveoli :  $2 \times 0.1\text{mm} \rightarrow 2 \times 0.2\text{mm}$
  - chip packaging : 0.8mm → 1.0mm
  - PCB thickness : 1.0mm → 1.1mm

**Total:** 223.2mm → **222.2mm** + 1mm clearance

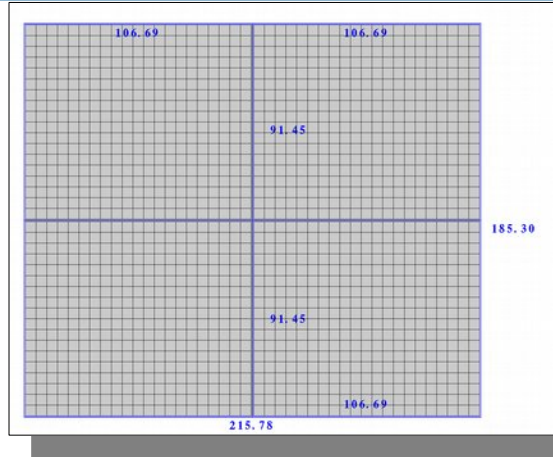




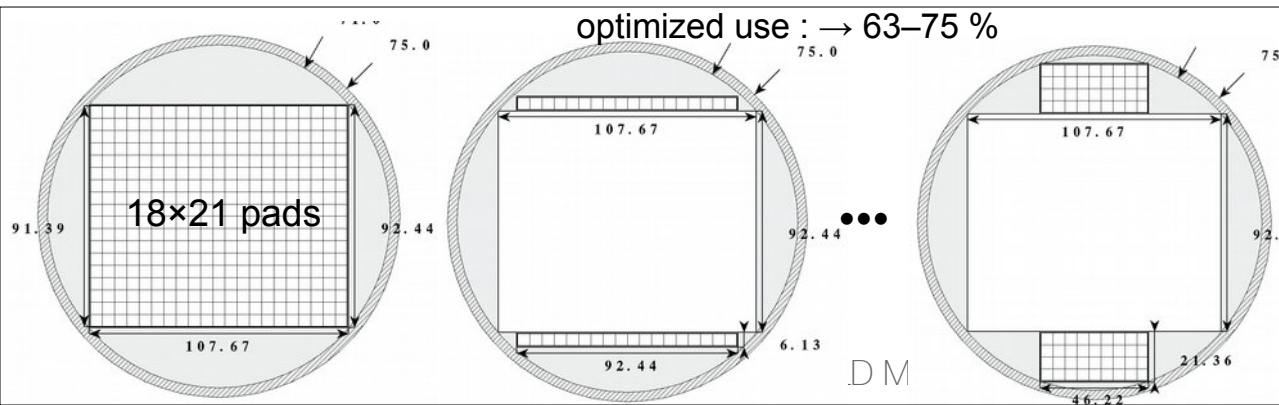
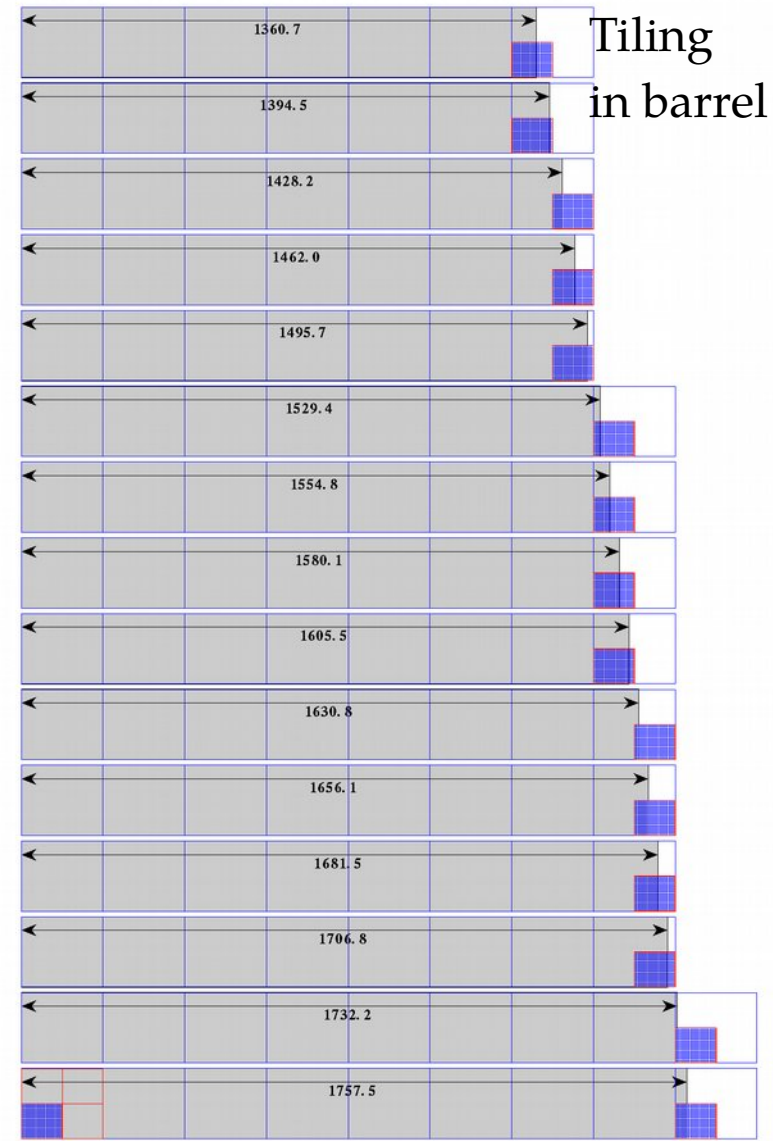
# 150 mm (6'') Wafers



DBD like wafers on 150mm ingot  
54 % use of surface



Pad size = 5.08mm  
(prototype = 5.5mm)



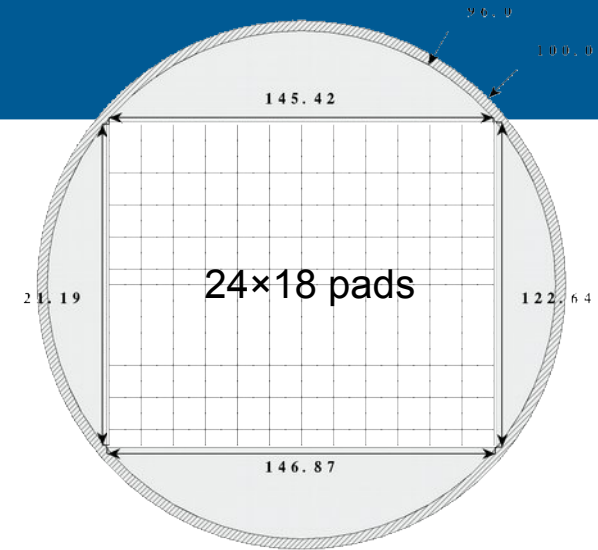
# Going to 200mm Wafers...

From CMS HGCal development & Hamamatsu contacts future is 200mm (8") ingots, 725 $\mu$ m thickness

Mechanical constraints  $\rightarrow$  ~187 mm alveoli, ~12 cm wafer

$\rightarrow$  1.5 Wafers  $\otimes$  cell # mult. of 3  $\otimes$  cell width ~5 mm  $\otimes$  paving with ~64ch ASICs

$\rightarrow$  30 or 36 cells in width



## Optimised ReadOut electronics

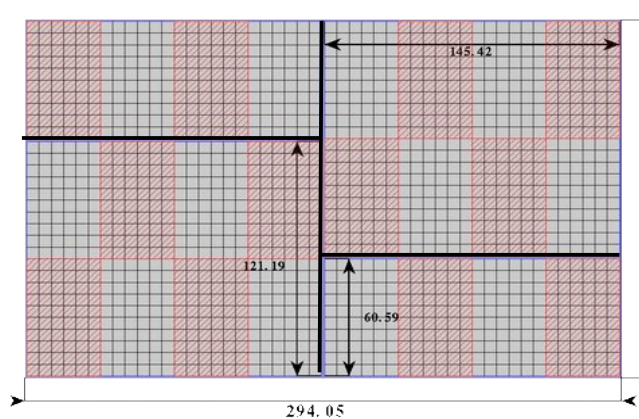
– 6 $\times$ 6mm<sup>2</sup>, ASICs of 60ch.

wrt 5 $\times$ 5mm<sup>2</sup> ( $\Delta$   $\neq$  5.5<sup>2</sup> of prototypes)

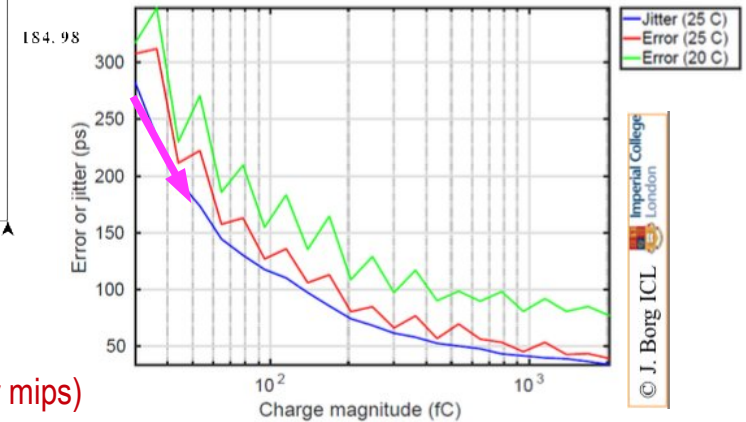
**30%** less electronics consumption cost

– ASU: 1440 pads, 24 ASICs

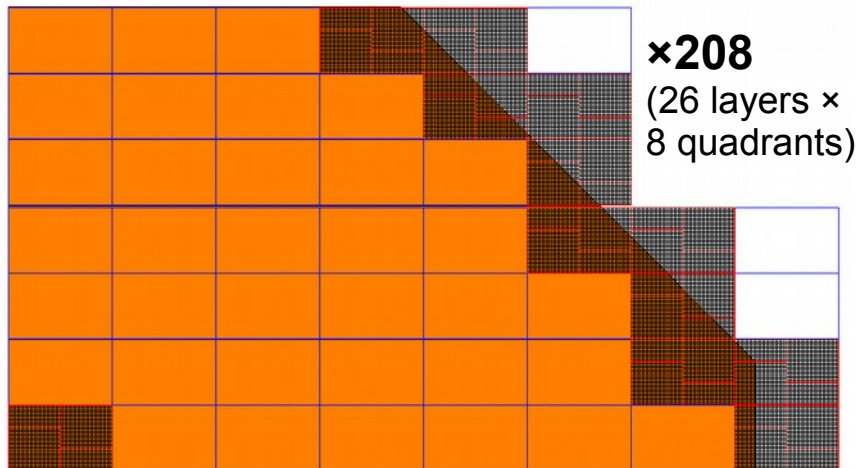
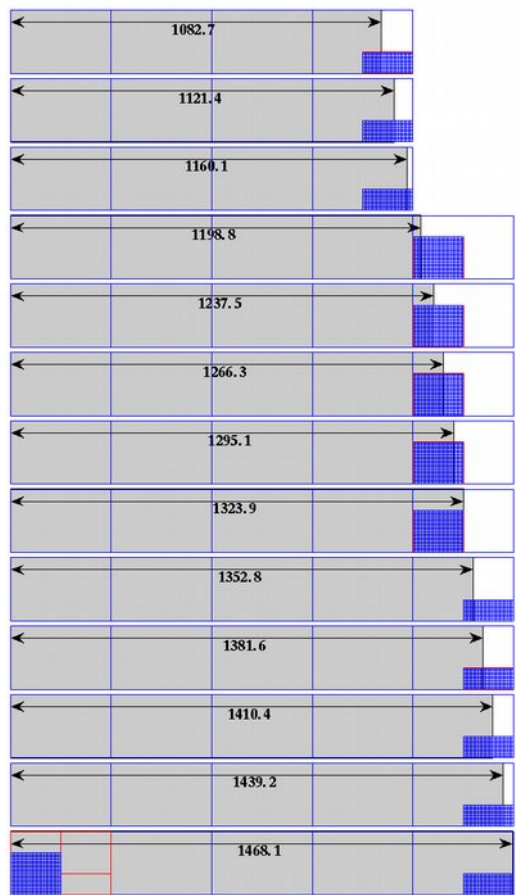
– Noise  $\sim C \sim \text{width}^2/\text{th.} \sim \text{cst}$ , Signal  $\sim \text{th}$   $\nearrow$ , S/N  $\sim \times 1.5$ ; depl. Voltage  $\sim \text{th}^2 (\times 2)$   
 $\Rightarrow$  Improved timing perf (esp. for mipS)



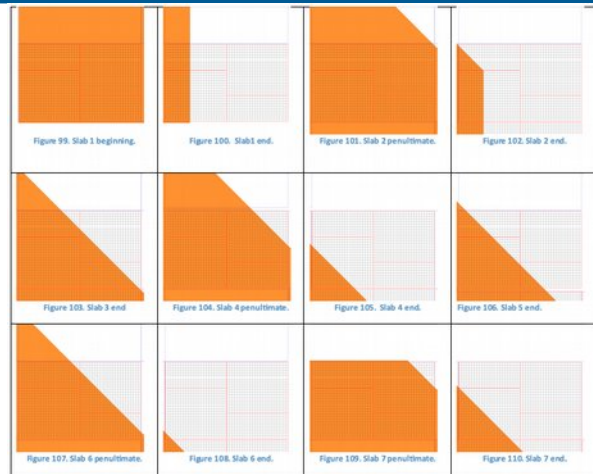
wafers on 200mm ingot ; 63 % use of surface



# Tiling with 200mm (8'') wafers



**×208**  
(26 layers × 8 quadrants)

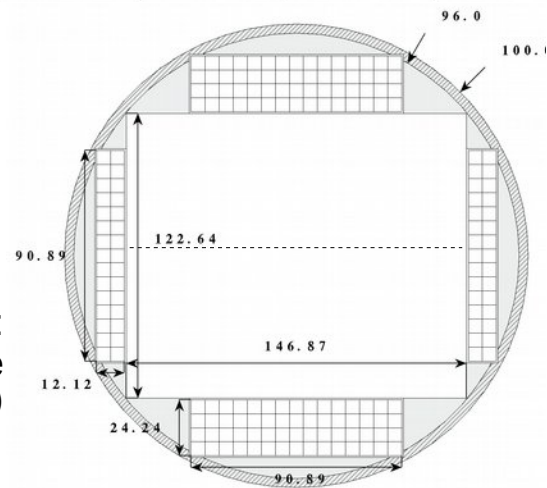


*Matching of large and small rectangles, triangles and diamonds to be detailed for optimal use*

add'l small rectangles:  
87 % use of surface  
(83 % for an hexagonal shape)

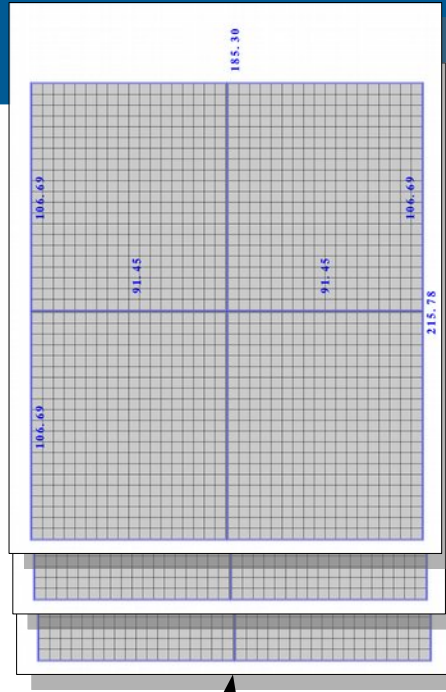
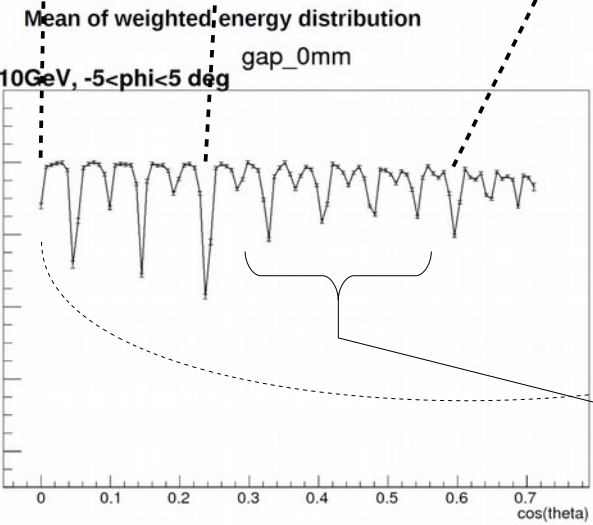
**×400**

(2 sides × 5 columns × 40 modules)

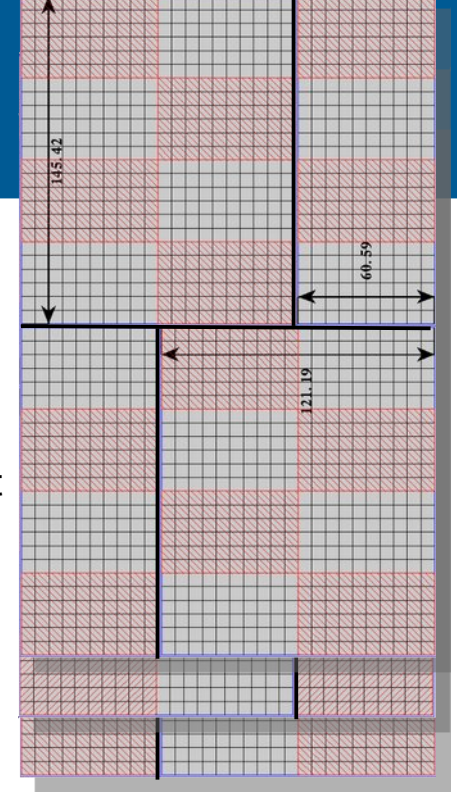




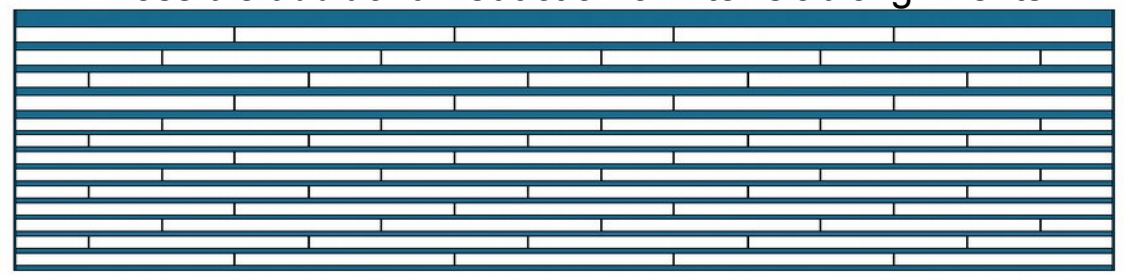
# Reduced gaps



Reduced alignment  
of inter-wafer gap



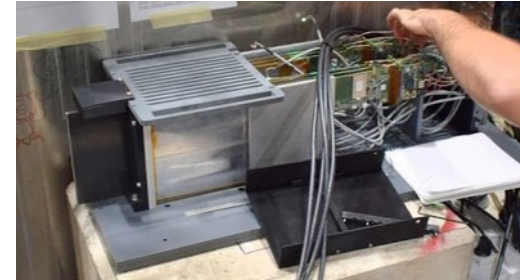
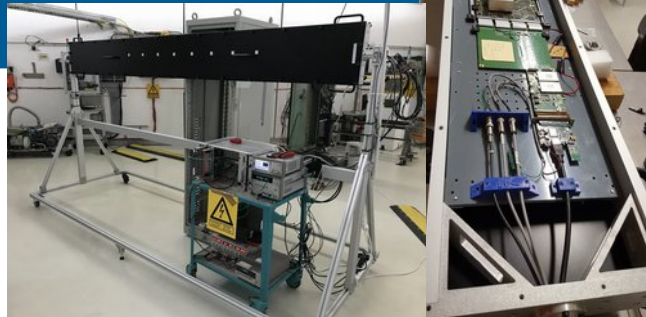
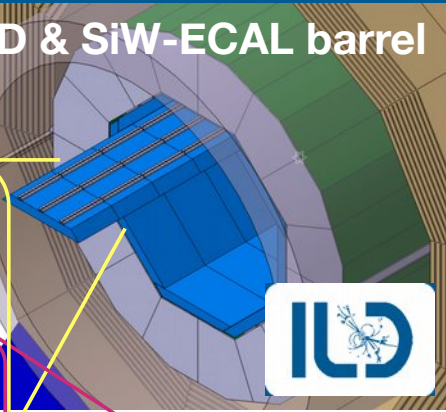
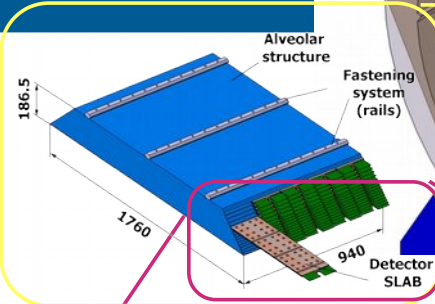
Possible *additional* reduction of inter-slab alignments



# ILD & SiW-ECAL barrel

2018

# Prototypes



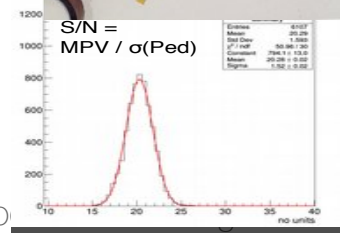
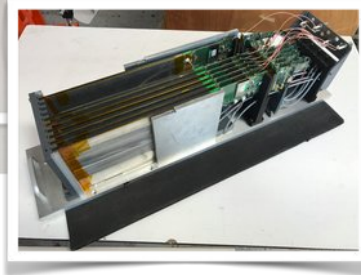
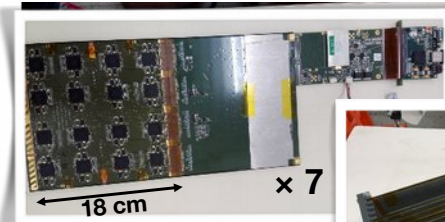
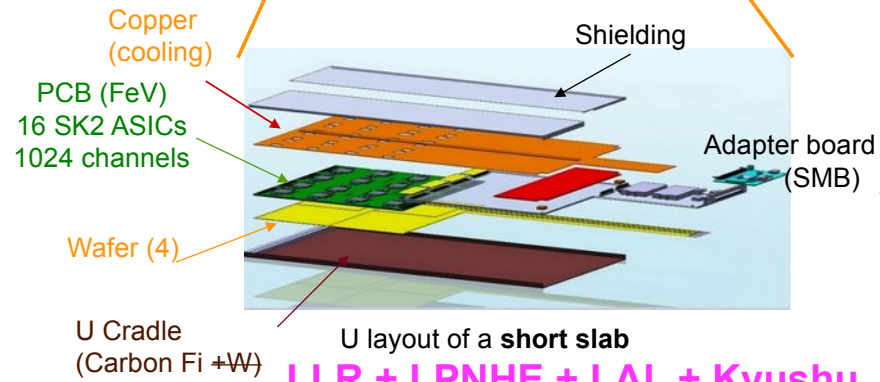
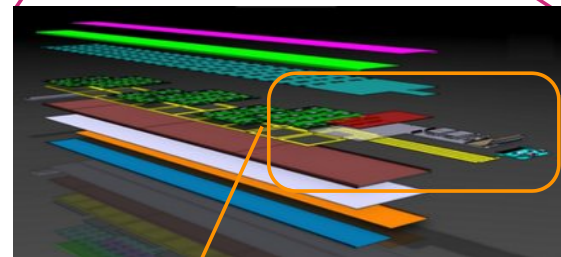
## SLAB « long » ( $\leq 12$ ASU)

- Partie électronique + Baby W. (Signals, Power P.,)
- ⇒ Design Realistic SLAB

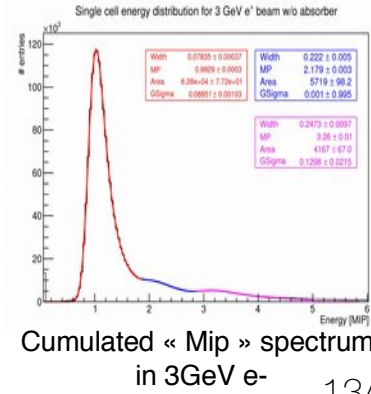
2018

## Prototype technologique (1 ASU)

Tests au DESY (8 layers) & CERN (10 layers  $\supset$  4 FEV13, 650 $\mu$ m)



$S/N_{\text{Trig}} \sim 12$





# 1<sup>st</sup> “electric long slab”

*M. Anduze, F. Magniette, J. Nanni,  
Realisation: G. Fayolle*

## Scale to support electronics

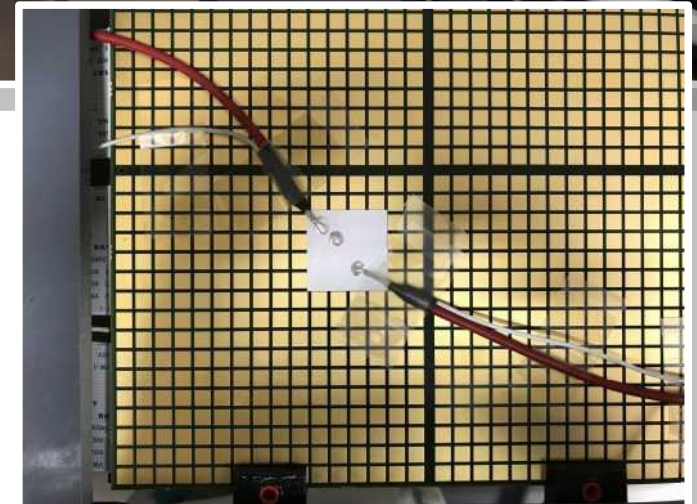
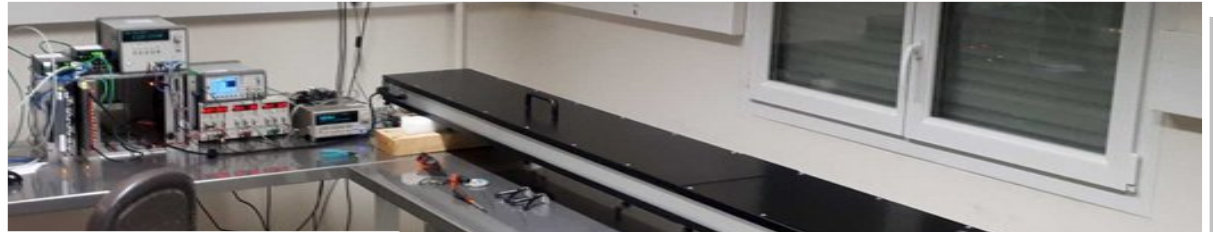
- Support of interface boards + 12 ASUs (DBD)
- 2+6+4 ASUs = ~3.2 m
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom

## Mechanical characteristics

- Movable: table and to beam test
- Rotatably along long axis (for beam test)
- Rigidity :  $\leq \sim 1$  mm per ASU
- No electrical contacts scale / cards

## Shielding

- vs Light and CEM

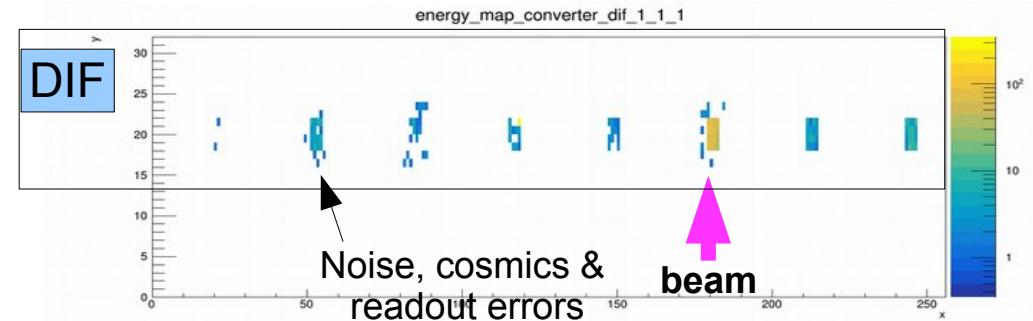
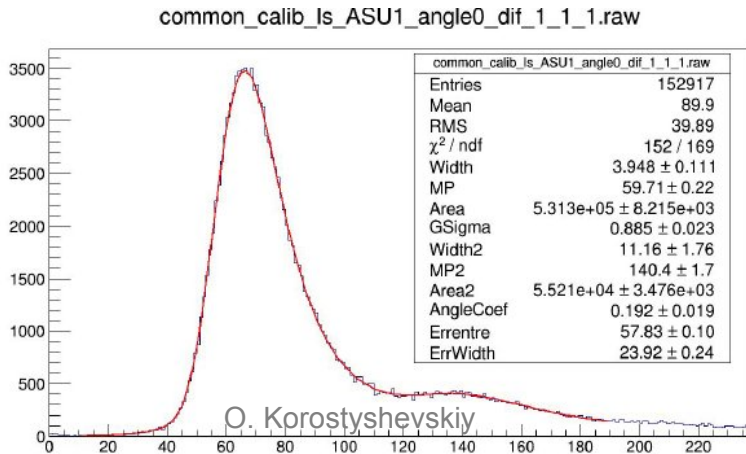
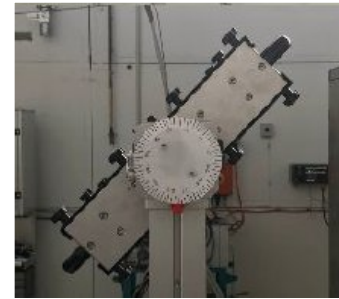




# DESY-2018 beam test

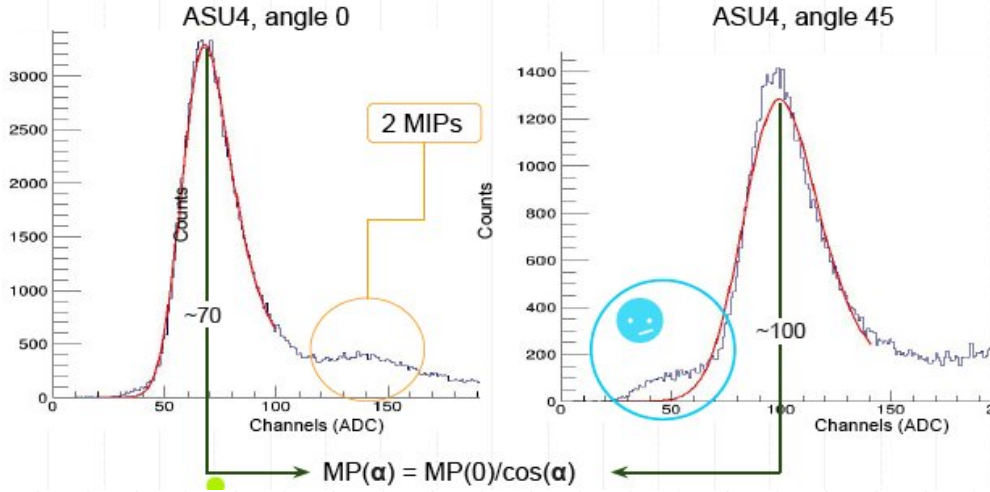
2 weeks beg of July: full test of all prototypes:

- Electric long slab: 8 FEV11 + baby-wafers ( $320\mu\text{m } 2\times 2\text{cm}^2$ ):
- RC Filtering of HV between (every second) boards required
- Very clean response to “mip” (punch through  $e^-$ )

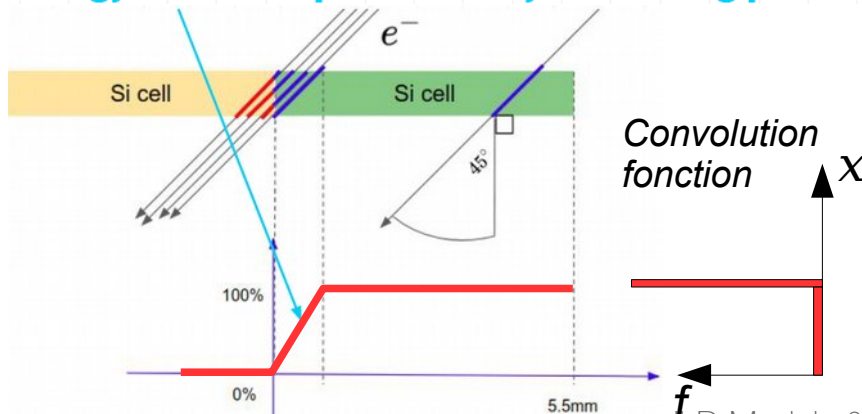


# Mip analysis

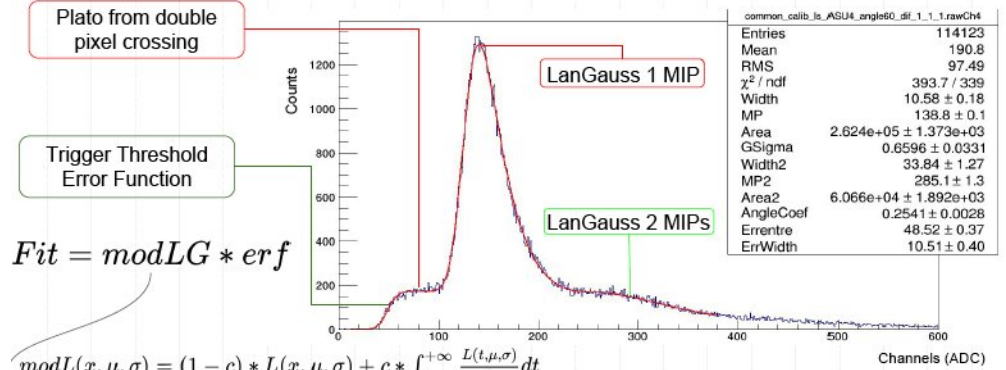
O. Korostyshevskiy



Pixel energy fraction depends linearly on crossing position



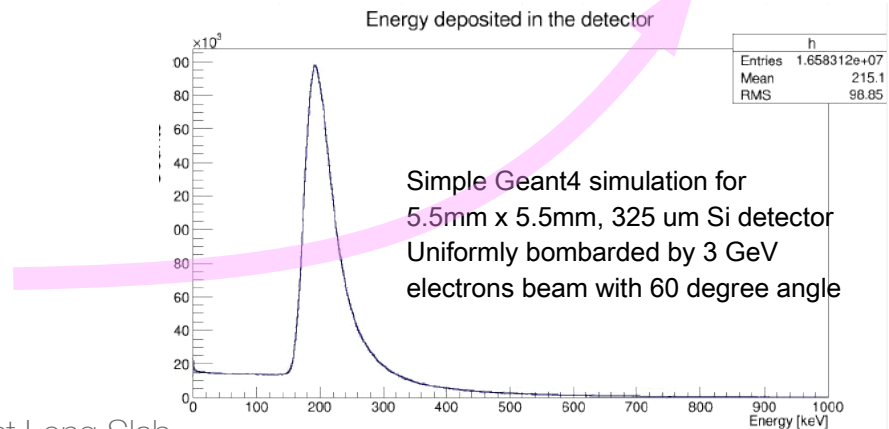
Fit with Mod LanGau function



$$Fit = modLG * erf$$

$$modL(x, \mu, \sigma) = (1 - c) * L(x, \mu, \sigma) + c * \int_x^{+\infty} \frac{L(t, \mu, \sigma)}{t} dt$$

$$modLG = \int_{-\infty}^{+\infty} modL(t, \mu, \sigma) * G(x - t, \mu_G, \sigma_G) dt$$

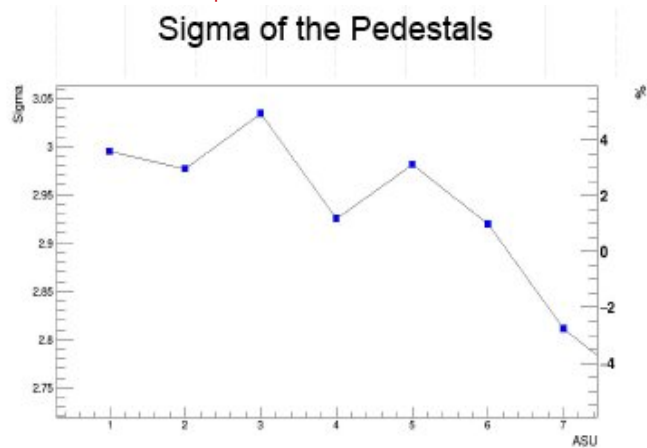


Simple Geant4 simulation for 5.5mm x 5.5mm, 325 um Si detector Uniformly bombarded by 3 GeV electrons beam with 60 degree angle

# MIP response vs position

mip MPV \*cos( $\theta$ ) vs ASU#

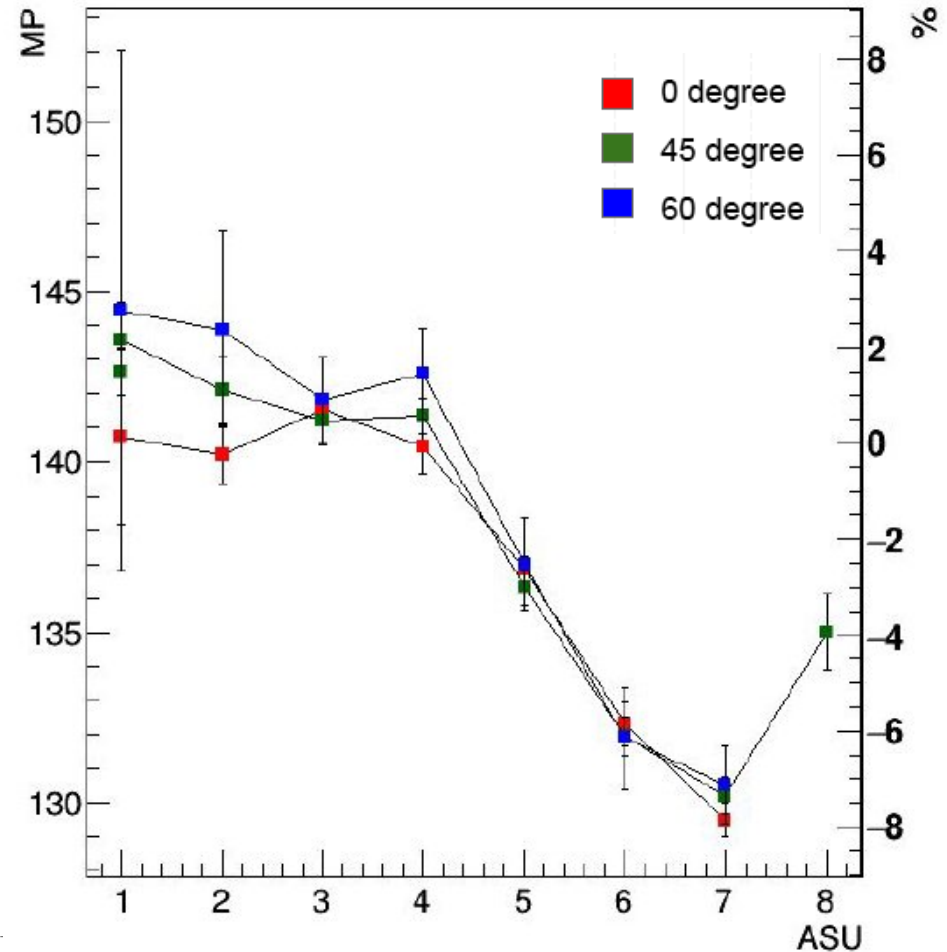
- OK for 4 1<sup>st</sup> ASU's
- Small drop ~of signal ~2%/ASU for  $\geq$  ASU#5
- Also hints similar drop on  $\sigma_{ped}$



⇒ Voltage & Gain drop ?

Power pulsed mode with ballast et end of slab

(or just random build-up effect from chip variability ?)



# Conclusions & prospectives

3 models described in detail for the ILD SiW-ECAL: *baseline*, *small*, small with 26 layers:

- 725 $\mu\text{m}$  thickness with 200mm (8") wafers ; 5.08  $\rightarrow$  6mm cell size
  - ~ identical photon resolution expected
  - 13% gain cost on Silicon surface, PCB, and 40% on electronics (and power consumption) wrt DBD
  - Improved S/N ratio & timing, less channeling @ 90°

⊗ Feasibility improved:

- **Single ASU + 1st connexion: S/N ratio, Stability, Uniformity between elements; assessed**  
CALICE technical prototype (11 working ASU as of now)
  - Wafer of 325 $\mu\text{m}$ , **650 $\mu\text{m}$  tested**  $\rightarrow$  725  $\mu\text{m}$  ? Hamamatsu ✓ Others: LFoundry(SMIC), Infineon, Elma, On-Semi
  - Wafer production: learn from HGAL, statistics from current wafer batch ?
- **Long SLAB: 1<sup>st</sup> readout over long chain: design R&D, power distribution, grounding; connexions between ASU's**
  - $\Rightarrow$  adjustment on HV & LV distribution, clock distribution needed  $\Rightarrow$  realistic ( $\supset$  mech. constraints) design in 2019 ?

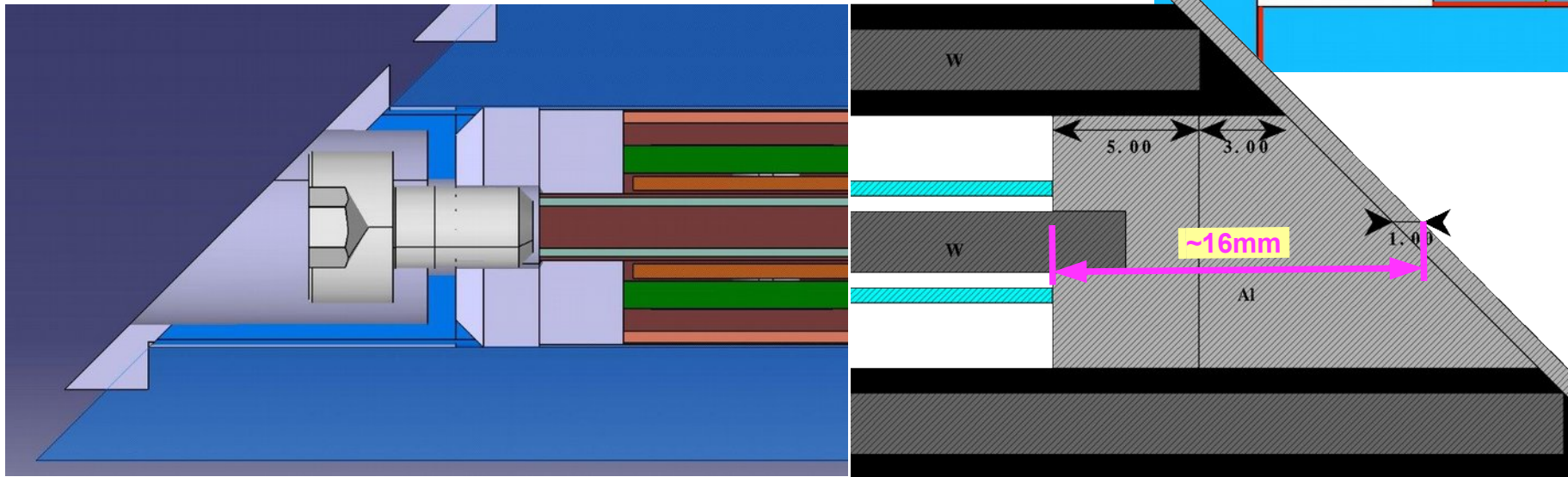
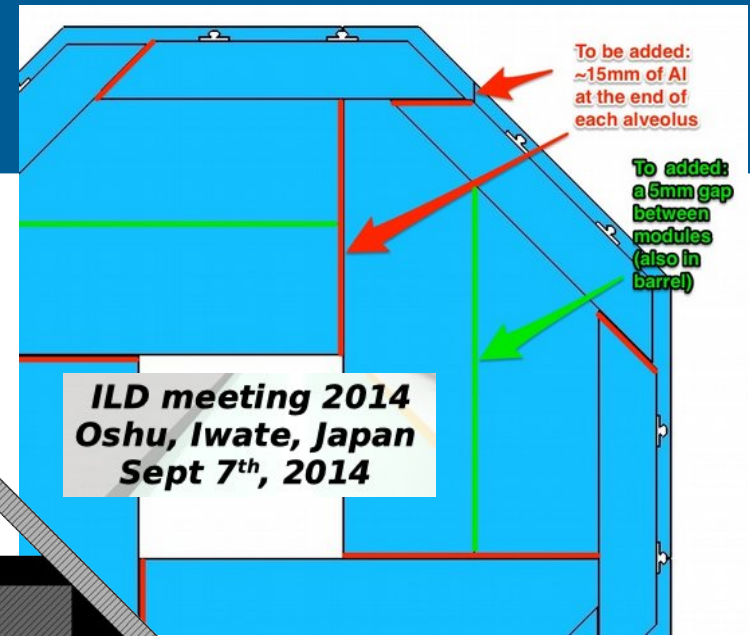
# Back-up

# Slab plug

The slab plug is identical for both models.

On top of the TDD model an aluminium plate of 0.7mm has been added (simulation)

Example of realistic design (M.A.)



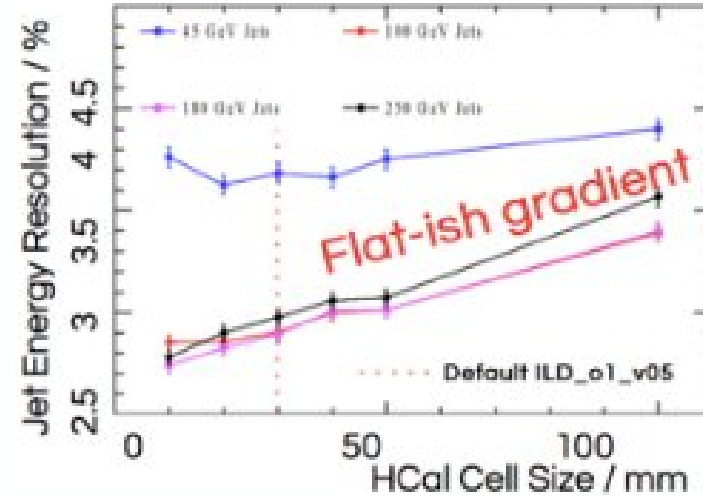
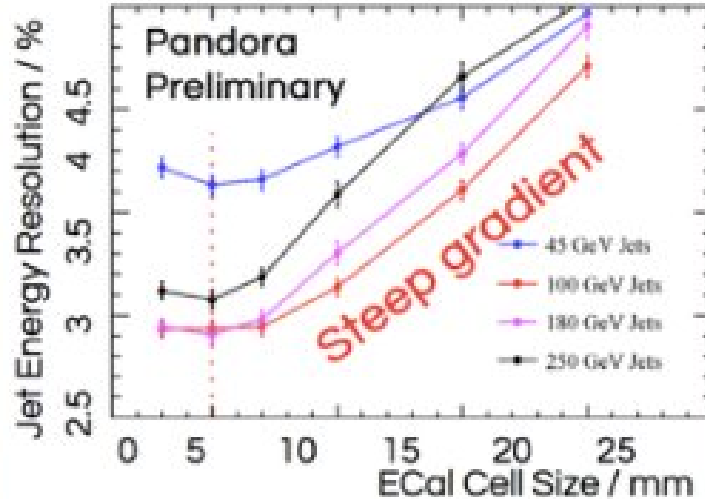


# Sketch for a Historical Picture of the Progress of the ILD Silicon ECAL

Milestone	Date	Object	Details	REM
1 <sup>st</sup> ASIC proto	2007	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1 <sup>st</sup> ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1 <sup>st</sup> prototype of a PCB	2010	FEV7	8 SK2	COB
1 <sup>st</sup> working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1 <sup>st</sup> working ASU in BT	2012	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1 <sup>st</sup> run in PP	2013	FEV8-CIP		BGA, PP
1 <sup>st</sup> full ASU	2015	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1 <sup>st</sup> SLABs	2016	FEV10 & 11	7 units	
pre-calo	2017	FEV10 & 11	7 units	S/N ~ 20, 6–8 % masked
1 <sup>st</sup> technological ECAL ?	2018	SLABvFEV10 & 11 & 13 SK2a+ COB + Compact stack	SK2 & SK2a (▷timing)	Improved S/N Timing...

# Optimal cell-size (DBD)

## \* Detector optimisation studies (Cambridge/DESY):



\*See optimisation studies slides for reconstruction details.