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On-going Development of CMOS Pixel Sensors: on the road of reaching ILC vertex detector requirements

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CMOS Pixel Sensors (CPS) are currently developed for the CBM Micro-Vertex Detector at FAIR/GSI, extrapolating from the ALPIDE
chip fabricated for the ALICE-ITS. The MIMOSIS sensor for CBM will provide resolutions of 5 mum and 5 mus to comply with the CBM requirements and a 50 times higher data flow capacity compared to ALPIDE. Sensors adapted to the ILC requirements are expected to be directly derivable from this chip, with spatial resolution of about 4 mum, read-out time of about 1-2 mus and instantaneous data flow of about few GB/s. This talk will describe the MIMOSIS architecture and the roadmap to adapt it to the ILC requirements. Furthermore, the MIMOSIS-0 sensor, fabricated in 2017 (in the 0.18 mum Tower-Jazz process) has been tested this current year and its results will be shown. Based on this architecture, power consumption estimates of the ILD vertex detector has been reevaluated more precisely and will also be presented. Finally, 2 double sided ladder PLUME have been operated in the BEAST-II infrastructure at superKEKB and were running continuously
from March to July 2018. As a first successful use of CMOS sensors
in an e+e- environment, a feedback experience will be provided.

Presenter: BESSON, Auguste Guillaume (Centre National de la Recherche Scientifique (FR))

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