HV-CMOS: Design of a sampling pixel to minimize time walk

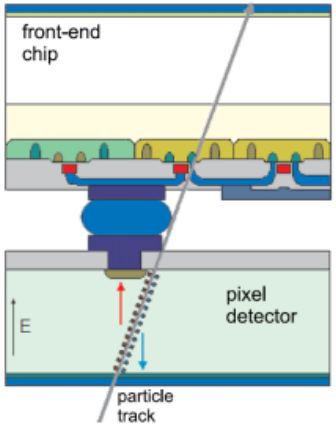
O. Alonso, S. Moreno, D. Prades, A. Vilà, E. Vilella, J. Vossebeld, G. Casse and A. Diéguez

SIC, Department of Electronic and Biomedical Engineering, University of Barcelona, Spain

oalonso@el.ub.edu

Overview

Hybrid Pixel Detectors



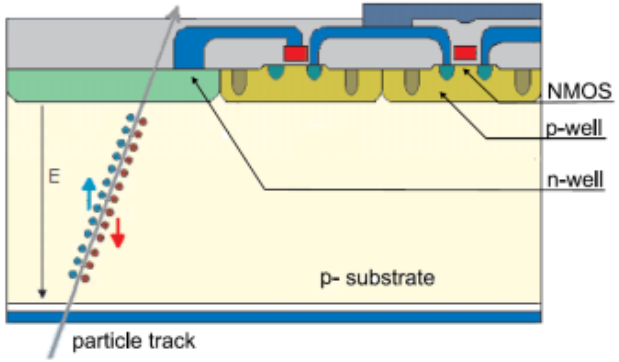
Advantages:

- Choice of the best technology for the sensing device and the RO circuitry
  - ➔ Radiation tolerance to high integrated fluences (2×10^{16} 1 MeV n_{eq}/cm^2)
  - ➔ Capability to cope with high data rates

Disadvantages:

- Bump-bonding process
  - ➔ Complex and expensive assembly process
  - ➔ Limited fabrication rate
- Multi-layer nature
  - ➔ Substantial material thickness (300 µm)
  - ➔ Limited accuracy to measure particles trajectories

Depleted Monolithic Pixels



Images taken from the presentation of T. Hemperek @ PIXEL 2016

Advantages:

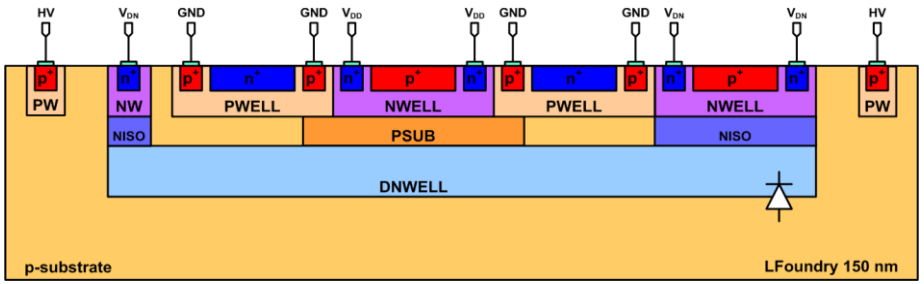
- Integration of the sensing device and the RO circuitry in a single layer of silicon thanks to industry standard processes of fabrication
  - ➔ No need for interconnection with solder bumps
  - ➔ Fast turn-around production and lower costs
  - ➔ Thin material thickness (50 µm)

Disadvantages:

- For some future experiments, the best radiation tolerance (10^{15} 1 MeV n_{eq}/cm^2) and timing resolution (13 ns) achieved so far need to be improved

Overview

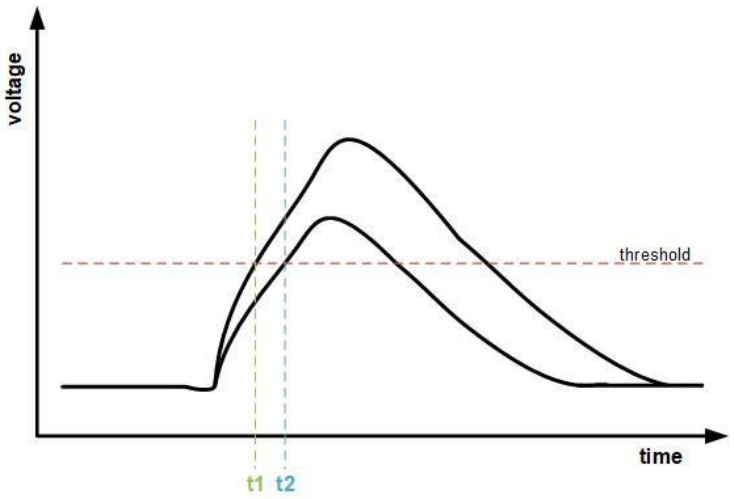
- HV-CMOS sensors emerging as an attractive solution for future experiments in particle physics:
  - Fast signal collection times (potentially hundreds of ps)
  - Radiation tolerances up to 10^{15} n_{eq}/cm^2
- HV-CMOS sensors will be used for the first time in the tracker of the **Mu3e** Phase-I experiment
- HV-CMOS sensors are also considered for future experiments like:
  - Inner Tracker (ITk) of the ATLAS detector (Phase-II Upgrade)
  - Vertex Locator (VELO) of LHCb
  - Compact LInear Collider (CLIC)



Cross-section of a HV-CMOS pixel designed in 150 nm Technology from Lfoundry (image taken from "Report on recent activities in HV-CMOS detectors for Mu3e, ATLAS and RD50", E. Vilella et al.)

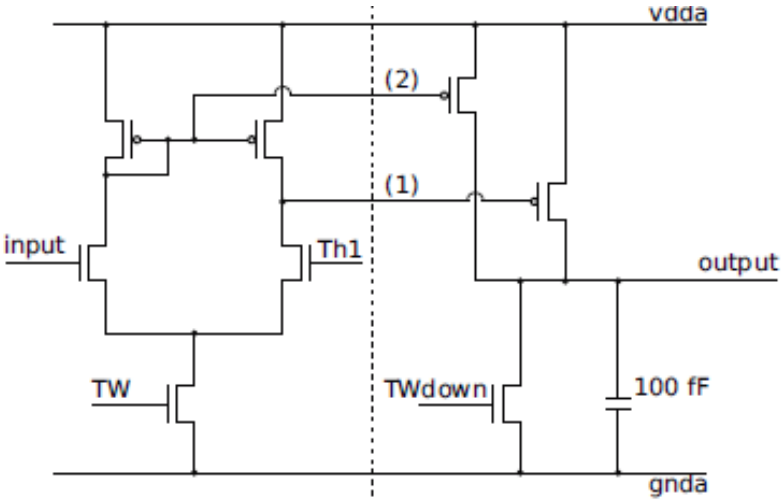
Overview

- Fast collection times enables HV-CMOS sensor for precision 4D tracking with information about the energy.
- The standard way to measure the time of particle arrival is to set a threshold and saving the time when the signal exceeds it
- Time walk decreases the time precision
- Some authors achieved to lower the time walk down to 10 -14 ns applying some “corrections”

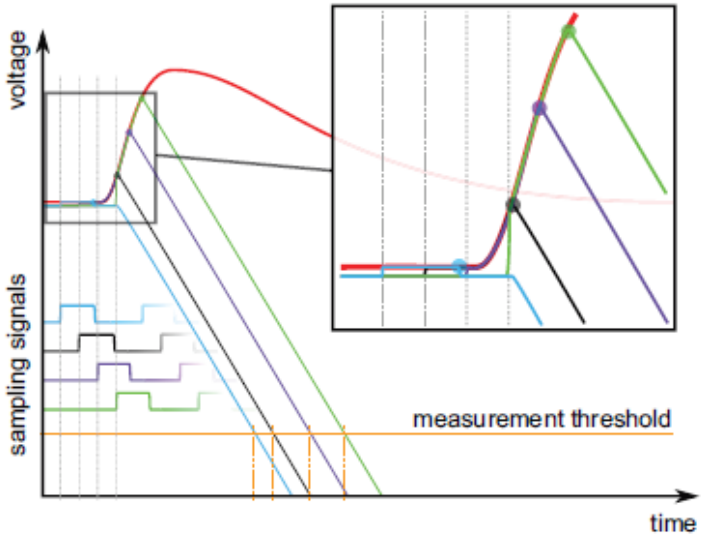


Overview

1. HVCMOS Pixel Detectors – Methods for Enhancement of Time Resolution (R. Schimassek et al.)



Simplified schematics of the time walk compensating comparator showing the comparator stage on the left and the time walk compensation stage on the right



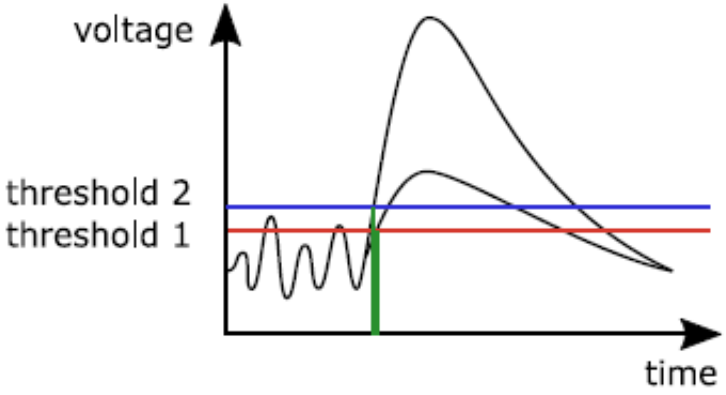
Measurement principle of the signal sampling method as implemented on an integrated sensor

Time walk below 25 ns

Time walk below 10 ns (in simulations)

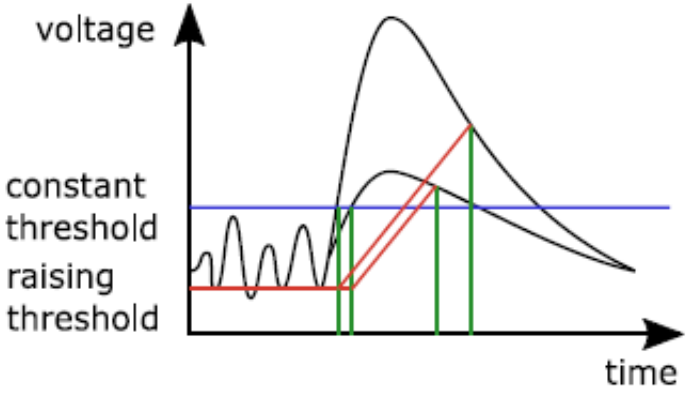
Overview

2. MuPix8 — Large area monolithic HVCMOS pixel detector for the Mu3e experiment (H. Augustin et al.)



Using two threshold voltages: One threshold near to the noise level; the second threshold has to be higher to confirm that the first timestamp is not noise.

Time walk around 14 ns



Using and ADC: It uses one constant threshold voltage and one linear rising threshold. The constant threshold saves the timestamp and activates the linear rising threshold. The voltage of the ramp signal should start below the baseline of the chip. The advantage is less noise and a better linearity

Time walk below 14 ns

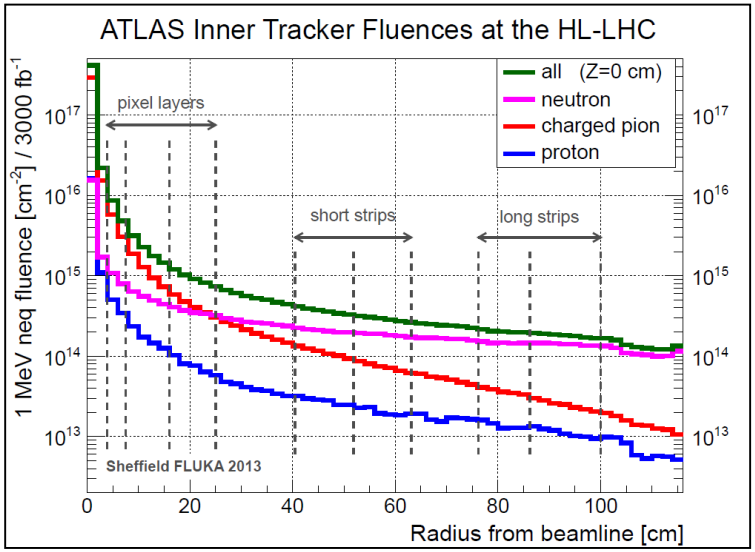
Outline

- Overview
- Objectives
- Circuit proposals
  - Analog Sampling
  - TDC
  - TDC + Analog Sampling
  - Simulated results
- Conclusions

Objectives: CERN-RD50

CERN-RD50 project

- An international R&D collaboration aimed at developing radiation hard semiconductor devices for high luminosity colliders:
  - High Luminosity-LHC (HL-LHC)
  - Future Circular Collider (FCC)
- Semiconductor detectors will be exposed to hadron fluences equivalent to:
  - **HL-LHC:** >10^{16} 1 MeV n_{eq}/cm^2
  - **FCC:** >7×10^{17} 1 MeV n_{eq}/cm^2
  - ➔ detectors used now at LHC cannot operate after such irradiation.
- R&D in new structures:
  - N in p sensors
  - 3D
  - LGAD
  - Depleted CMOS



Ref.: I. Dawson, P. S. Miyagawa, Atlas Upgrade radiation background simulations

- Depleted CMOS technology has emerged as a prime candidate for future tracking detectors in particle physics experiments that require **high-speed sensors** with the **ability to cope with high occupancy and integrated radiation dose**.
- It is a priority for RD50 to study this type of device: the collaboration has started a new effort to develop matrices of pixels and dedicated test structures in depleted CMOS processes.
- Key areas that will be covered in this presentation: **Time resolution**

Objectives: CERN-RD50

RD50-ENGRUN1 - Aims:

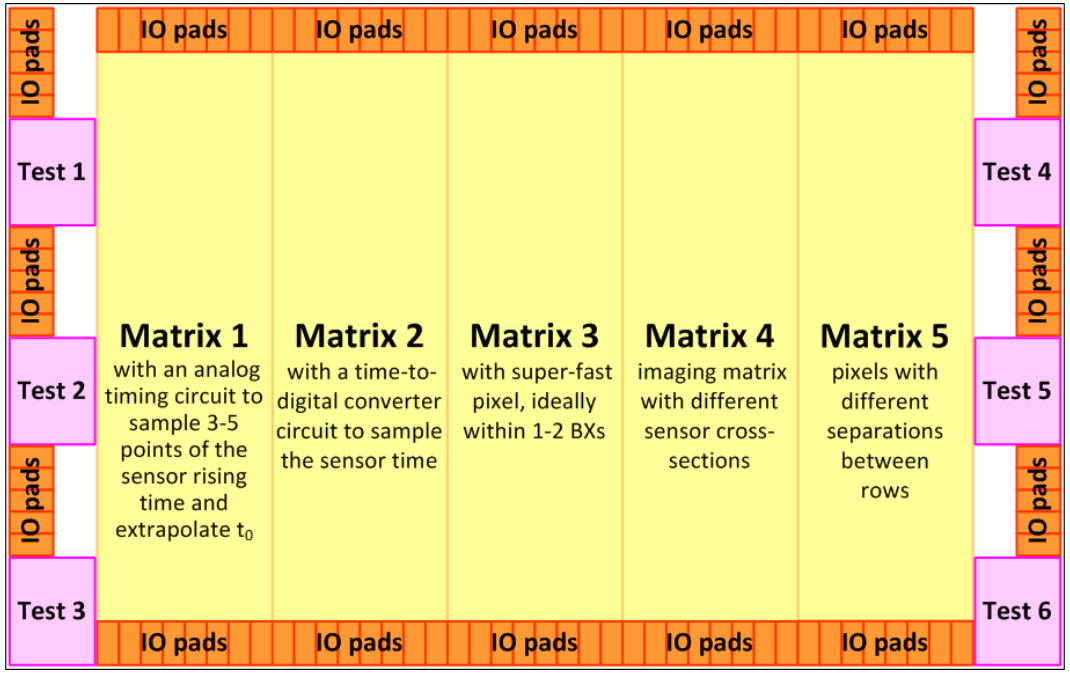
- Improve the current time resolution of HV-CMOS sensors by a factor 10 with dedicated RO circuits
- Implement new sensor cross-sections
- Study pre-stitching options to increase the device area beyond the reticle size limitation
- Improve the current radiation tolerance with careful sensor design and backside processing

Technology:

- 150 nm HV-CMOS from LFoundry
- Large area submission (MLM)

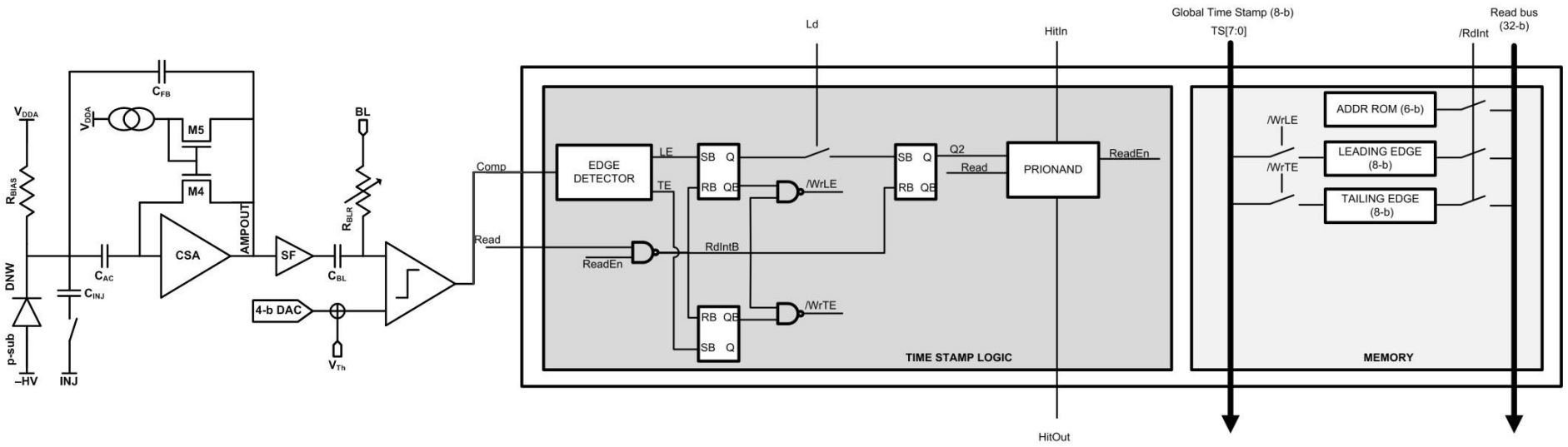
Design effort:

- FBK-Trento (N. Massari and C. Zhang)
- IFAE-Barcelona (R. Casanova)
- IFIC-Valencia (R. Marco)
- Uni. Barcelona (O. Alonso, S. Moreno and A. Diéguez)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang) + overall coordination
- Uni. Seville (J. M. Hinojo, F. Muñoz and R. Palomo)
- Bonn/CPPM/IRFU collaborate with support



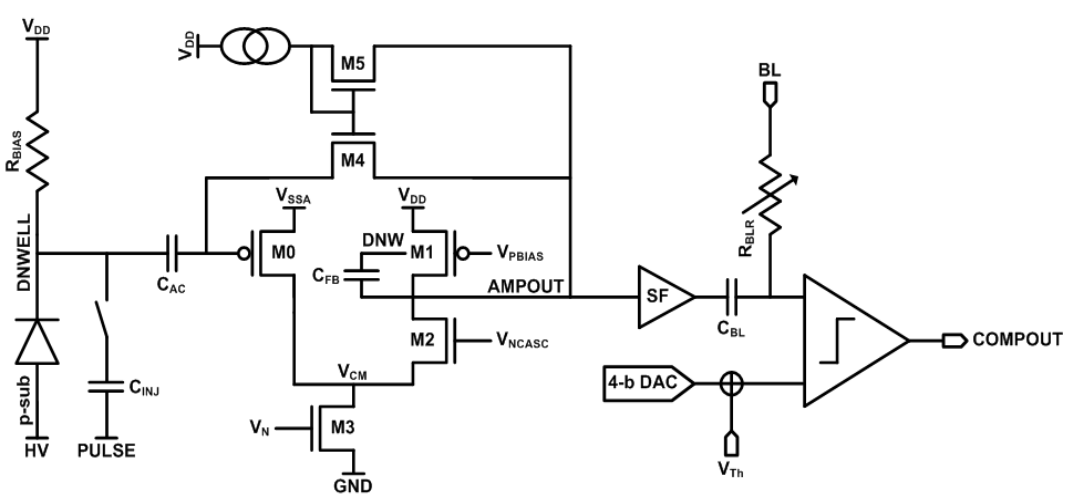
Test structure 1 Simple CMOS capacitors to study oxide thickness
Test structure 2 10 x 10 matrix of very small pixels with passive RO
Test structure 3 10 x 10 matrix of very small pixels with 3T-like RO
Test structure 4 Small matrix of pixels for TCT, e-TCT and TPA-TCT
Test structure 5 Single pixels for sensor capacitance measurements
Test structure 6 …

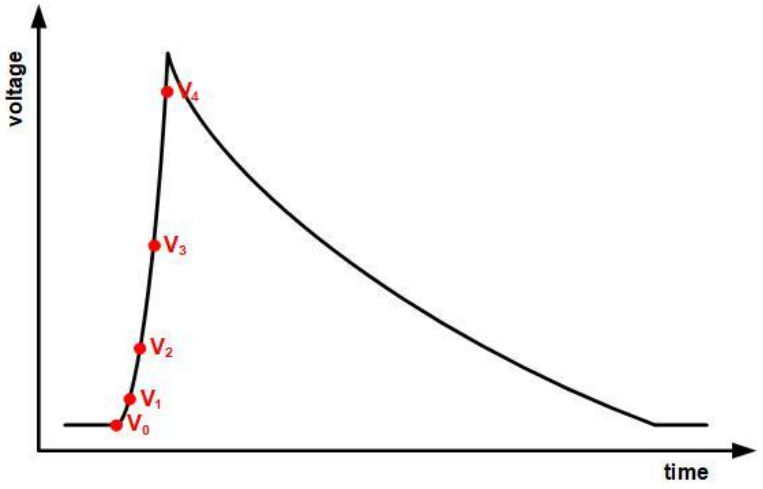
Objectives



- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- The **digital readout** is based on the FE-I3:
  - **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
  - ToT = TE – LE (off-chip)
  - **One 8-bit ROM memory** to store the pixel address
  - **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

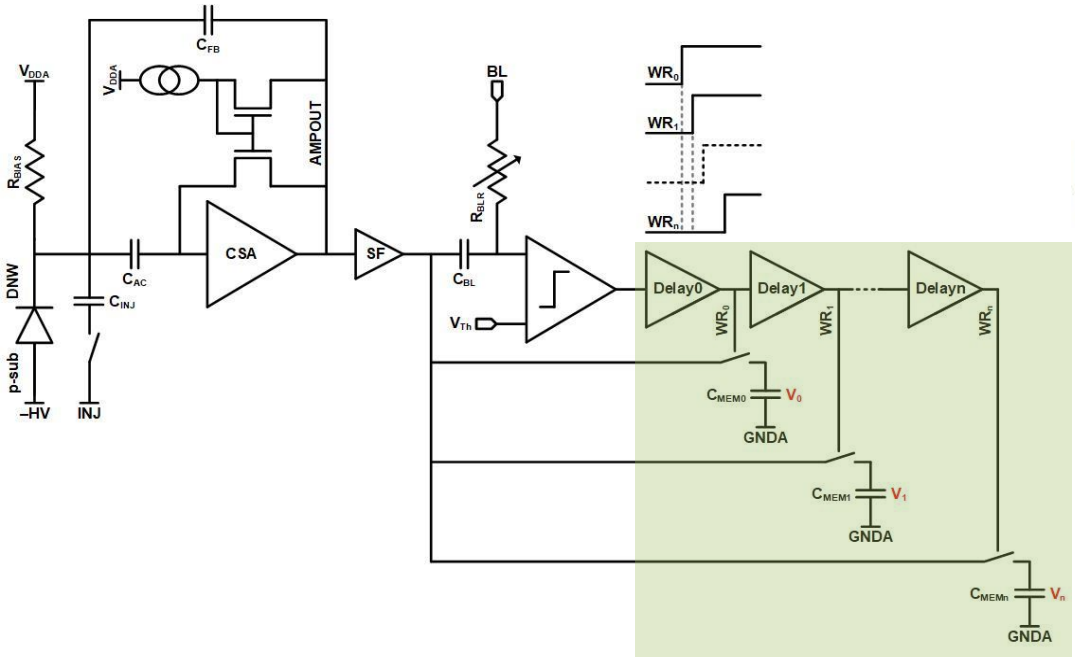
Circuit proposal: Analog Sampling (AS)

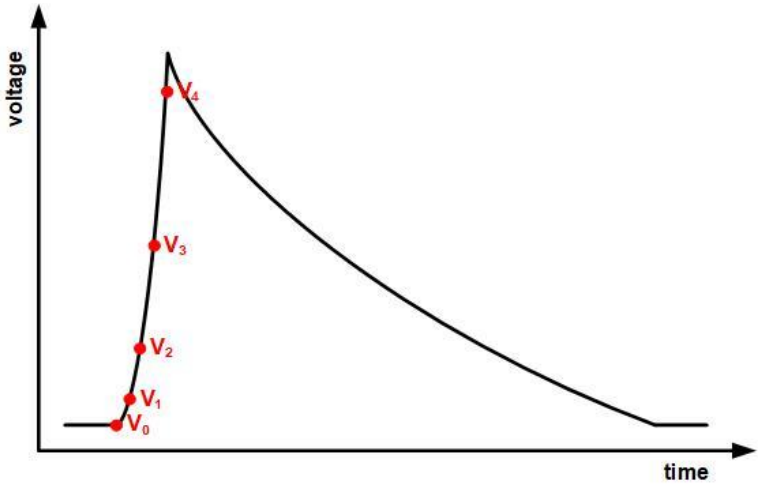




- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

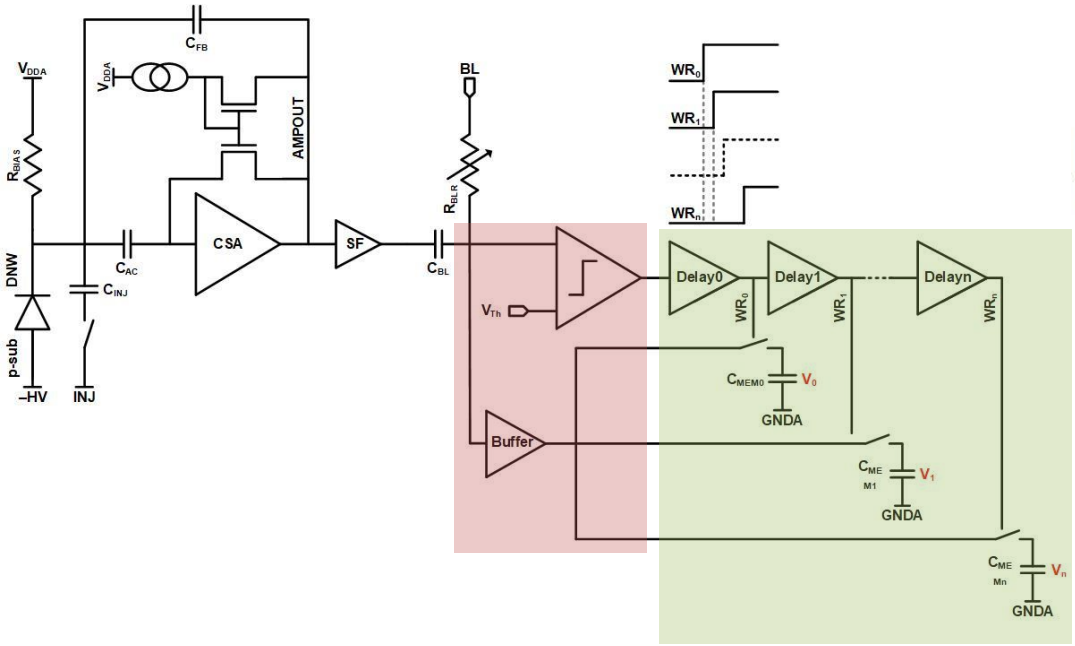
Circuit proposal: AS

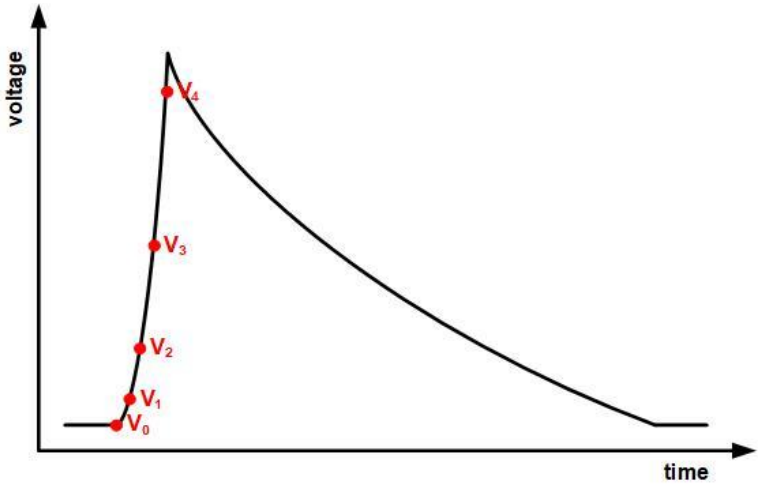




- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
  - Programmable chain delay to sample 5 points of SF signal
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

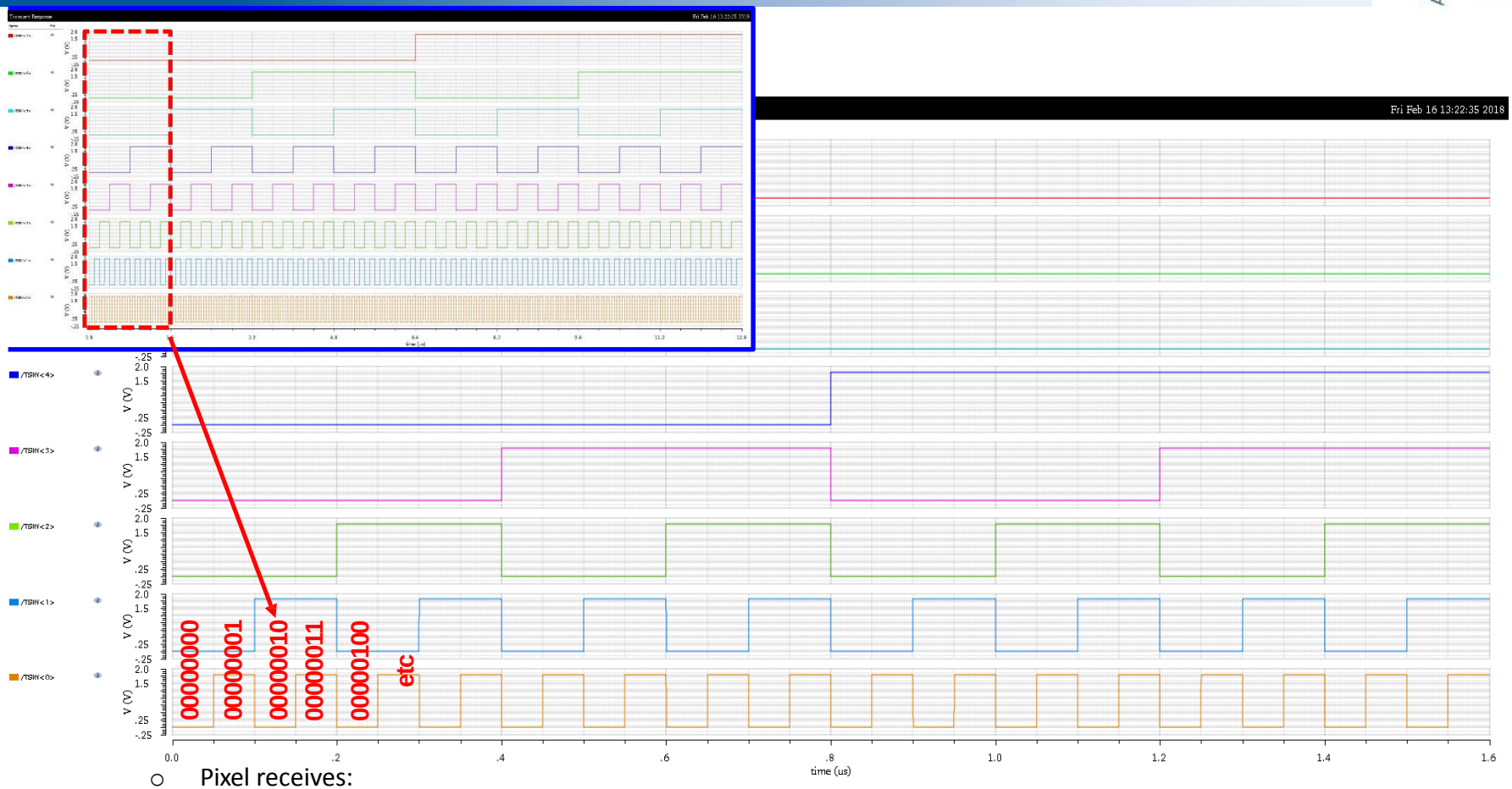
Circuit proposal: AS





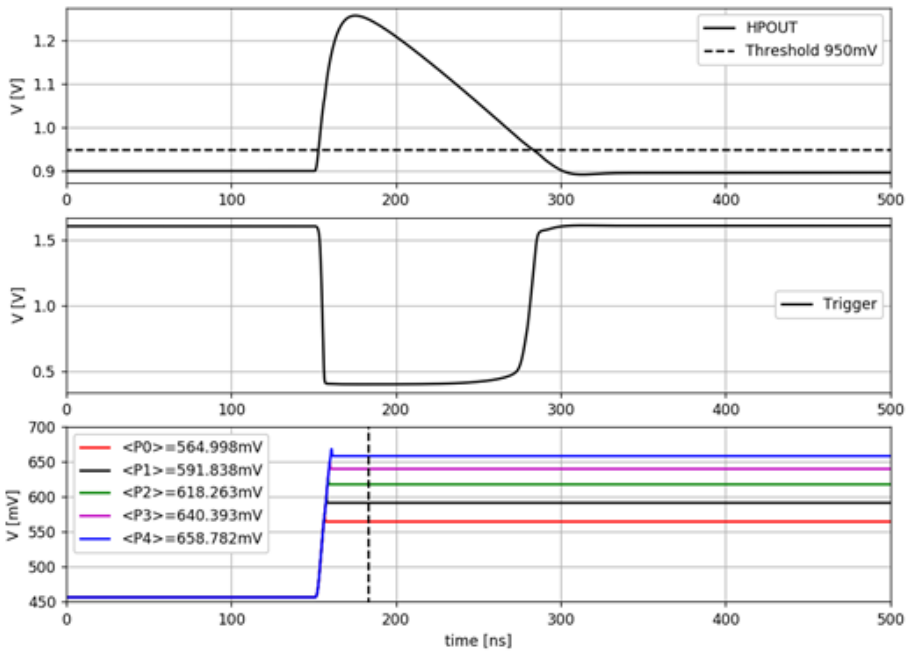
- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - Fast discriminator
  - Buffer needed to drive the capacitors
  - Programmable chain delay to sample 5 points of SF signal
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

Circuit proposal: AS

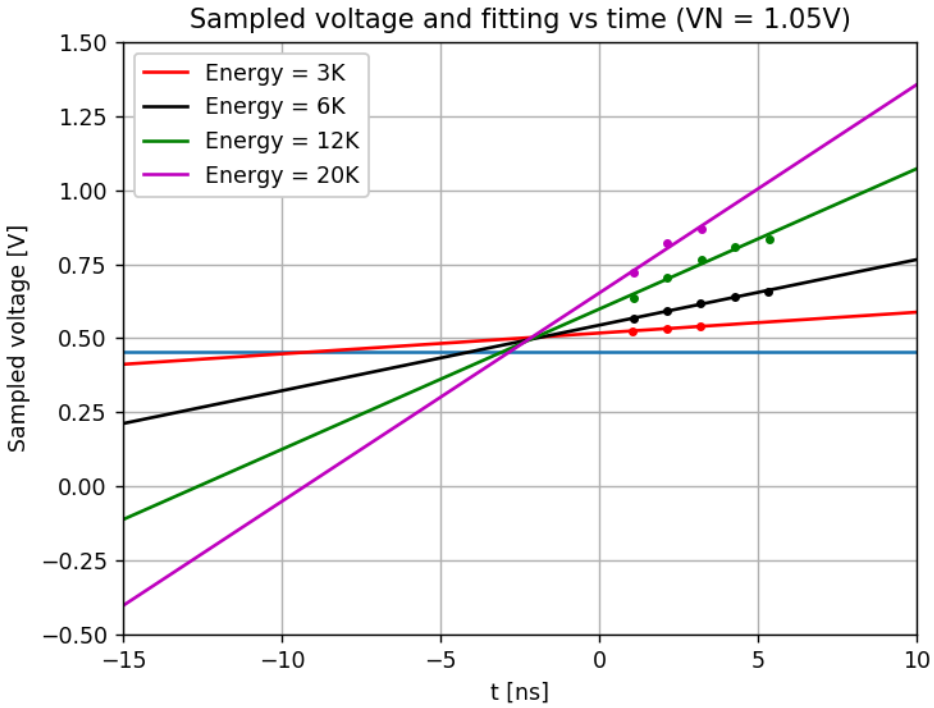


- Pixel receives:
  1. An 8-bit Gray encoded TS running at 40 MHz
  2. The clock at 40 MHz

Circuit proposal: AS

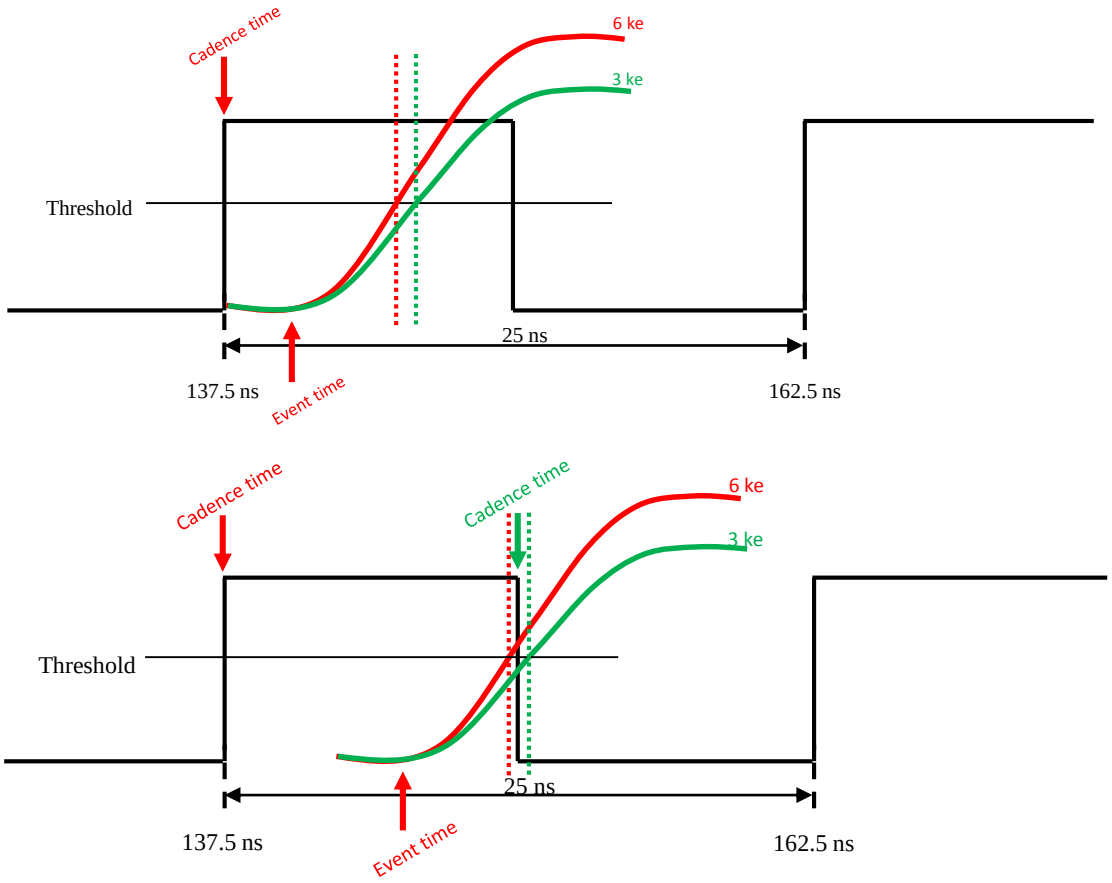


Amplified signal, discriminator output and analog values stored



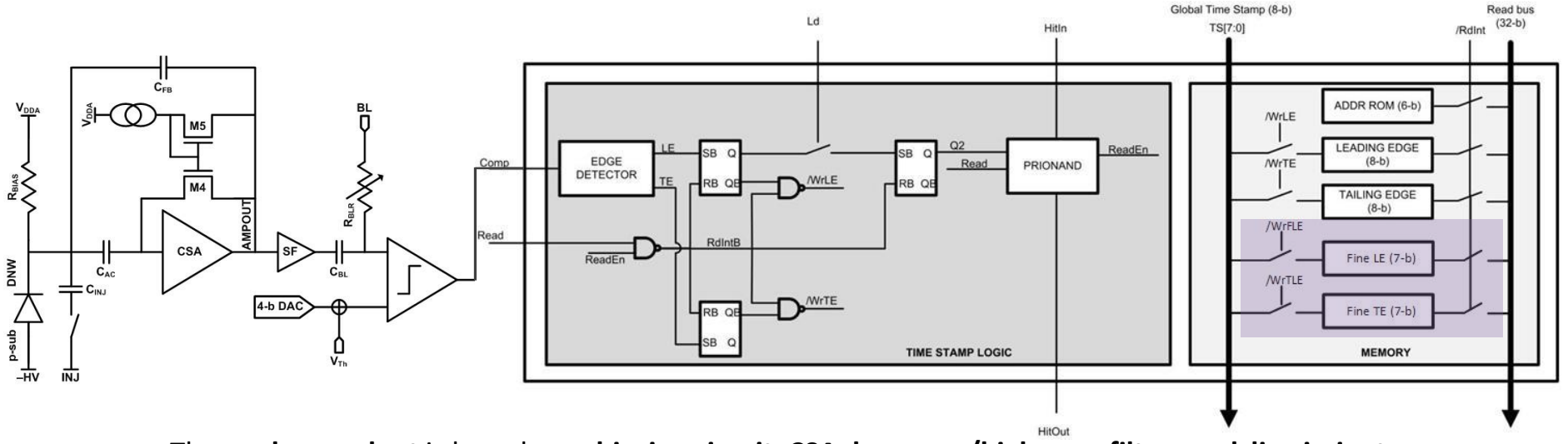
Linear fits done for different energies. Time walk around 5.7 ns (without any correction)

Circuit proposal: AS



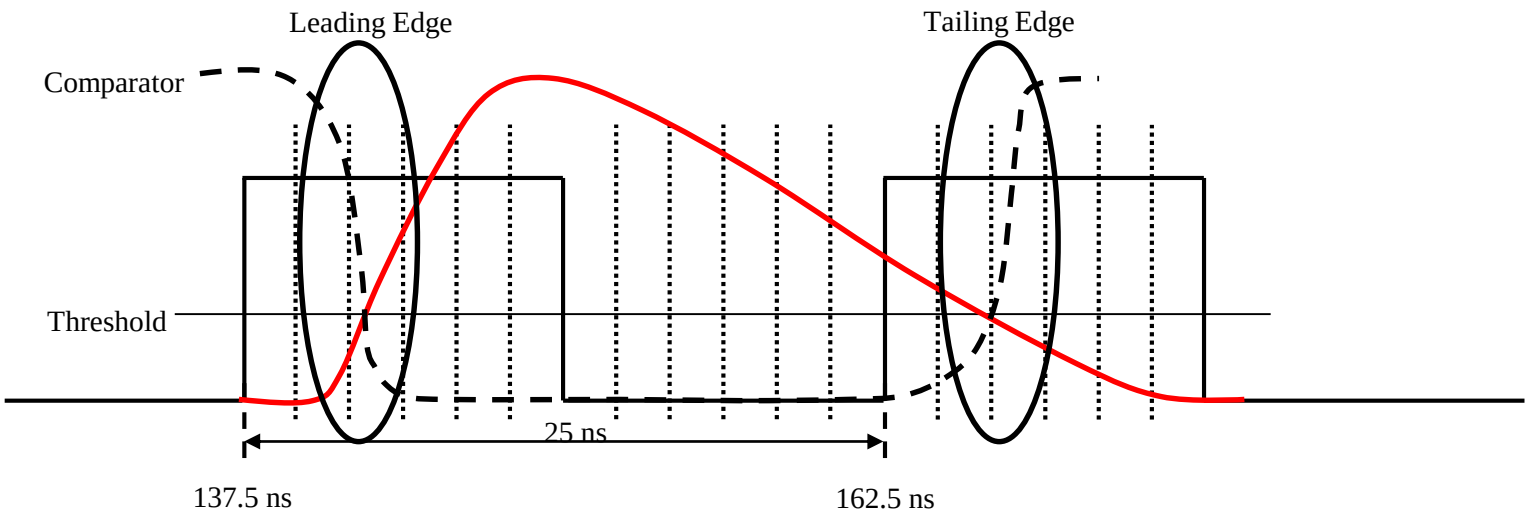
- Clock @ 40 MHz, however we can distinguish if the hit has occurred when the clock was high or low.
- We can position our time “0” at the previous or at the following edge. In any case, the worst case is having a time precision below half the period (12.5 ns)
- When we have two hits happening at the same time, the measured time-stamp still can be different depending on the energy of the particle. As we have the information of the energy (slope) we can correct it off-chip.
- Power consumption of the pixel is 30.5 uW

Circuit proposal: TDC



- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- The **digital readout** is based on the FE-I3:
  - **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
  - ToT = TE – LE (off-chip)
  - **One 8-bit ROM memory** to store the pixel address
  - **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored
- Fine TDC common for all the pixels (6 phases + clock polarity)
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

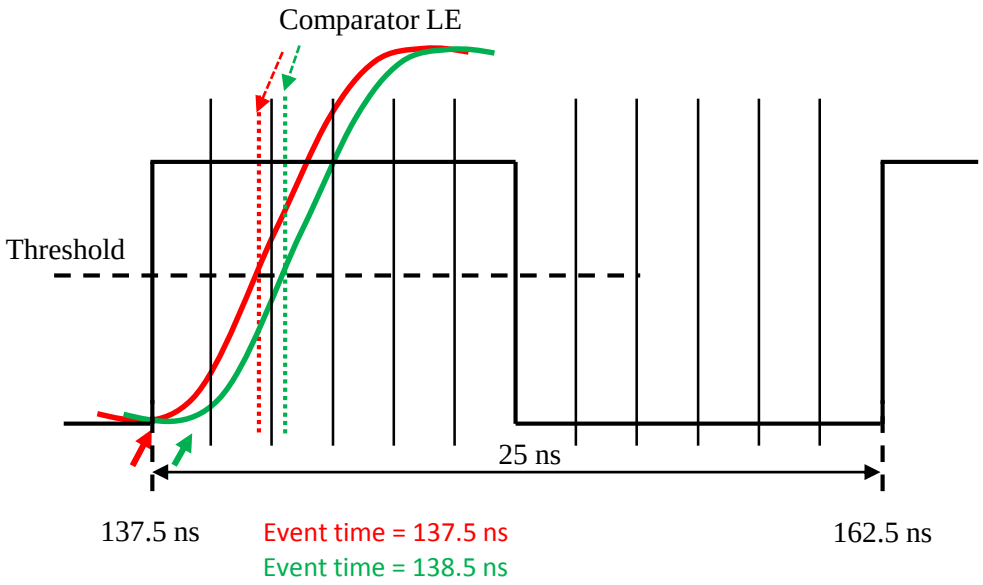
Circuit proposal: TDC

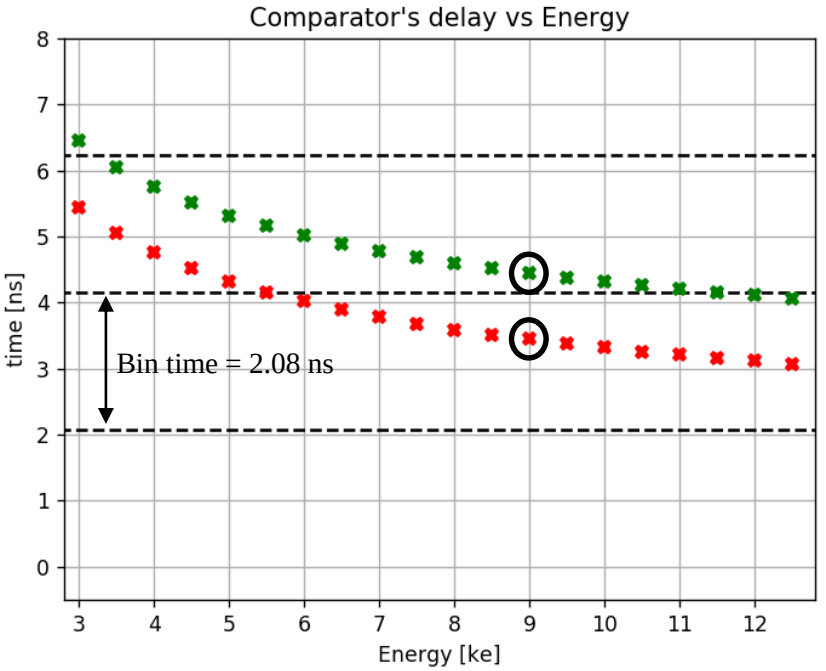


- Clock @ 40 MHz, however we can distinguish if the hit has occurred when the clock was high or low.
- We can position our time "0" at the previous or at the following bin-edge. Programmable windows, in this case, each bin is approx. 2.08 ns
- Power consumption of the pixel is 31.7 uW (Fine TDC is common for all the pixel matrix)
- When we have two hits happening during the same bin (time window), the measured time-stamp still can be different. As we have the information of the energy (ToT) we can correct it off-chip. However, our minimum time precision must be the size of a bin (2.08 ns)

Circuit proposal: TDC

Simulation for 9 Ke$^-$

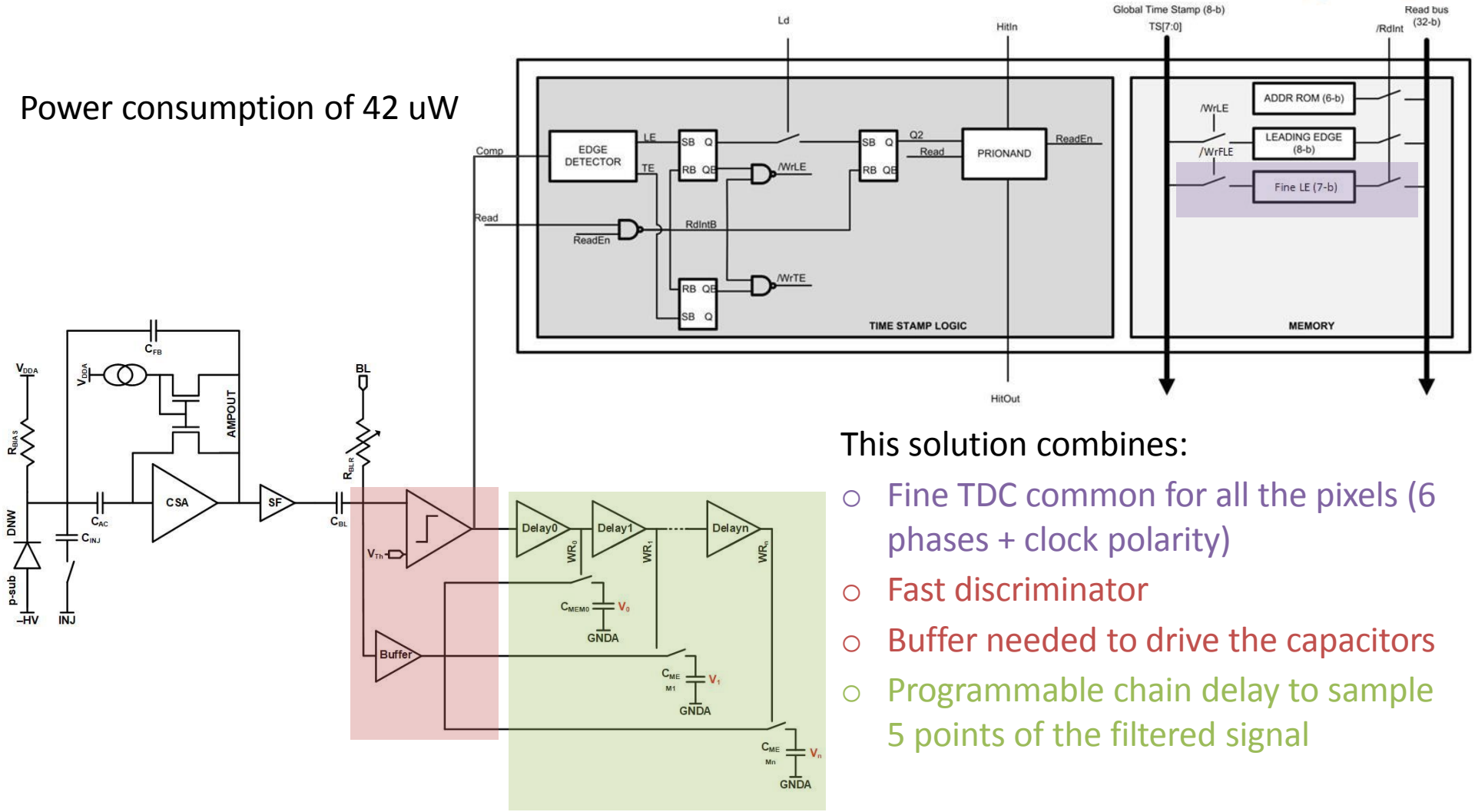




- When we have two hits happening during the same bin (time window), the measured time-stamp still can be different. As we have the information of the energy (ToT) we can correct it off-chip. However, the minimum time precision is 2.08 ns (the size of a bin)

Circuit proposal: TDC + AS

Power consumption of 42 uW



This solution combines:

- Fine TDC common for all the pixels (6 phases + clock polarity)
- Fast discriminator
- Buffer needed to drive the capacitors
- Programmable chain delay to sample 5 points of the filtered signal

Circuit proposal: Simulated results

Event time [ns]	Time resolution TDC [ns] @ 3K	Time resolution TDC + AS [ns] @ 3K	Time resolution TDC [ns] @ 6K	Time resolution TDC + AS [ns] @ 6K	Time resolution TDC [ns] @ 12K	Time resolution TDC + AS [ns] @ 12K
137.5	2.08	0.91	2.08	0.67	0	0.83
138.5	0.99	1.99	1	0.41	1	0.17
139.5	1.99	0.99	2	0.6	0.09	0.91
140.5	2.99	0.01	0.92	0.49	0.91	0.09
141.5	1.92	1.07	1.92	0.51	0.16	0.99
142.5	2.92	0.07	0.84	0.57	0.84	0.01
143.5	1.84	1.15	1.84	0.43	0.24	1.07
144.5	2.84	0.15	0.76	0.65	0.76	0.07
145.2	1.46	1.53	1.46	0.05	0.62	1.45
145.5	1.76	1.23	1.76	0.35	0.32	1.15
146.5	2.76	0.23	0.68	0.73	0.68	0.15

Time window = 2.08 ns TDC time resolution above 2.08 ns TDC+AS time resolution below 2.08 ns

Conclusions

- Compared with the state-of-the-art the proposed solutions can lower the time walk and increase time resolution:
  - Design simple
  - More power consumption
- Other solutions, with higher pixel areas and higher power consumption claim to arrive to 100 ps. In our case we are working with pixels from 50x50 um^2 to 80x80 um^2
- With a 80 MHz clock AS can easily increase the time resolution reported in the literature => how much can we speed up the clock ?
- Submission scheduled to January 2019