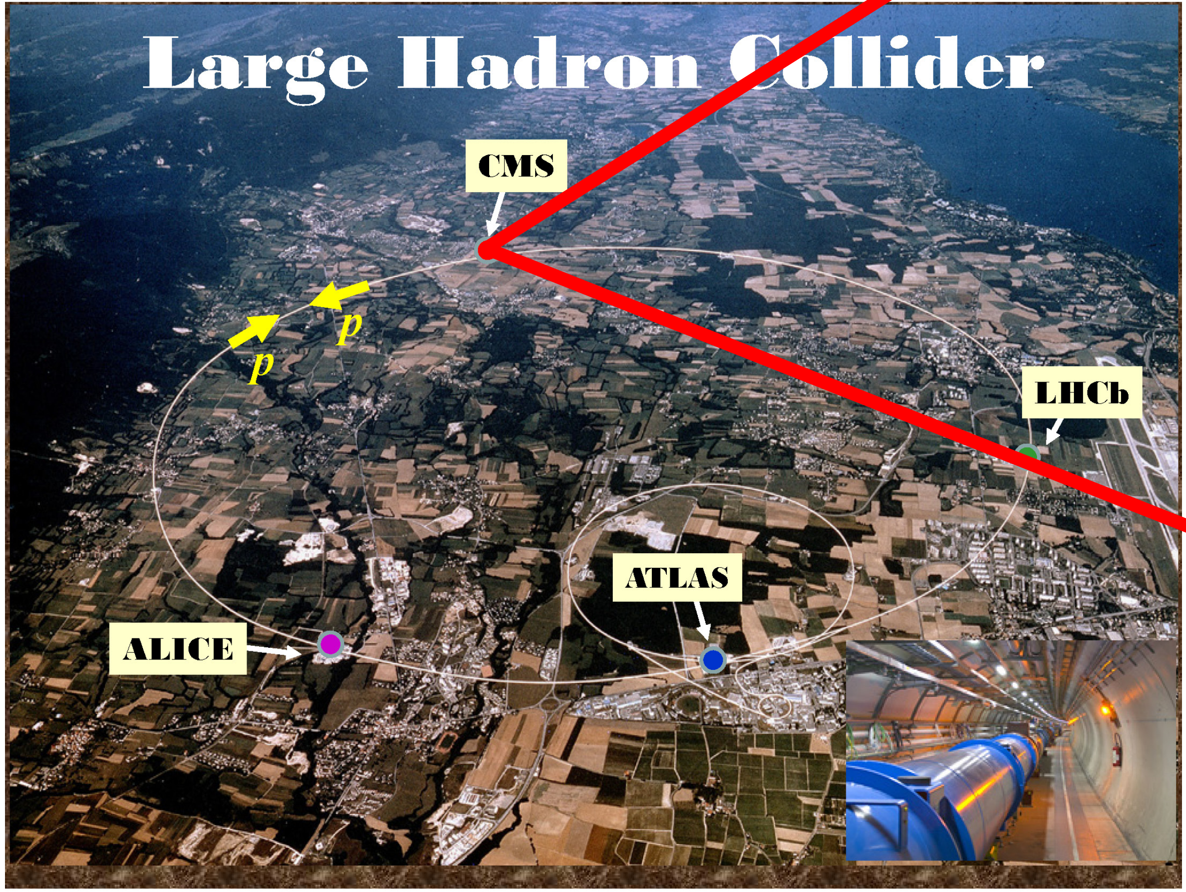
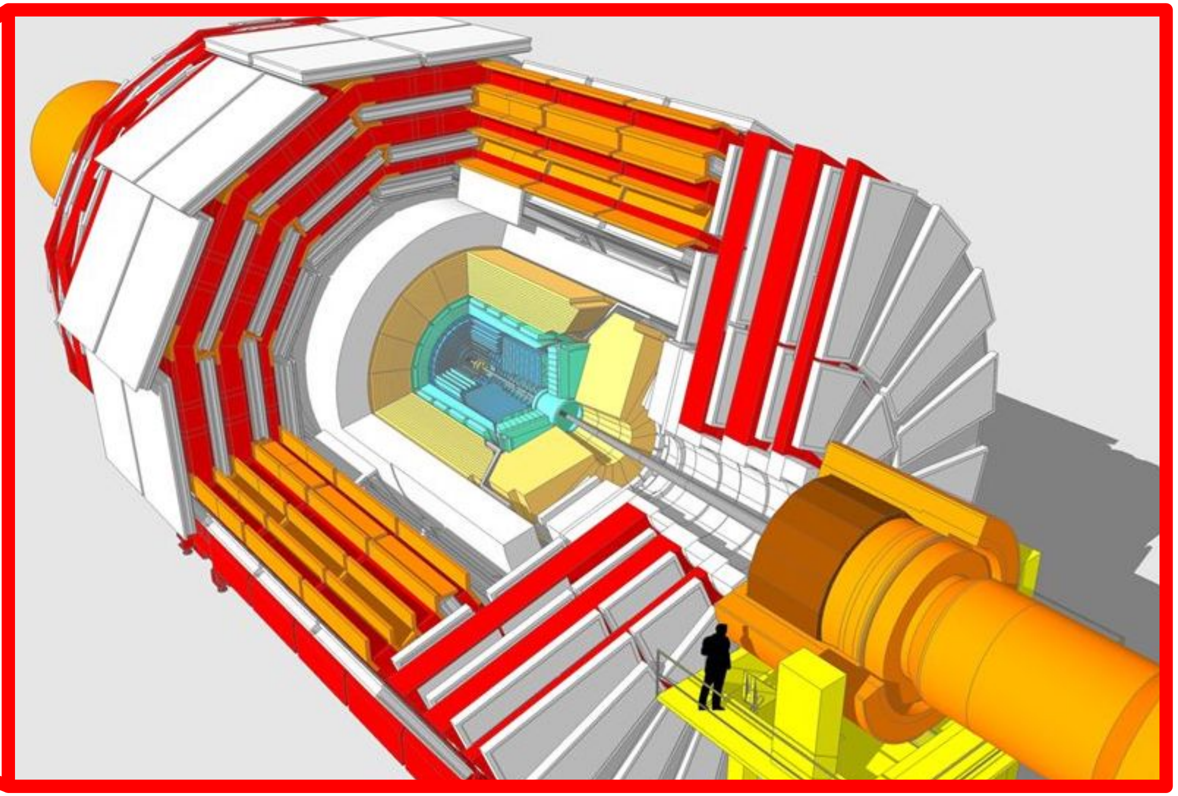
The CMS Tracker: Run 2 Experience and Upgrades

BY MATTHEW KILPATRICK
RICE UNIVERSITY
ON BEHALF OF THE CMS COLLABORATION

Compact Muon Solenoid (CMS)

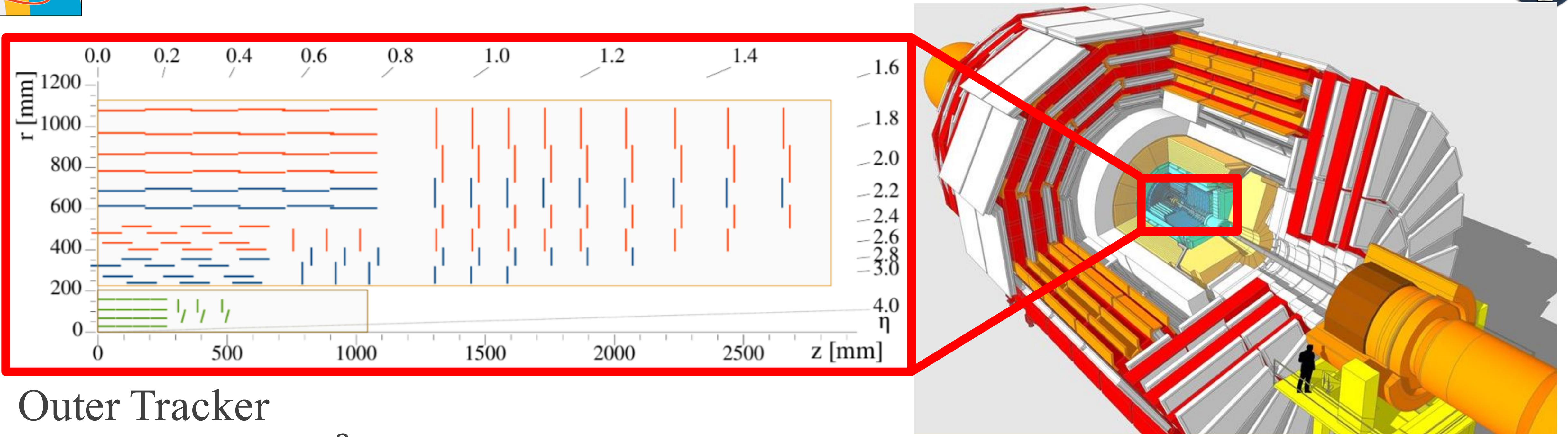




LHC

- $\sqrt{s}$ =13 TeV p-p collisions
- Luminosity: $2{\times}10^{34}\,\text{cm}^{-2}\text{s}^{-1}$

The Tracker



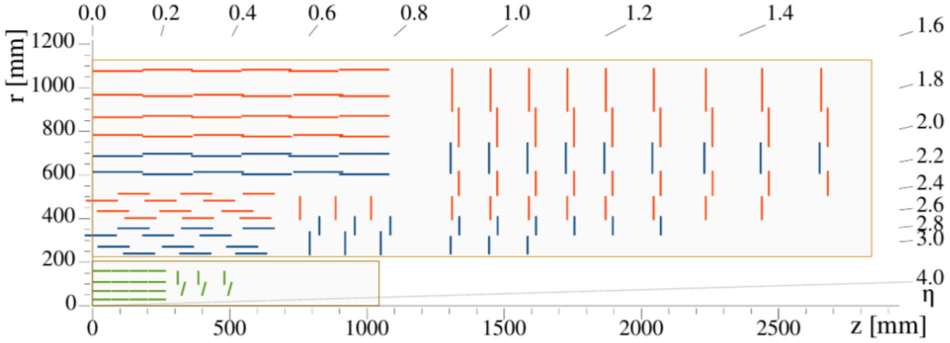
Outer Tracker

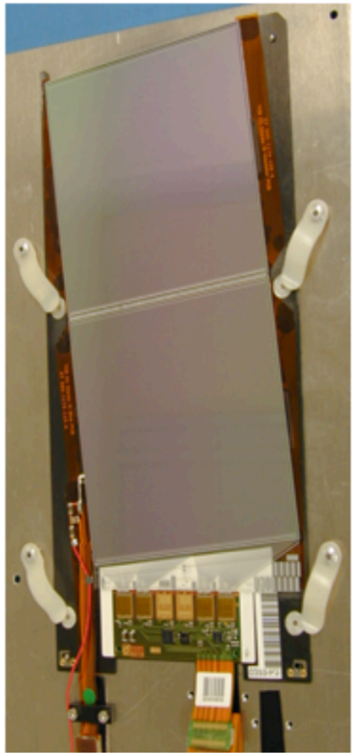
- Active area: 200 m^2,15148 modules
- 10 layers in barrel region
- 9 + 3 disks in inner disks and endcaps
- Orange: single sided module
- Blue: double sided module
- Analog readout

Modules

Types

- 320 μm thick sensors in the inner layers
- 500 μm thick sensors for the outer layers
  - Increase thickness to increase S/N
- Pitch of $80 - 120\ \mu m$
- ~10 cm length
- Single sided modules
  - Reverse p-n silicon sensor
- Double sided stereo modules
  - Two silicon sensors mounted back to back
  - Strips aligned at 100 mrad relative angle
  - Better 3D tracking
- Spans radii from 25 cm to 110 cm and $\pm$ 280 cm along the beamline





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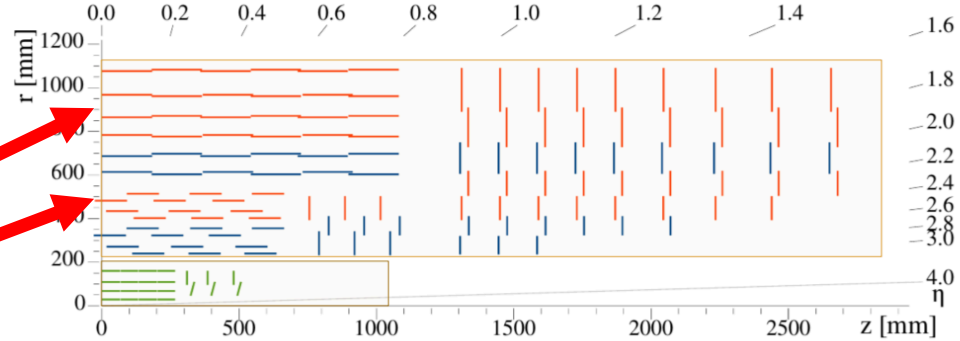

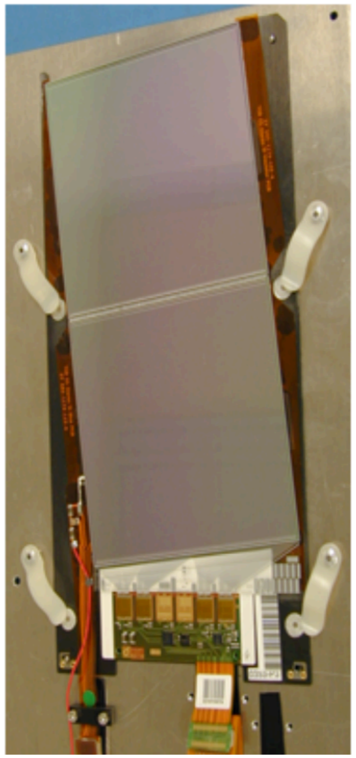

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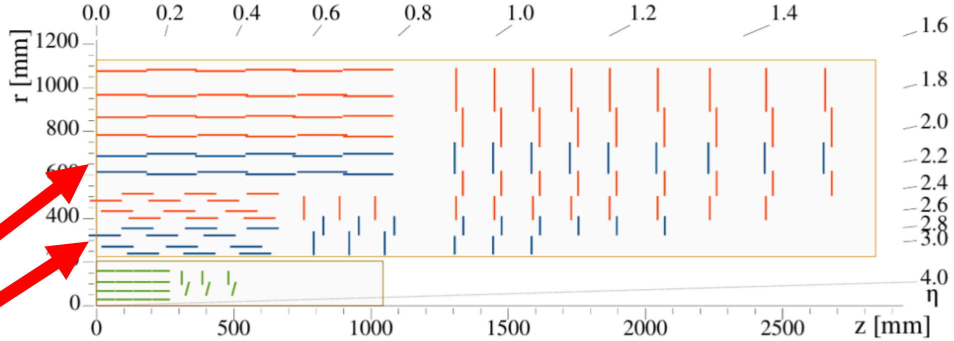
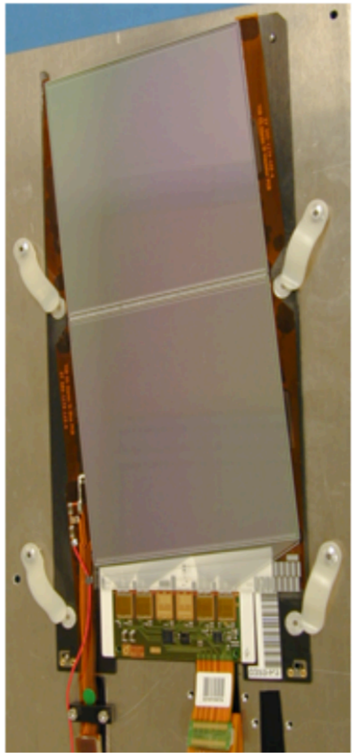
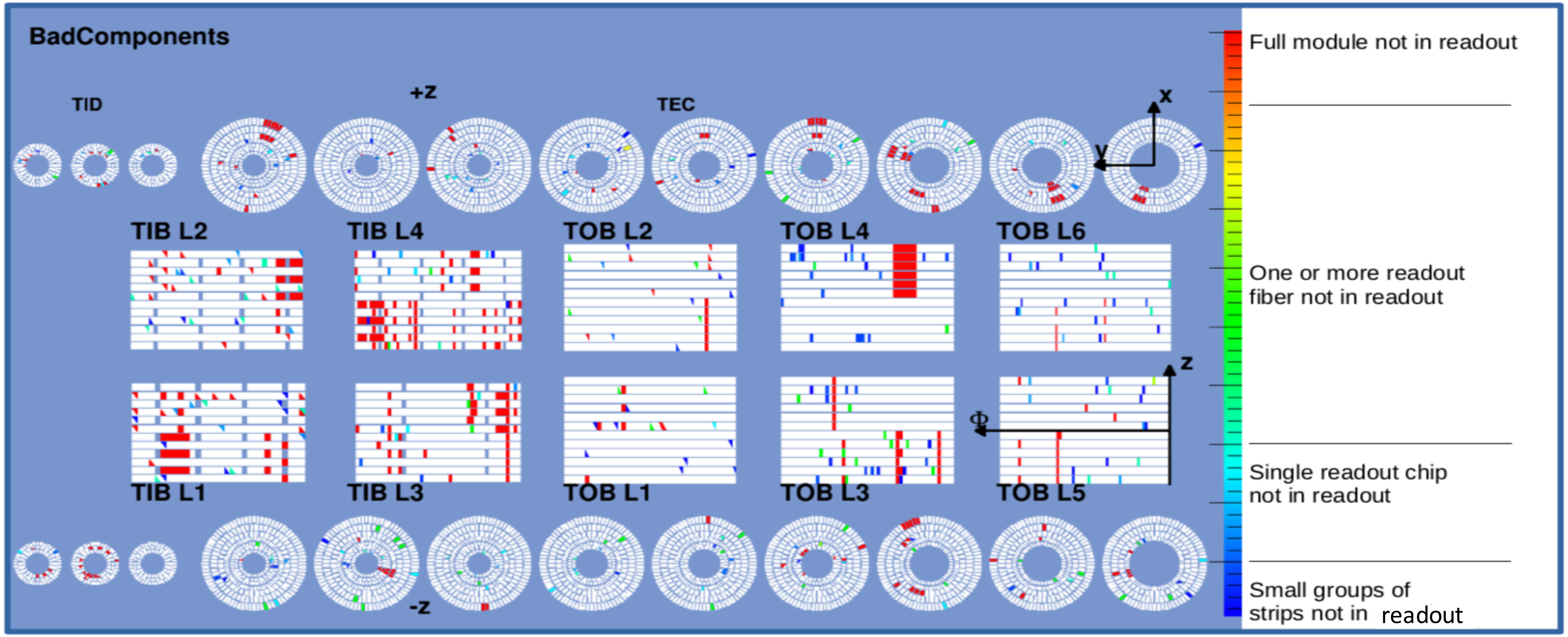




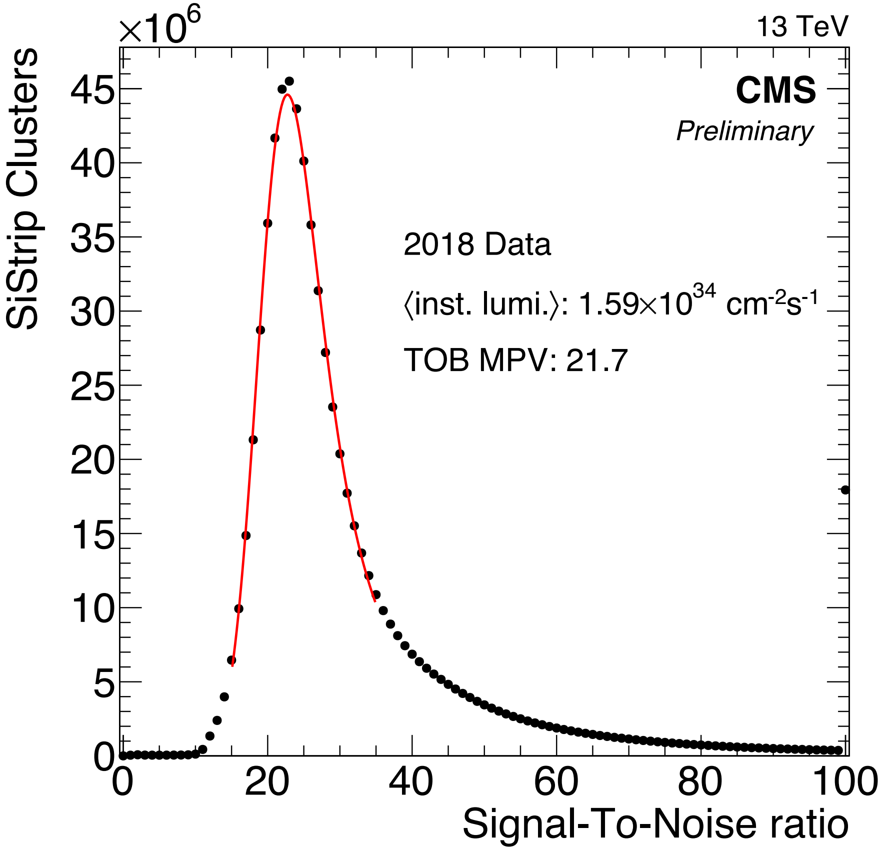
Outer Tracker Active Channels

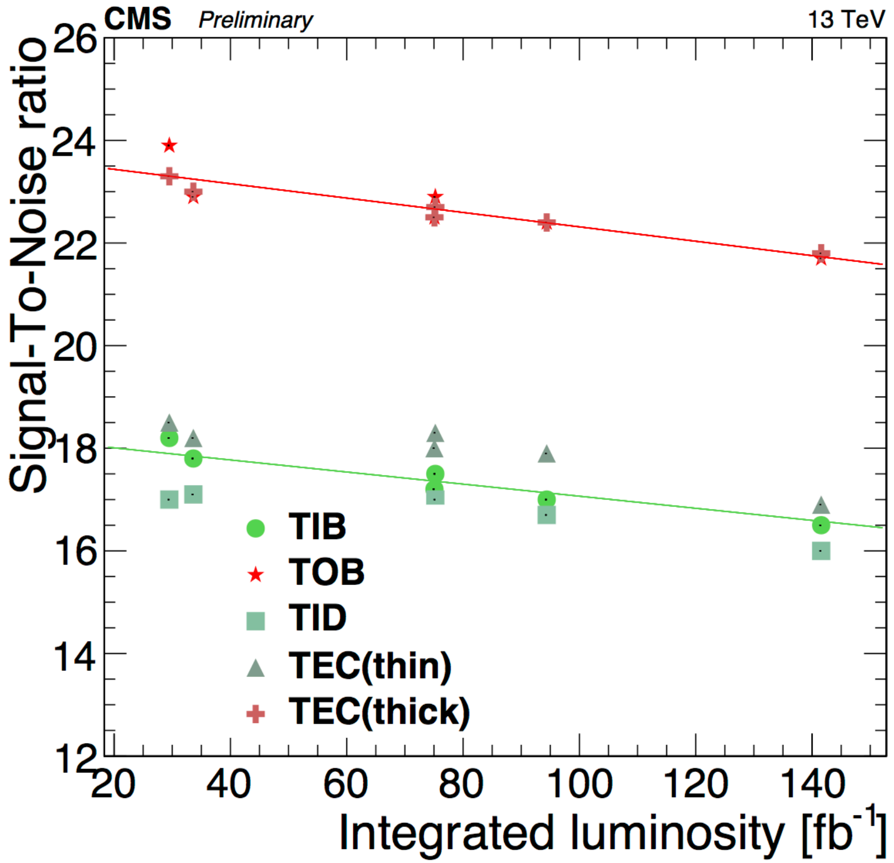
TOB: Tracker Outer Barrel
TIB: Tracker Inner Barrel
TEC: Tracker End Cap
TID: Tracker Inner Disk



- 10 years of operation!
  - ~96.5% active
- Module not readout (red) occurred early in detector lifetime
  - Various causes: powering issues, Bad LV, or configuration problem
  - Occurred during installation
- Strip Tracker has been stable for quite some time

Signal-to-Noise

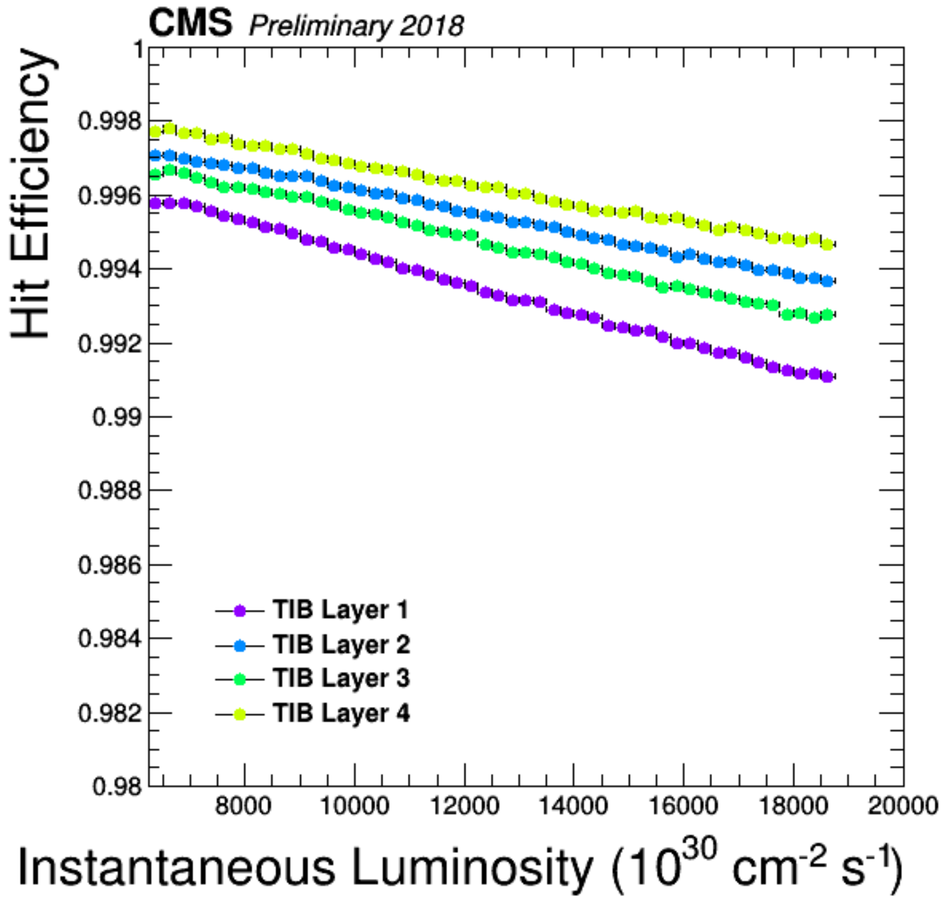


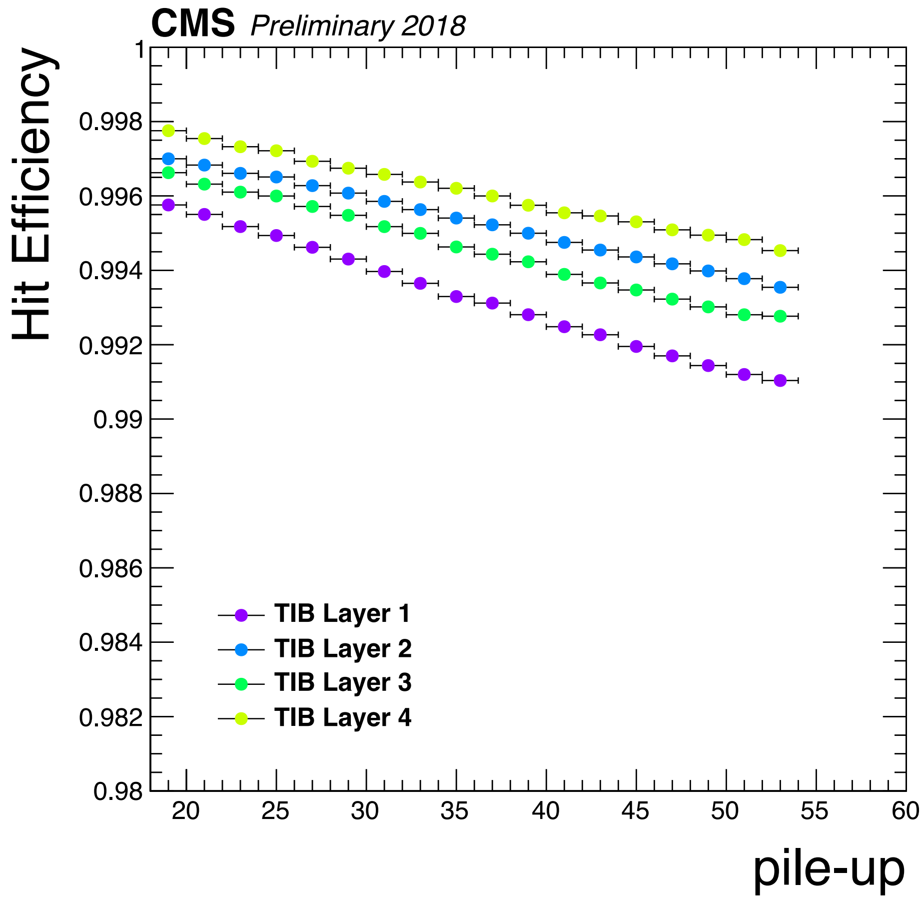


- Large signal-to-noise ratio
- Steady decrease with increased luminosity
  - Expected to decrease with increased fluence

TOB: Tracker Outer Barrel
TIB: Tracker Inner Barrel
TEC: Tracker End Cap
TID: Tracker Inner Disk
Thin: Single
Thick: Double

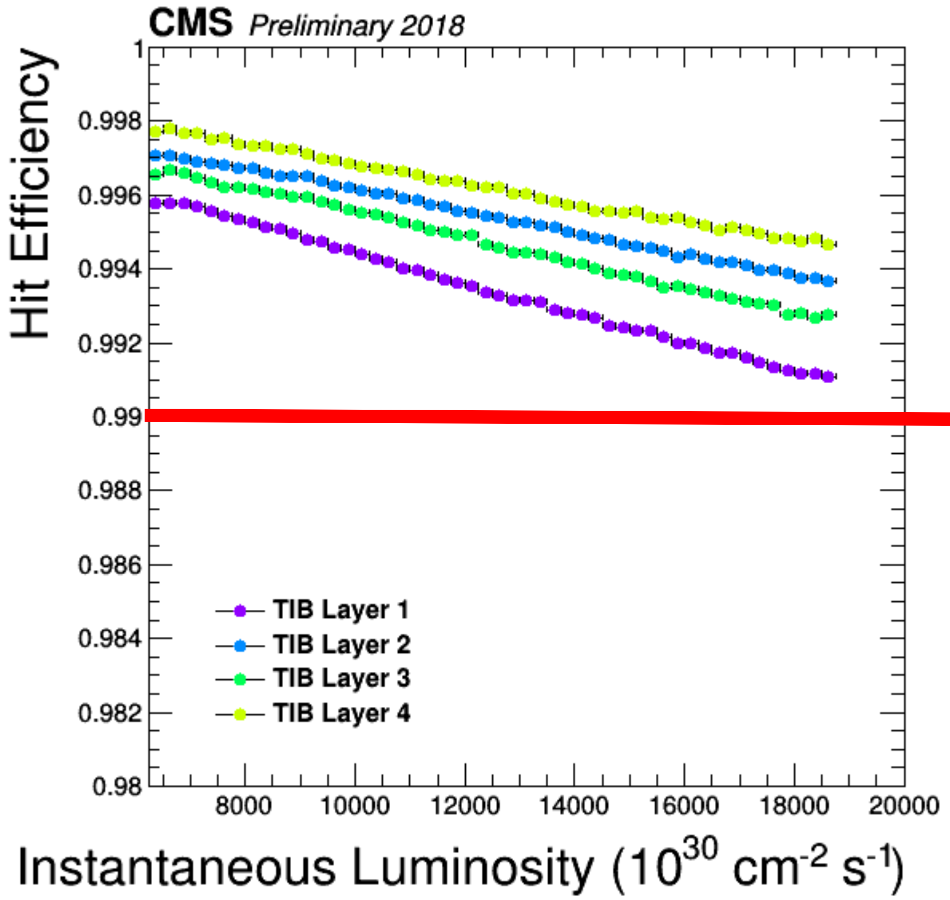
Hit Efficiency

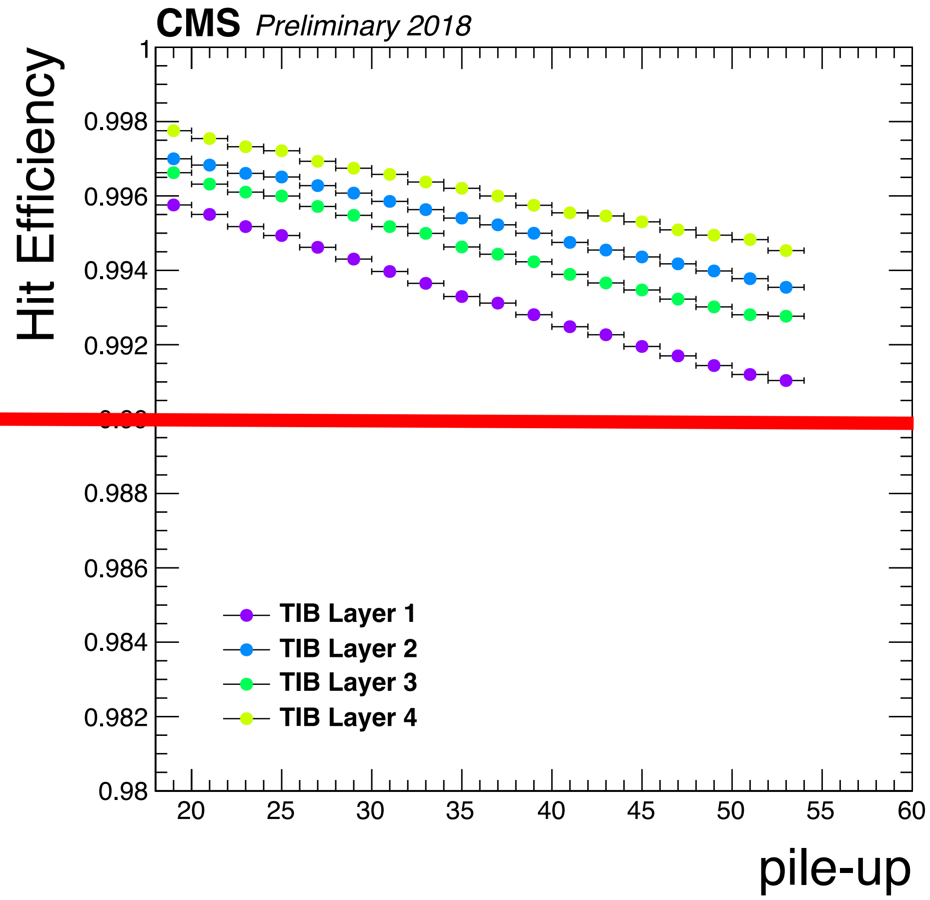




- ~99% efficiency for all layers
- Scales linearly with instantaneous luminosity and pile-up
  - Pile-Up: Number of primary vertices in an event

Hit Efficiency





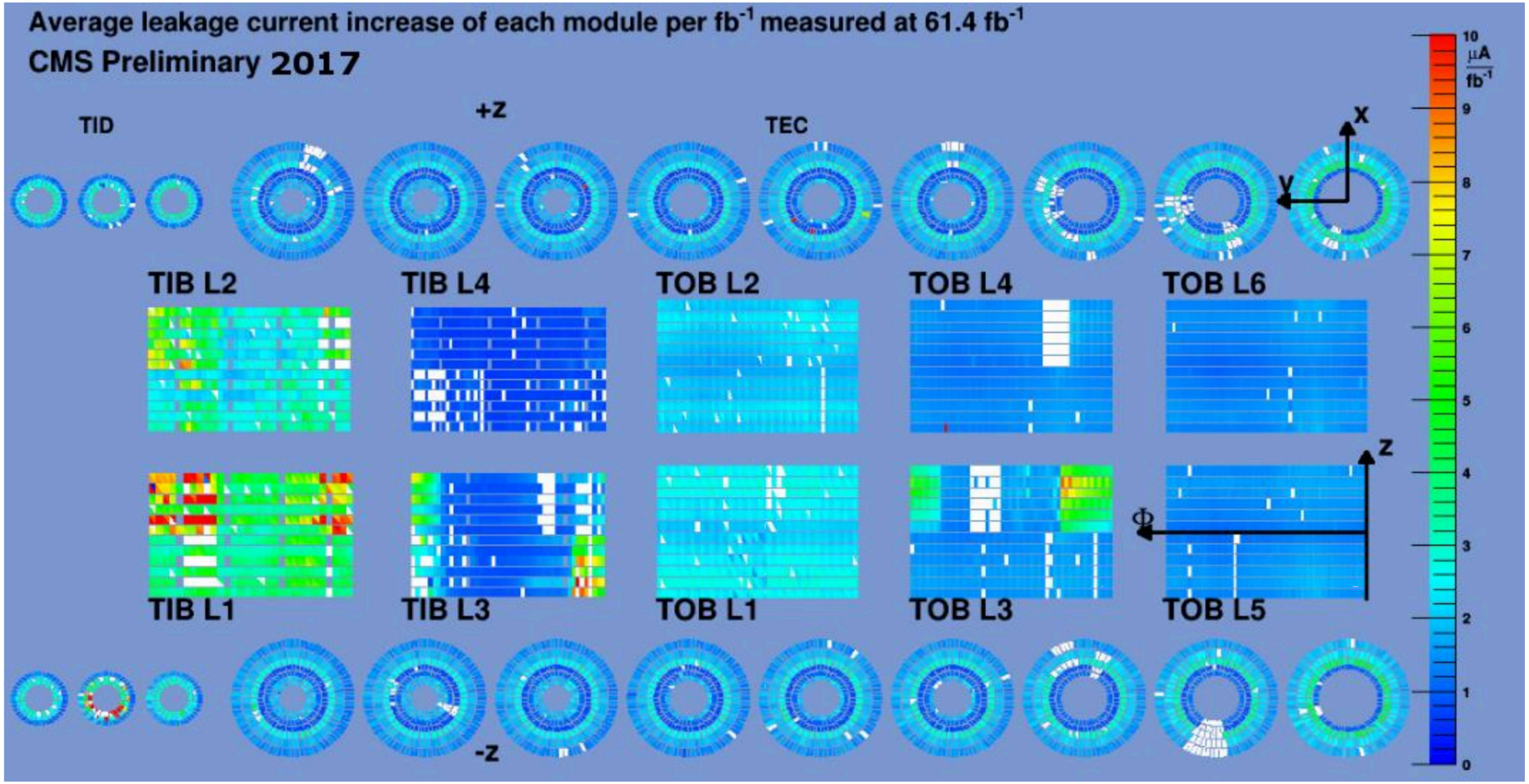
- ~99% efficiency for all layers
- Scales linearly with instantaneous luminosity and pile-up
  - Pile-Up: Number of primary vertices in an event

Leakage Current Increase

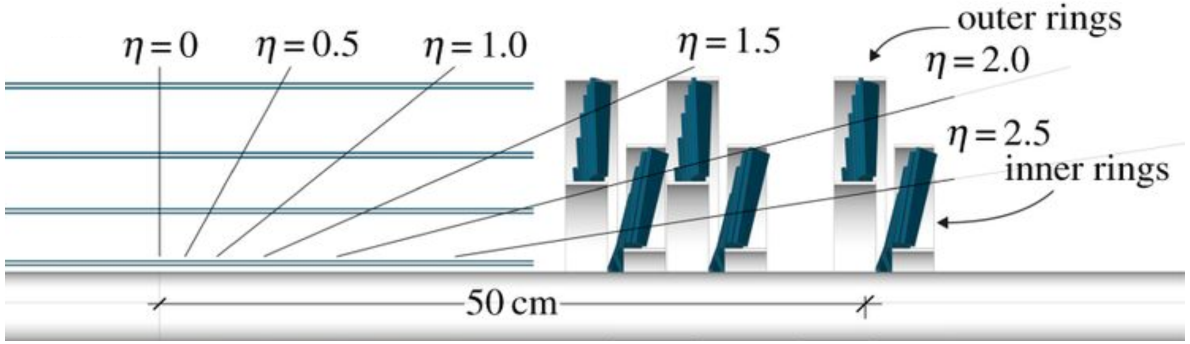
- Leakage current increase normalized by luminosity

Features:

- Green regions are closed cooling loops
- Not scaled to temperature
- Degraded cooling contacts
- Different thickness of detector

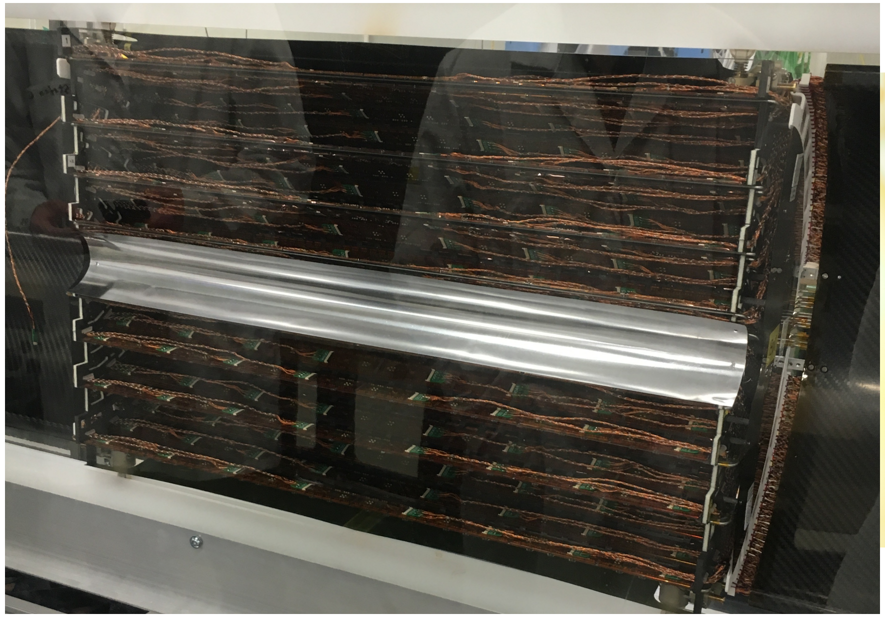


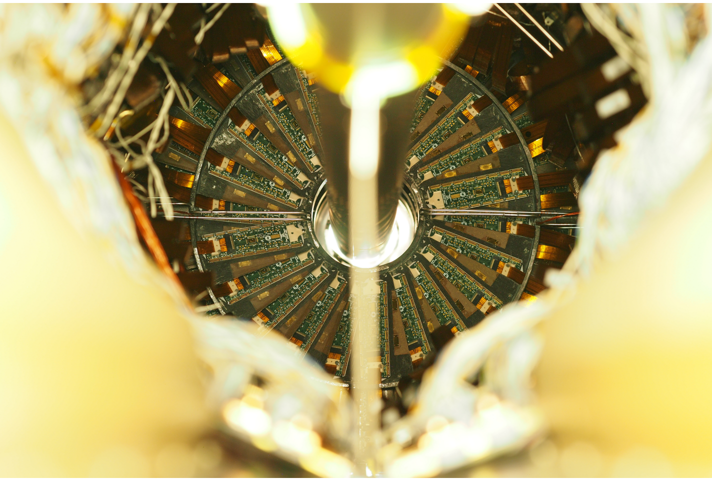
Phase 1 Pixels



Replaced in winter 2016/2017

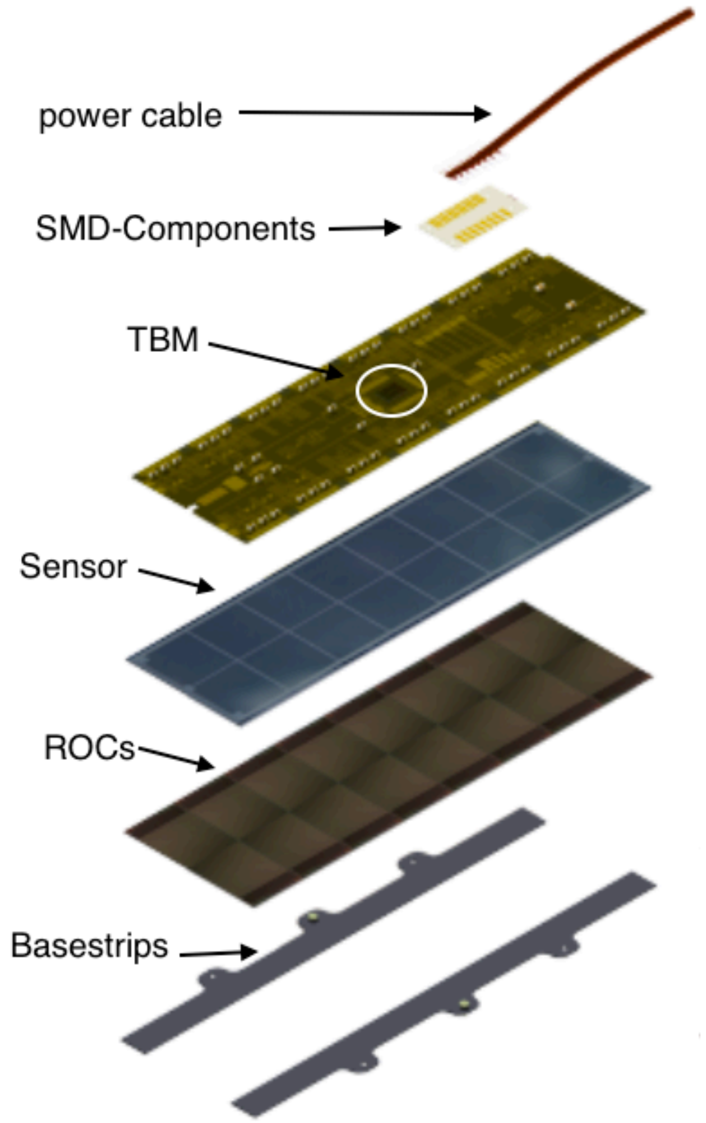
- 4 barrel layers
- 3 endcap disks on each side
- 124 million pixel channels
- Approximately 1 m long
- Designed for peak luminosity of 2.5×10^{34} $cm^{-2}s^{-1}$ with 50 ns bunch crossings
- Analog → digital
  - New data acquisition (DAQ)
- DCDC powering
- CO_2 cooling
  - Light weight
  - Cost effective
- Layer 1 closer to beam line
  - 43 mm to 30 mm
- Layer 4 extends to 160 mm



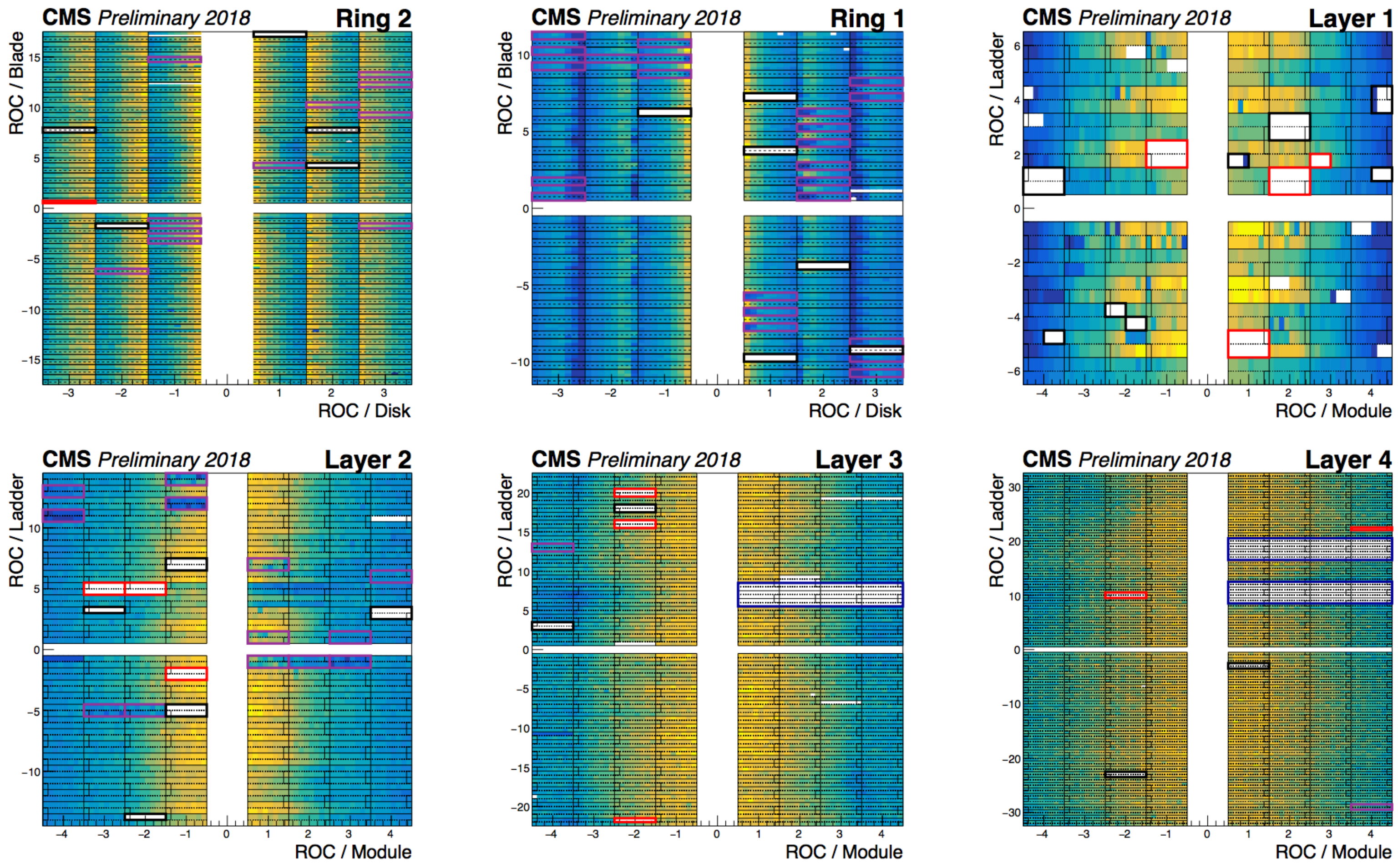


Phase 1 Modules

- 285 μm thick n-doped silicon sensors
- 100×150 μm^2 pixel area
- 2×8 Readout chips (ROCs)
  - Fast digital readout
  - 160 Mbps
- Token Bit Manager (TBM)
  - Controls event readout and various resets
  - Combines signals from both ROCs
    - 160 Mbps → 320 Mbps

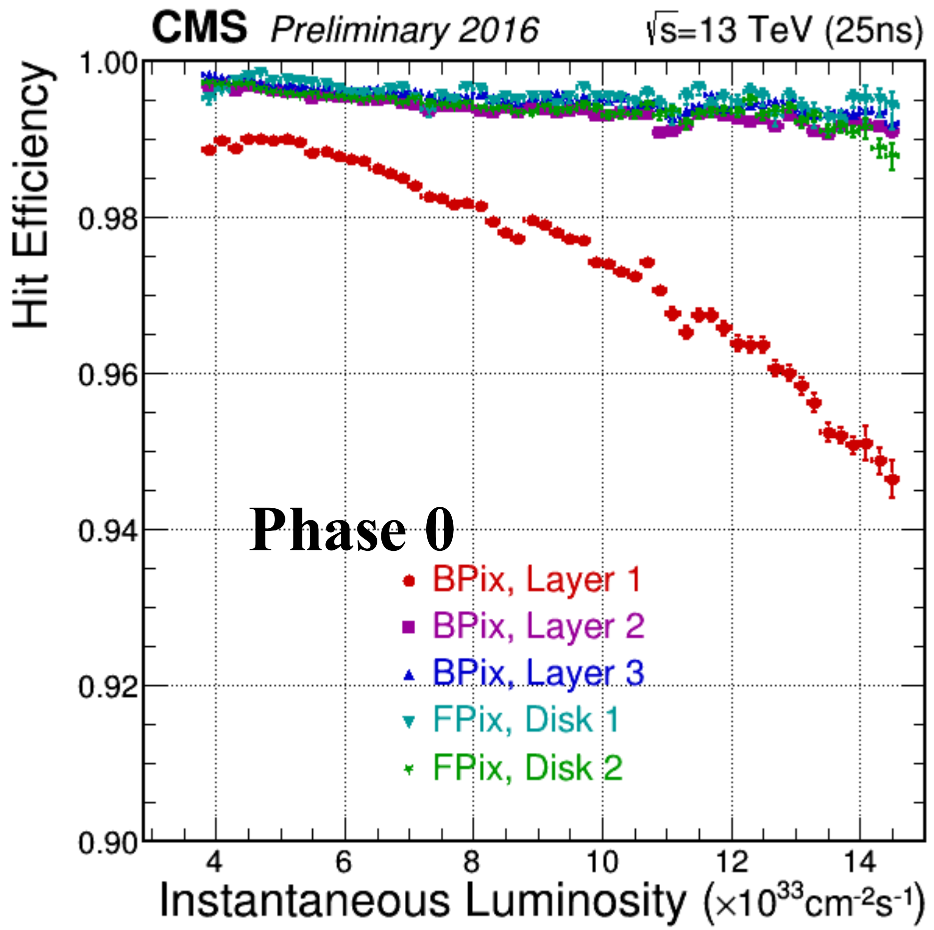


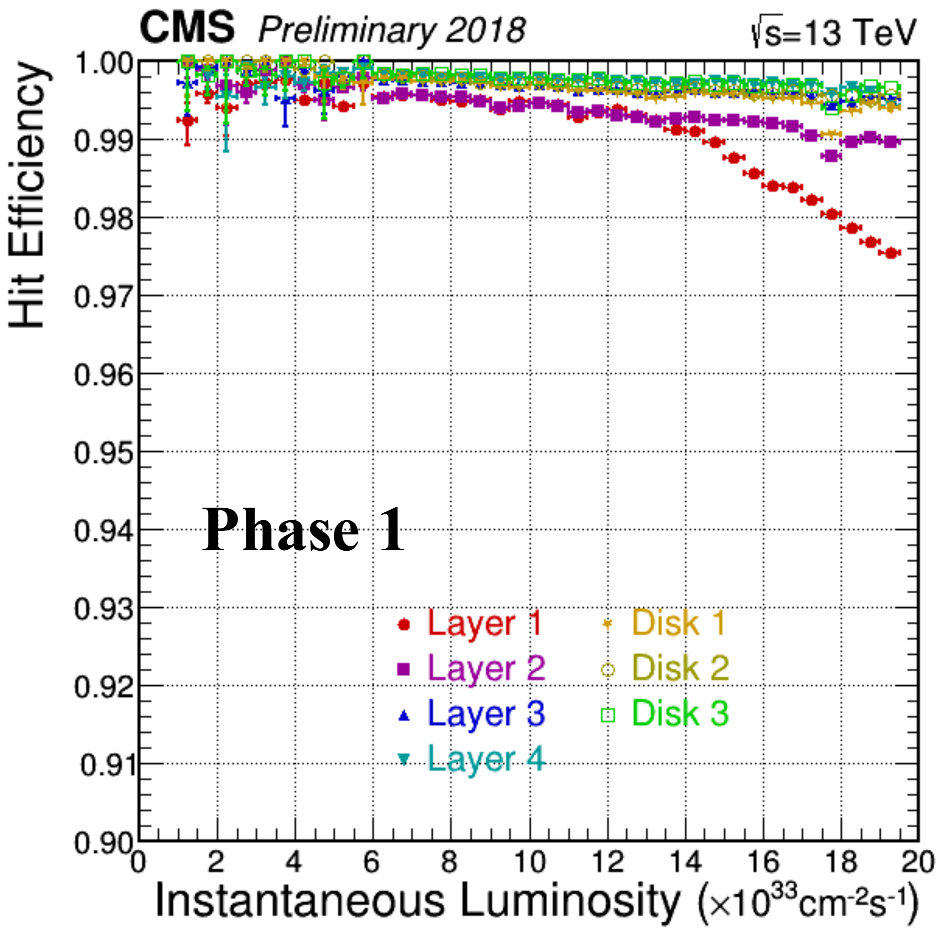
Active Channels in Phase 1



- Currently 94.3% active
  - Barrel/Forward pixel: 93.5/96.7 %
- Features
  - Modules excluded during 2017 (black)
  - New bad components 2018 (red)
  - ROCs connected to bad DCDC converters (violet)
    - Higher level of noise
  - Sectors have HV switched off (blue)
    - Lost connections in the supply tube

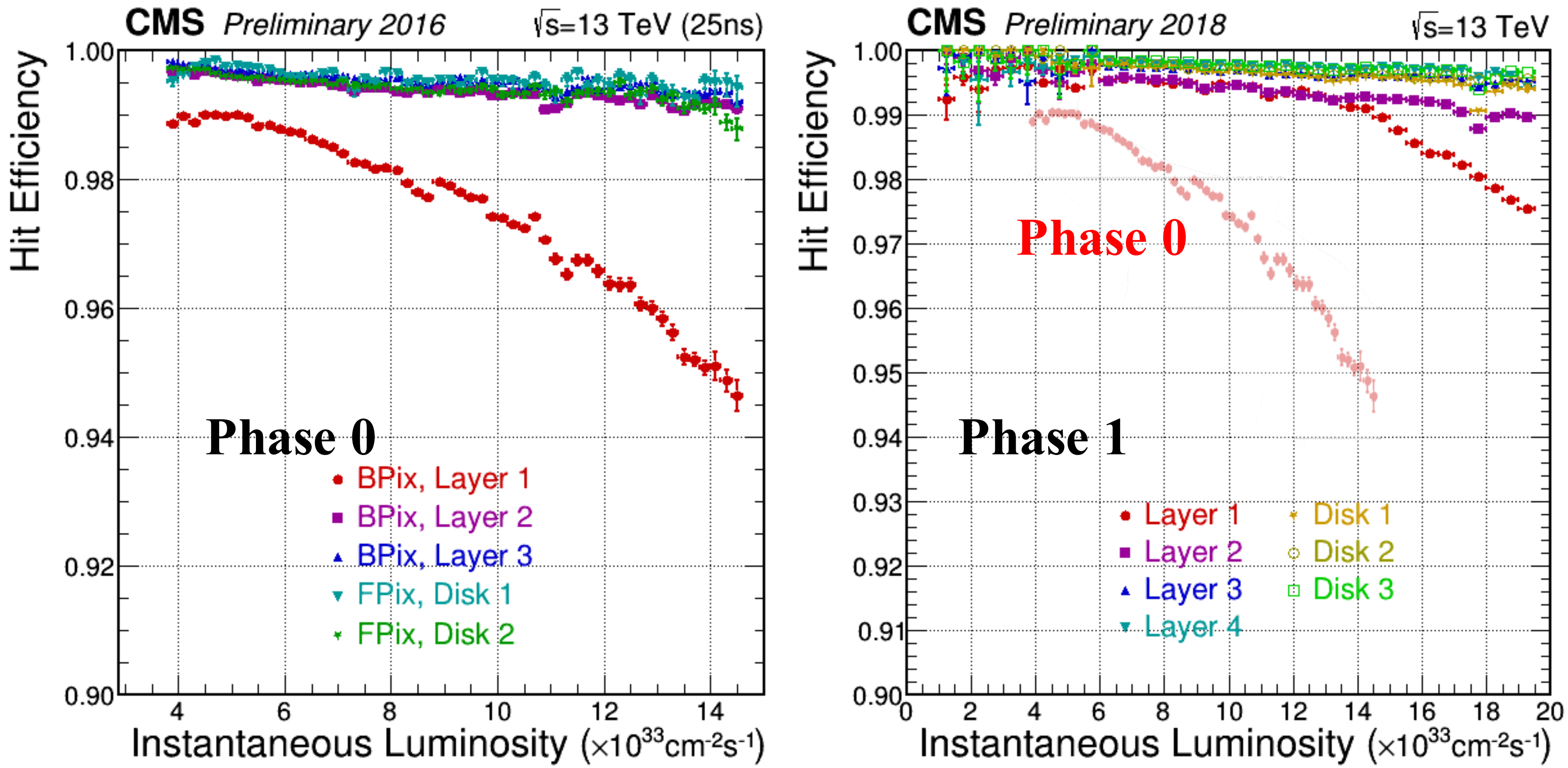
Performance





- Layer 1 has higher efficiency over large range in luminosity

Performance

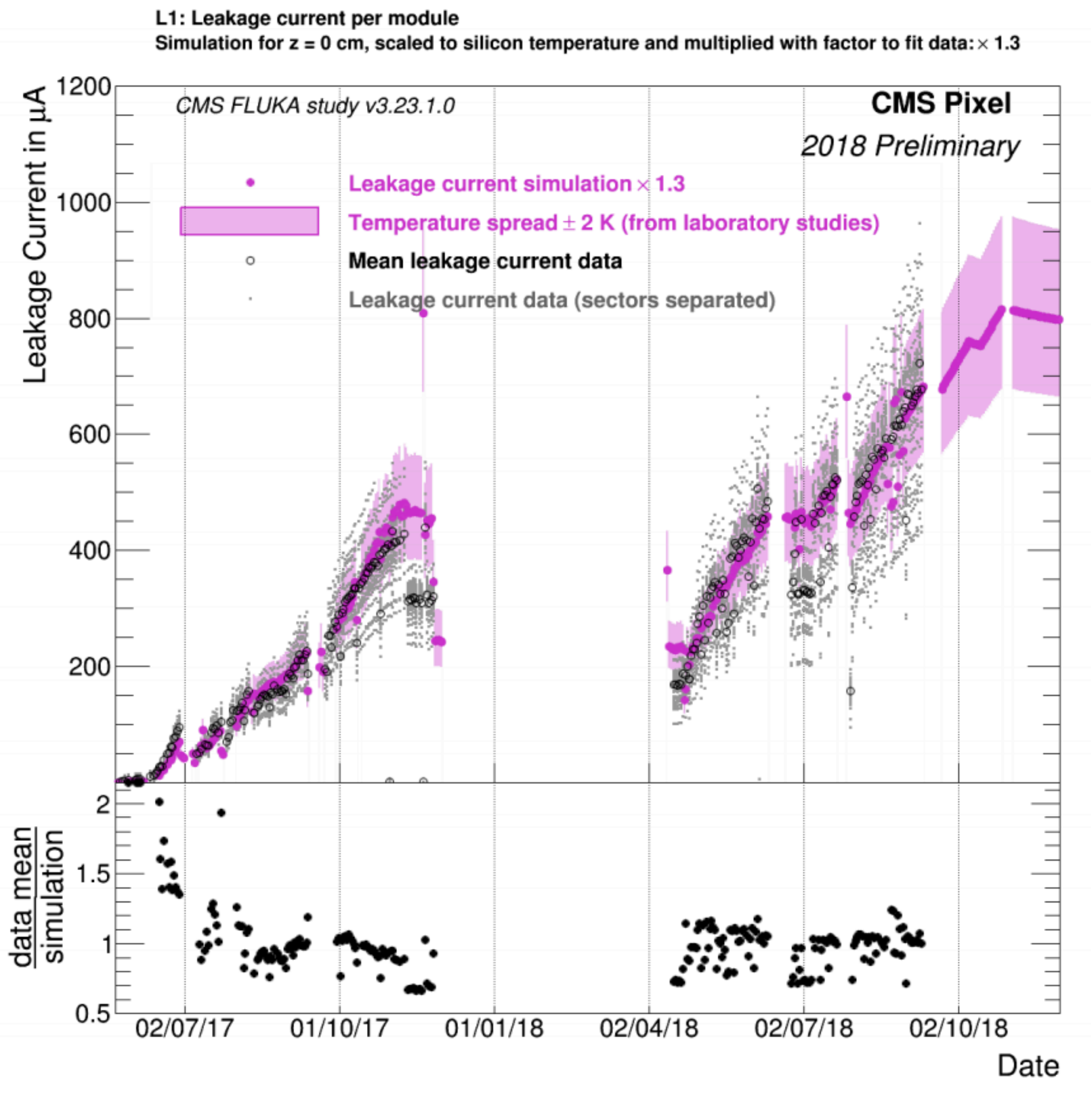


- Layer 1 has higher efficiency over large range in luminosity

Leakage Current

Leakage current simulation

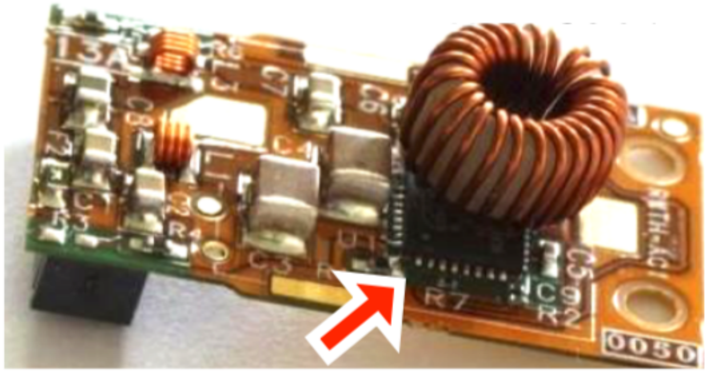
- Compared to data from the detector
- Tracker detector is susceptible to radiation damage
- Monitor damage
- Accurately predict the damage as a function of time
- Annealing causes drop in depletion voltage



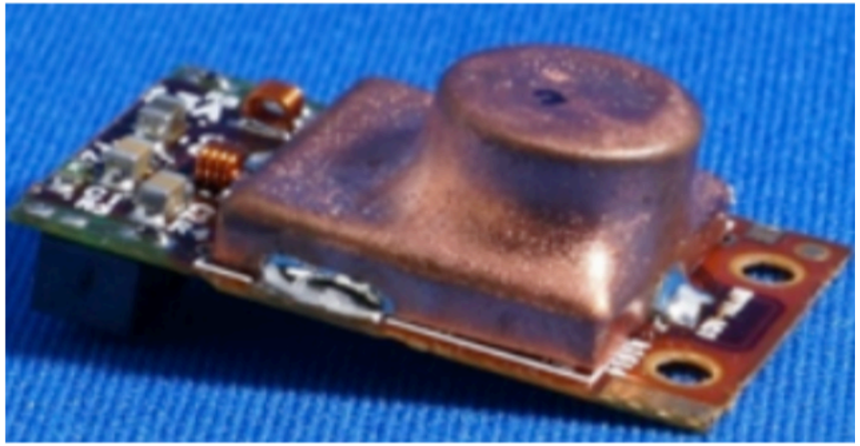
DCDC Converter Issue

Component Failures

- During last two months of operation in 2017
- 65 out of 1184 converters failing
- Able to narrow down cause to a flaw in chip design
- Failure Mechanisms
  - Active state, irradiated, disabled mode
  - Increases leakage current
- **Solution!**
  - Fix being tested, to be integrated for pixels in LS2
- At same point in 2018
  - Same irradiation and voltage, but no failures

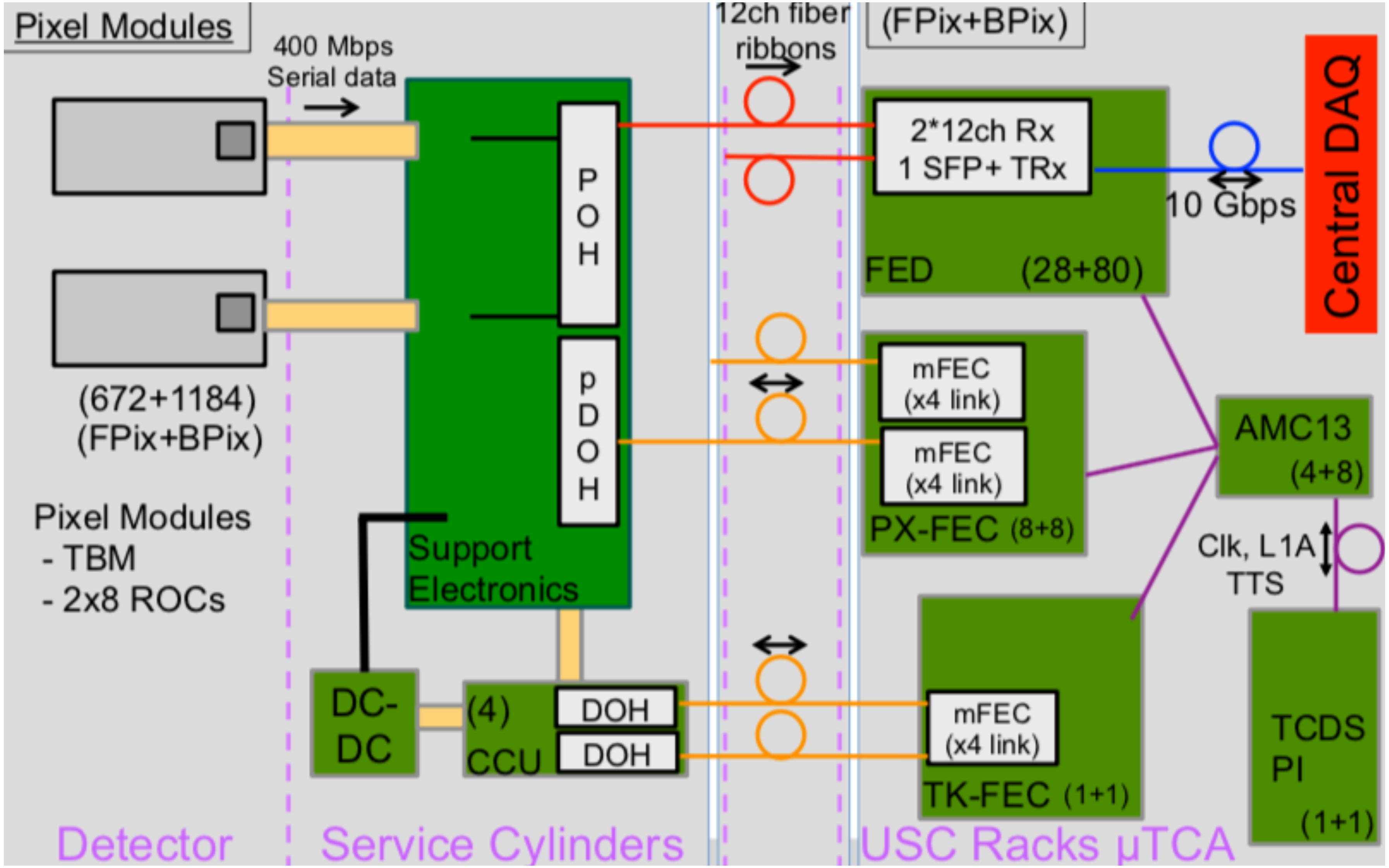


FEAST2 chip used by many detectors at LHC



DCDC Converter

Upgraded Data Acquisition (DAQ)



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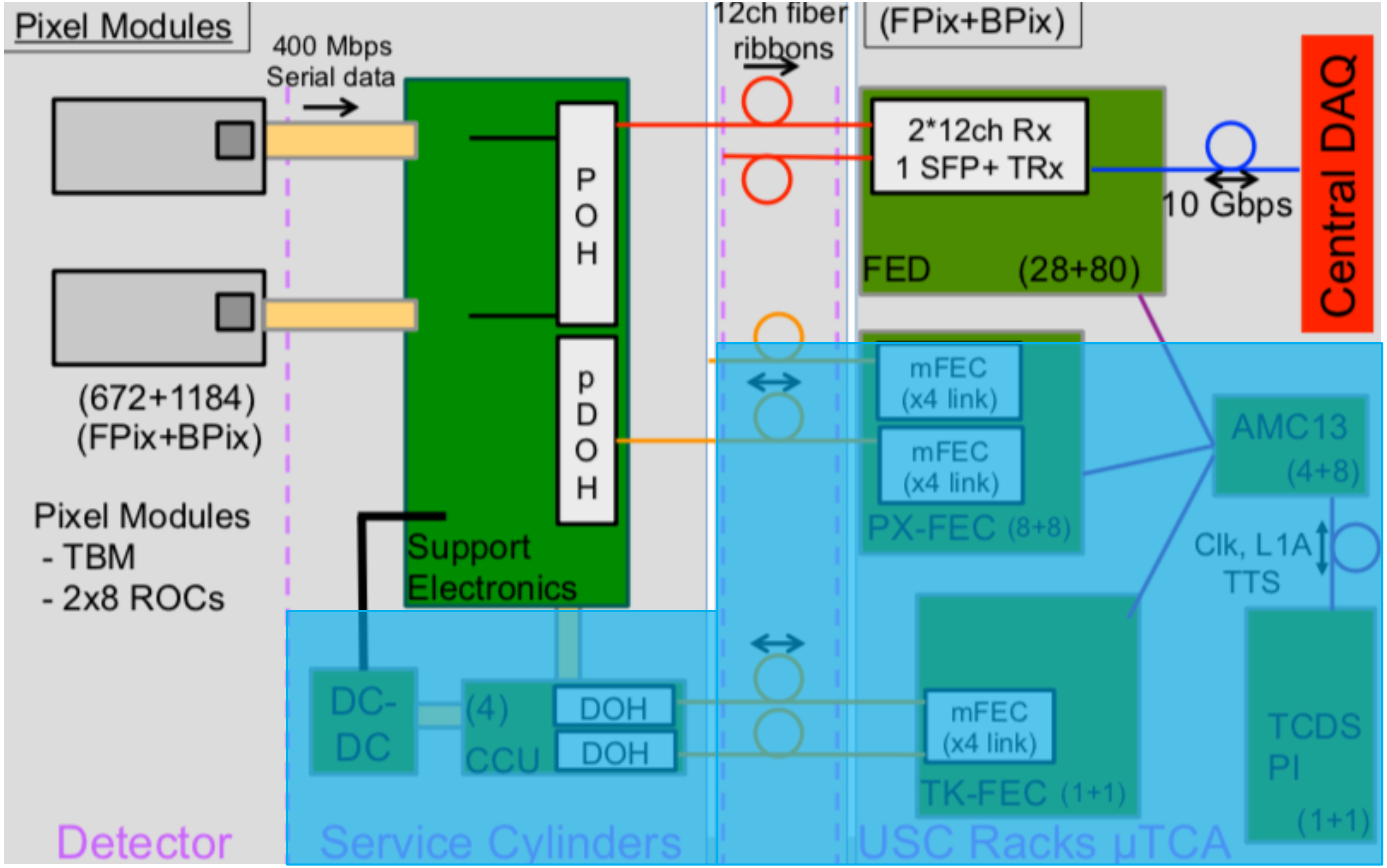
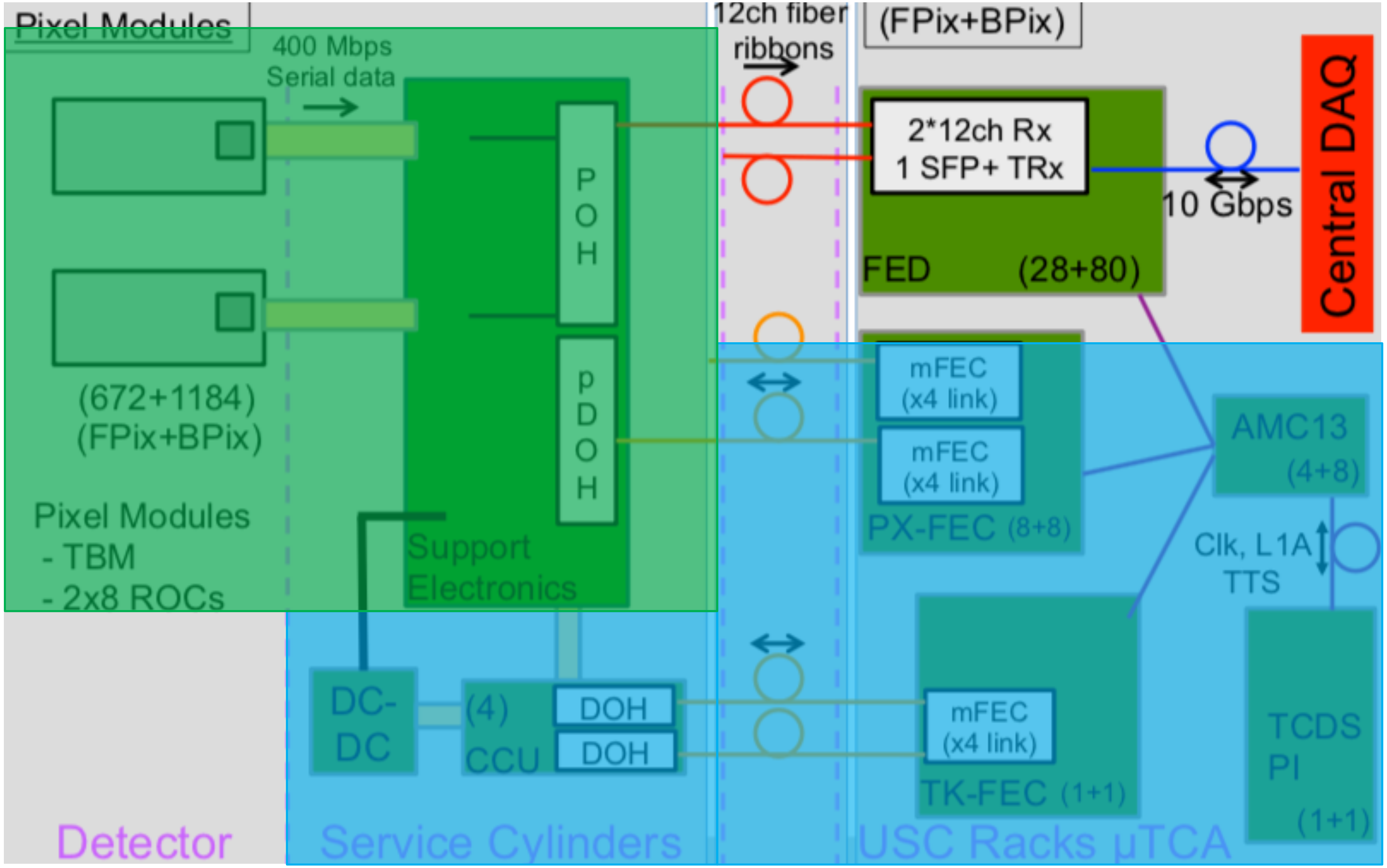


Provides power/clock/ trigger signals to detector

Upgraded Data Acquisition (DAQ)

Pixels start reading out event



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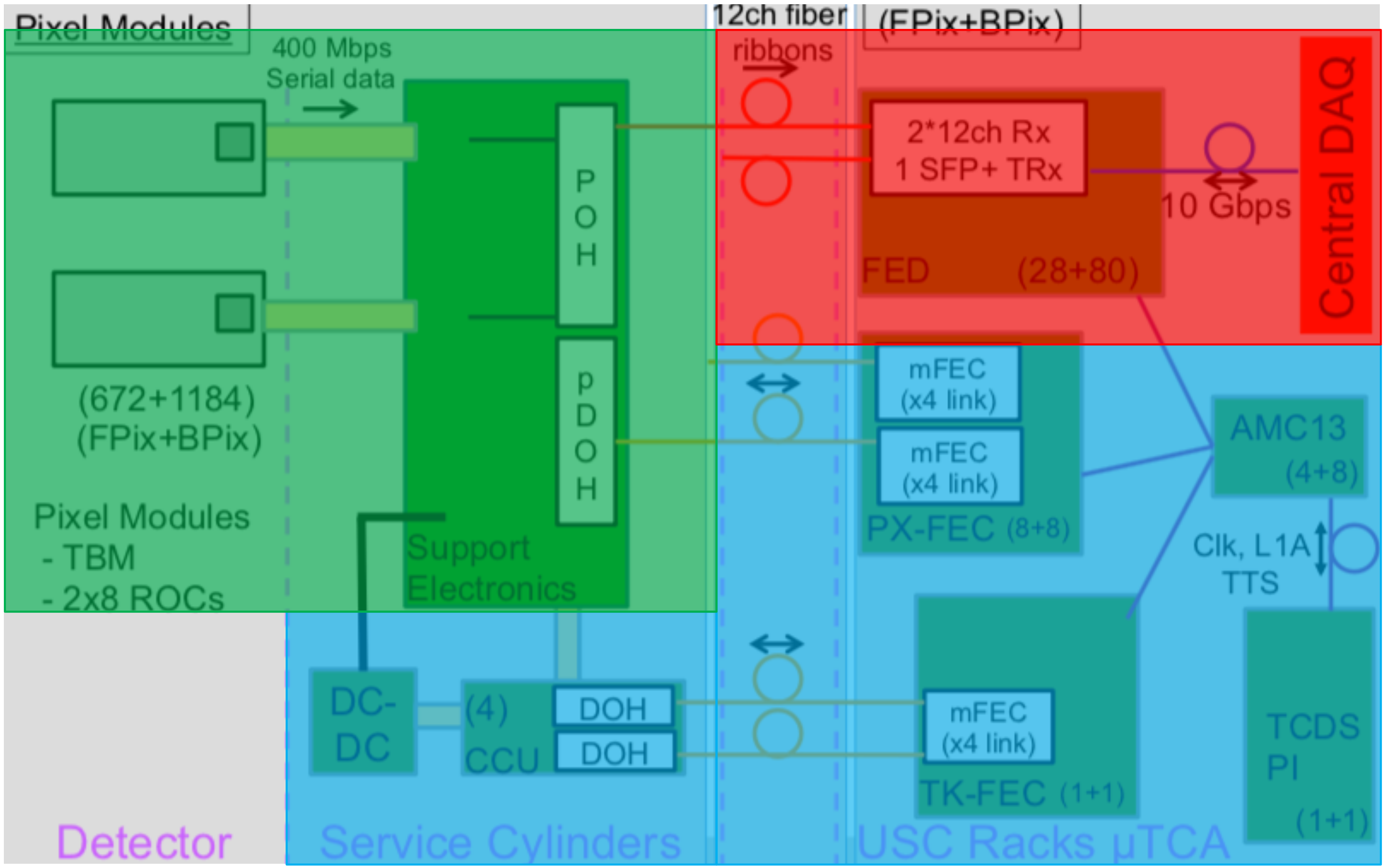


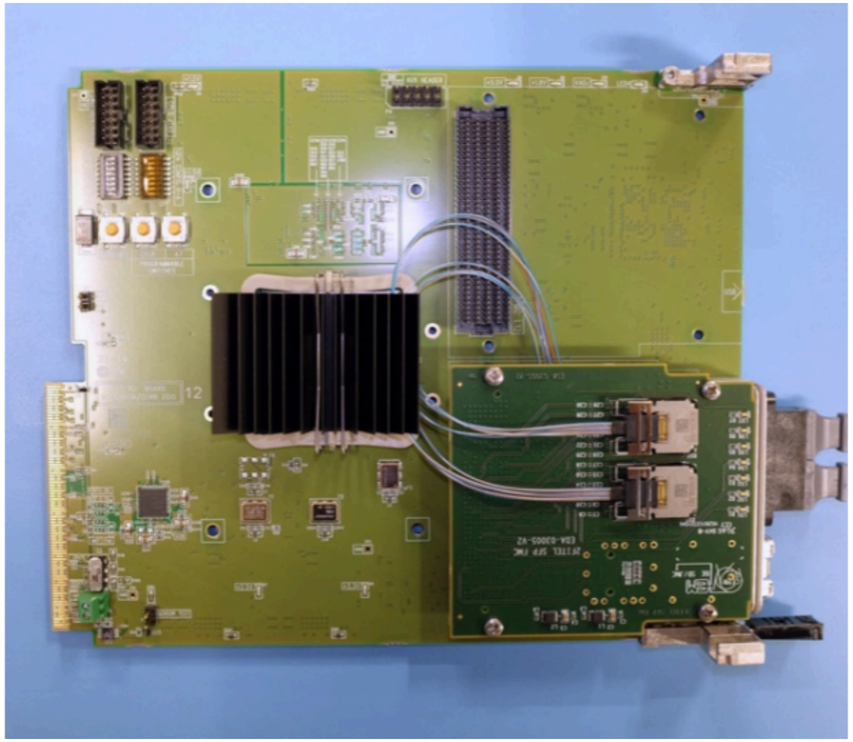
Event processing

Provides power/clock/ trigger signals to detector

Front-End Driver (FED)

FED: Custom μTCA card based on FPGA mezannine card carrier 7 (FC7)

- Firmware developed by IPHC/HEPHY and tested by Rice University
- 2 12-ch optical fiber inputs
  - 400 Mbps
- Event processing
  - Handle any event, even irregular
  - Ex: Event stops reading out halfway through
- Groups all channels into a single package
- Sends off to the Central DAQ of CMS
- Emulations show max throughput of ~7.5 Gbps



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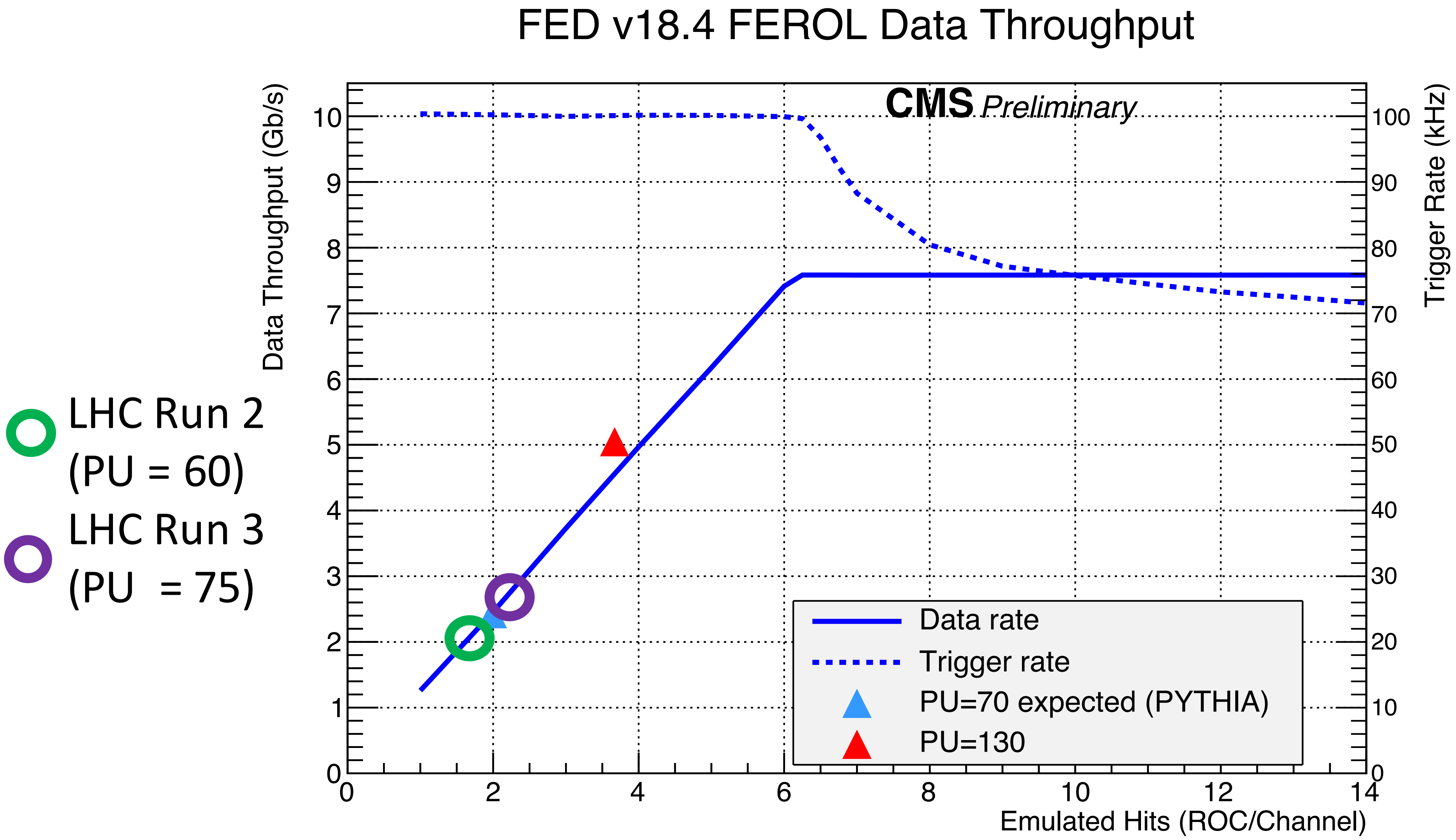
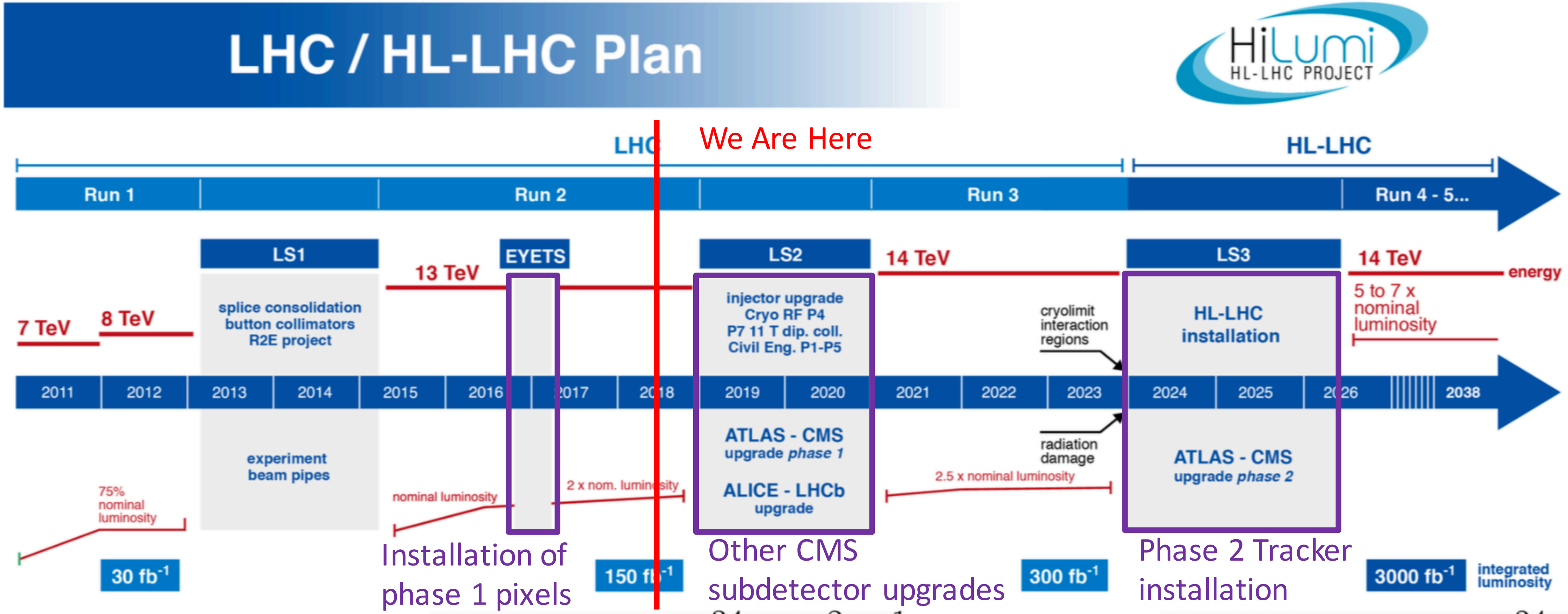


Upgrades for HL-LHC



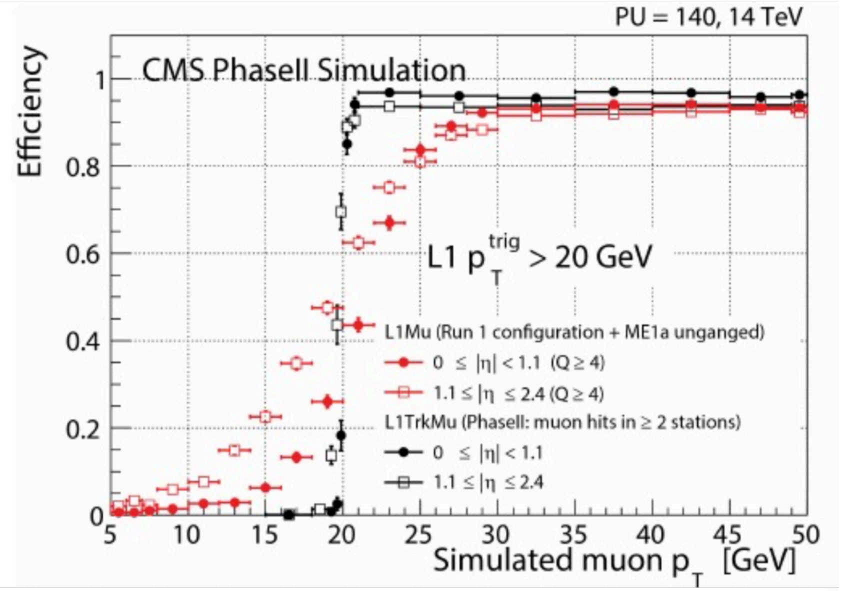
$$\mathcal{L}_{peak} \sim 1.5 \cdot 10^{34} cm^{-2} s^{-1}$$
$$\langle PU \rangle \sim 40 - 50$$

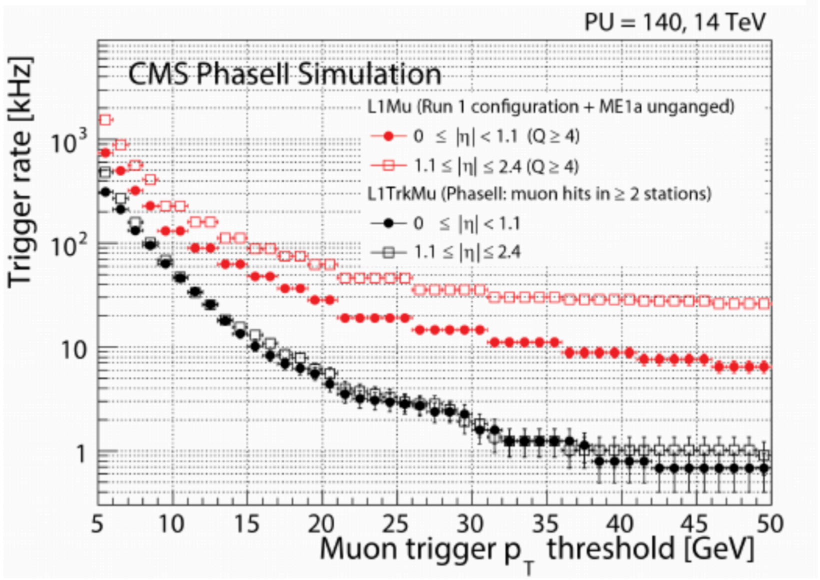
$$\mathcal{L}_{peak} \sim 5 - 7.5 \cdot 10^{34} cm^{-2} s^{-1}$$
$$\langle PU \rangle \sim 140 - 200$$

CMS Tracker Upgrade

Requirements

- Radiation hardness
  - 10x higher dose
- Inclusion in Level-1 trigger
  - Algorithms are inefficient at high pileup
  - Allow for increased latency
- Increased granularity
  - Channel occupancy of about 1%
  - High channel density
- Reduced material in tracking volume
  - Less material will increase tracking efficiency
  - Material densities, characteristic radiation lengths, and nuclear interaction length will impact event reconstruction

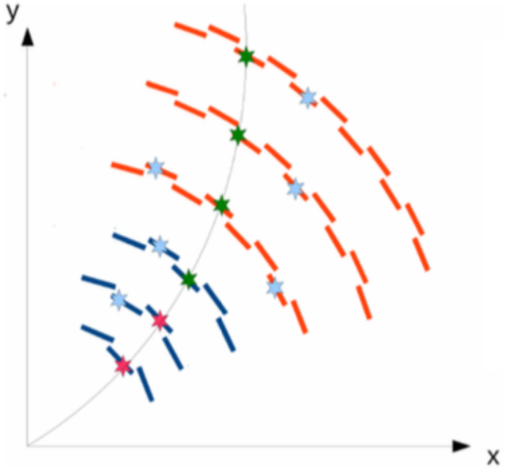


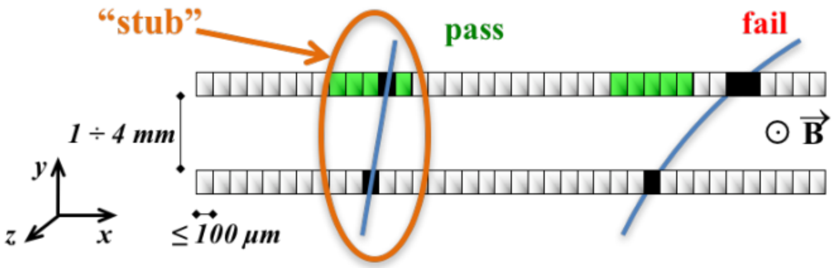


Level-1 Trigger and Track Finding

Tracklets

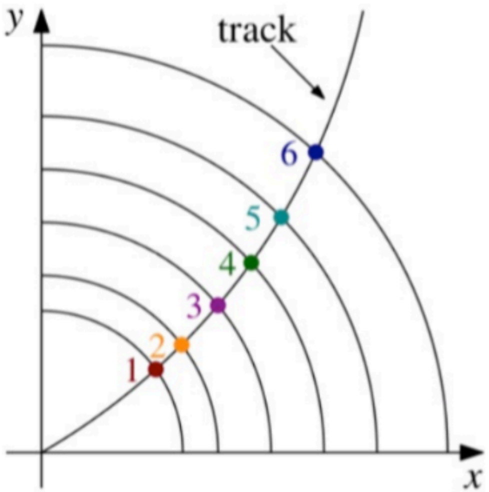
- Formed from stubs in adjacent layers of a module
- Minimize χ^2 and extrapolate tracks
- Remove duplicates

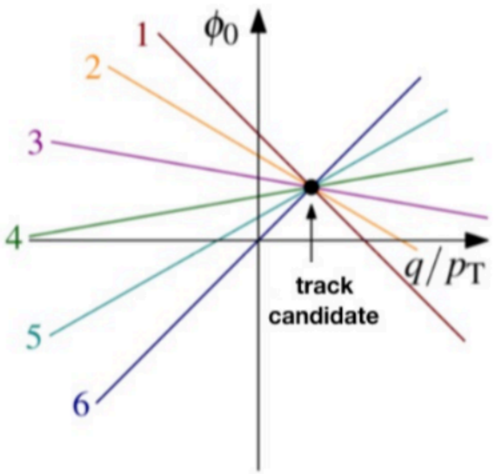




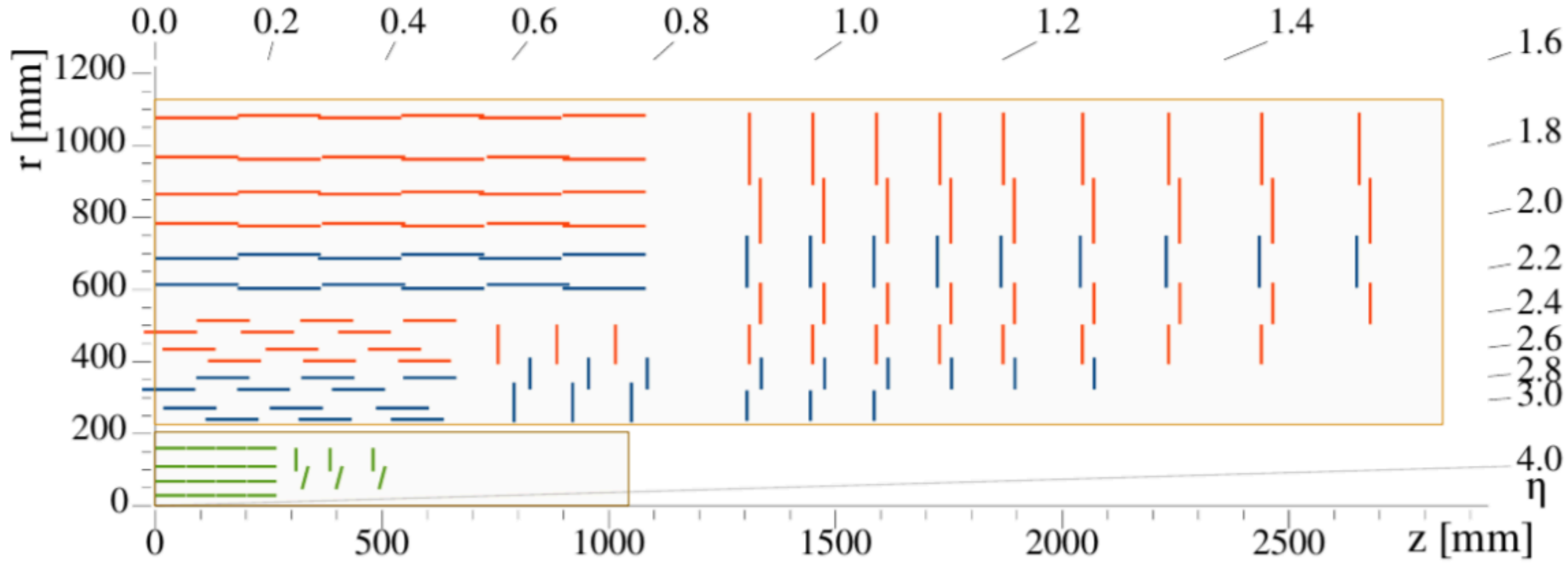
Hough transform approach

- Candidate track through transformation
- Minimize χ^2
- Remove duplicate

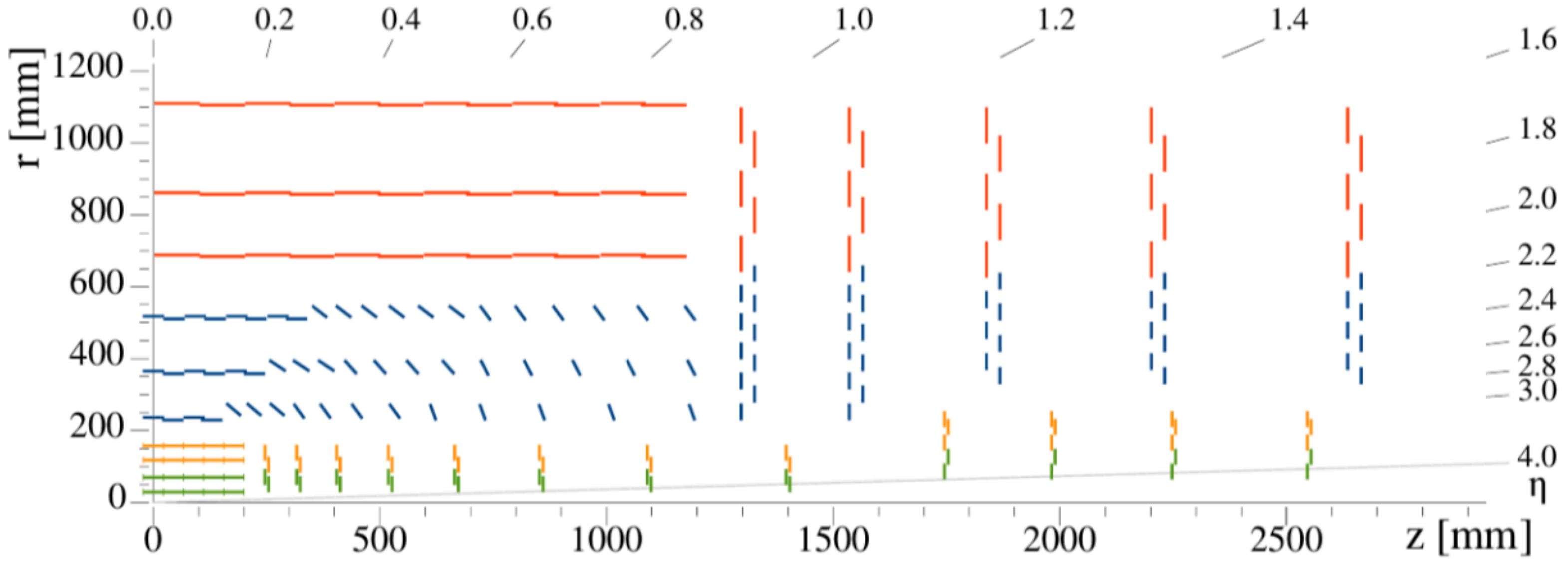




New Geometry



Current Tracker

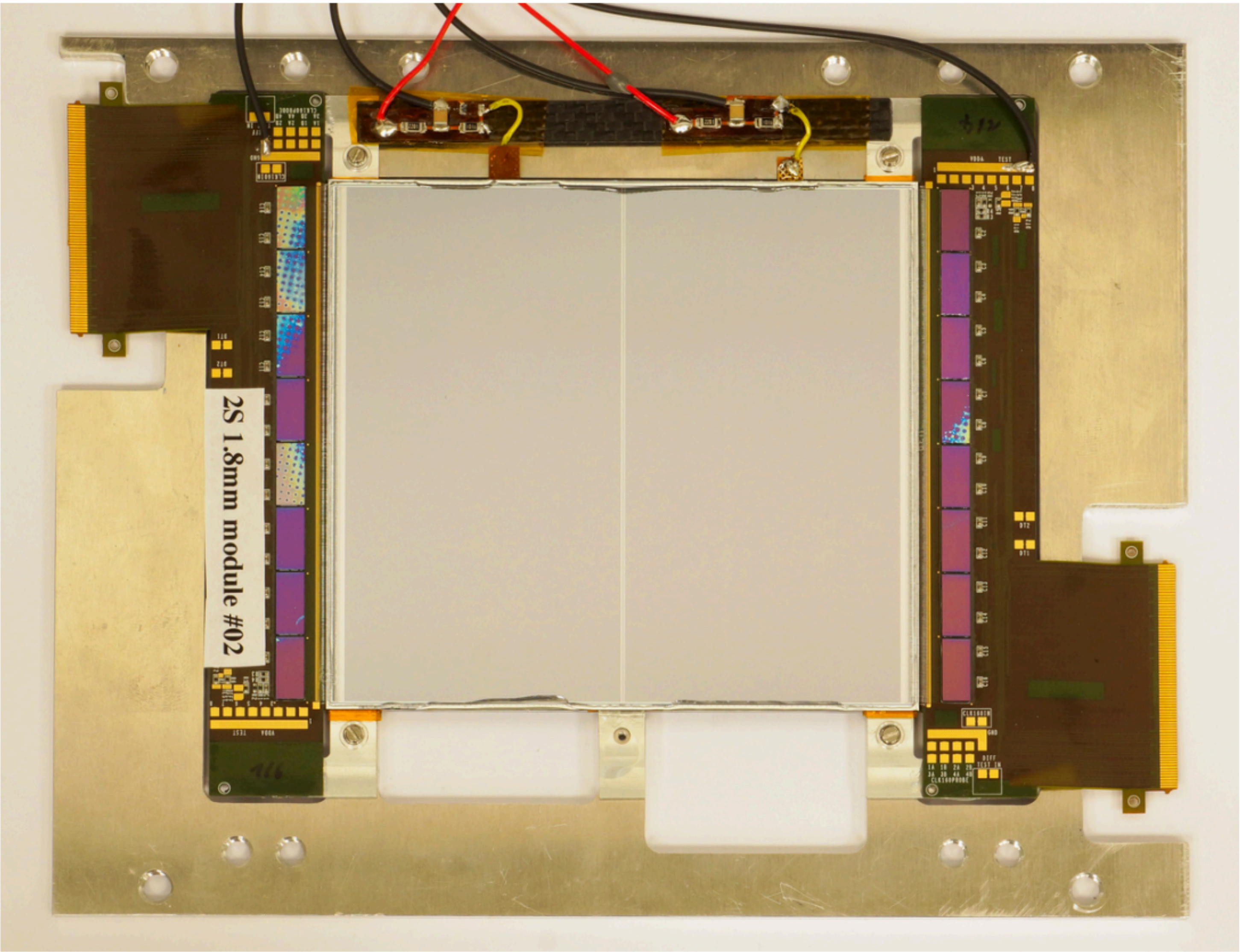


New Tracker
- Increases eta coverage
- Angled outer tracker modules
- Smaller pixels + more channels
  - To give the same occupancy

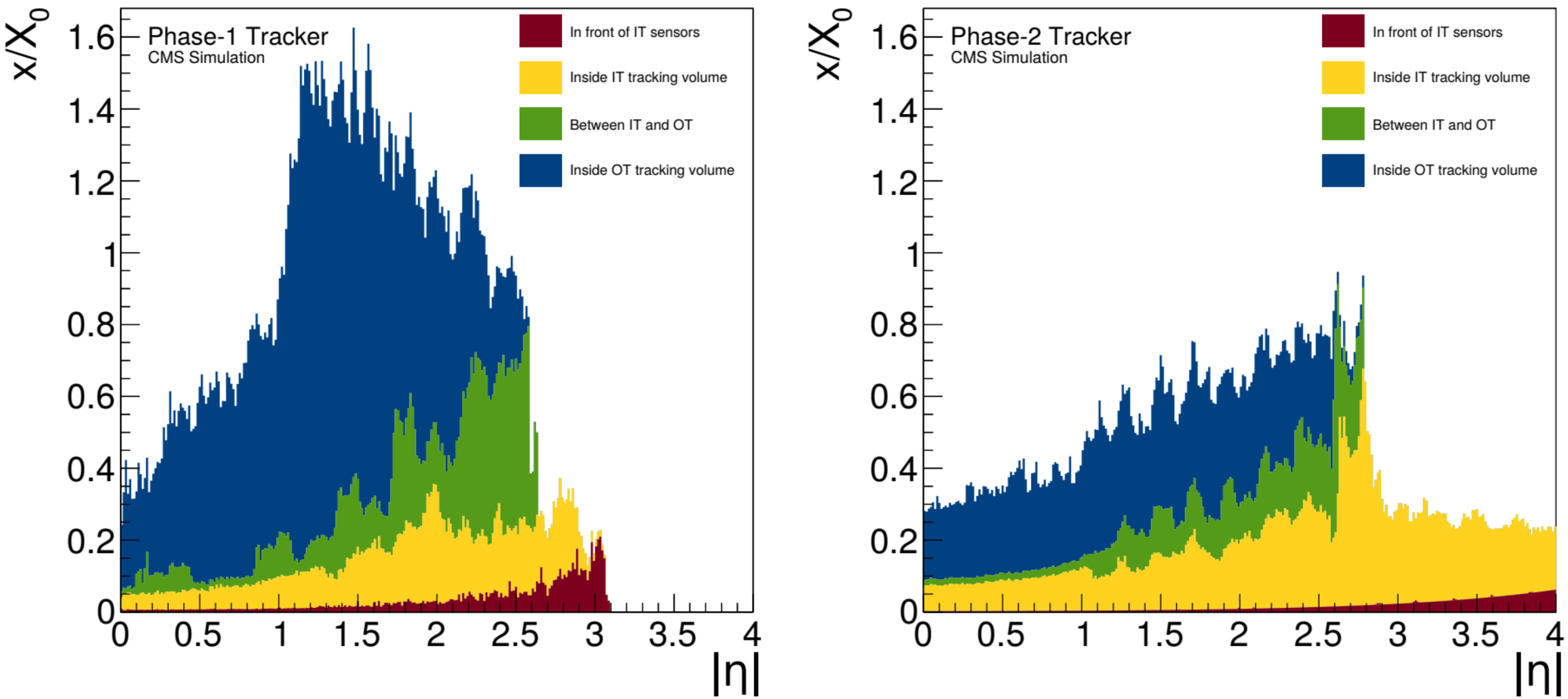
Module

Outer tracker module

- 2 sensors stacked on top of each other
  - 1.8 mm between sensors
- 10 cm long
- 1024 strips on each sensor
- External HV and LV for testing

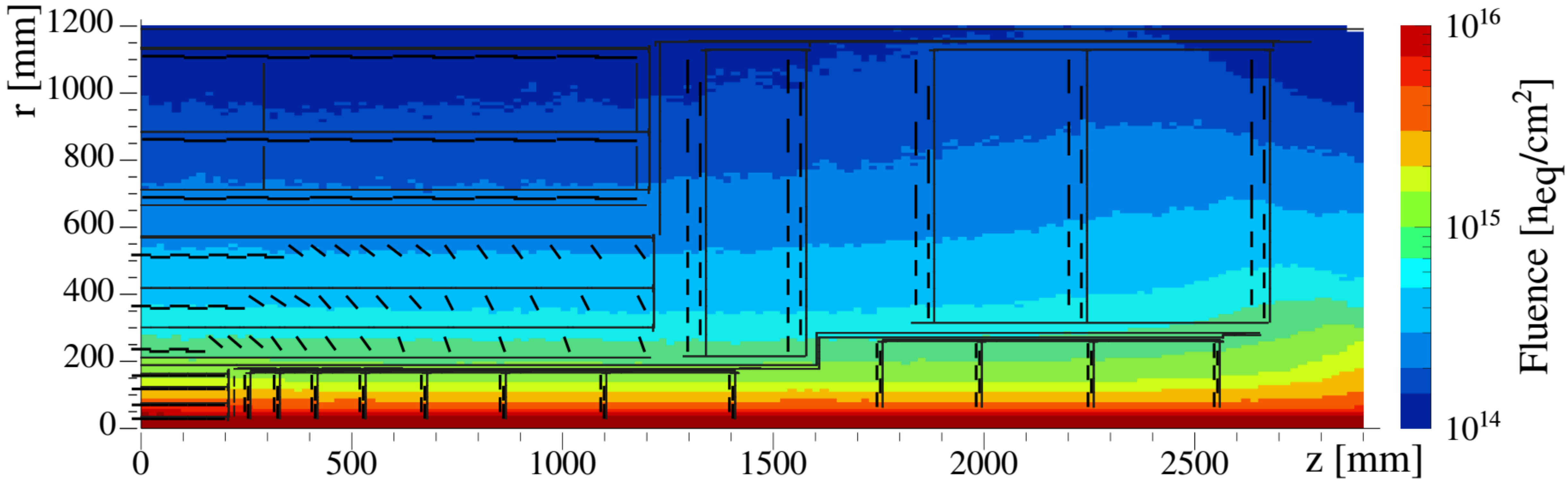


Material Budget



- Less material to limit secondary interactions
- Significant reduction of interactions in outer tracker (OT)

Integrated Particle Fluence



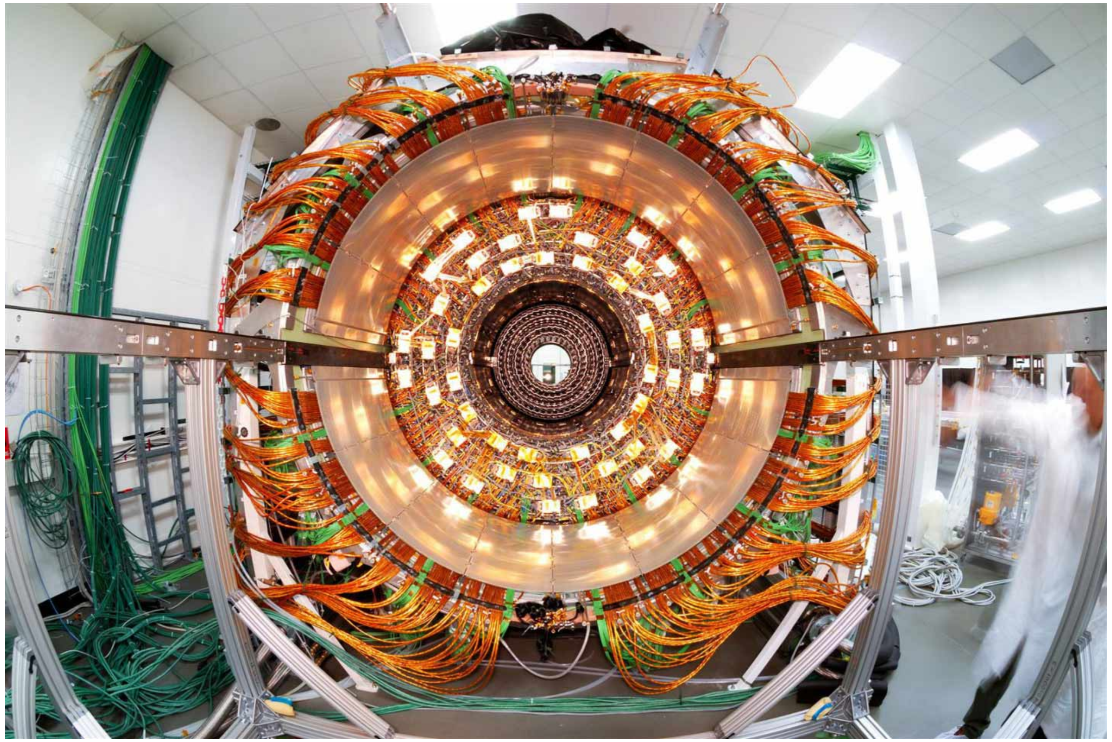
- Highly dependent on radius
- Simulated for integrated luminosity of 3000 fb^{-1}
- Inner tracker dose
  - Maximum fluence $2.3 \times 10^{16}\ n_{eq}/\text{cm}^2$ at $r = 28$ mm

Summary

Outer Strip Tracker
- 96.5% readout after 10 years!
- Large signal-to-noise ratio
- Stable!

Pixel Tracker
- Upgrade installed during winter 2016/2017
- Hit efficiency improved from phase 0 detector
- Leakage current is well understood
- DCDC converter issue bypassed
- DAQ bandwidth increased

HL-LHC Upgrade start 2024
- Entire tracker to be upgraded
- Improved detector geometry
- Radiation hardness to be improved



Acknowledgements

I would like to thank Karl Ecklund (Rice), the CMS Tracker Group, and the CMS Collaboration.

Department of Physics at Rice, CMS Collaboration,

Department of Energy Grant #DE-SC0010103

References

[1] A. Dominguez, D. Abbaneo, K. Arndt, and Bacchetta, CMS Technical Design Report for the Pixel Detector Upgrade, Tech. Rep. CERN-LHCC-2012-016. CMS-TDR-11 (CERN, Geneva, 2012)

[2] A. Affolder, the CMS Silicon Strip Tracker (SST) Collaboration, The CMS Silicon Strip Tracker: Design and Production Status, https://doi.org/10.1016/j.nuclphysbps.2004.08.037

[3] https://agenda.infn.it/getFile.py/access?contribId=98&sessionId=4&resId=0&materialId=slides&confId=13450

[4] https://agenda.infn.it/getFile.py/access?contribId=130&sessionId=13&resId=0&materialId=poster&confId=13450

[5] https://indico.cern.ch/event/686555/contributions/2972183/attachments/1677123/2692957/180705_CMS_Tracker_Upgrade_Delcourt.pdf

[6] https://pos.sissa.it/309/018/pdf

[7] https://agenda.infn.it/getFile.py/access?contribId=104&sessionId=3&resId=0&materialId=slides&confId=10190

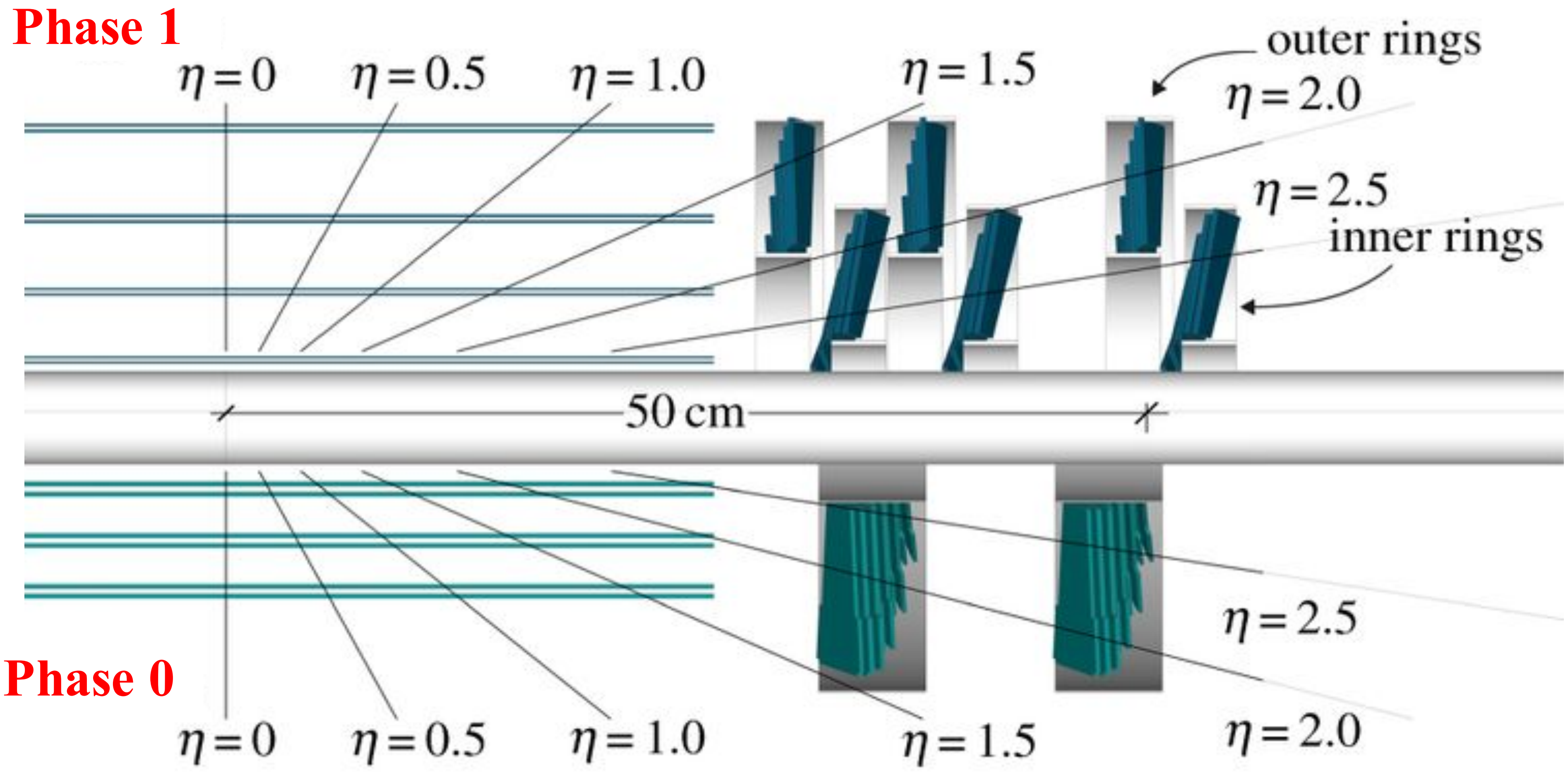
[8] https://indico.cern.ch/event/758190/contributions/3172360/attachments/1732998/2801747/progress_report_2_1.pdf

[9] CMS Collaboration, The Phase-2 Upgrade of the CMS Tracker, Teck. Rep. CERN-LHCC-2017-009. CMS-TDR-014 (CERN, Geneva, 2017)

[10] https://indico.cern.ch/event/765022/contributions/3175638/attachments/1733308/2803556/2018_10_16_Plot_approval_BPix_Ileak_vdep.pdf

Backup

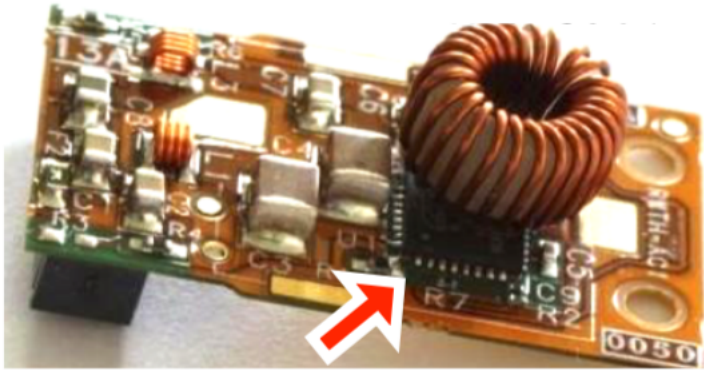
Pixel Phase 1 layout compared to Phase 0



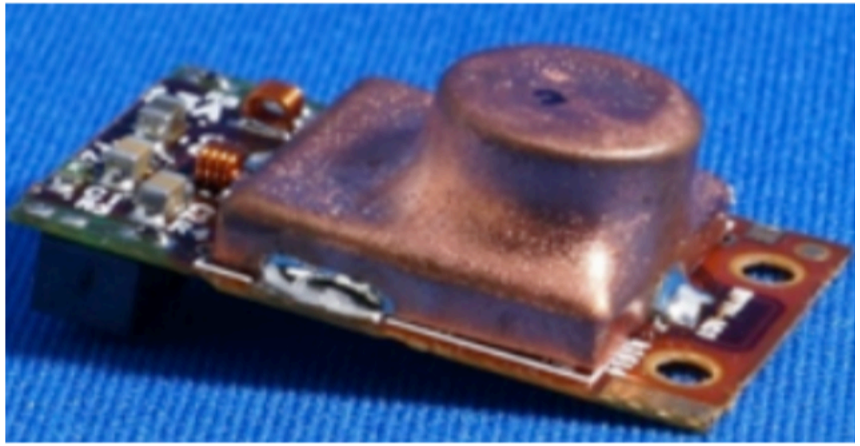
DCDC Converter Issue

Component Failures

- During last two months of operation in 2017
- 65 out of 1184 converters failing
- Able to narrow down cause to a flaw in chip design
- Failure Mechanisms
  - $V_{in} > 5$ V (Active state)
  - Irradiated to about 1 Mrad
  - Switched to disabled mode (used in power cycling)
  - Increases leakage current which charges a capacitor until it damages transistors in control circuit
- Used power cycling as a reset mechanism
- Solution?
  - Fix being tested, to be integrated for pixels in LS2
  - Change power cycling method
  - No longer disable converters
- At same point in 2018
  - Same irradiation and voltage, but no failures

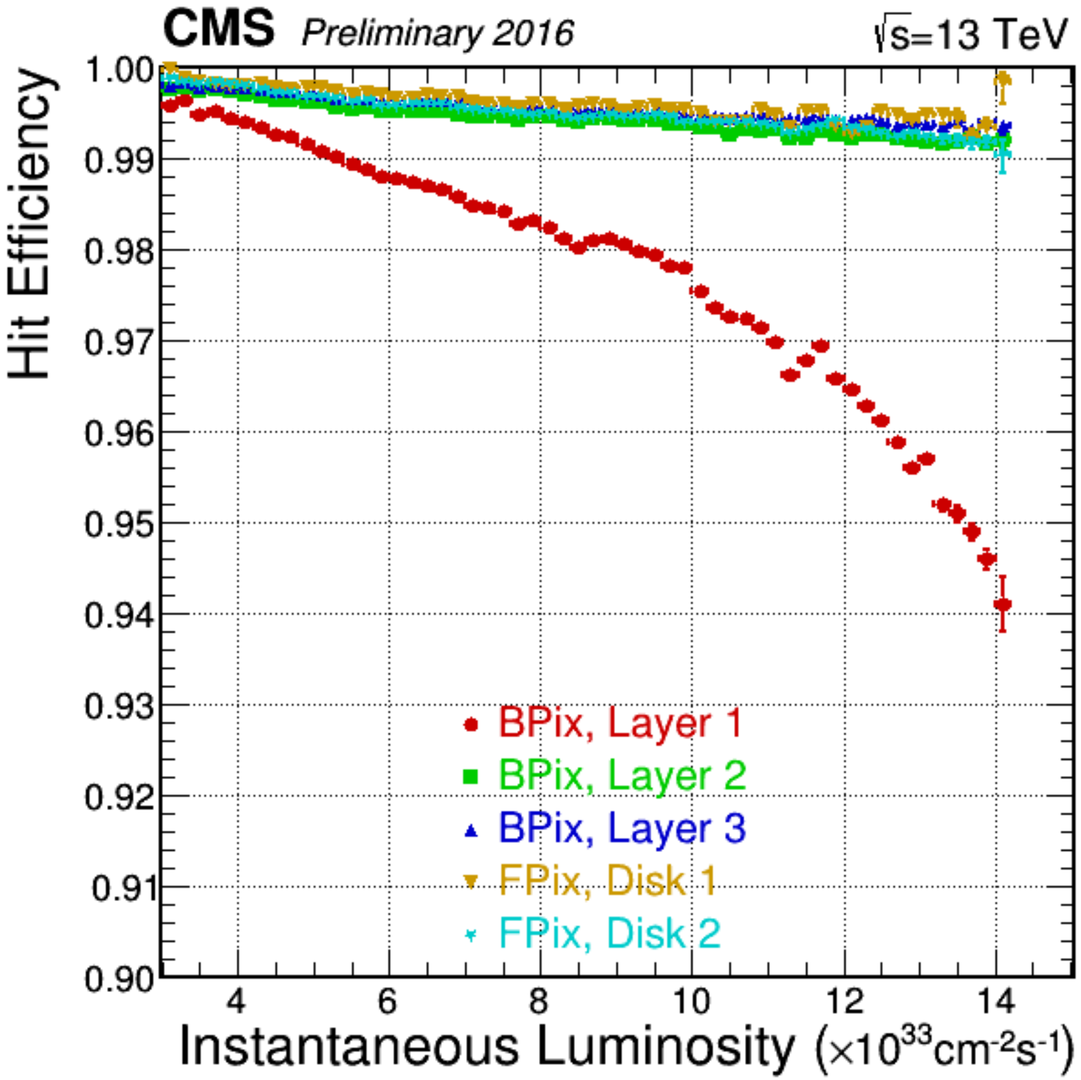


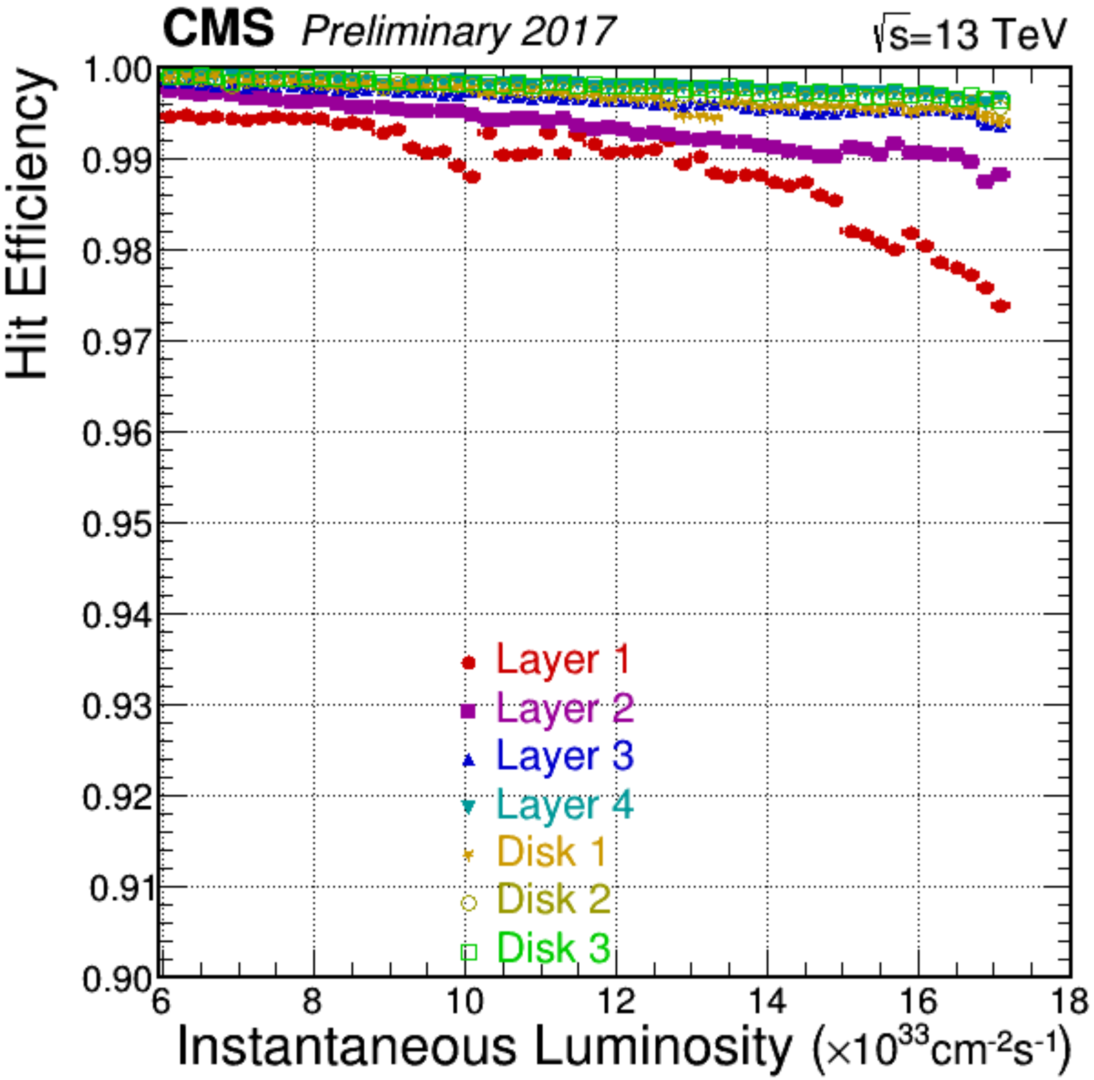
FEAST2 chip used by many detectors at LHC



DCDC Converter

Hit Efficiency





https://twiki.cern.ch/twiki/pub/CMSPublic/PixelOfflinePlots2016/HitEfficiency_vs_InstLumi_LayersDisks_2016Data_Update2.png
https://twiki.cern.ch/twiki/pub//CMSPublic/PixelOfflinePlotsAugust2017/HitEfficiency_vs_InstLumi_LayersDisks_2017Data.png