Inter-calibration slope and dLY

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AHCAL analysis workshop at Tokyo

Yuji Sudo (DESY)

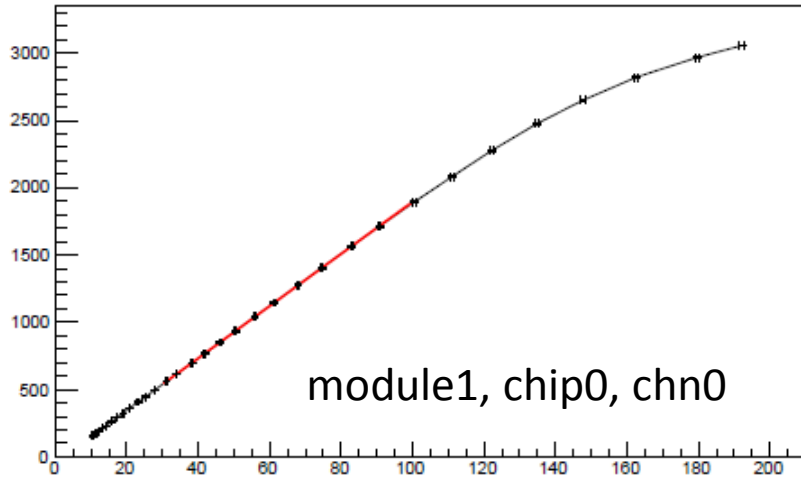# HG vs LG

after pedestal subtraction
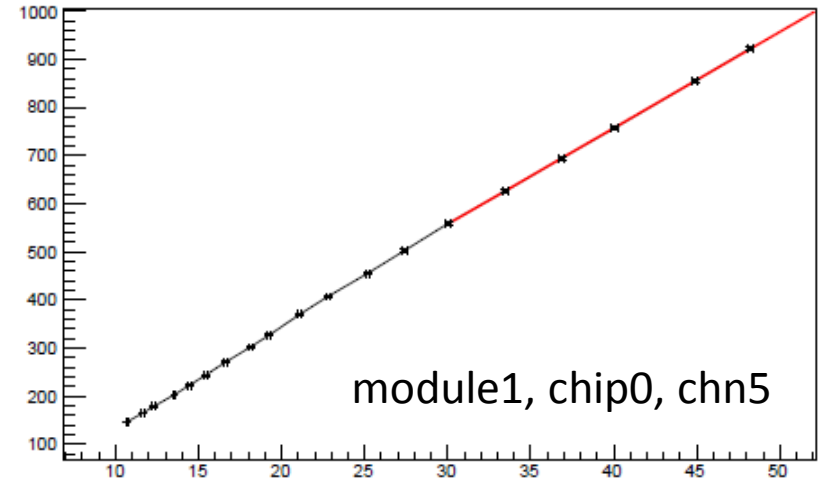fitting range 30 < LG < 100
total amount of charge in a chip < 60000 ADC (HG)
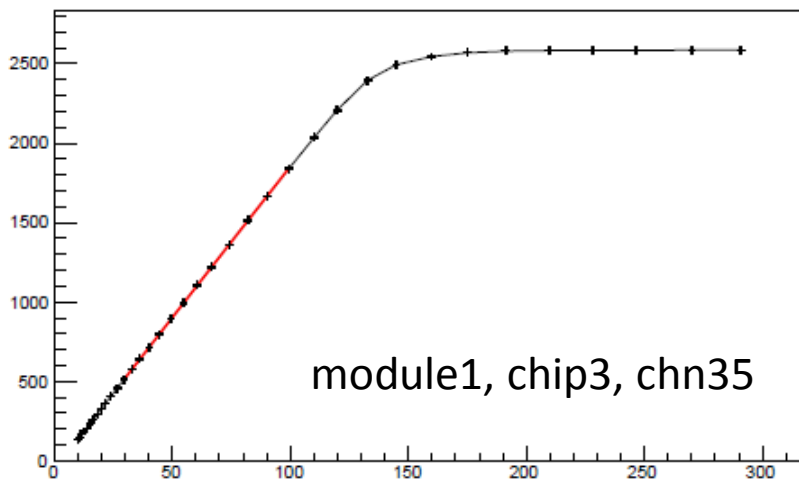at least 5 points in the fitting range

graph_IC_module1_chip0_chn0

module1, chip0, chn0

graph_IC_module1_chip0_chn5

module1, chip0, chn5
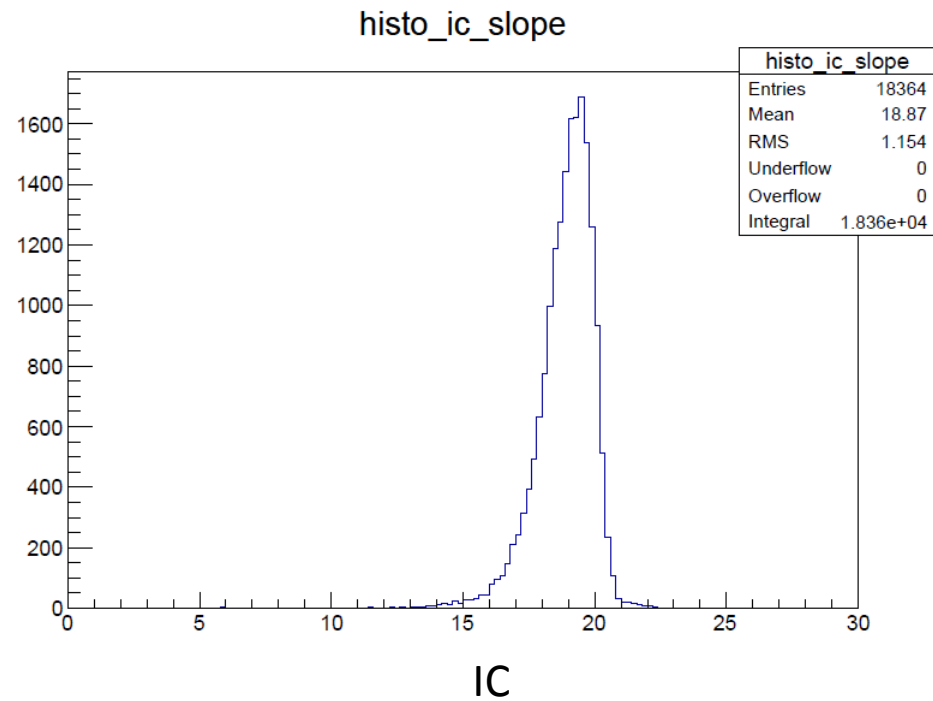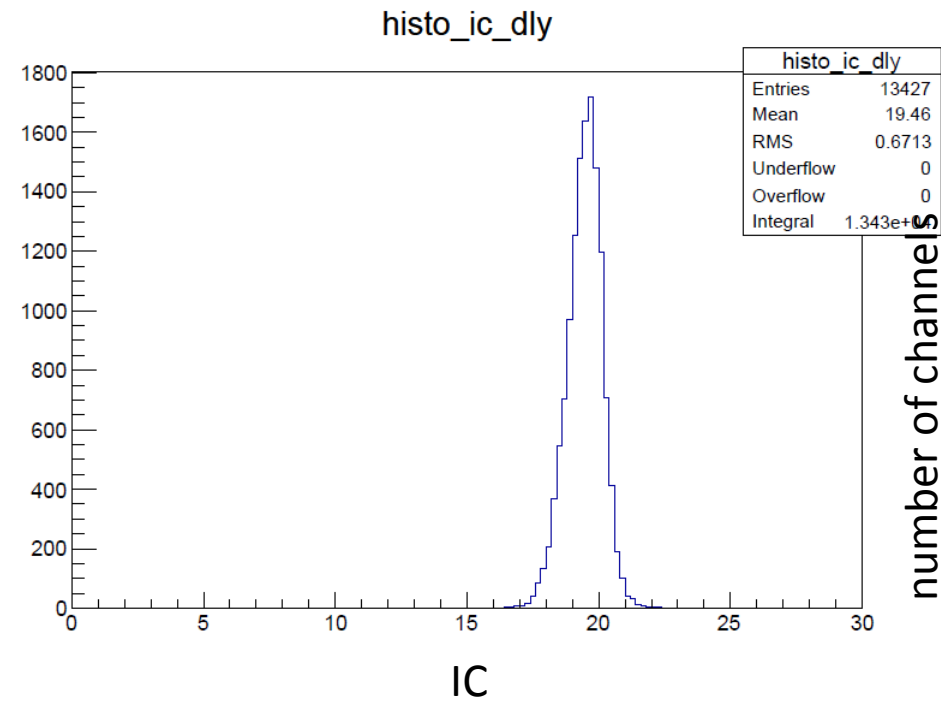

graph_IC_module1_chip3_chn35

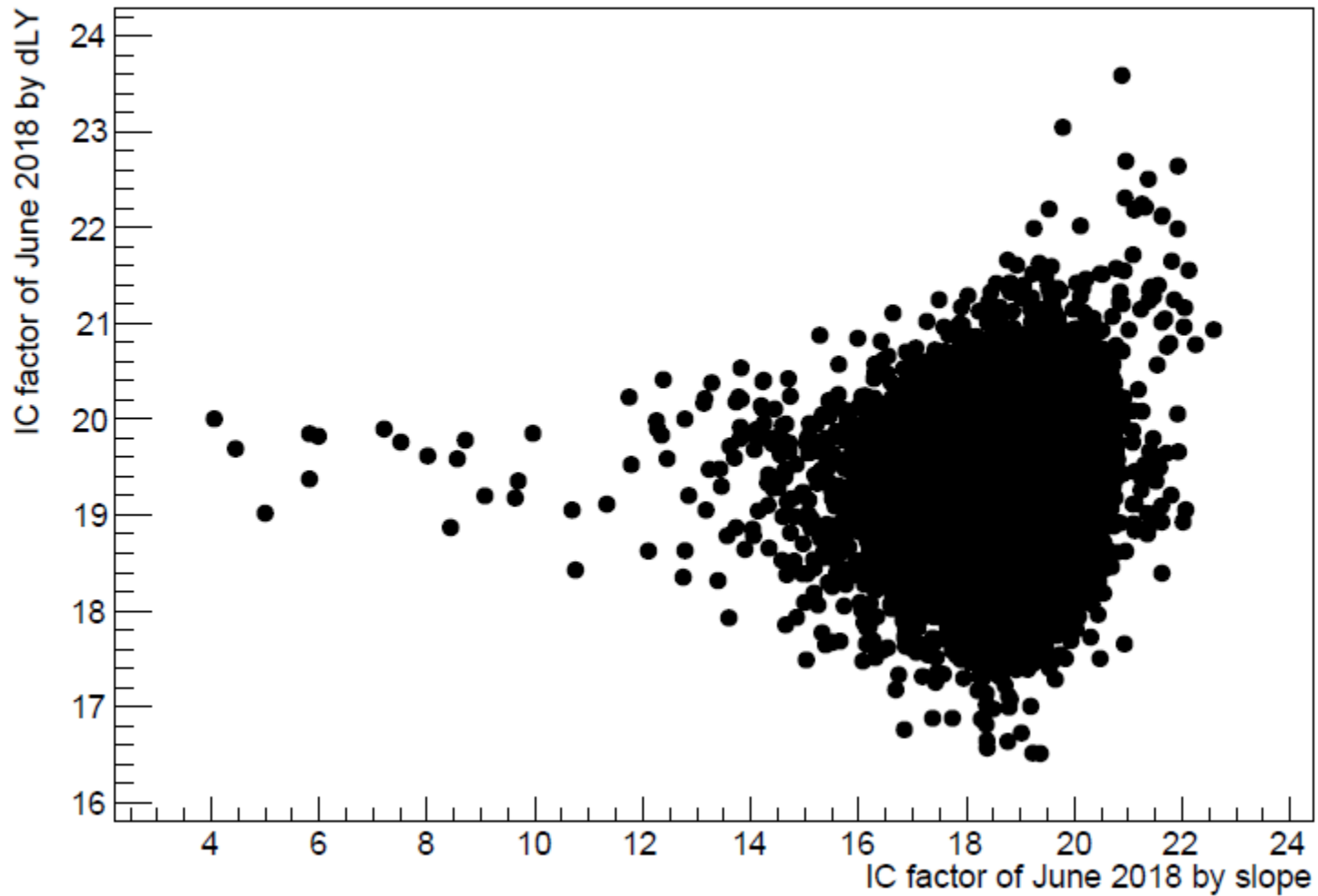module1, chip3, chn35

graph_IC_module1_chip7_chn29

module1, chip7, chn29
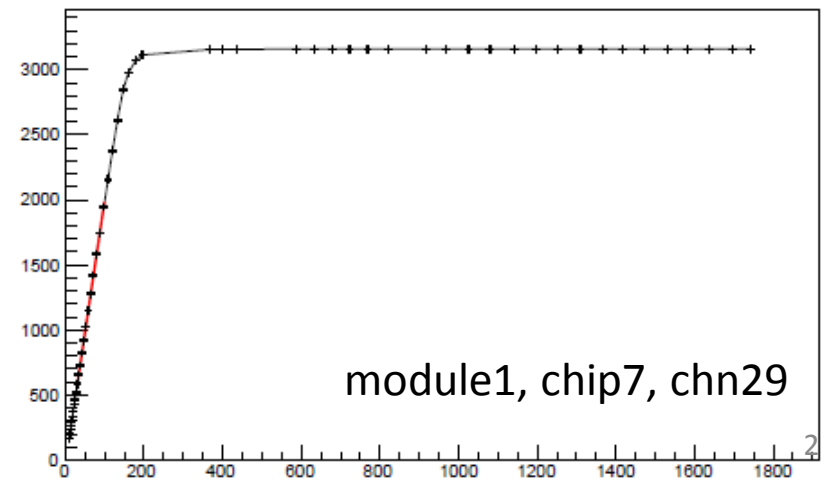
IC factor dLY and slope

IC factor dLY vs Slope

ratio of IC factor IC_{dLY}/IC_{slope}

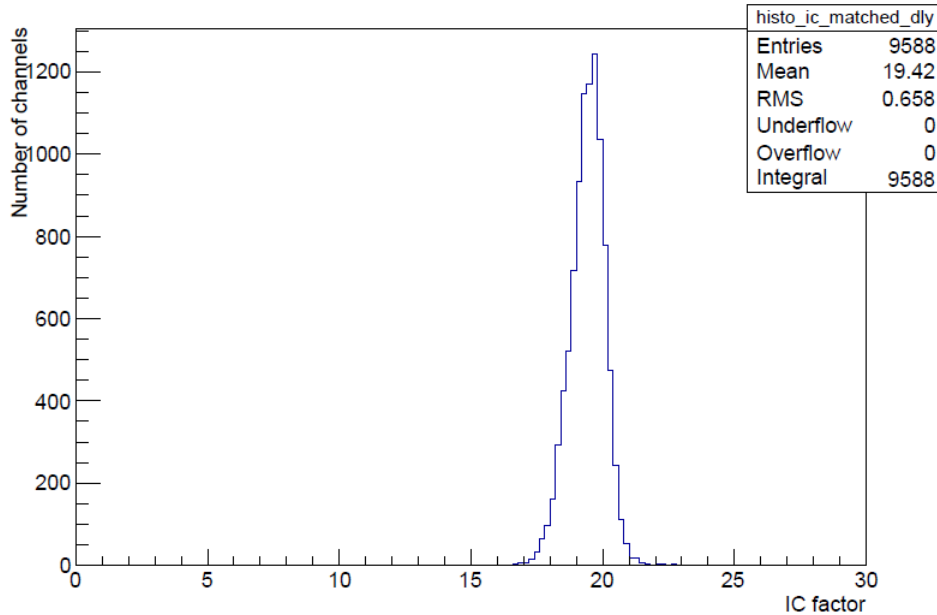

histo_ratio_dly_ov_slope
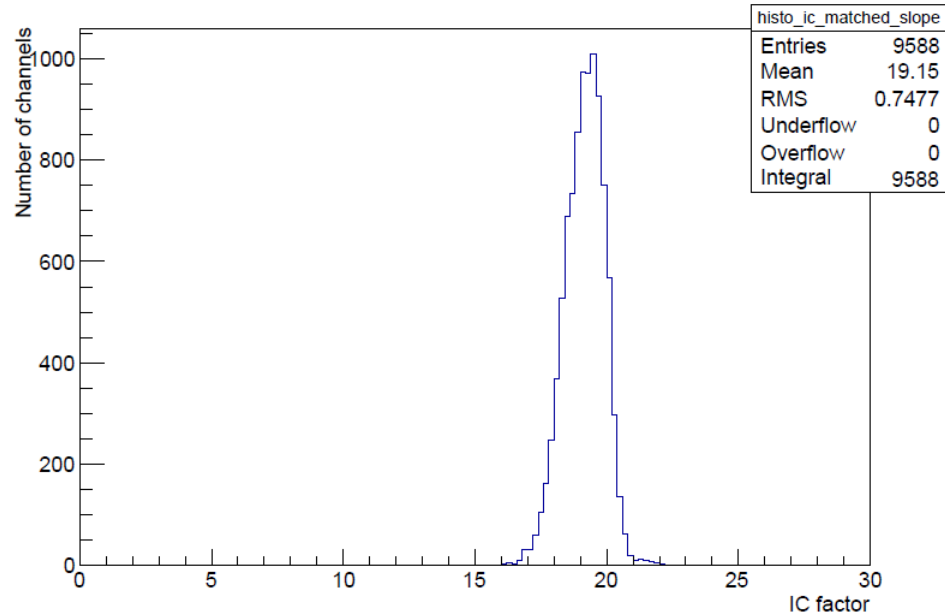
histo_ratio_dly_ov_slope	
Entries	11087
Mean	1.031
RMS	0.06215
Underflow	0
Overflow	97
Integral	1.099e+04
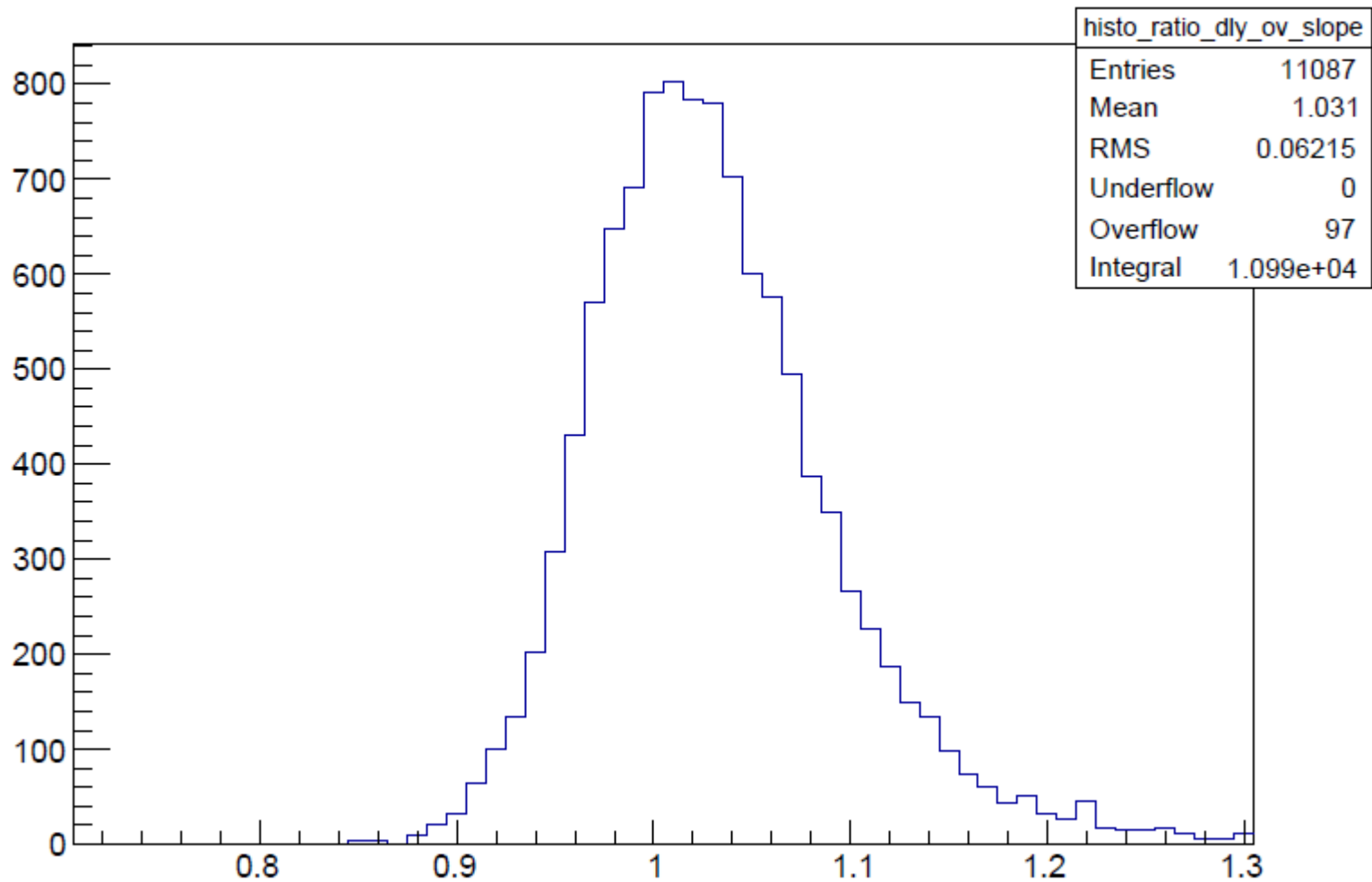
IC factor dLY and slope
$0.9 < IC_{dLY}/Ic_{slope} < 1.1$

IC factor extracted by dLY and slope

1. fill IC value extracted by dLY   within mean +/- 3*rms of IC histogram of dLY on p.6
2. fill IC value extracted by slope within mean +/- 3*rms of IC histogram of slope on p.6
if a IC value is not filled by first step.

histo_ic_dly_slope

histo_ic_dly_slope	
Entries	20326
Mean	19.31
RMS	0.7388
Underflow	0
Overflow	0
Integral	2.033e+04

more than 90% channels