Inter-calibration slope and dLY bug fixed

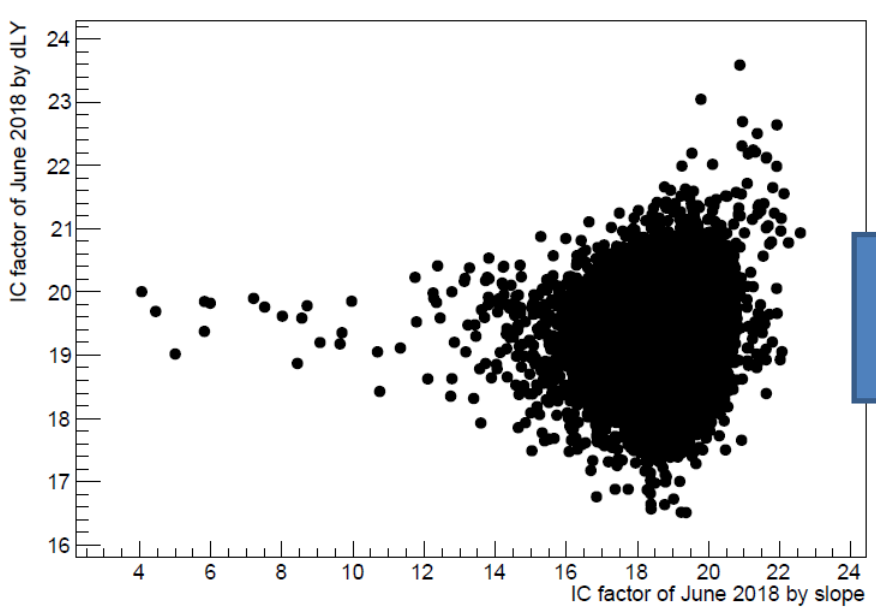
22.08.2018

AHCAL analysis workshop at Tokyo

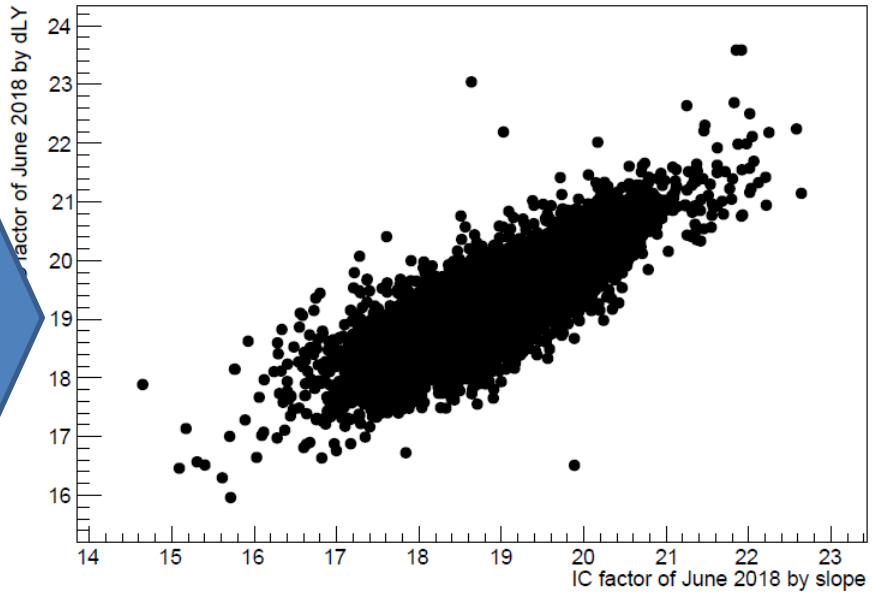
Yuji Sudo (DESY)

IC factor dLY vs Slope

before

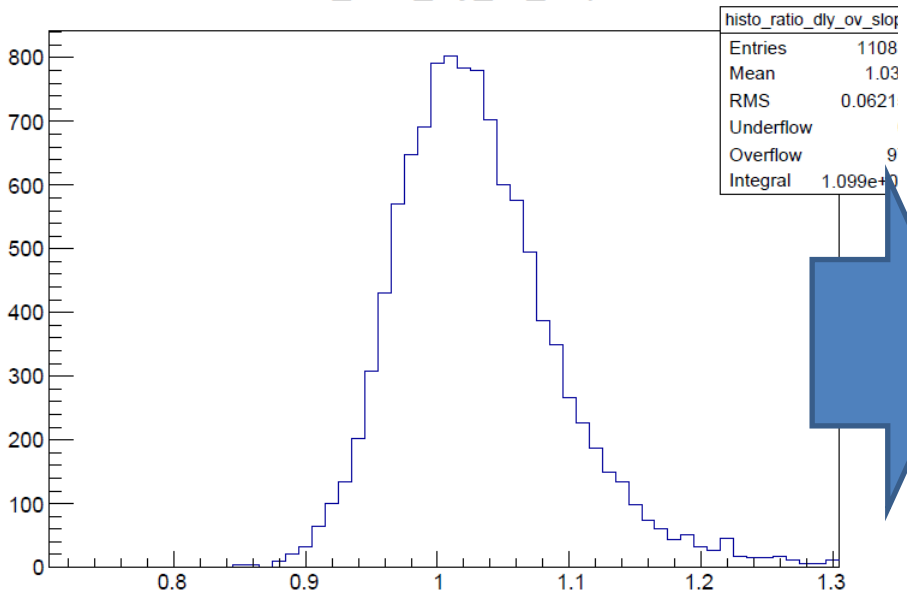


bug fixed

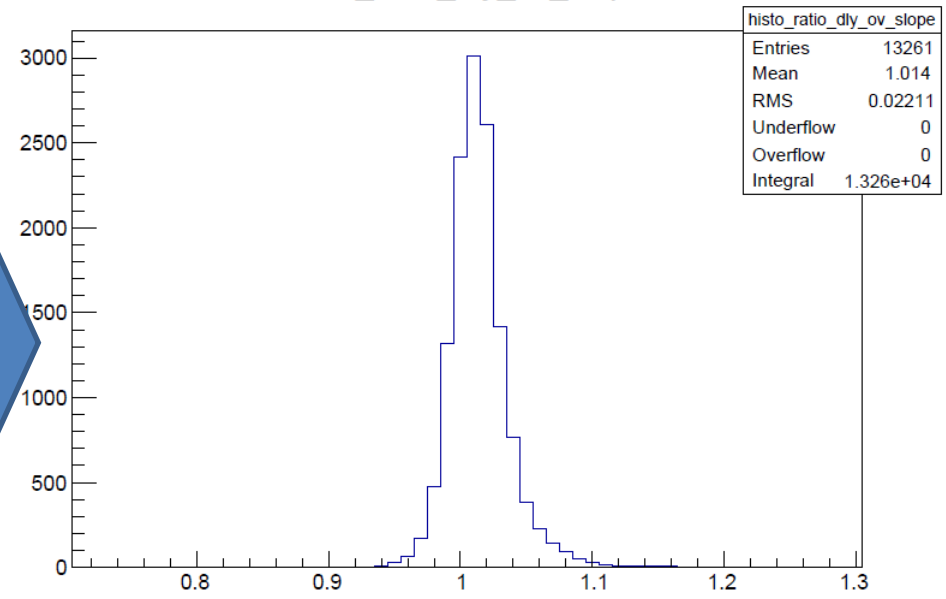


ratio of IC factor IC_{dLY}/IC_{slope}

before



bug fixed

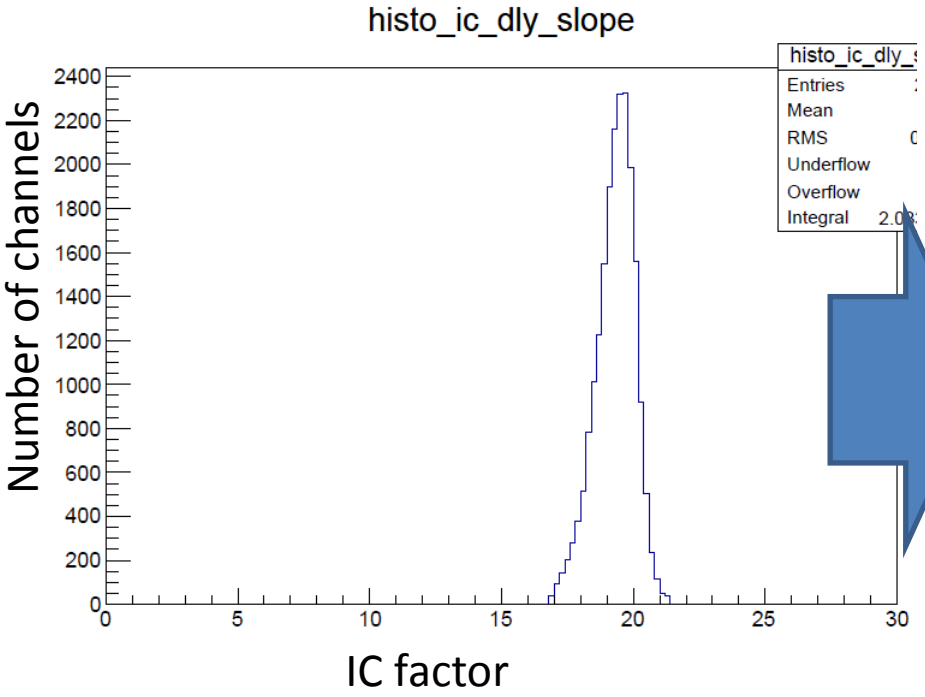


IC factor extracted by dLY and slope

1. fill IC value extracted by dLY within mean +/- 3*rms of IC histogram of dLY on p.8
2. fill IC value extracted by slope within mean +/- 3*rms of IC histogram of slope on p.8

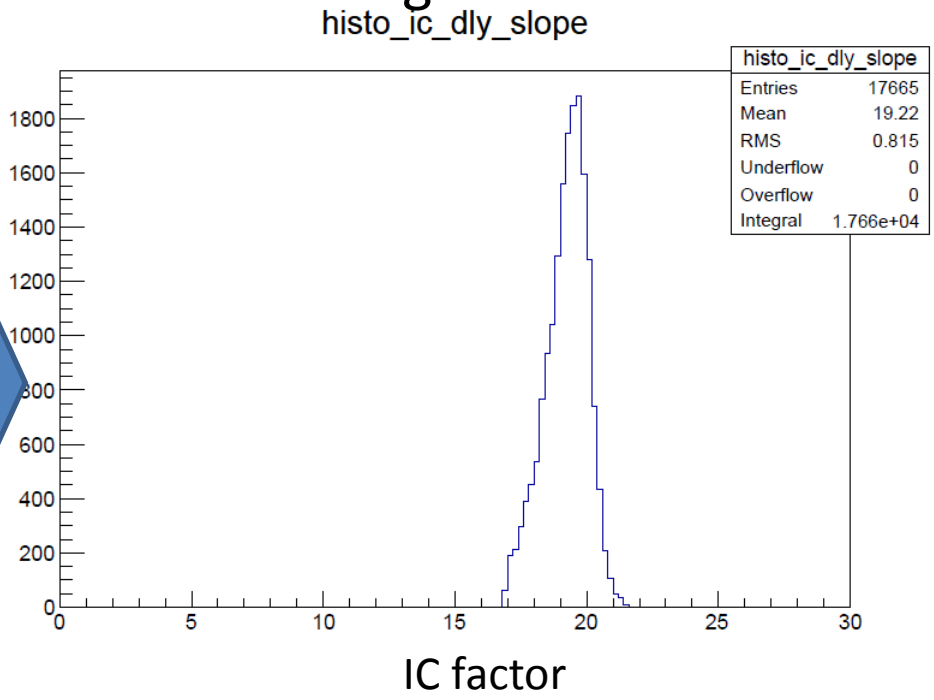
if a IC value is not filled by first step.

before



more than 90% channels

bug fixed

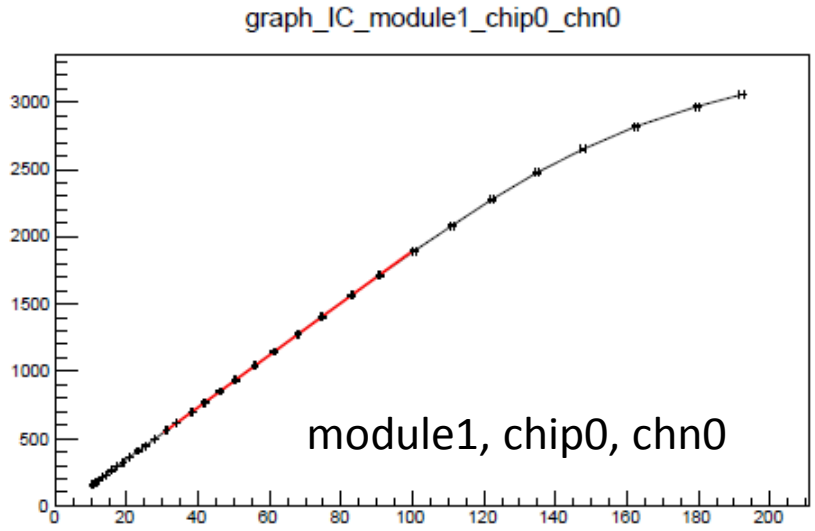


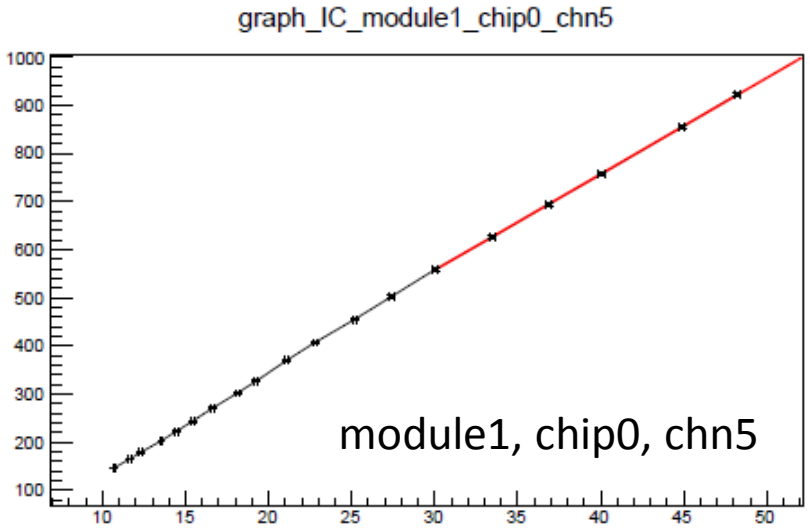
~80% of channels

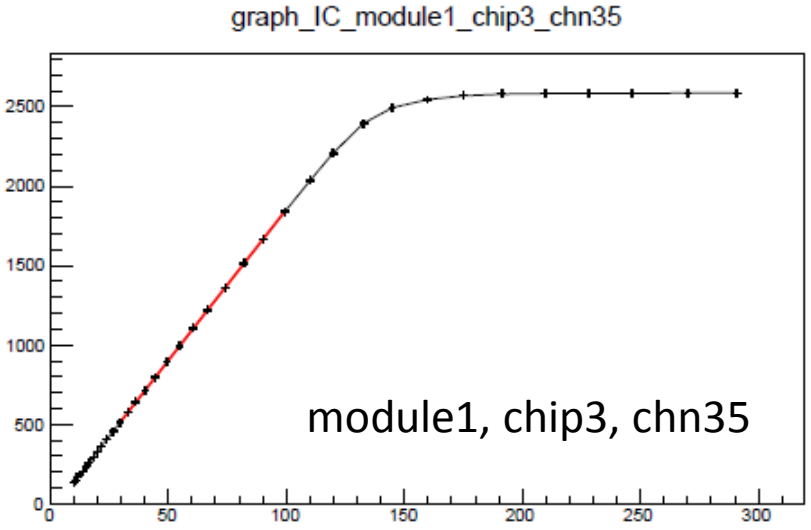
backup

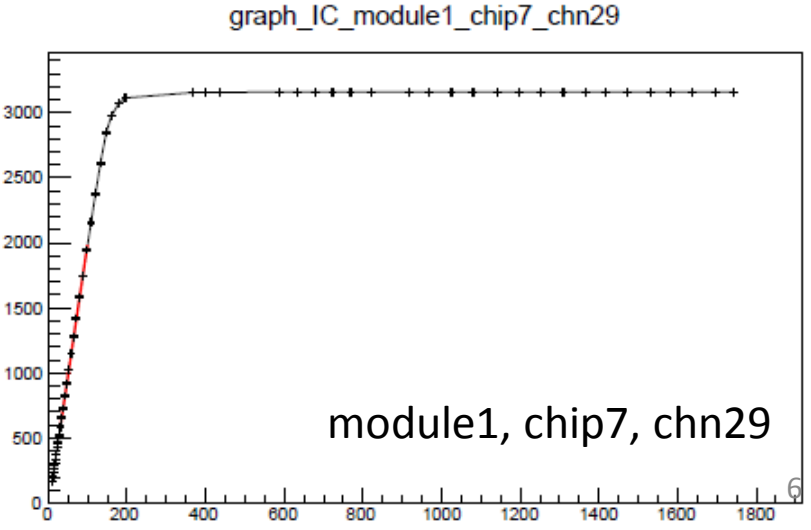
HG vs LG

after pedestal subtraction
fitting range 30 < LG < 100
total amount of charge in a chip < 60000 ADC (HG)
at least 5 points in the fitting range

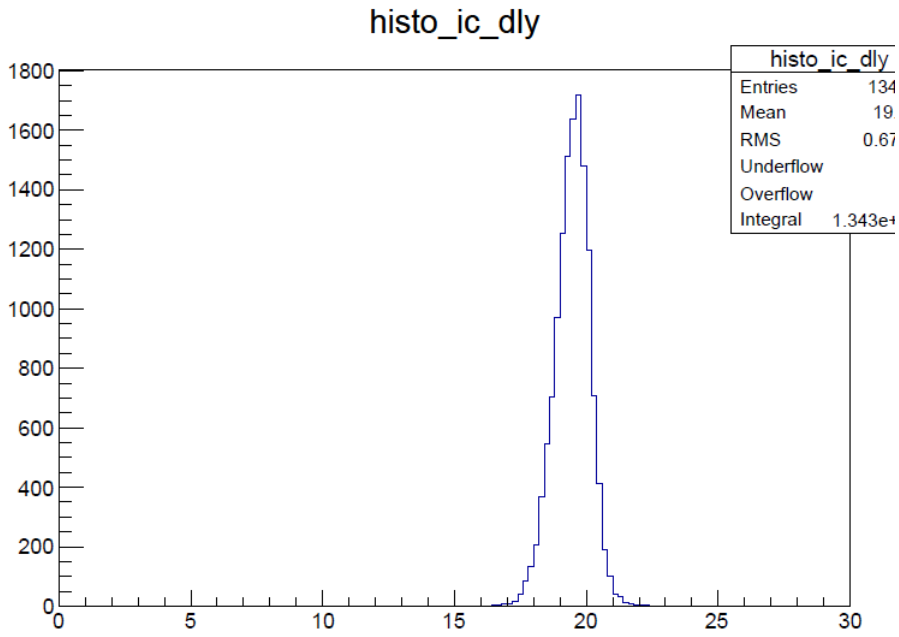


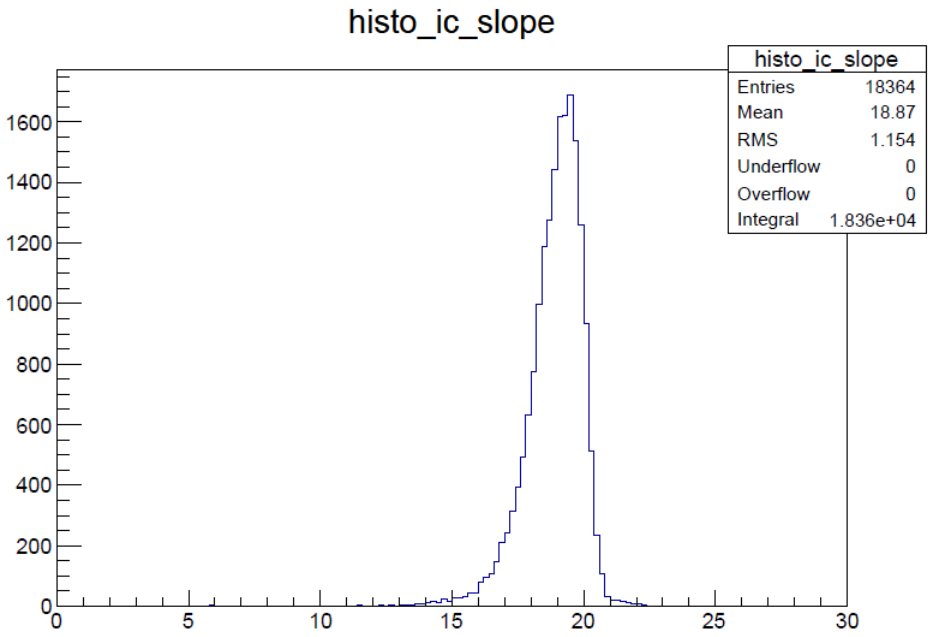






IC factor dLY and slope





IC factor dLY and slope

$0.9 < IC_{dLY}/Ic_{slope} < 1.1$