

Inter-calibration
slope and dLY
bug fixed

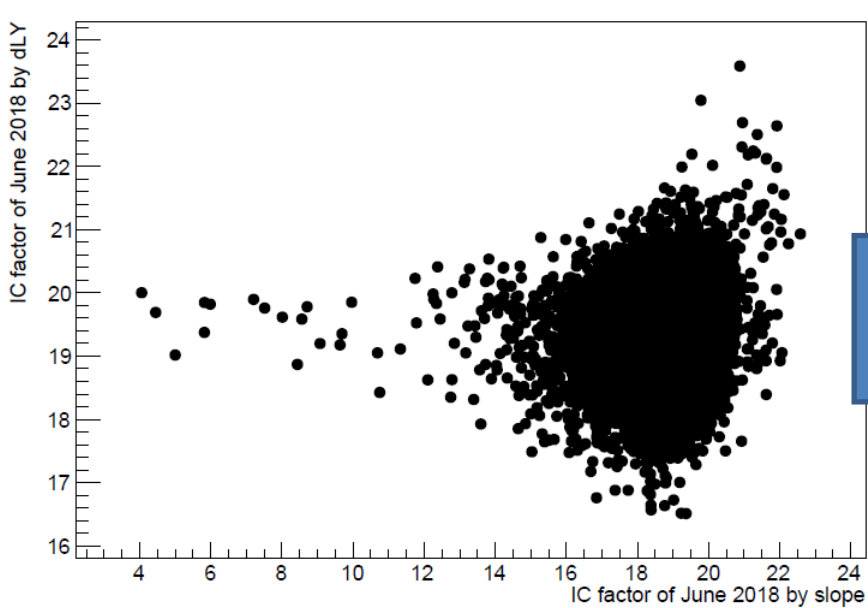
22.08.2018

AHCAL analysis workshop at Tokyo

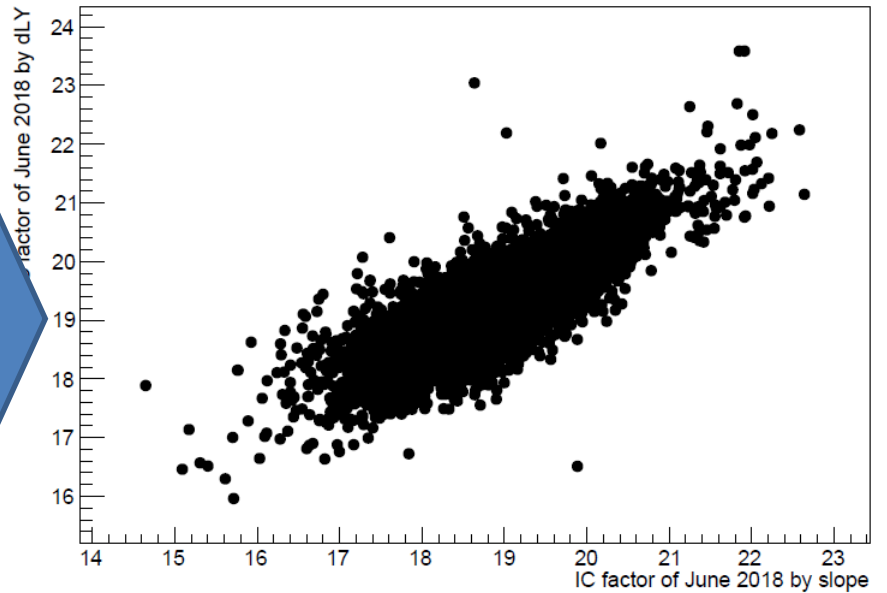
Yuji Sudo (DESY)

IC factor dLY vs Slope

before



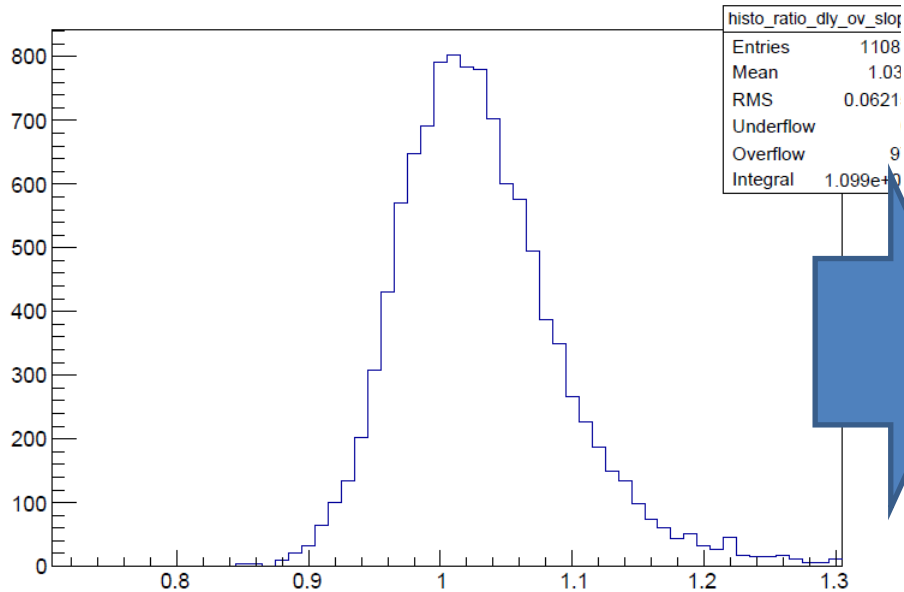
bug fixed



ratio of IC factor IC_{dLY}/IC_{slope}

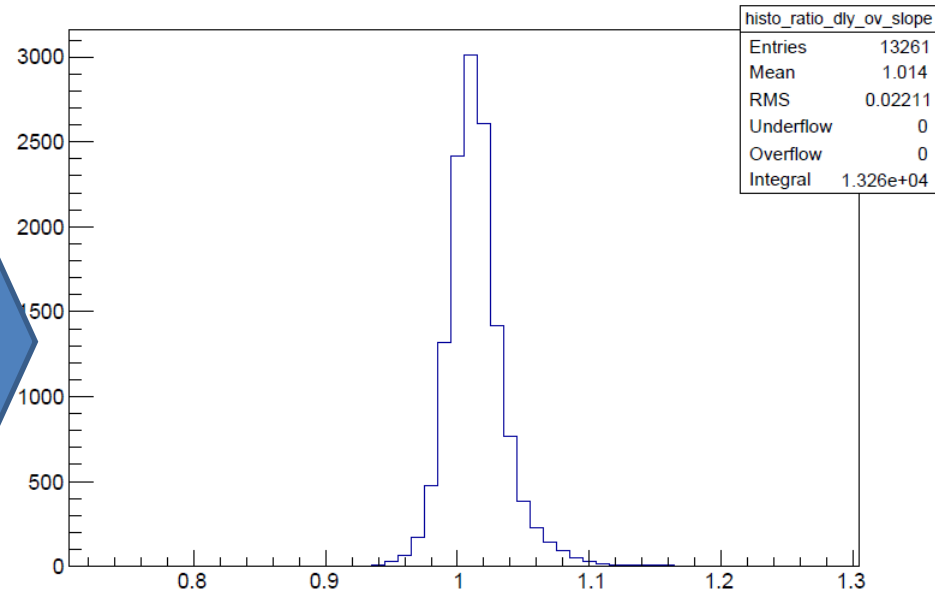
before

histo_ratio_dly_ov_slope



bug fixed

histo_ratio_dly_ov_slope

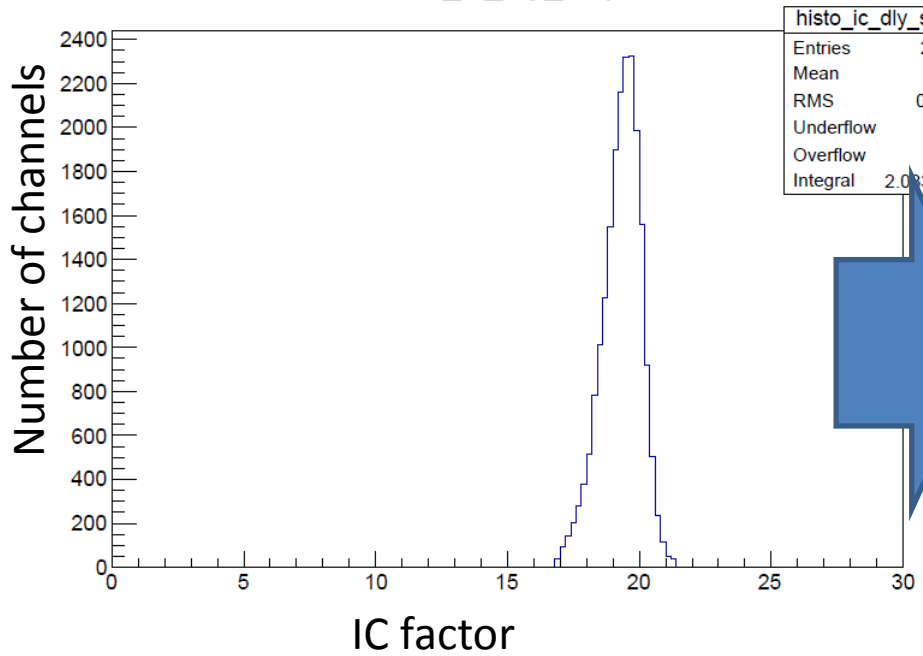


IC factor extracted by dLY and slope

1. fill IC value extracted by dLY within mean $\pm 3 \times \text{rms}$ of IC histogram of dLY on p.8
2. fill IC value extracted by slope within mean $\pm 3 \times \text{rms}$ of IC histogram of slope on p.8 if a IC value is not filled by first step.

before

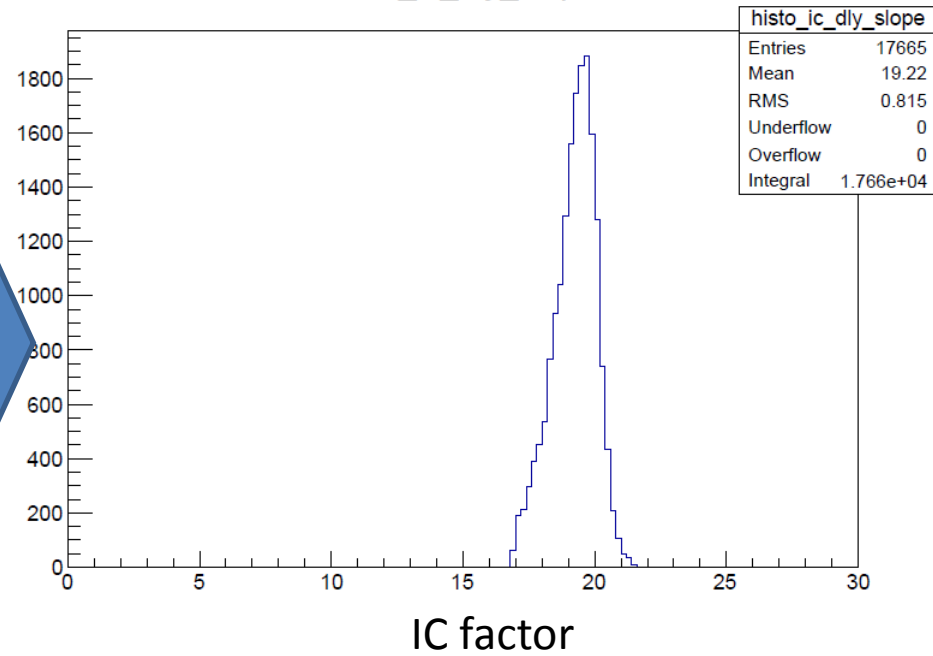
histo_ic_dly_slope



more than 90% channels

bug fixed

histo_ic_dly_slope



~80% of channels

backup

HG vs LG

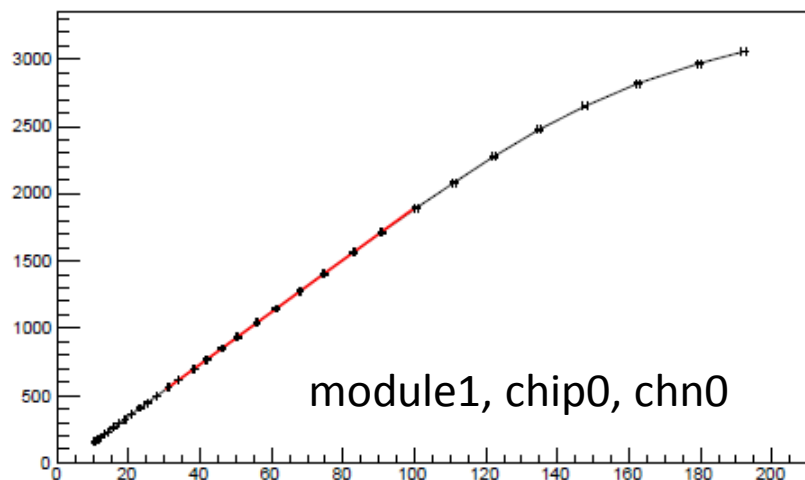
after pedestal subtraction

fitting range $30 < LG < 100$

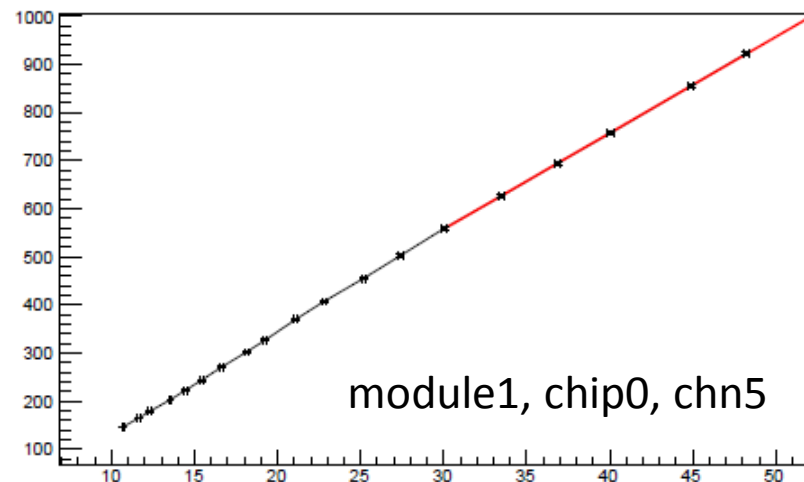
total amount of charge in a chip < 60000 ADC (HG)

at least 5 points in the fitting range

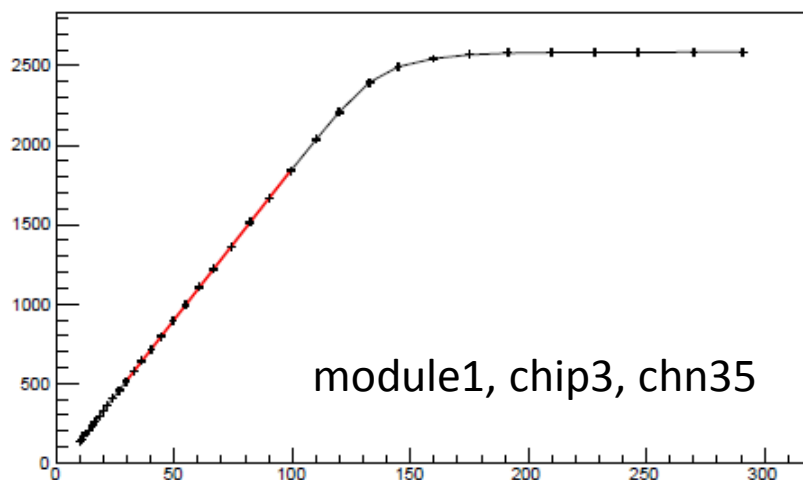
graph_IC_module1_chip0_chn0



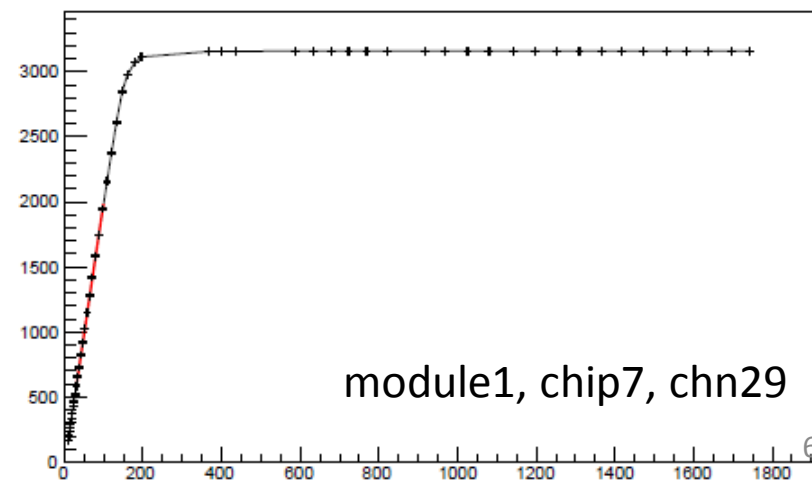
graph_IC_module1_chip0_chn5



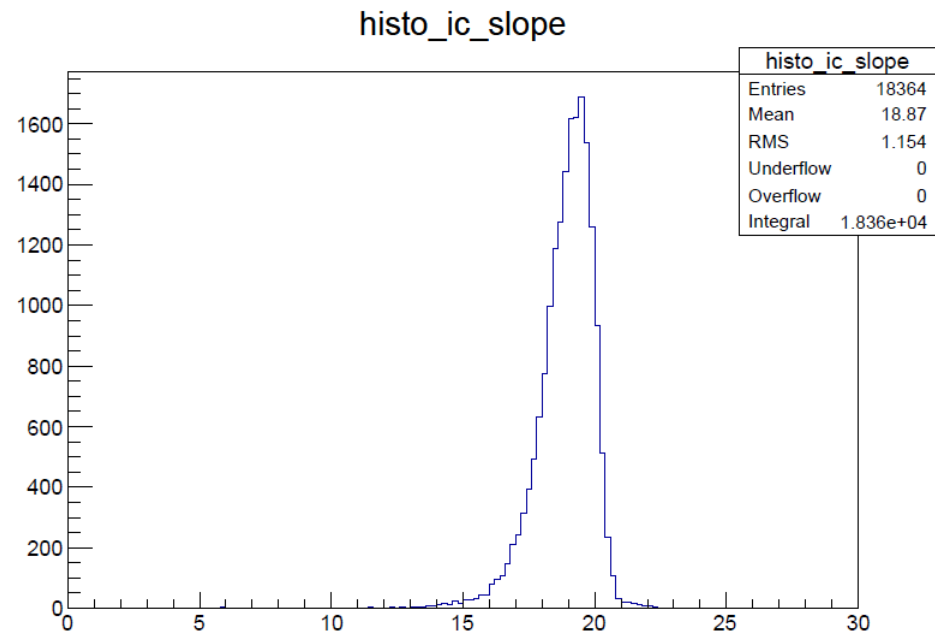
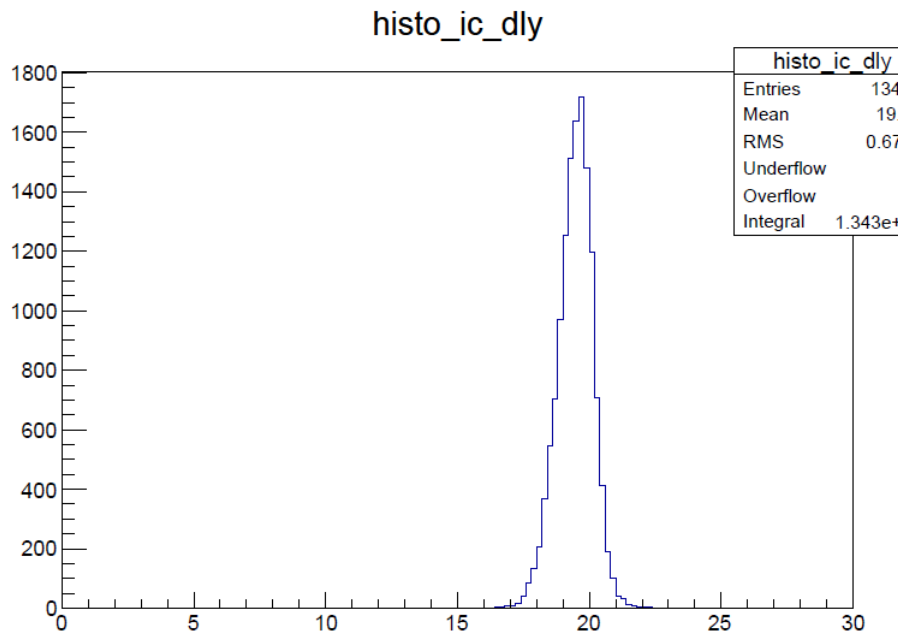
graph_IC_module1_chip3_chn35



graph_IC_module1_chip7_chn29



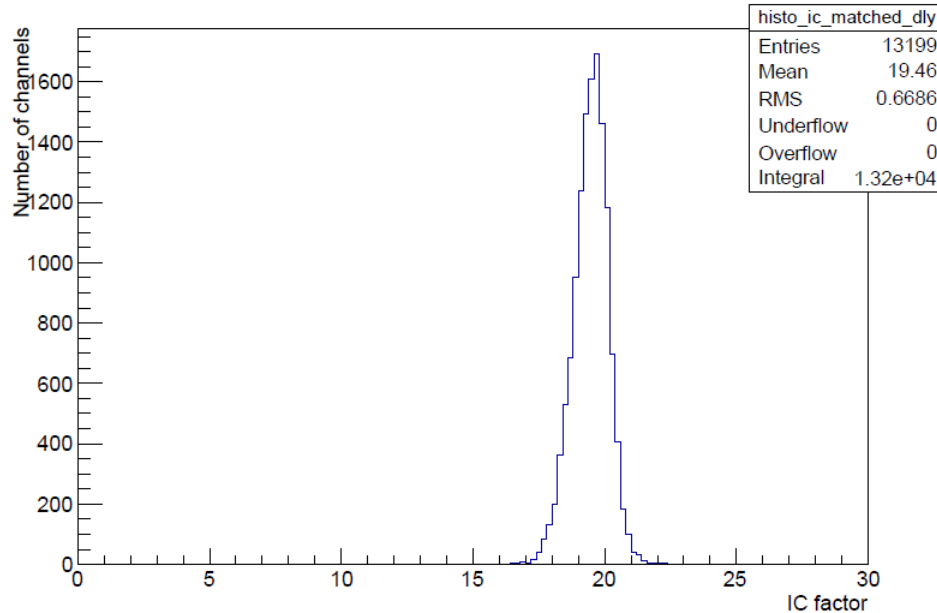
IC factor dLY and slope



IC factor dLY and slope

$$0.9 < IC_{dLY}/IC_{slope} < 1.1$$

histo_ic_matched_dly



histo_ic_matched_slope

