Temperature Compensation and HG/LG Inter-Calibration

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AHCAL Analysis Workshop at Tokyo

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Motivation of Temperature Compensation

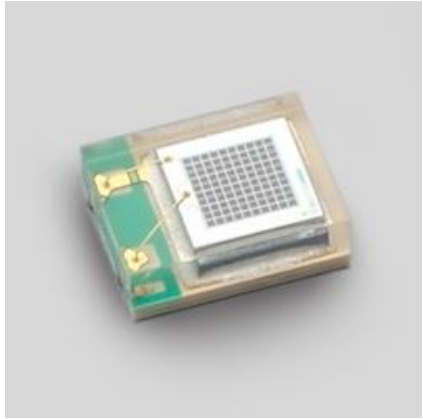
- SiPM gain depends on temperature. Because breakdown voltage depends on temperature.
  (large quenching resistor)

$$V_{ov} = V_{bias} - V_{break\ down}$$

- We want to keep gain (V_{ov})same as a value at reference point.
  Adjust bias voltage against temperature shift.

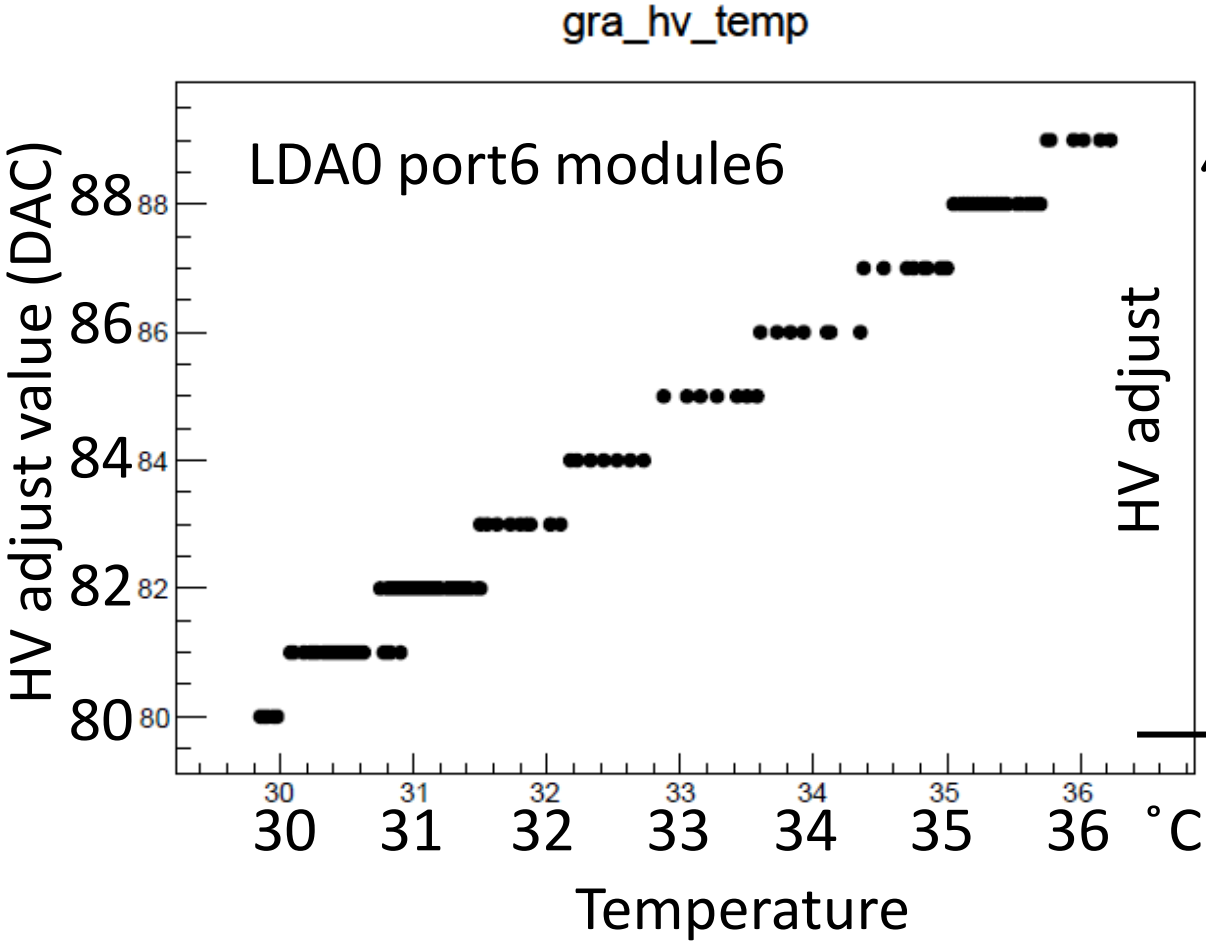
→temperature compensation by automatic HV adjustment

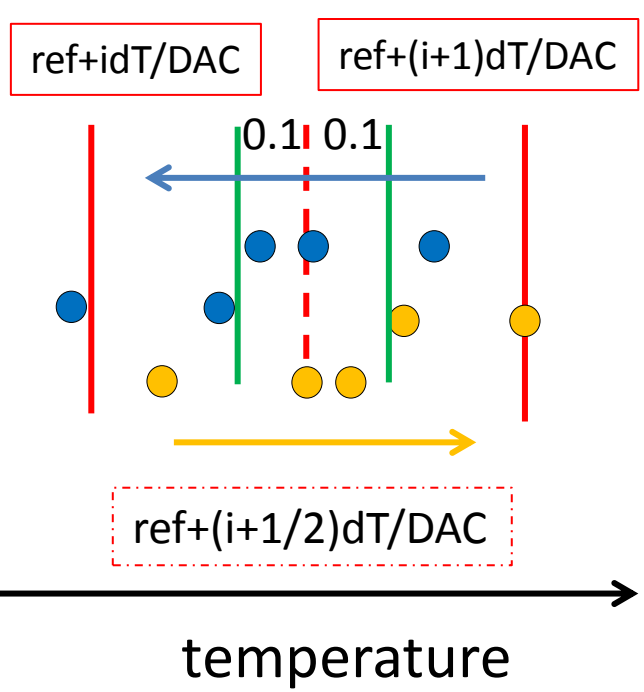
- dMIP/dV is ~1.1%/DAC
- dGain/dV of MPPC is ~ 0.6%/DAC



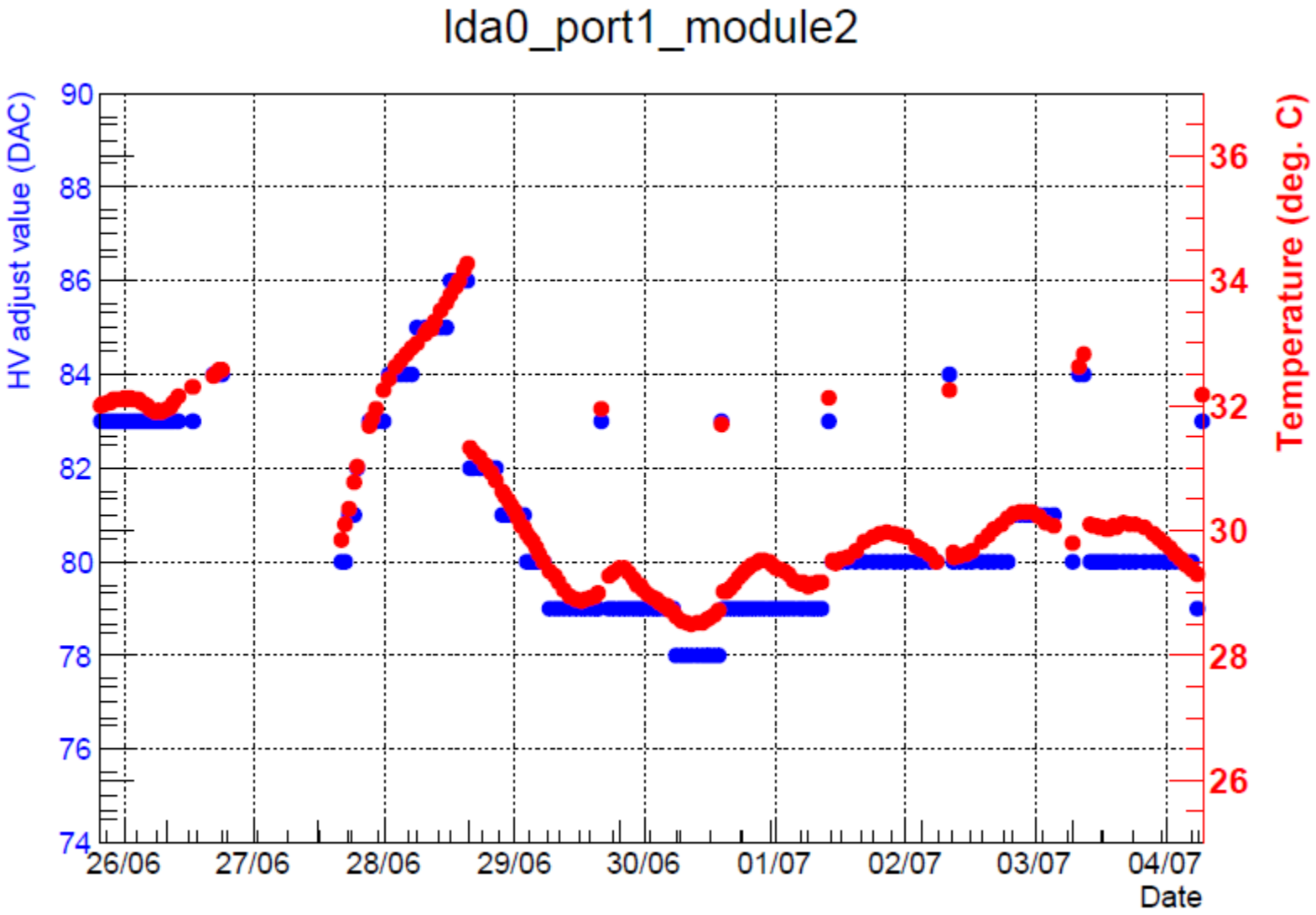
HV adjust vs Temperature

- 28th of June – 4th of July 2018
- There are over-lap of 0.2 degree C due to a hysteresis for stabilization at border

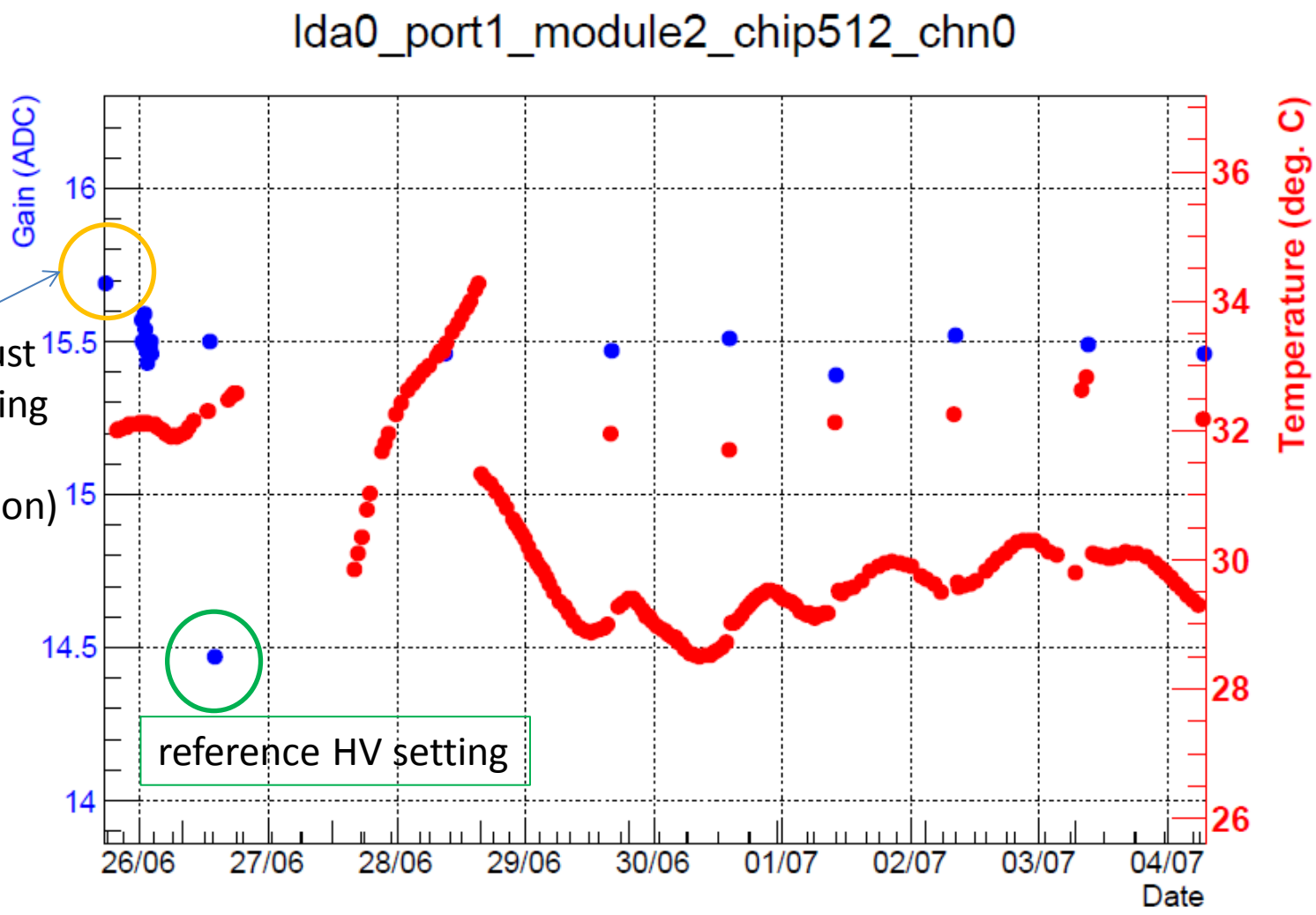




HV adjust value and Temperature vs Time

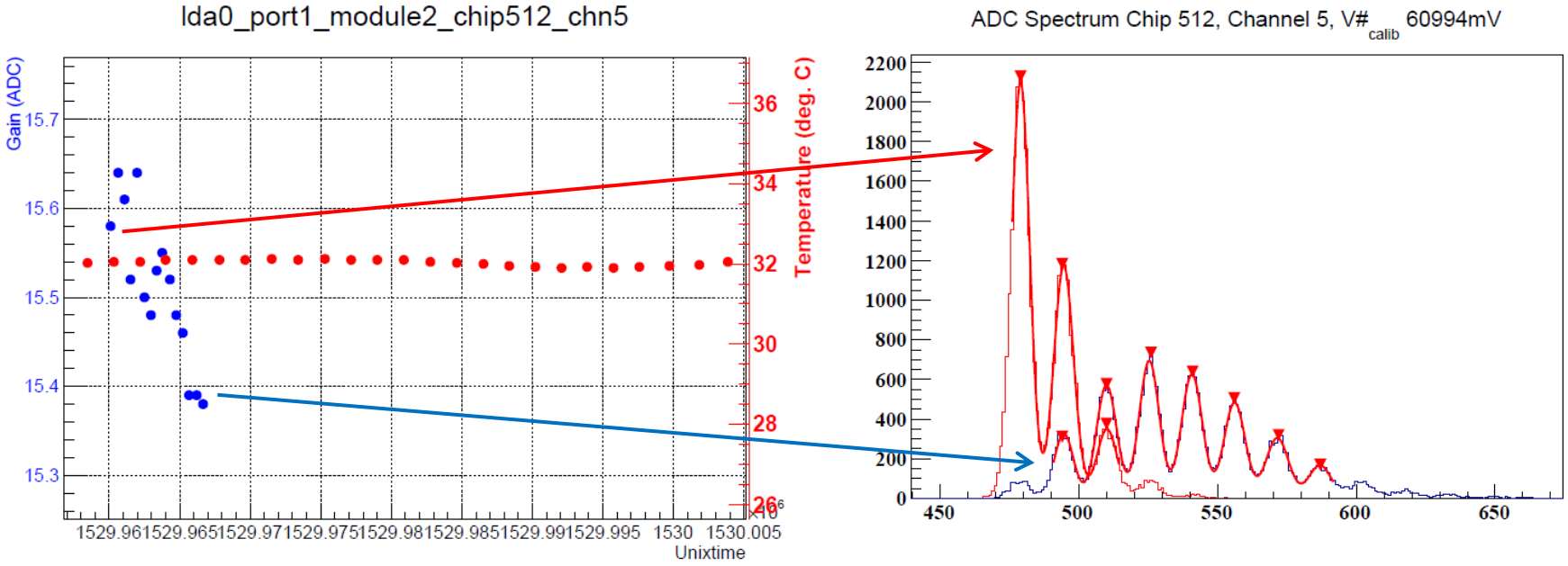


Gain and Temperature vs Time



no HV adjust (same setting as the last configuration)

LED V dependence on Gain?

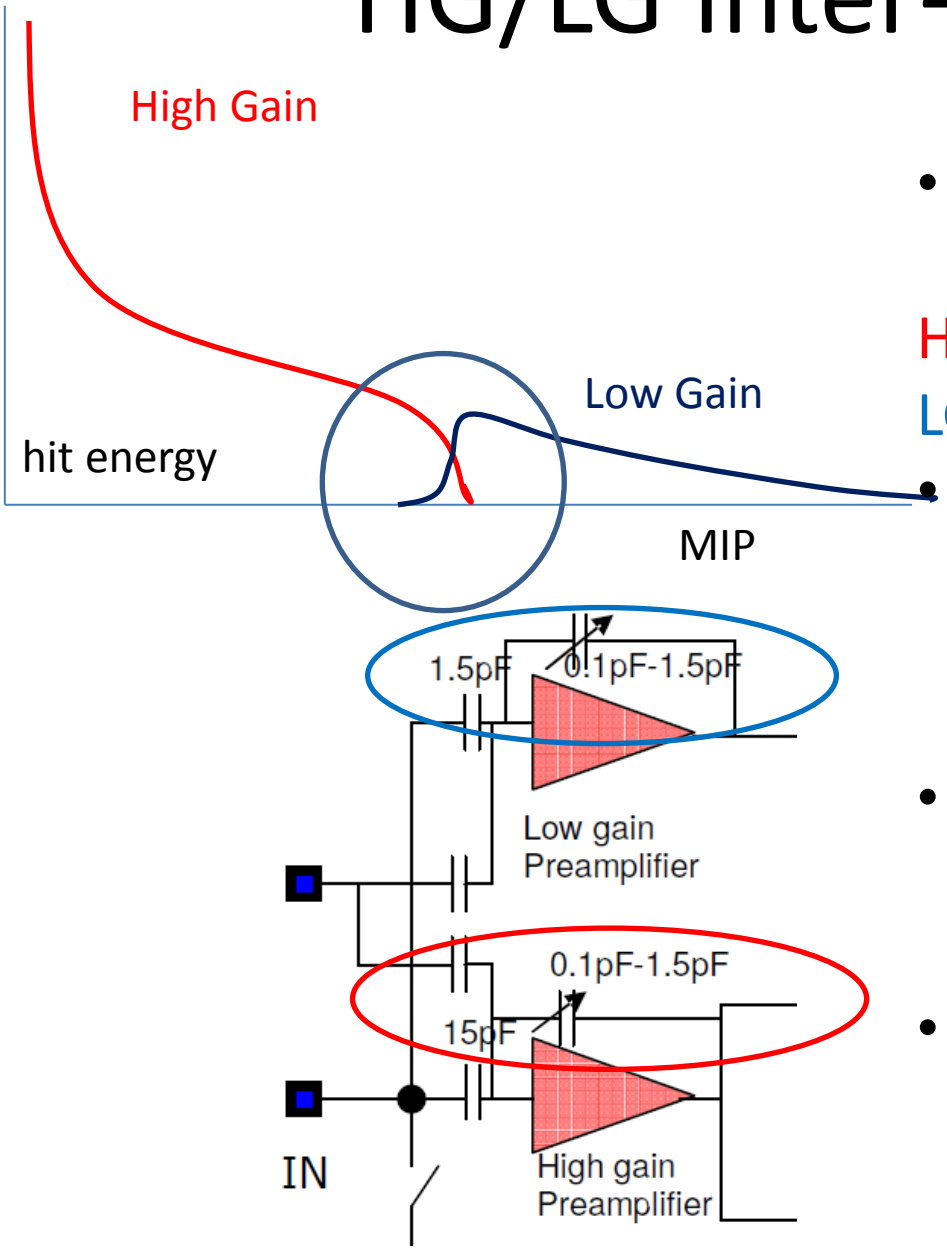


- Is there LED V (total amount of charge) dependence of Gain?
- same trend on many channels
- SPS looks O.K. for the first and the last measurement of point.

Summary 1

- Automatic HV adjustment on power board successfully works for the temperature compensation.
- There is a trend that gain is decreasing while LED V (total amount of charge in a chip) is increasing.
- Is there LED V (total amount of charge) dependence of Gain?

HG/LG Inter-Calibration



- SPIROC2B has 2 signal output lines. High Gain and Low Gain

HG -- small deposited energy hits

LG -- large deposited energy hits

- In principle, IC factor is constant and depends on ratio of capacitors because of the circuit design. (IC ~20 June 2018)
- In the real world, IC factor is different for each channel →IC for HG-LG is important
- After inter-calibration, HG and LG output should be connected smoothly

Methods to extract IC factor

LED runs

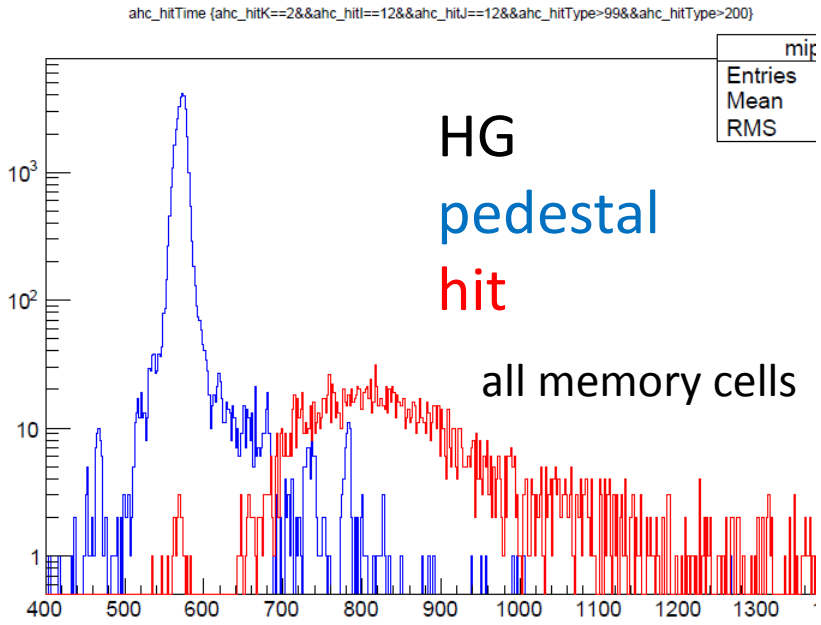
- slope of HG_ADC vs LG_ADC
- ΔHG_ADC/ Δ LG_ADC

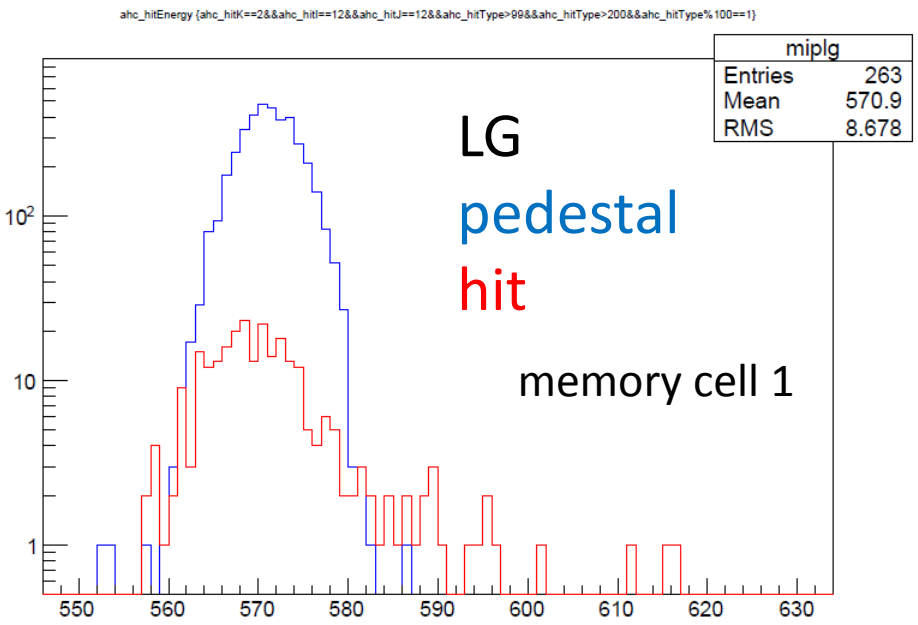
need more investigation

Beam runs

- Muon Run with IC mode (HG/LG)
  Pedestal shift with hit-bit?
- shower data – connect HG LG spectrum
  LG Pedestal is required

Muon Run with IC mode (HG/LG)
Pedestal shift with hit-bit?





IC factor from LED runs
dHG_ADC/dLG_ADC

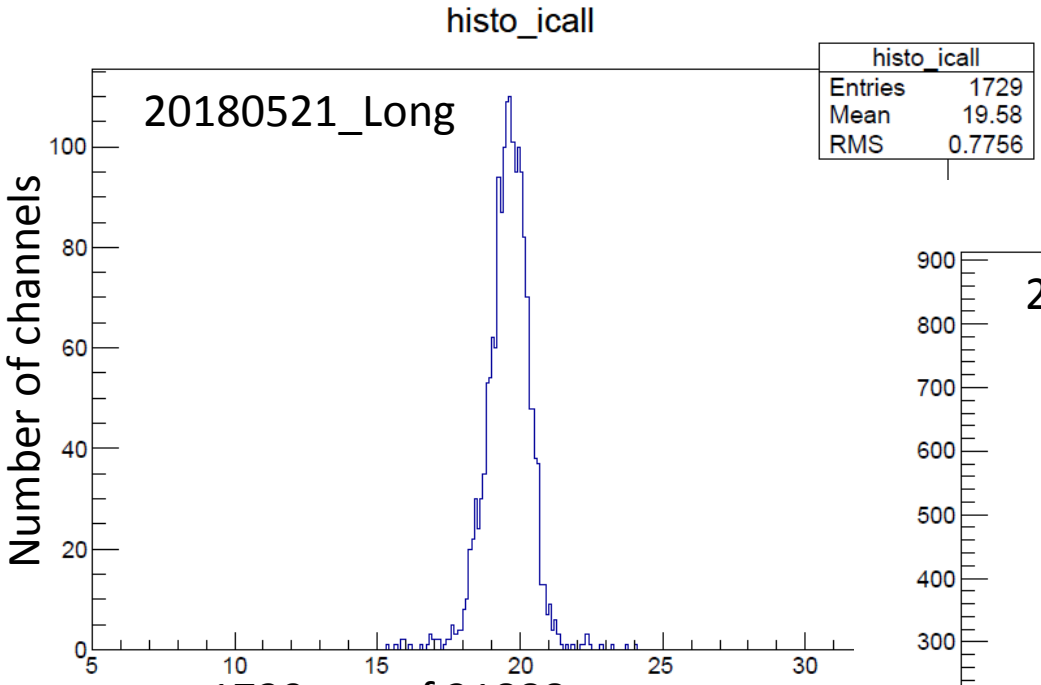
ΔLigit yield * HG_Gain = $(HG\_ADC_{i+1} - HG\_ADC_i)$
ΔLigit yield * LG_Gain = $(LG\_ADC_{i+1} - LG\_ADC_i)$

IC = HG_Gain/LG_Gain = $(HG\_ADC_{i+1} - HG\_ADC_i)/(LG\_ADC_{i+1} - LG\_ADC_i)$

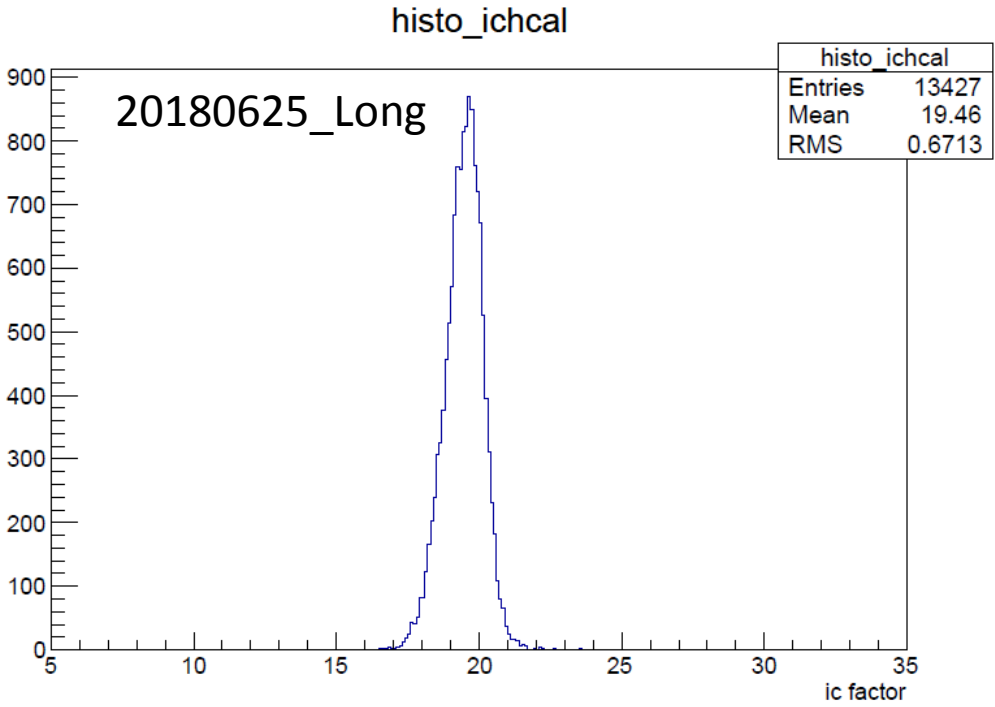
constraints

- $HG\_ADC_i > HG\_ADC_0$
- HG_ADC_i and $LG\_ADC_{i+1} > 10$
- HG_ADC_i and $HG\_ADC_{i+1} < 1500$
- $30 < LG\_ADC_{i+1} - LG\_ADC_{ped} < 100$
- total amount of charge in a chip < 60000
- $HG\_ADC_{i+1} - HG\_ADC_i > 100$
- HG_RMS_{i+1}-$HG\_RMS_i > 0$
- LG_RMS_{i+1}-$LG\_RMS_i > 0$

LED Run May and June 2018 LG1200



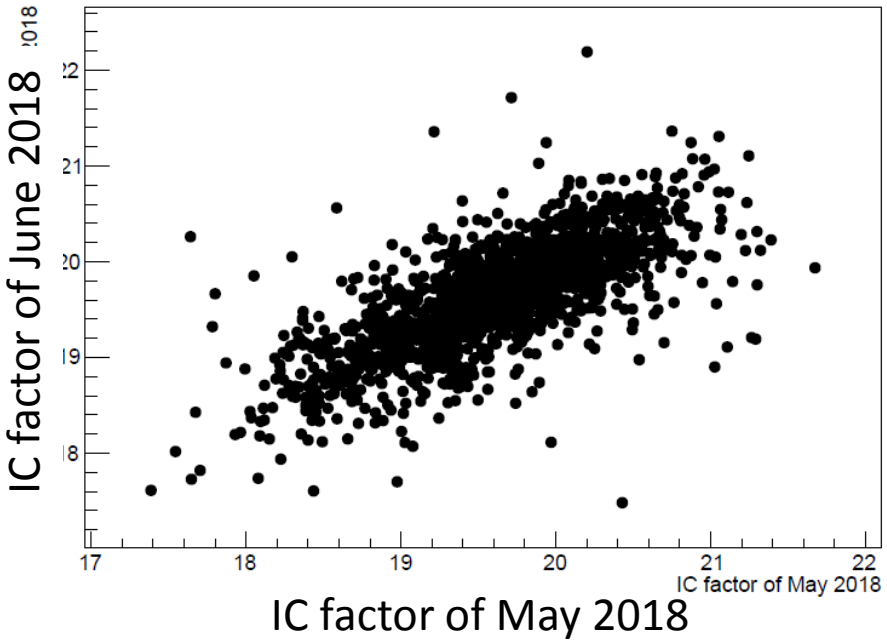
1729 out of 21888
5 sets of LED run for IC
(10+1 runs)

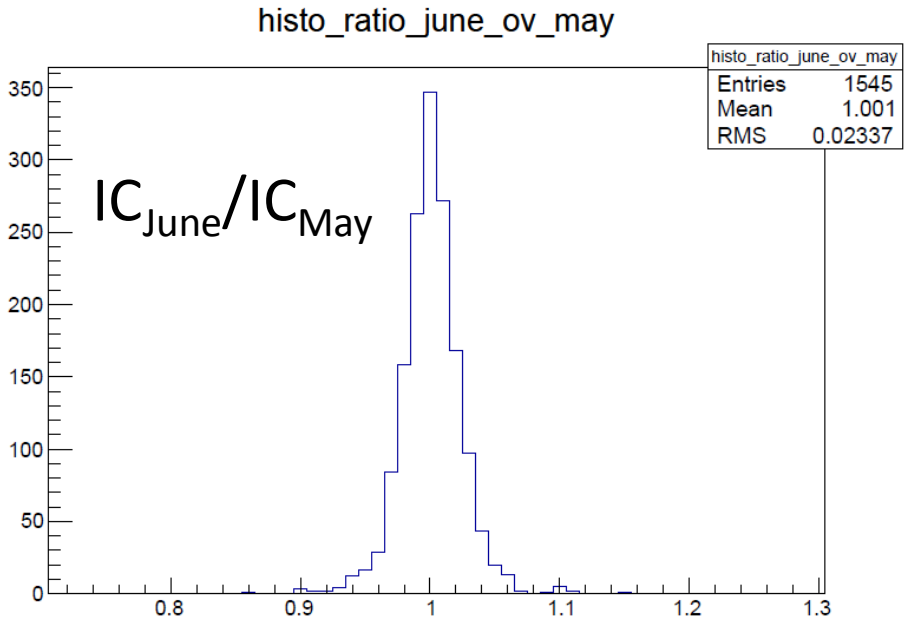


13427 out of 21888
101+1 runs

Comparing IC factor of June and May 2018

after reject outliers: range of plots is mean $\pm$ 3xRMS of IC histogram

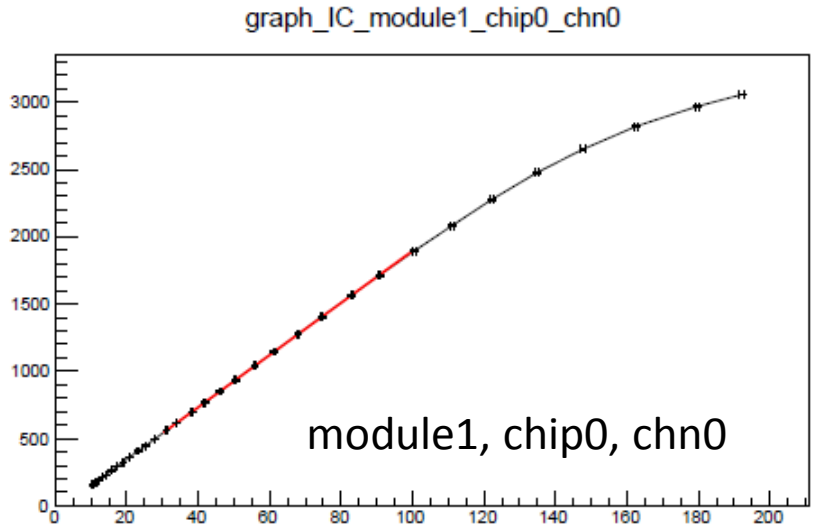


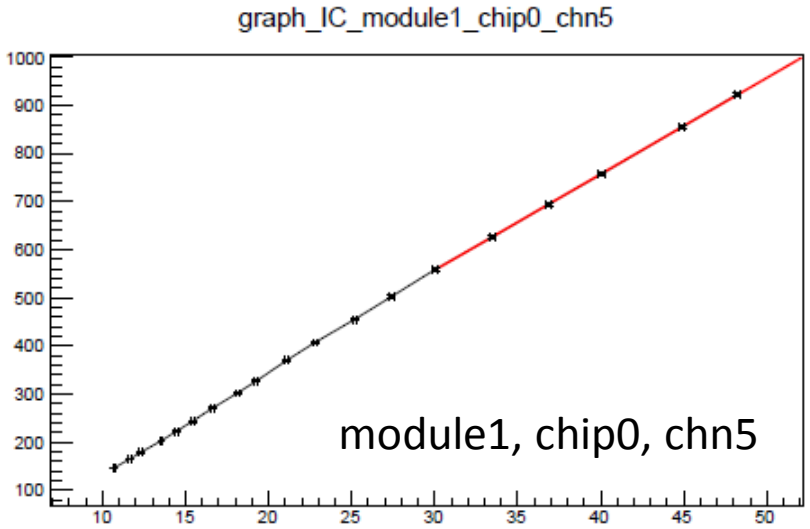


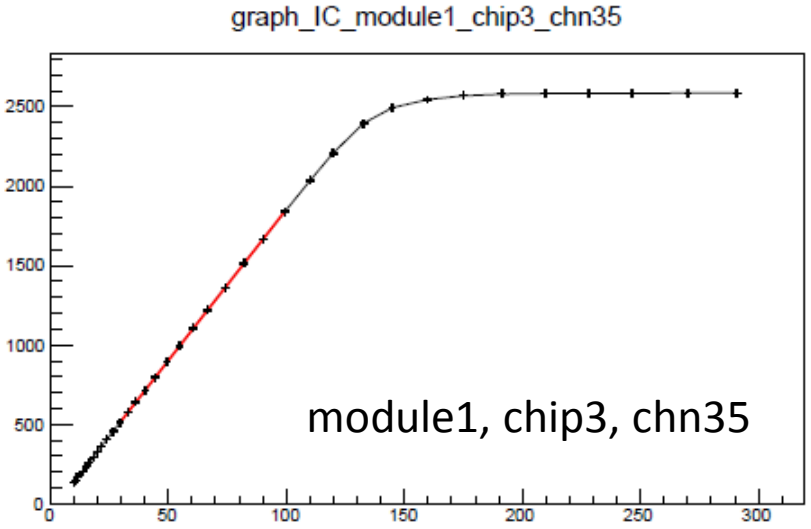
RMS of IC_{June}/IC_{May} is 2.3%

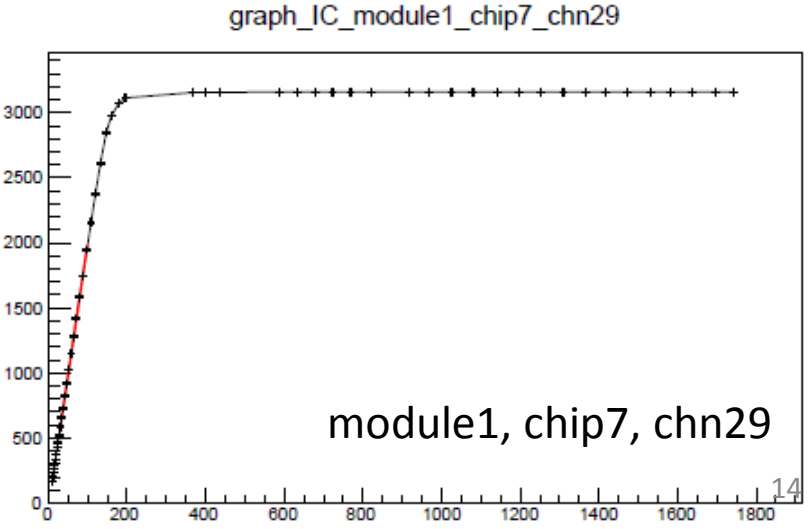
Slope of HG vs LG

after pedestal subtraction
fitting range 30 < LG < 100
total amount of charge in a chip < 60000 ADC (HG)
at least 5 points in the fitting range

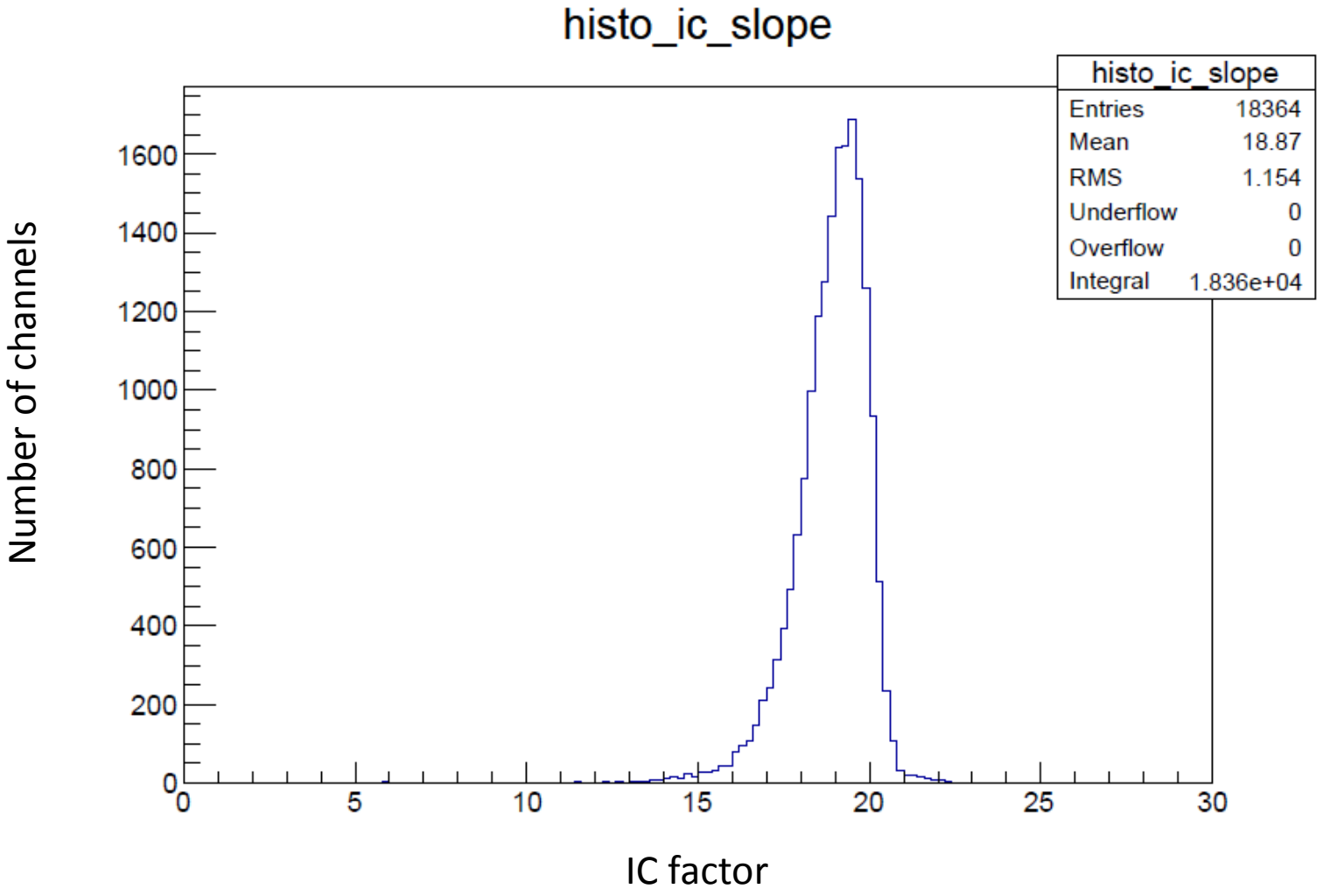






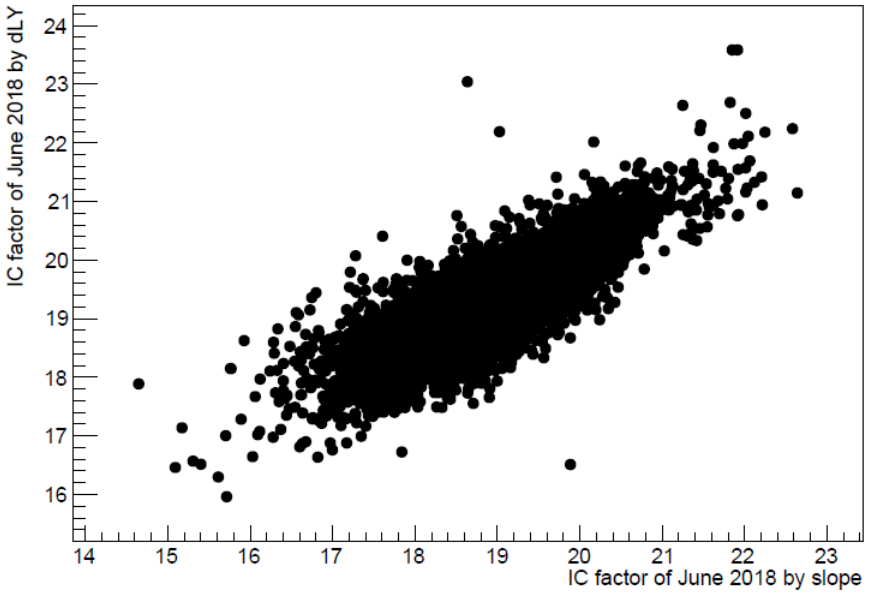


Slope of HG vs LG

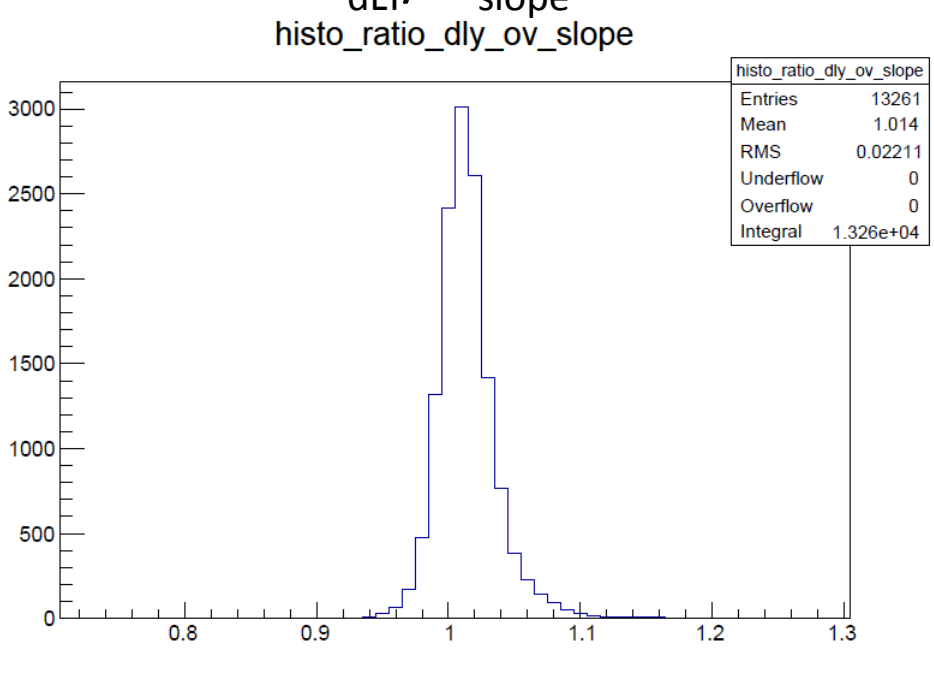


IC factor dLY vs Slope and IC_{dLY}/IC_{slope}

dLY vs Slope



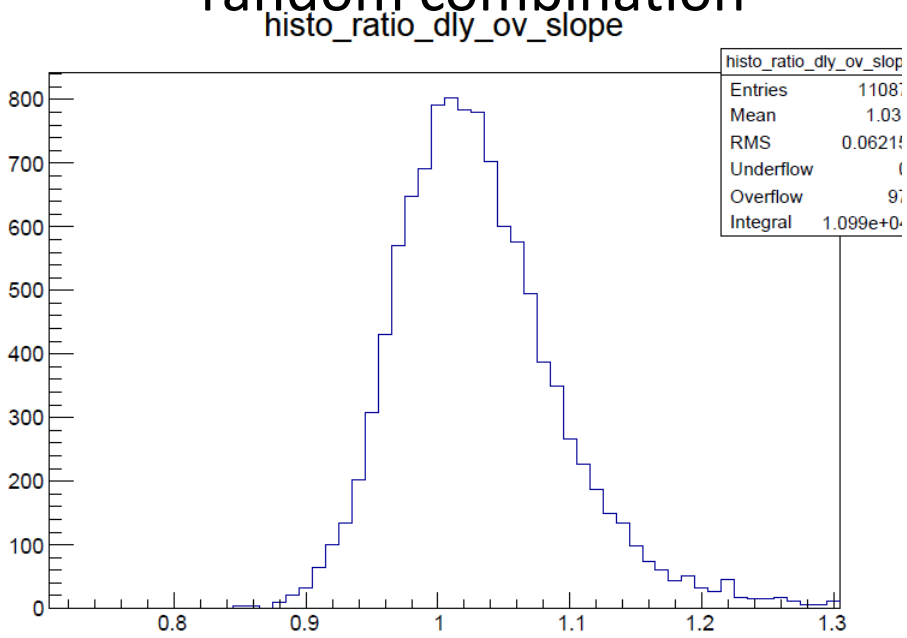
IC_{dLY}/IC_{slope}



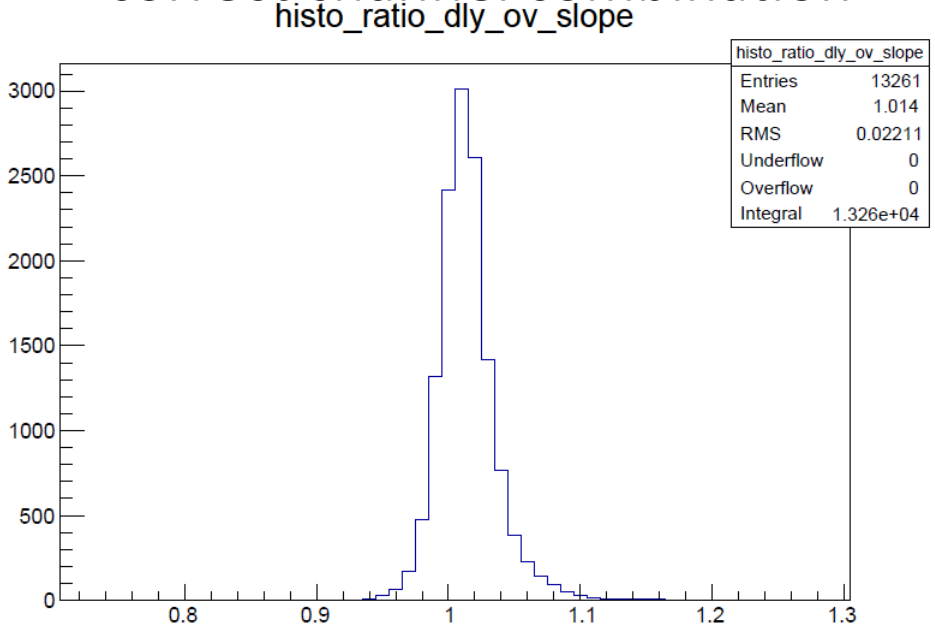
- Mean of IC_{dLY}/IC_{slope} 1.014 → 1.4% systematic shift
- RMS = 0.022

IC factor dLY vs Slope and IC_{dLY}/IC_{slope}

IC_{dLY}/IC_{slope}
random combination



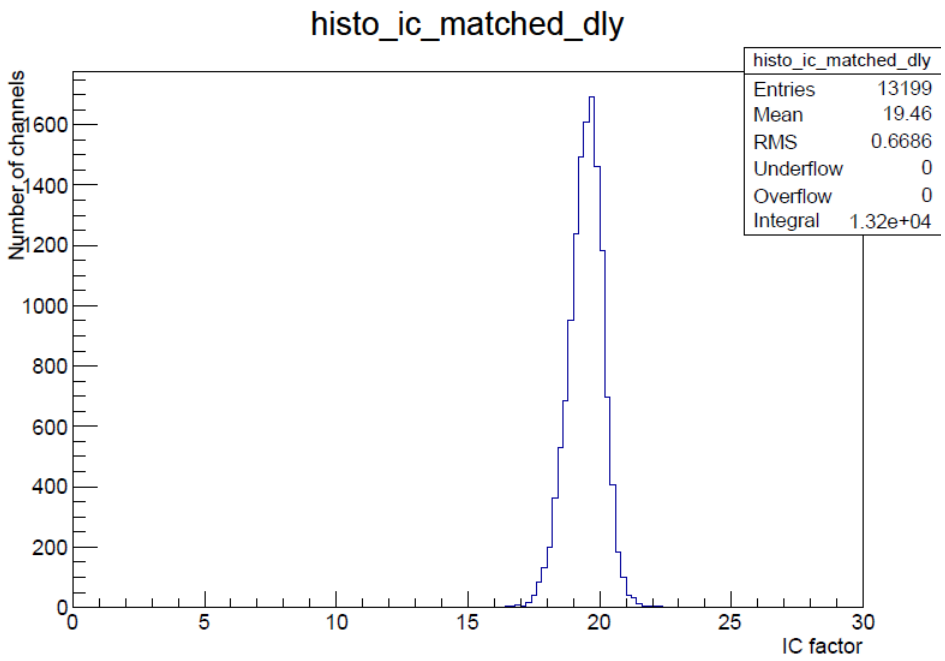
IC_{dLY}/IC_{slope}
correct channel combination

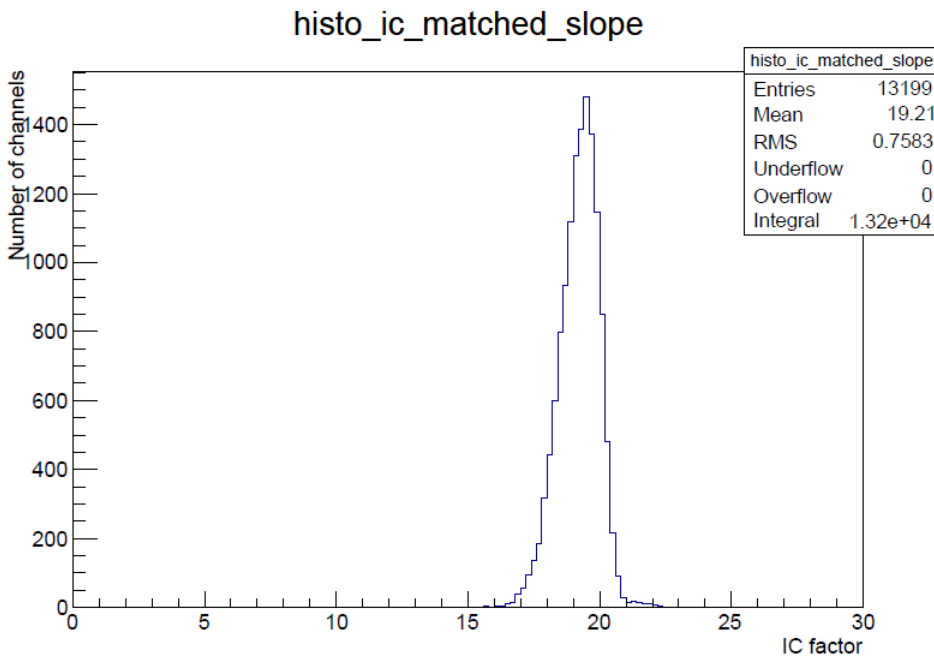


- RMS of IC_{dLY}/IC_{slope} with random combination ~6%
- channel by channel variation ~6%

IC factor dLY and slope

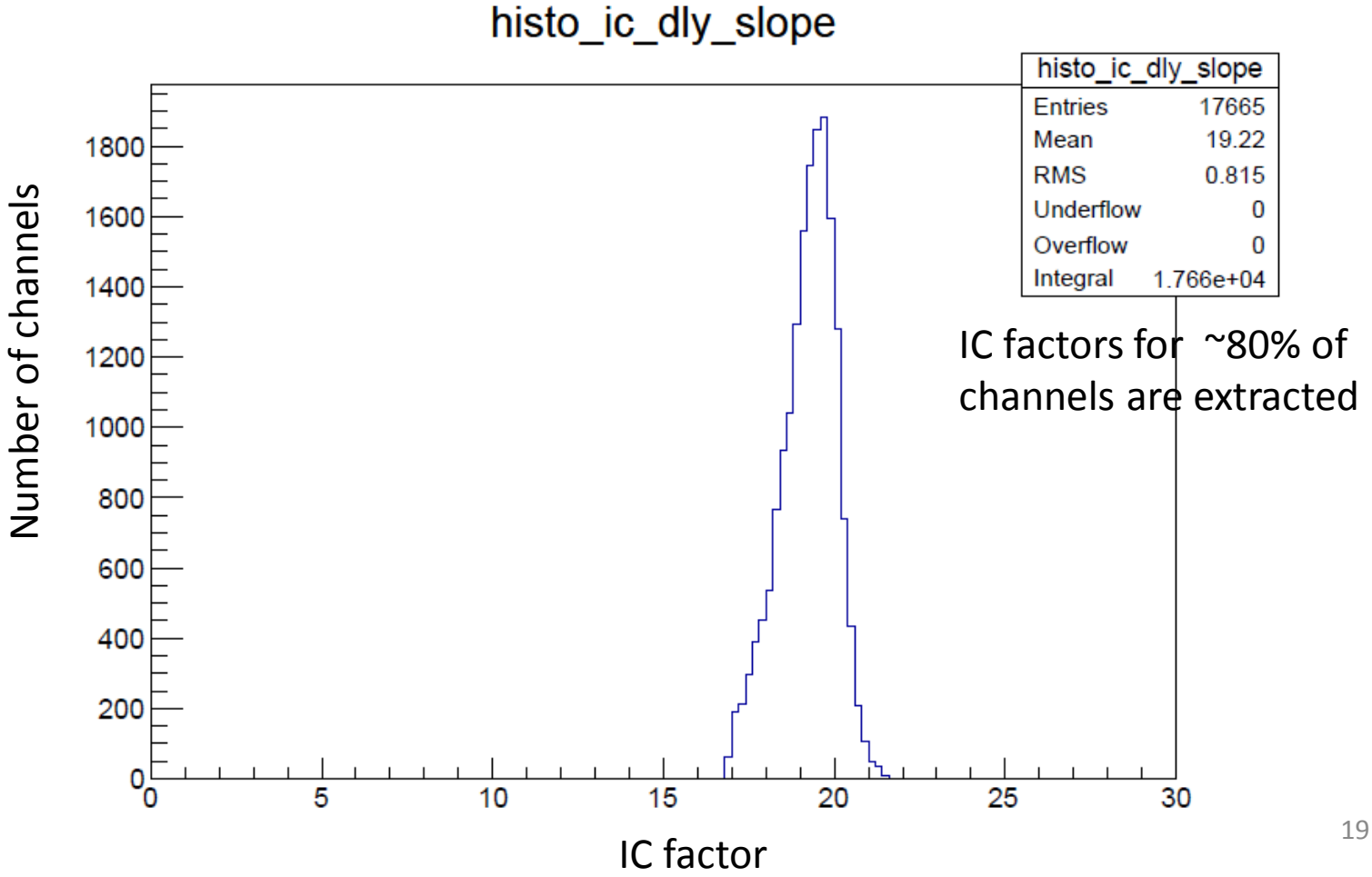
$0.9 < IC_{dLY}/Ic_{slope} < 1.1$





IC factor extracted by dLY and slope

1. fill IC value extracted by dLY within mean +/- 3*rms of IC histogram of dLY on p.18
2. fill IC value extracted by slope within mean +/- 3*rms of IC histogram of slope on p.18 if a IC value is not filled by first step.



IC factors for ~80% of channels are extracted

Summary 2

- no significant difference between slope and dLY methods
- channel by channel variation ~6%
- IC factor is extracted for 17665 channels by 2 methods

to do

- apply precise correction for slope
- Cleanup macros and adapt to latest softwares
- Documentation in confluence

need more investigation

Beam runs

- Muon Run with IC mode (HG/LG)
  Pedestal shift with hit-bit?
- shower data – connect HG LG spectrum
  LG Pedestal is required

Changes of Database

May 2018

- ahc2_ModuleConnection_180822 (38 layers)
- ahc2_ModuleLocationReference_180822 (38 layers)
- ahc2_HardwareConnection_180822 (38 layers)

June 2018

- ahc2_Intercalibration_180823

first IC factor w/o correction
module1-41:values from TB June 2018
module42: default value will be applied
module43-54: tail-catcher, values from TB July 2016
default value: 19.22

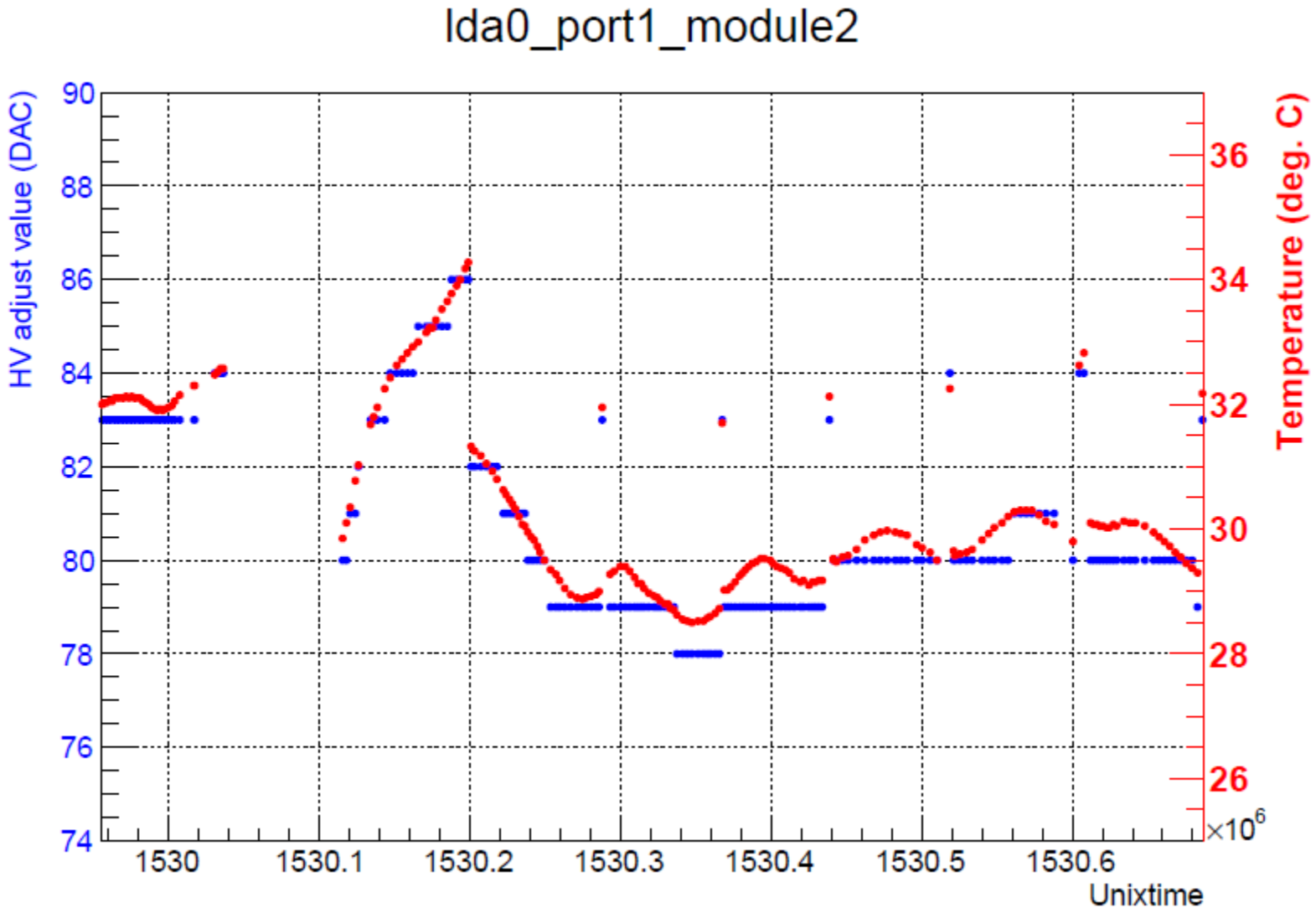
- ahc2_SaturationParameters_180822

MPPC 1.3x1.3 mm^2: 2934 (Npix*1.1)
2.0x2.0mm^2: 7040 (Npix*1.1)
SensL : 1300 (Aug. 2015 SPS)

backup

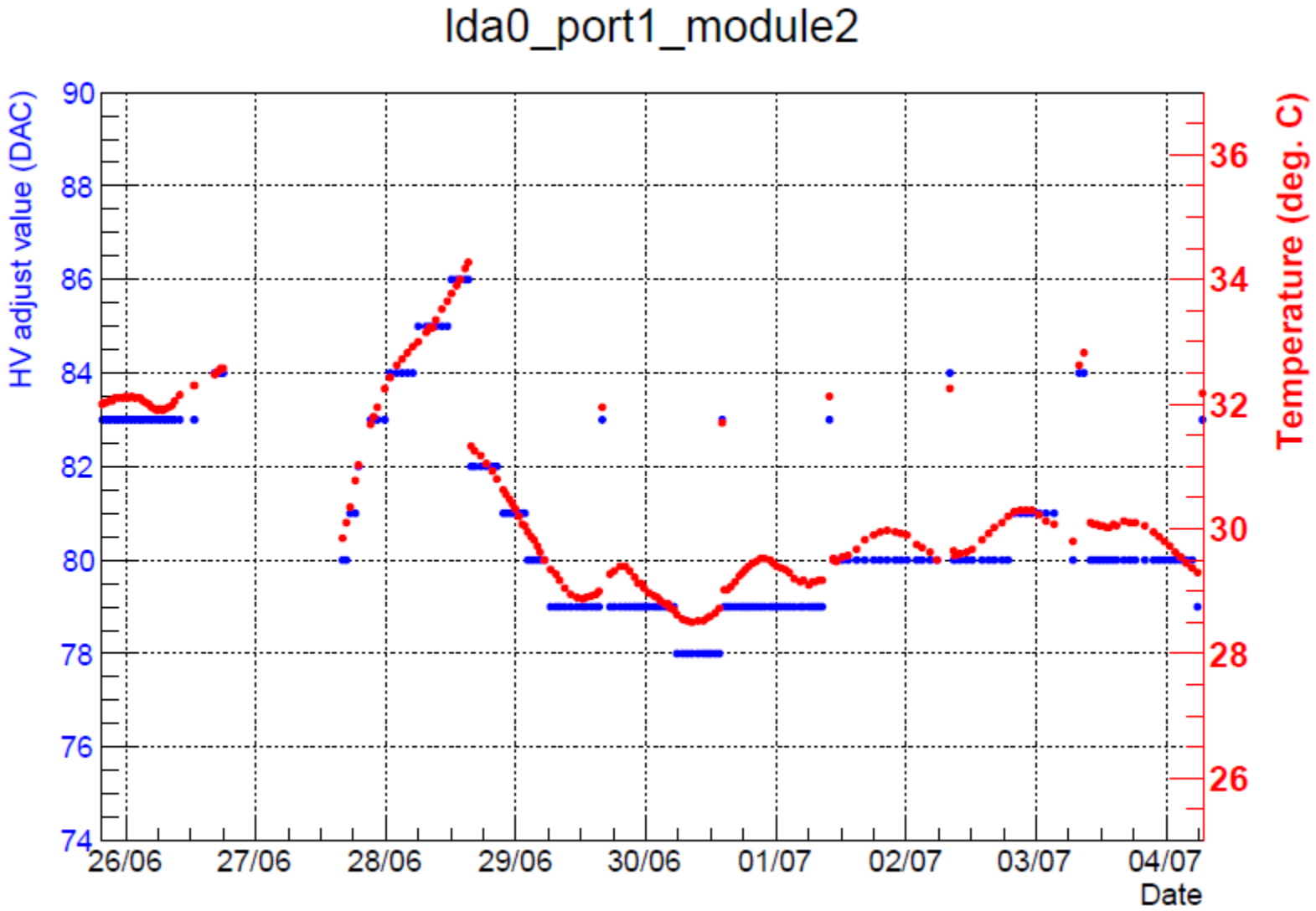
HV adjust value and Temperature vs Time

time in unixtime, red dots in front



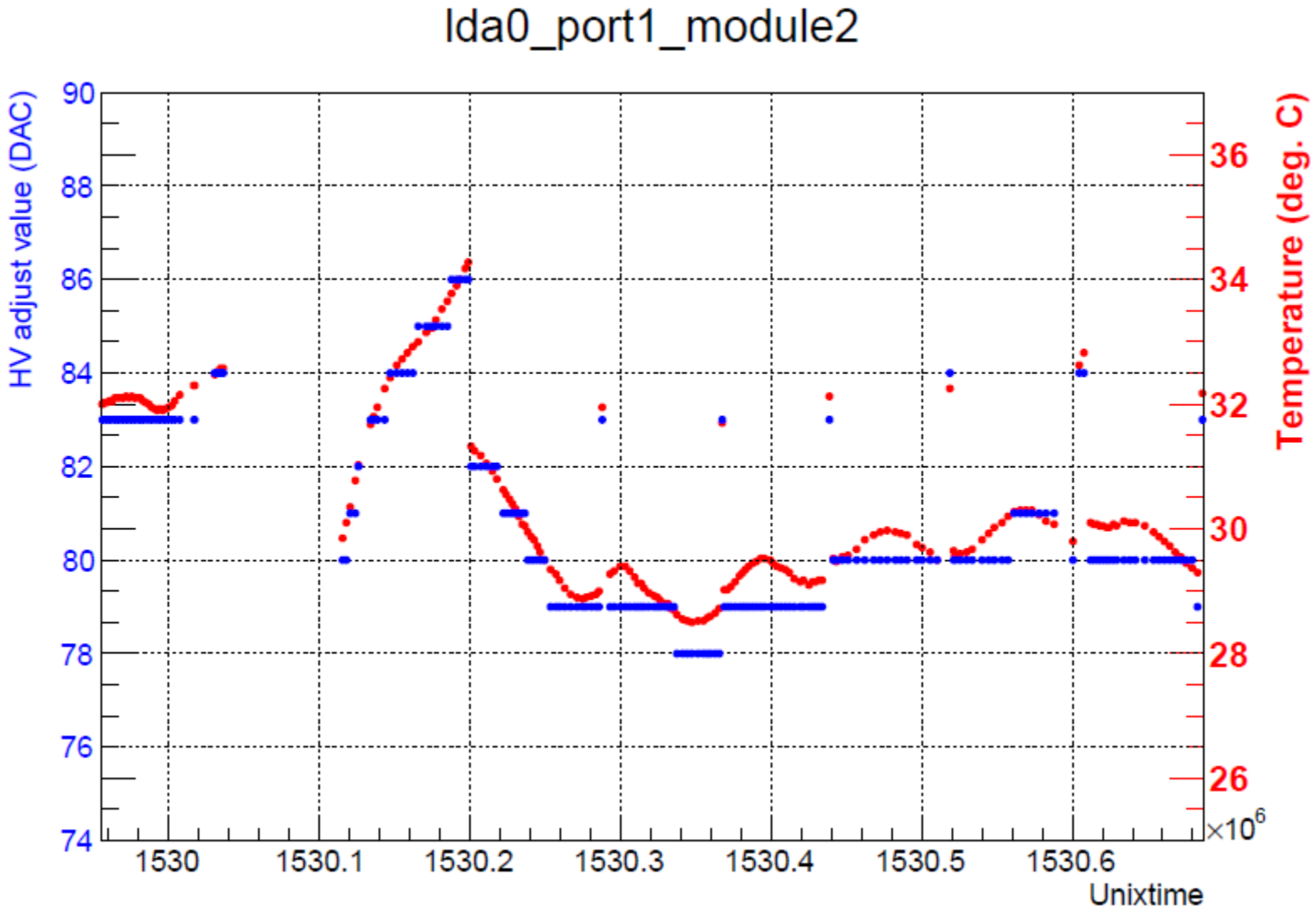
HV adjust value and Temperature vs Time

time in date, red dots in front



HV adjust value and Temperature vs Time

time in unixtime, blue dots in front



HV adjust value and Temperature vs Time

time in date, blue dots in front