ILCハドロンカロリメータの精細度の最適化に関する研究

Study on granularity optimization for ILD hadron calorimeter

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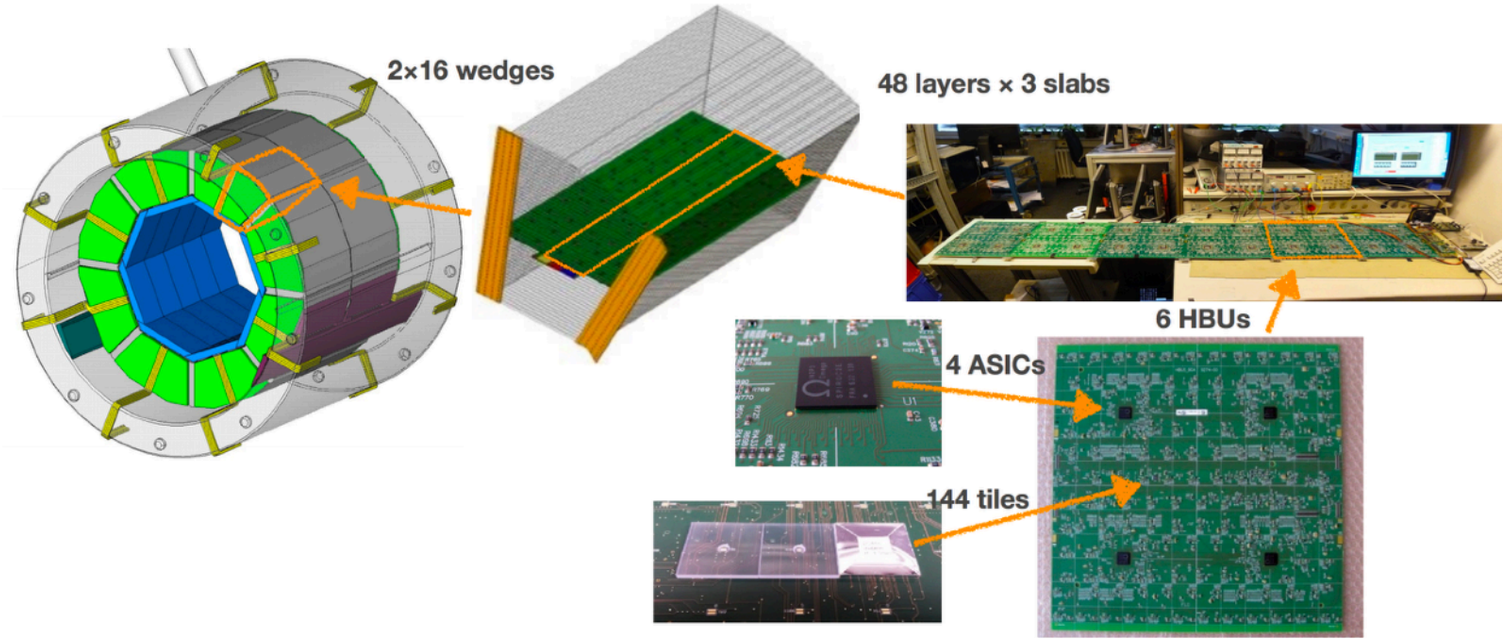
Summer Camp on ILC 2018

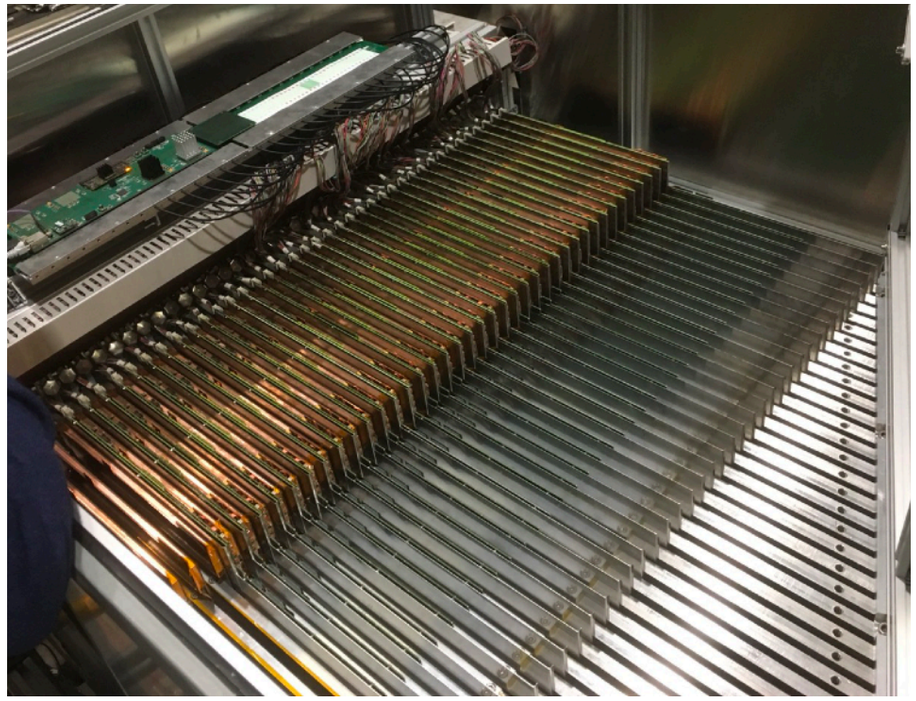
AHCAL (Analogue Hadron CALorimeter)

- 48 layers (scintillator active layer + steel/tungsten absorber layer)
- 8×10^6 scintillator tiles ($30\times30\times3mm^3$ each) readout by SiPM ($\sim1.3\times1.3mm^2$)
- International project
- Large technological prototype
  - 40 layers, 4 HBUs per layer
  - Use the same technology as foreseen in the full scale detector
  - Construction completed
  - **Test beam @CERN SPS in May and June 2018**

AHCAL overview



Large technological prototype

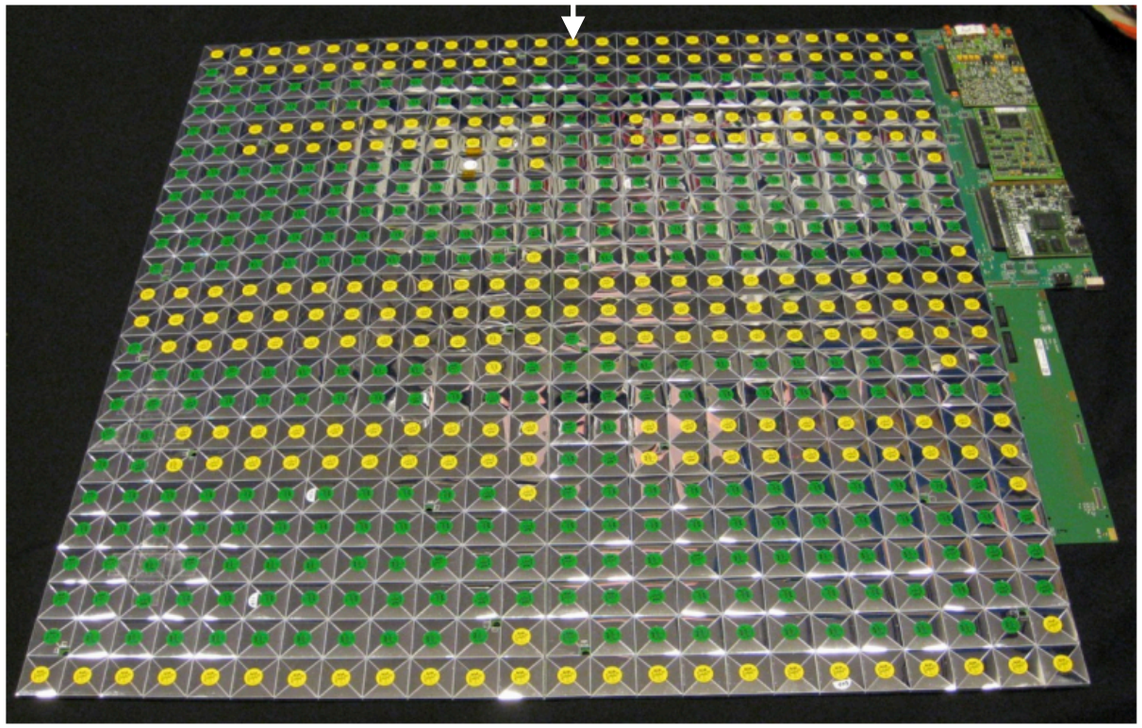


HBU(HCAL Base Unit) for large prototype

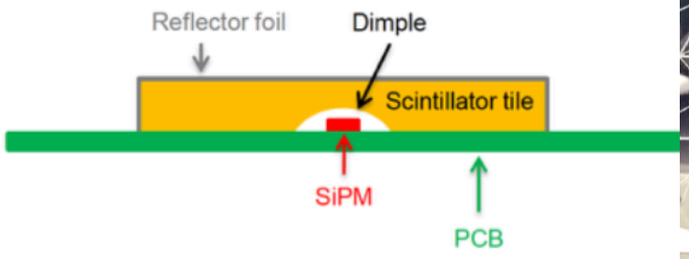
- 144 tiles (30×30×3mm^2) per one HBU, readout by SiPM (1.3×1.3mm^2)
- Each tile has a dimple for putting a SiPM.
- One LED for each tile for gain calibration.
- 160 HBUs (4 HBUs per layer) for large prototype

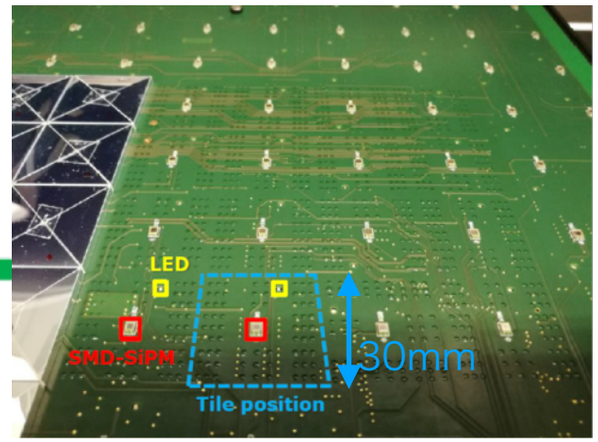
- Manufacturing process is almost automatized.
  - Production of PCB, tiles, reflectors, and tile wrapping, tile assembly

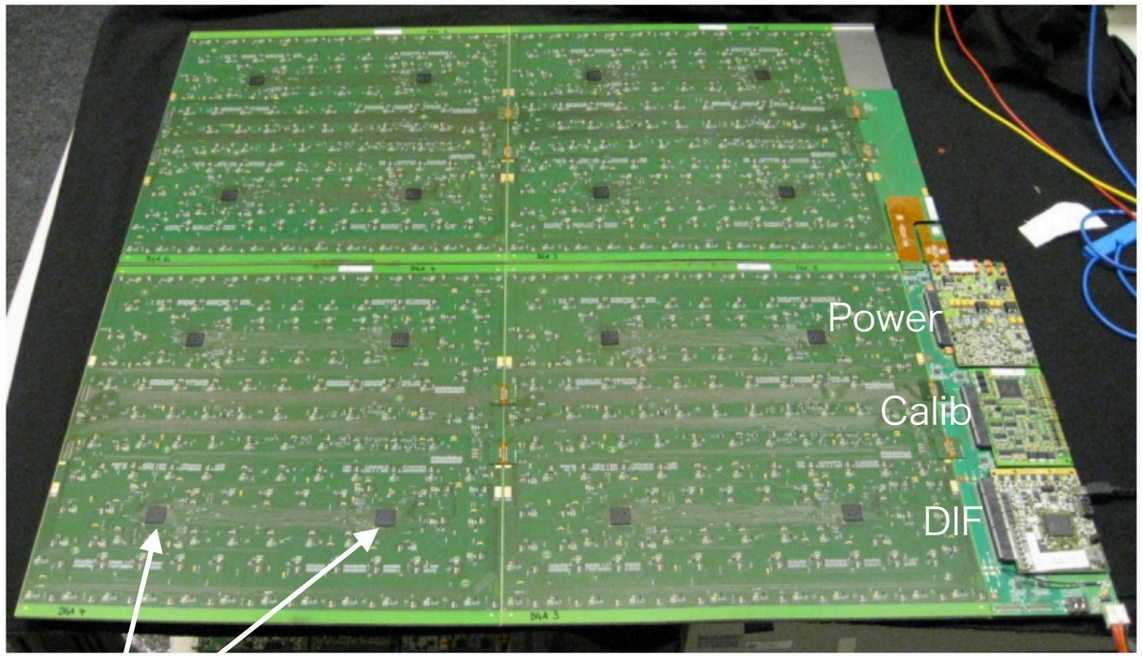
576×30mm-tiles assembled on 4 HBUs



HBUs assembled with 30mm tiles







HBUs at ASIC side

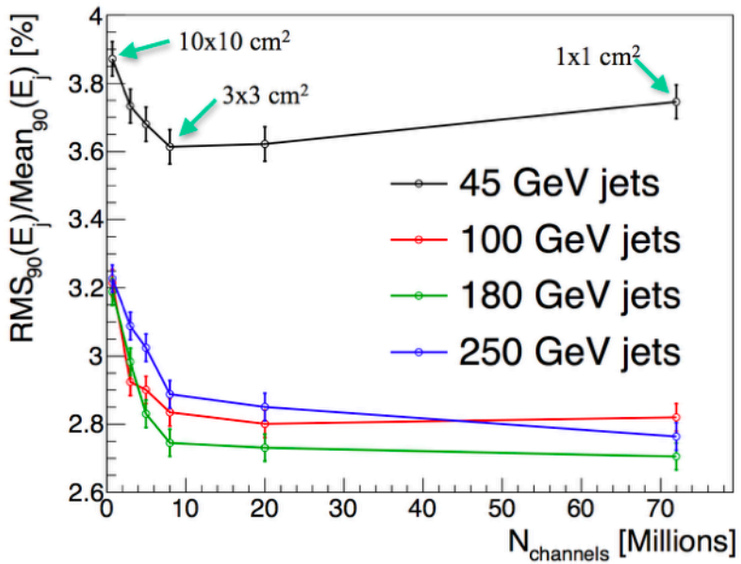
Motivation of this study

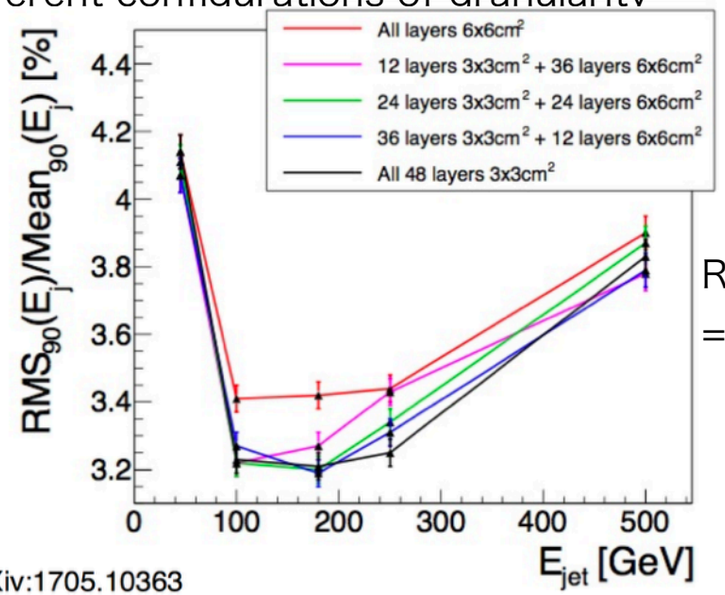
- Toward the construction of ILC, it is necessary to make a more realistic design of ILD detector.
- Granularity of AHCAL is revisited.
- Possibility of mixed granularity with larger scintillator tile at outer layers is under study.
  - We can reduce the number of readout channels, and thus reduce cost.
- Previous studies showed that 30mm x 30mm tile can be replaced with 60mm x 60mm tile at least up to latter half of layers without significant performance degradation.

↓

- The performance of the larger tile than 30mm square has been tested.
  - Light yield : (60mm^2) 18.2 p.e. (30mm^2) 43.1 p.e.
  - Excellent uniformity in tile response at 60mm^2 tile

Jet energy resolutions expected for different configurations of granularity



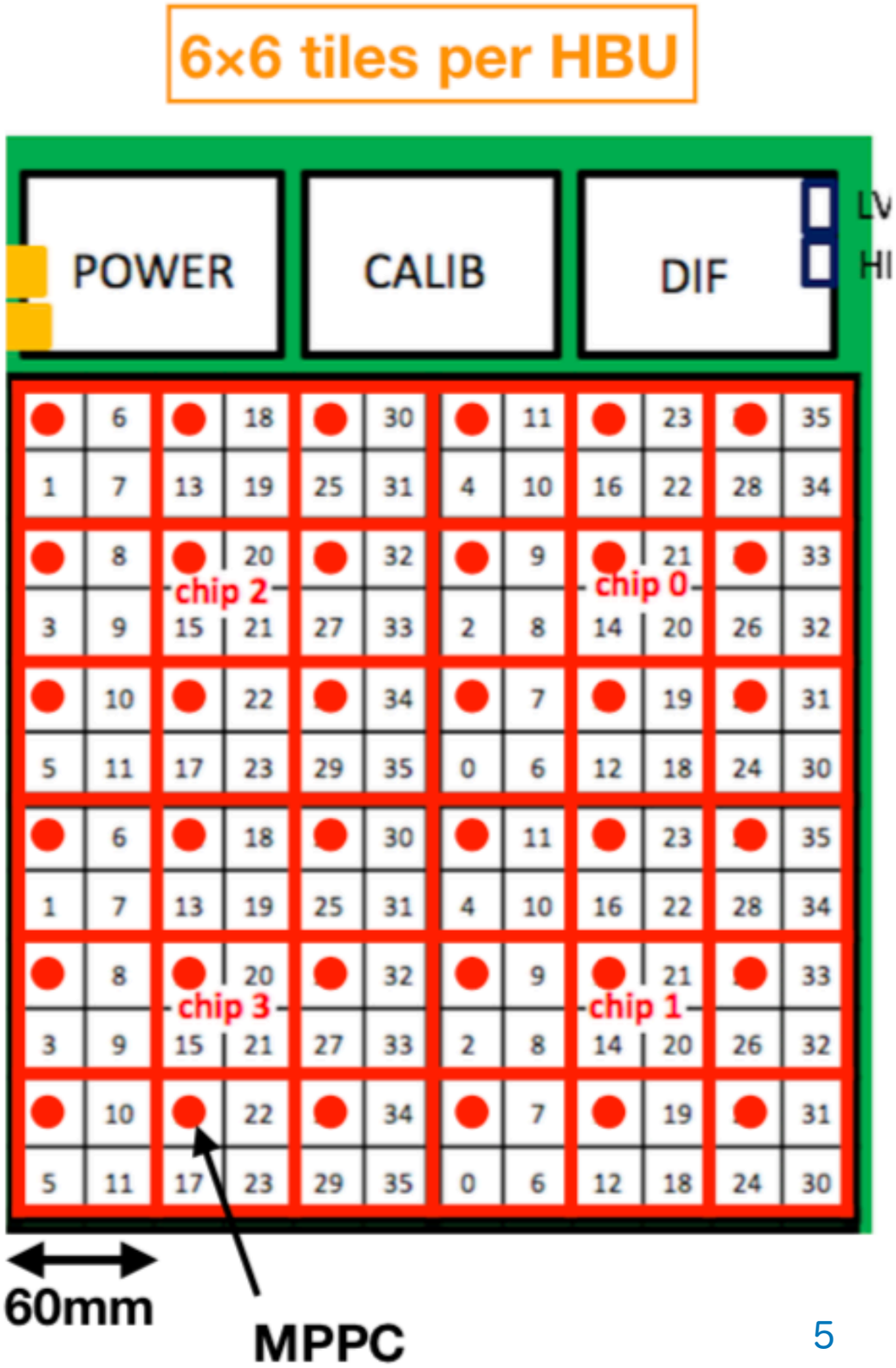


arXiv:1705.10363

RMS(Ej)/Mean(Ej)
=Jet energy resolution

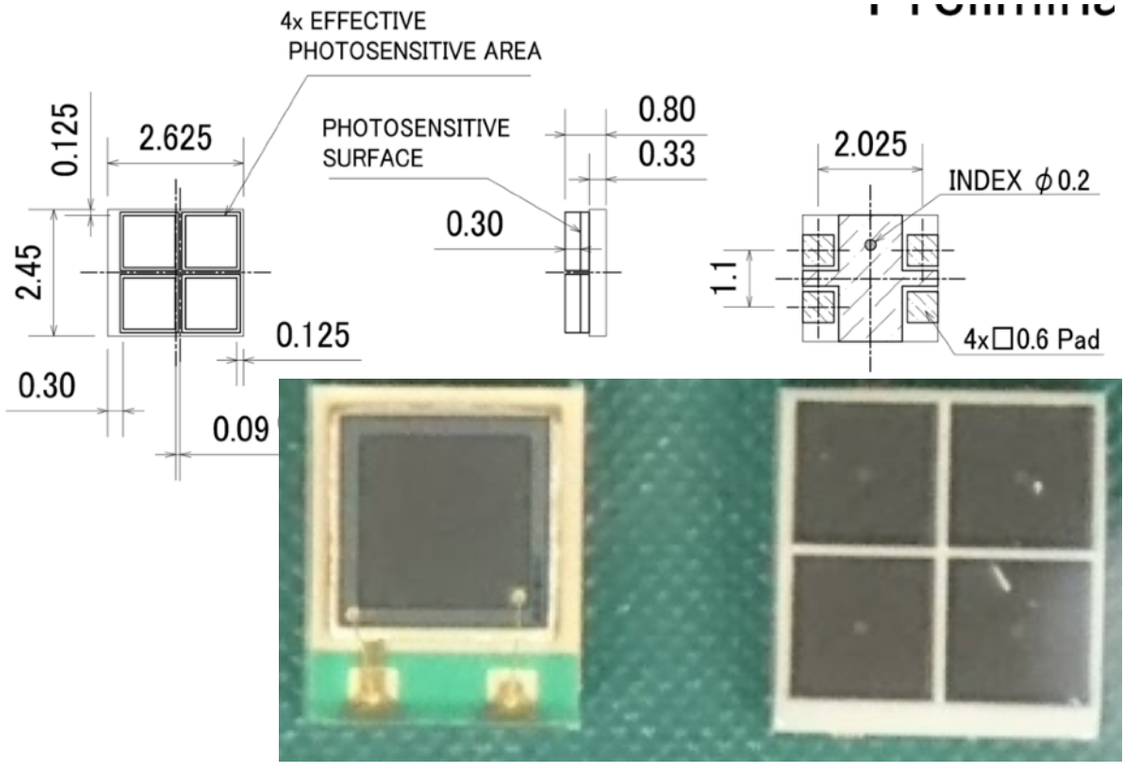
HBU with 60mm tile

- **Detection layer with special HBUs with 60mm tiles instead of default 30mm tiles is constructed.**
- Design concepts
  - Try to be as consistent with standard 30mm tile HBU as possible.
  - **Light yield degradation is compensated with larger SiPM** (1.3×1.3mm^2→2×2mm^2)
  - Use standard HBU (HBU6)
    - Tile is readout by SiPM at shifted position
  - Same design of reflector foil (ESR)
  - Manual tile assembly
- Four HBUs with 144 × 60mm-tiles in total has been produced and added to large prototype.
- Next time, dedicated HBUs will be produced where
  - Tile is readout by SiPM at center
  - # of readout channel × 1/4
  - # of ASIC × 1/4

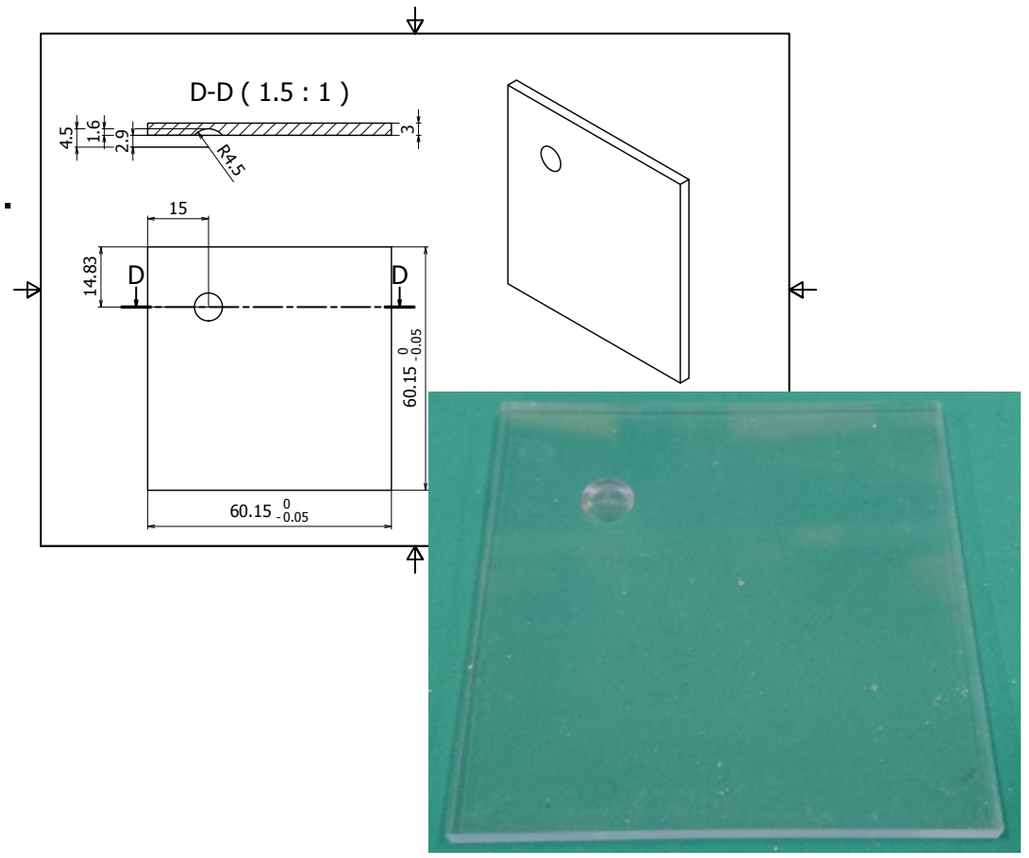


MPPC & Tile

- We produce custom MPPC with an active area of 2×2mm² (no standard MPPC with 2×2mm² active area and 25μm pixel pitch)
  - Discrete array of 4×TSV MPPC S13615-1025
  - No wire bonding → minimum dead space
- We expect **2.4 times larger** light yield by using 2mm×2mm MPPC than default 1.3mm×1.3mm MPPC

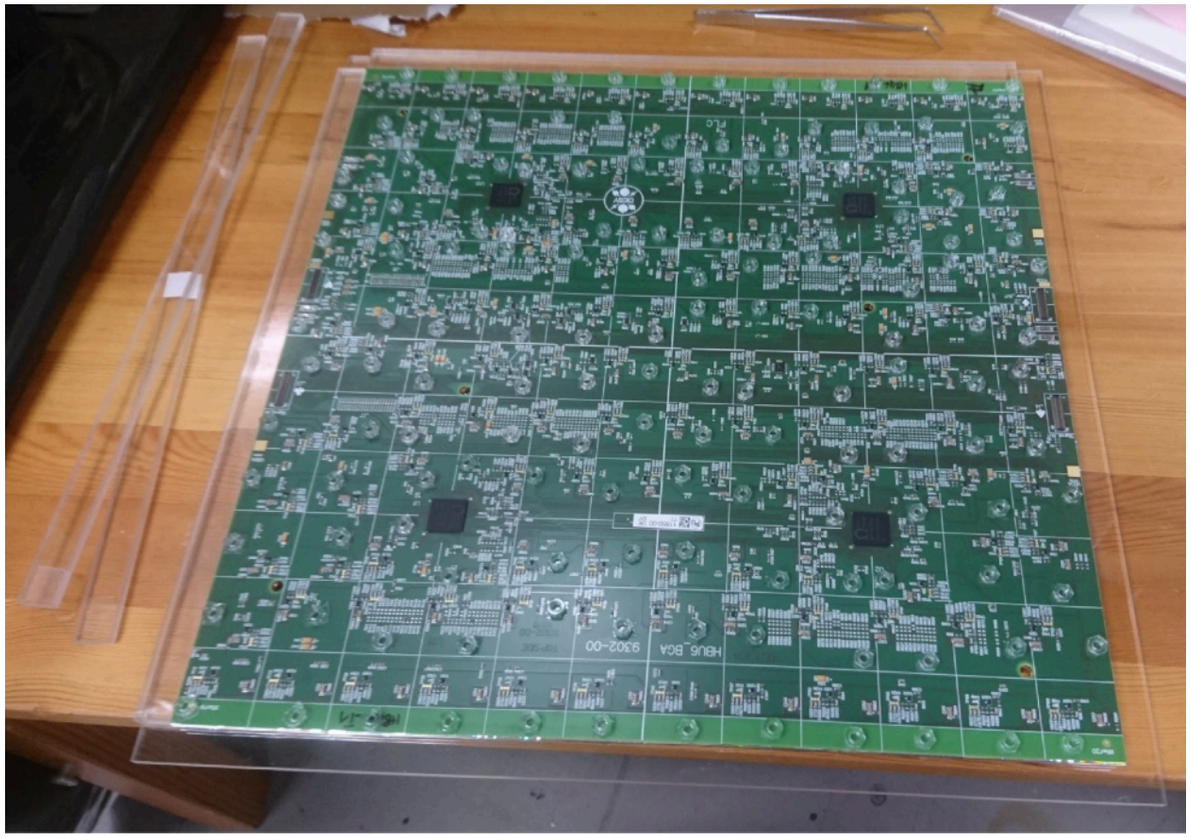


- Scintillator tiles are produced by injection moulding, which is suitable for mass production.
  - 60×60mm² tiles are cut out from a larger plate with a thinkness of 3mm produced by injection moulding
  - The light yield of this polystyrene-based scintillator is 70% of that of commercial PVT scintillator (EJ-212)

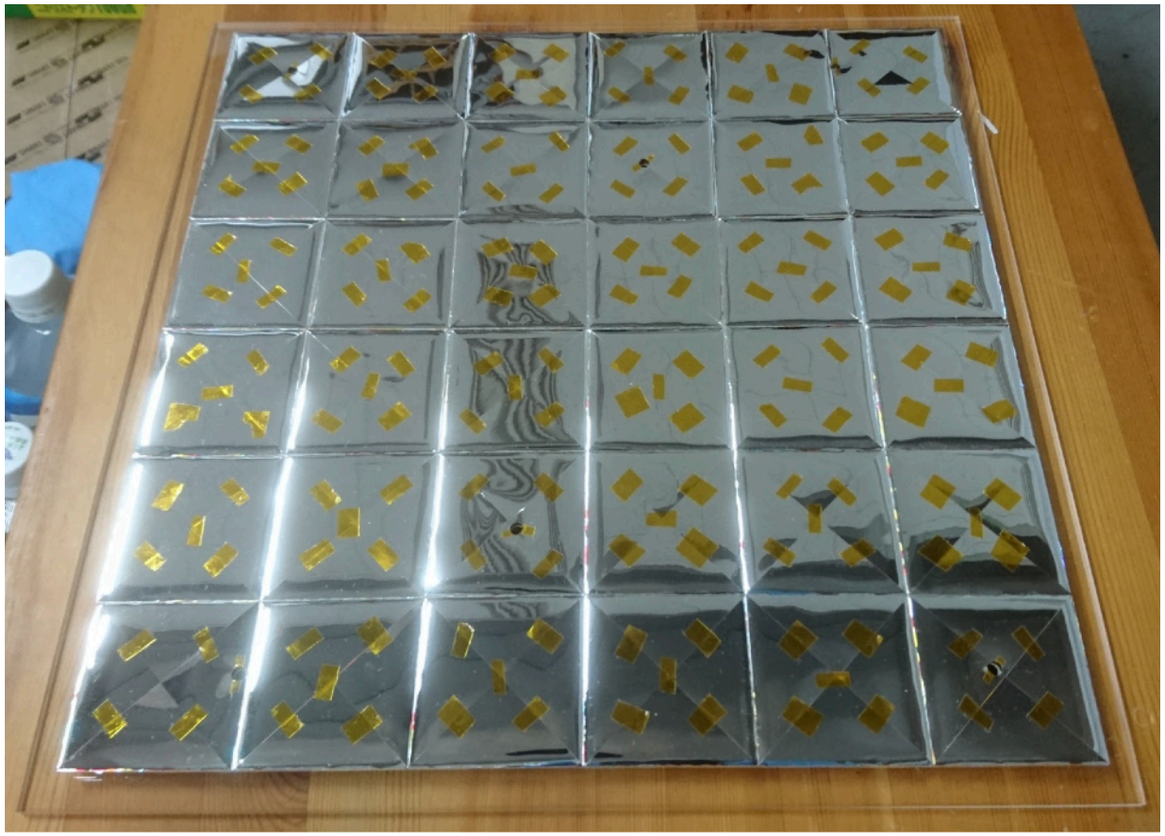


Completed HBU with 60mm tiles

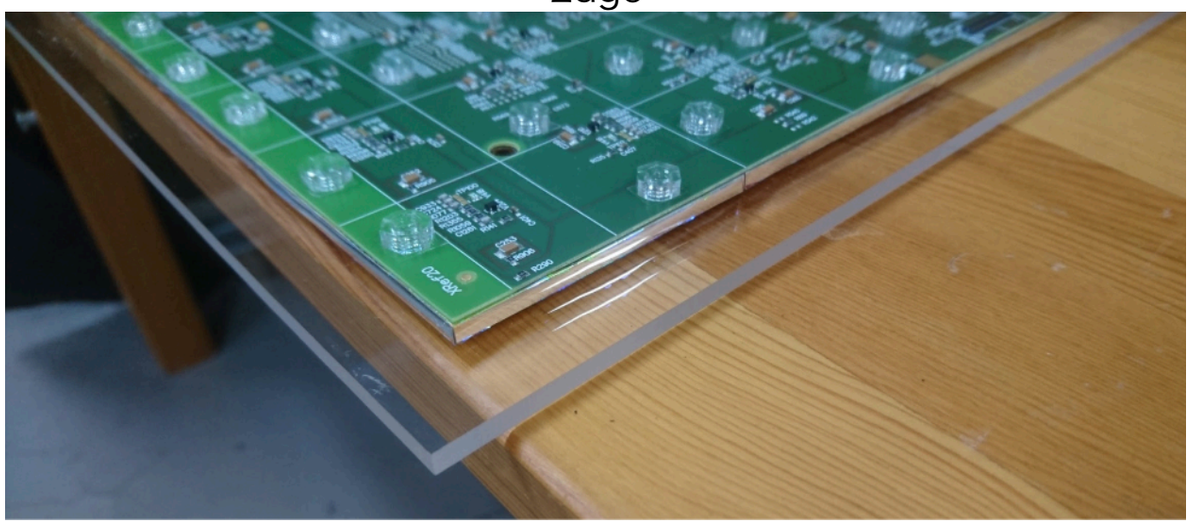
Front view



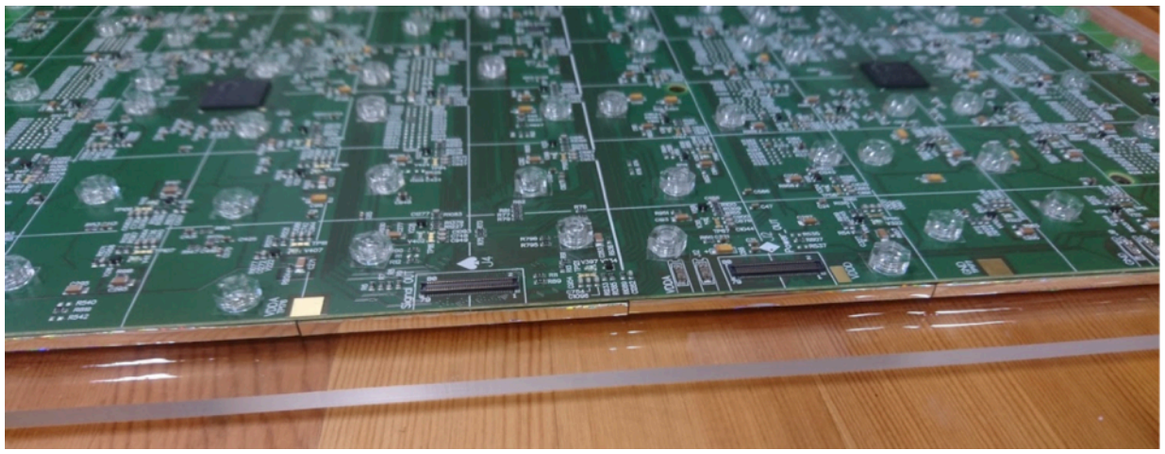
Back view



Edge



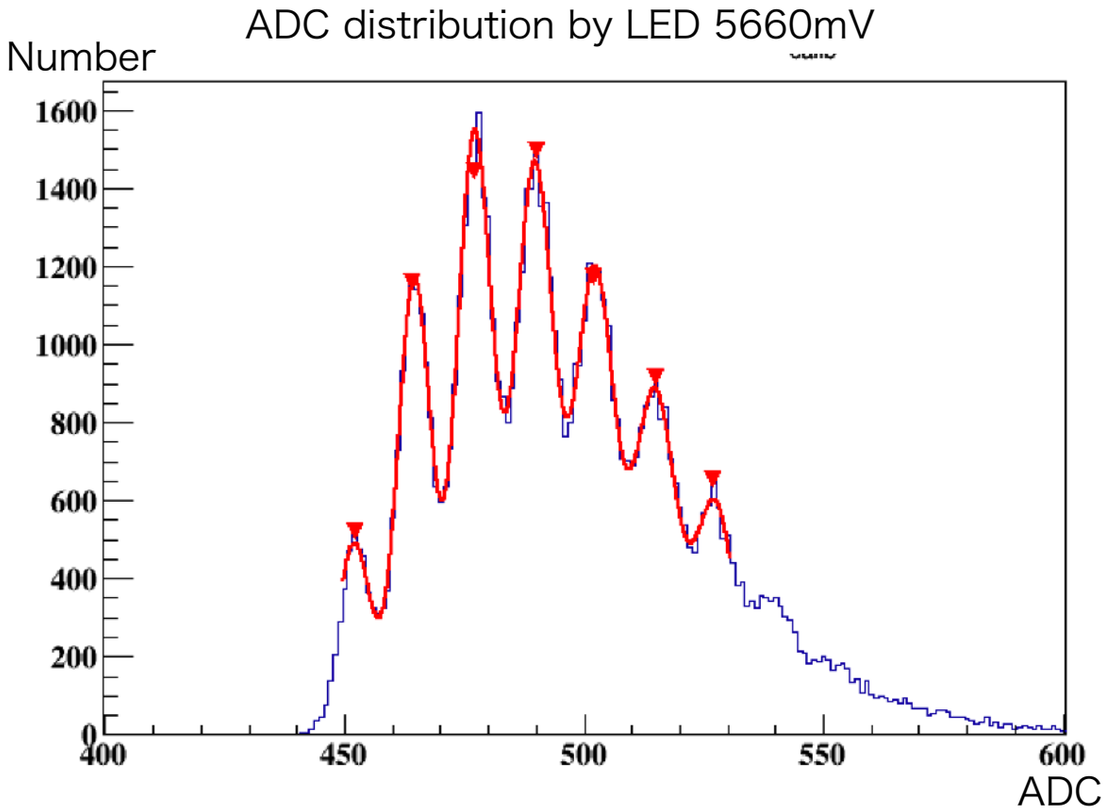
Side



Installation to test beam

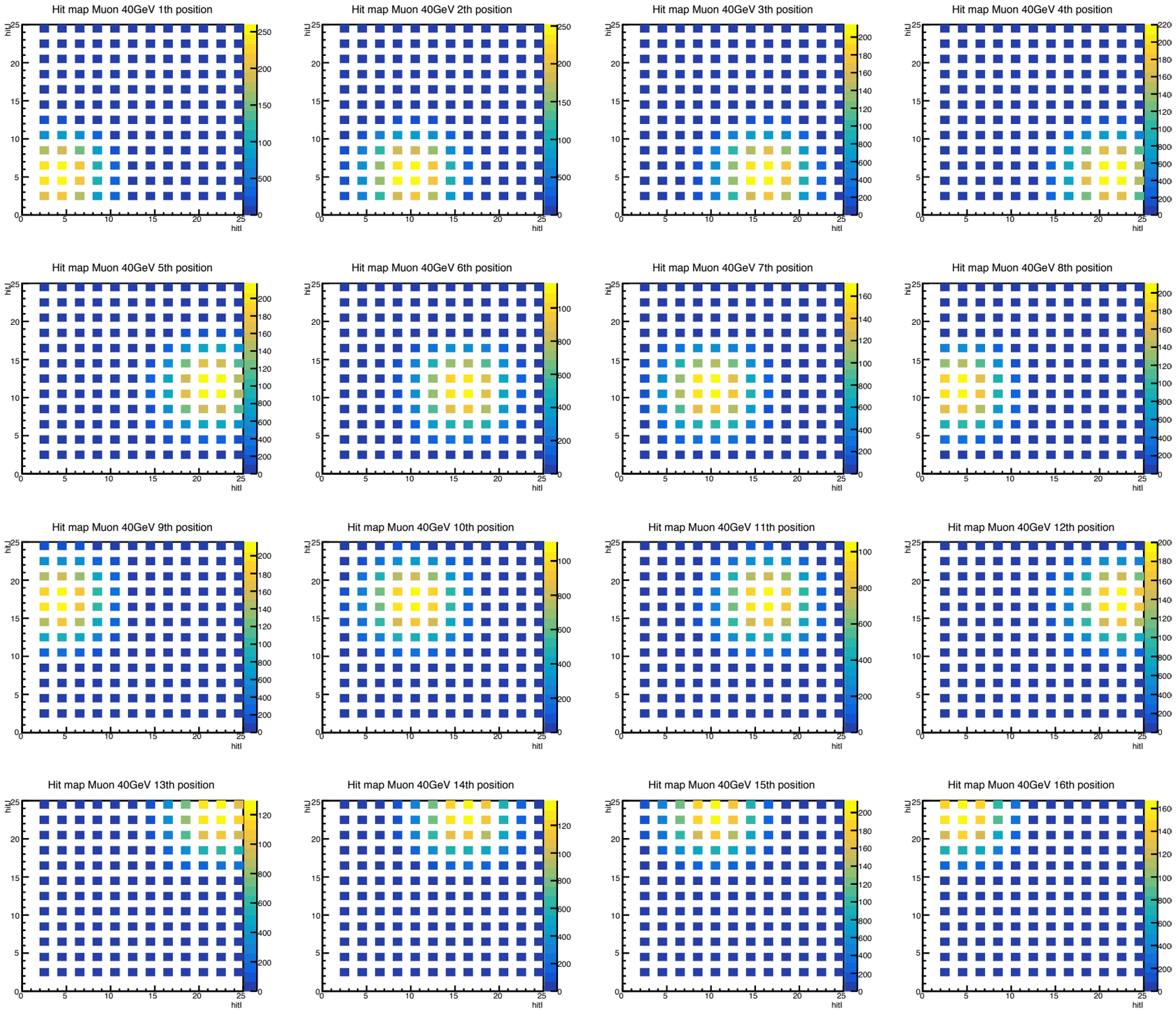
- Installed into the large prototype only at June test beam.
  - Not ready at May test beam
  - Called Tokyo Module
  - Installed as 38th layer

- Over voltage of 2mm² MPPC at Tokyo module is lower than standard 1.3mm² MPPC.
  - Concern about saturation due to higher light yield
- LED calibration successfully done
  - The peak of single photoelectron is clearly resolved



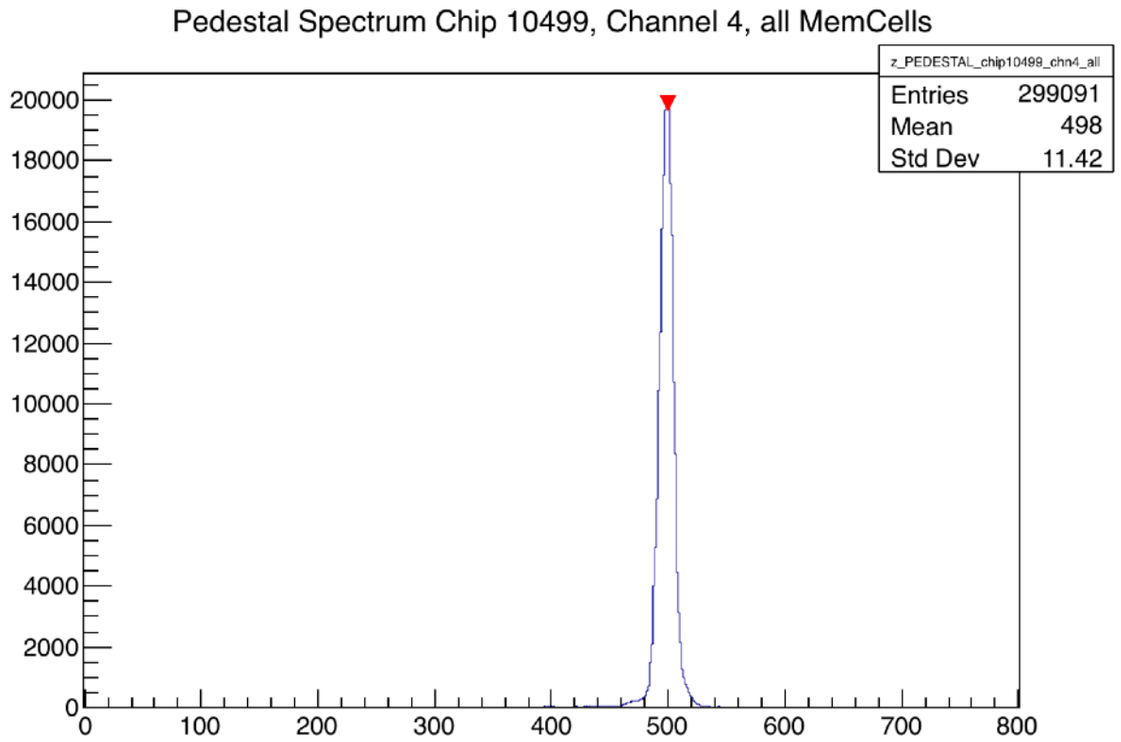
Hit map of Muon scan at 16 positions

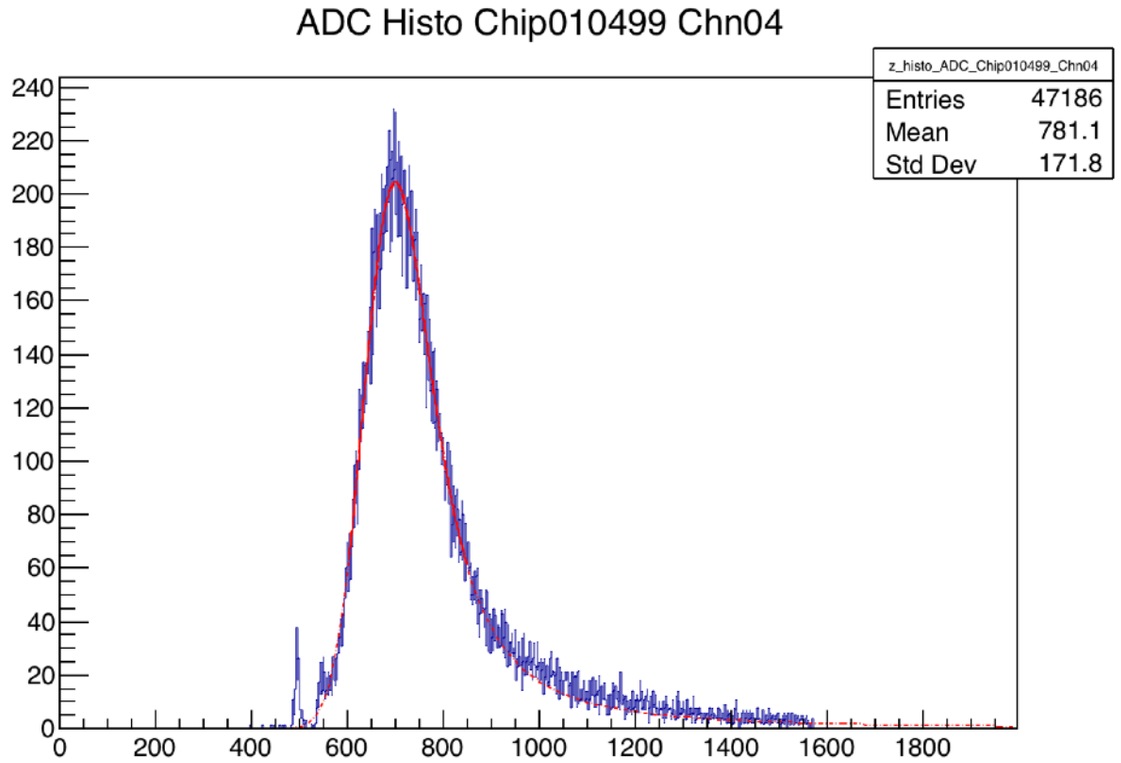
- 9 tiles covered at each beam position



Calibration

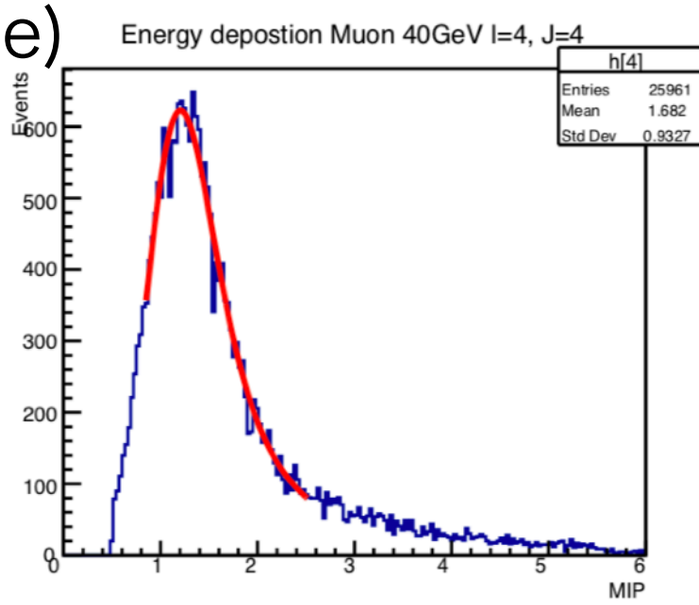
- Some calibrations such as pedestal, MIP and gain are necessary for reconstruction.
- Pedestal calibration
  - Now on going and checking quality
  - Using muon data which have no event hits
- MIP calibration
  - Now on going and investigating the codes
  - Using muon scan data
- Gain calibration
  - Now on going
  - Using LED data



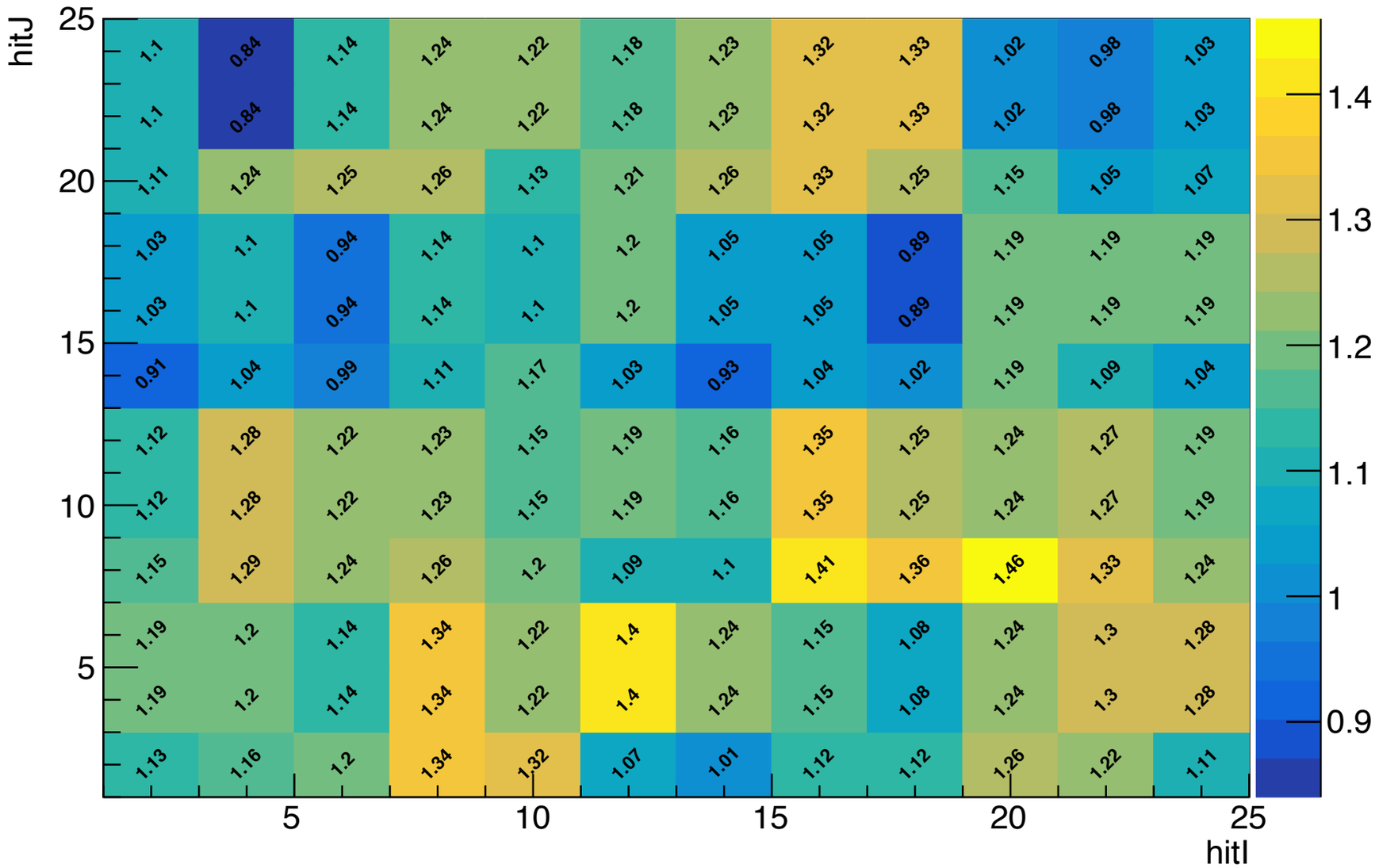


MIP map of Tokyo module (comparison with standard 30mm tile)

- Using the same pedestal and MIP values as the standard HBU.
- Tokyo module has slightly larger MIPs than 30mm^2 tile on standard HBUs.
  - Fit by Landau distribution convoluted with Gaussian.
  - **17%** larger on average.



MIP map of Tokyo module



Summary

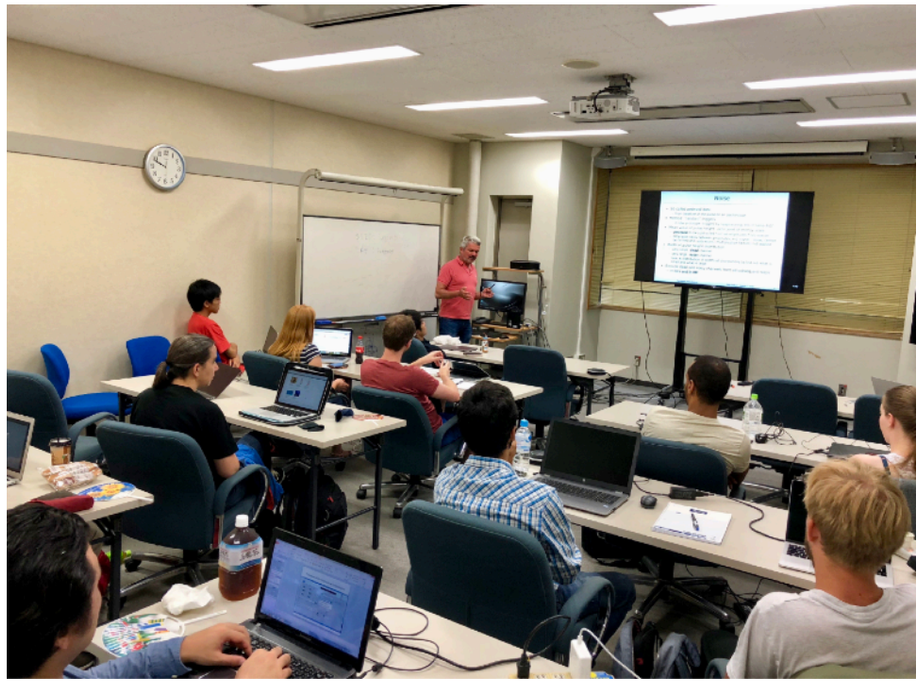
- Granularity of AHCAL is revisited.
  - Mixed granularity with larger scintillator tile for outer layers of AHCAL looks viable option for cost reduction
- Detection layer with special HBUs with 60mm tile is constructed
  - 2×2mm MPPC to recover reduction of light yield
  - 60mm square tiles with shifted readout
- Construction of special HBUs with 60mm tiles is completed.
- Tokyo module has been Installed into the large prototype at June test beam.
  - All channels work fine.
  - Tokyo module has slightly higher light yield than 30mm^2 tile on standard HBU.

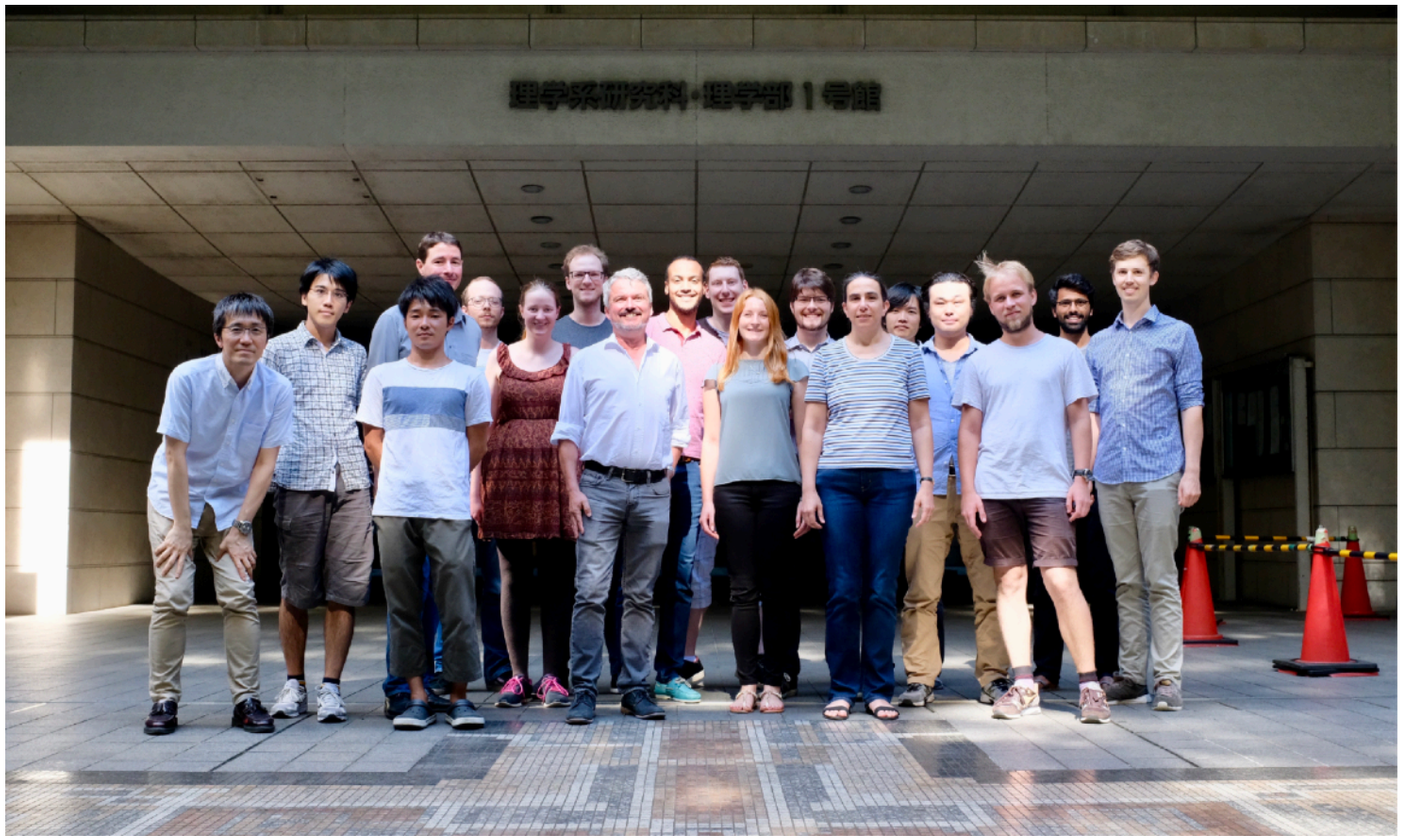
Outlook

- Calibrations
  - Pedestal, MIP, gain,,,
  - Quality check
- Compare with simulation
- Ganging cell study
  - Combining four pieces of 30mm^2 tiles into one 60mm^2 tile
  - Using test beam data and simulation data
- Try some configurations of 30mm^2 and 60mm^2 tile
  - Outer 1/4 layers
  - Half by half
  - All 60mm^2 tile

E-JADE AHCAL Tokyo analysis workshop

- 8/5 - 8/25 @The University of Tokyo
- 17 people from DESY, MPI, Uni Hamburg, etc
- Presentation for Introduction and conclusion, discussion, working together



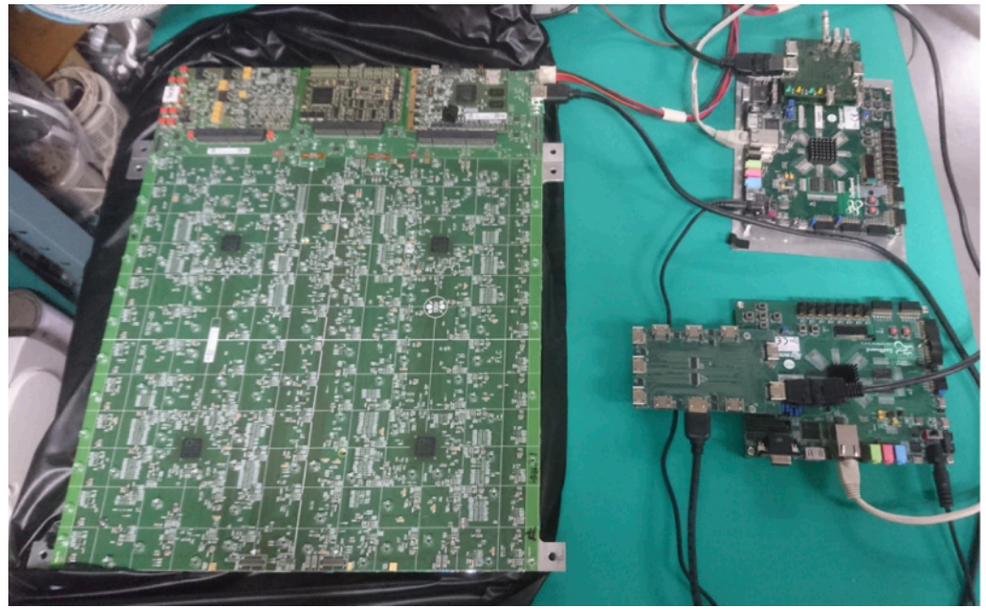


Backup

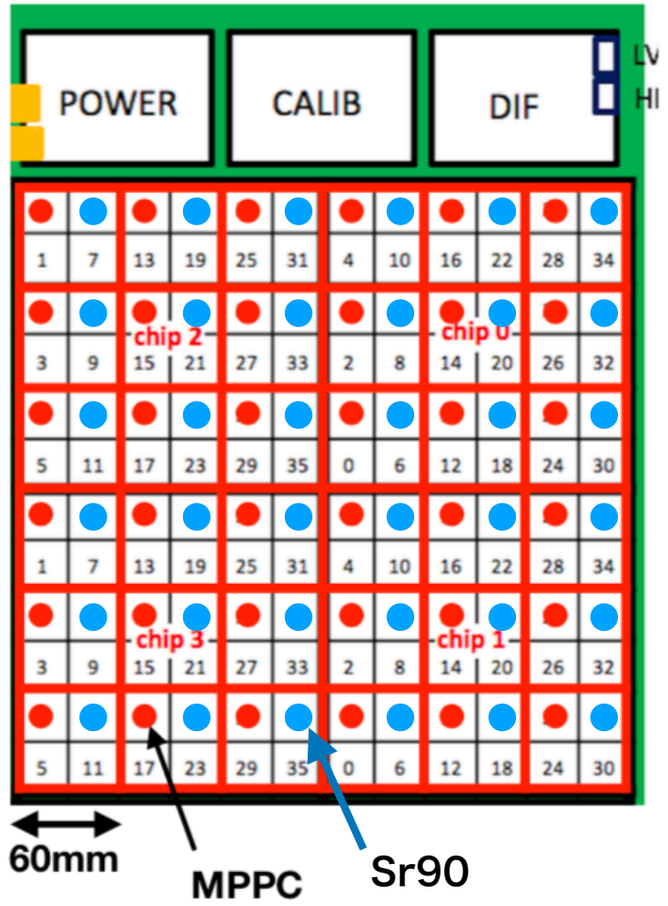
HBU operation test

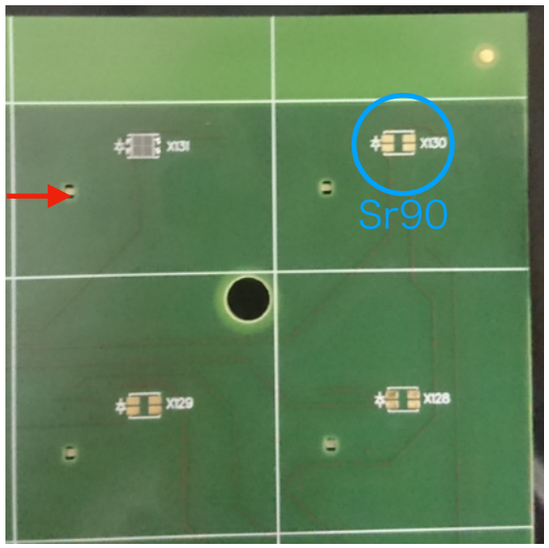
- Gain check by LED
  - Use One of 4 LEDs which is closest to MPPC
- MIP check by Sr90
  - Put Sr90 next to MPPC position (30mm away)
  - Self trigger
  - Note that β from Sr-90 is not MIP
    - Correction based on expected difference from MIP response
    - MIP value is **83%** at the peak value of Sr-90 according to simulation study.

Setup



6×6 tiles per HBU

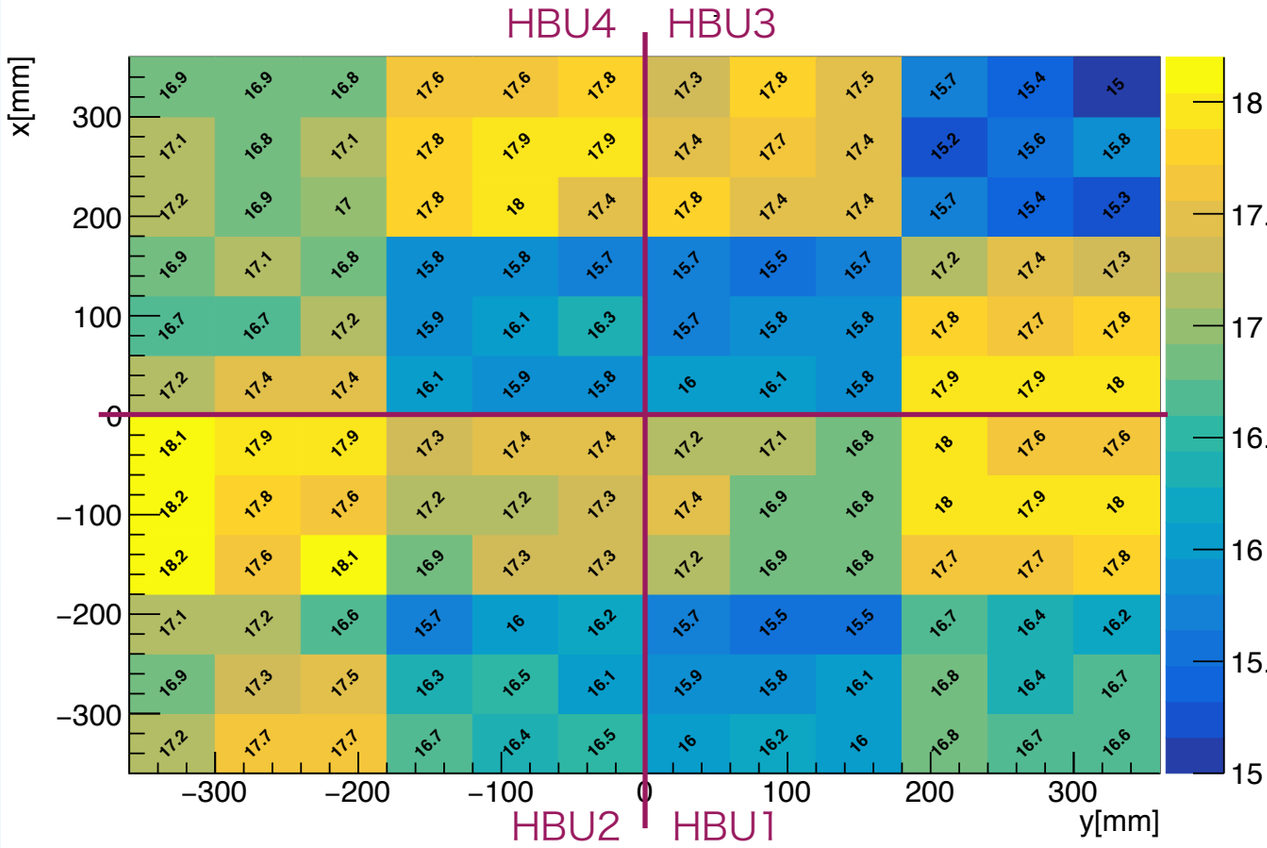




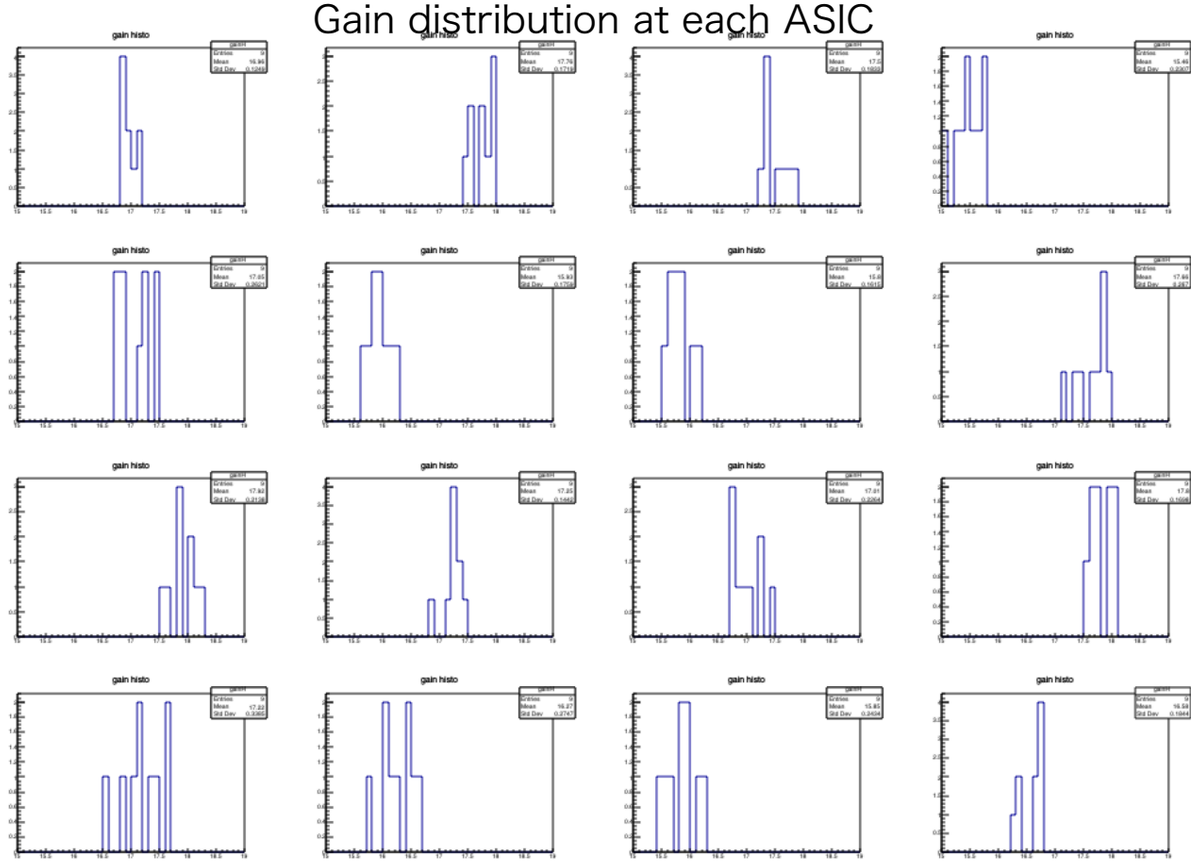
Gain

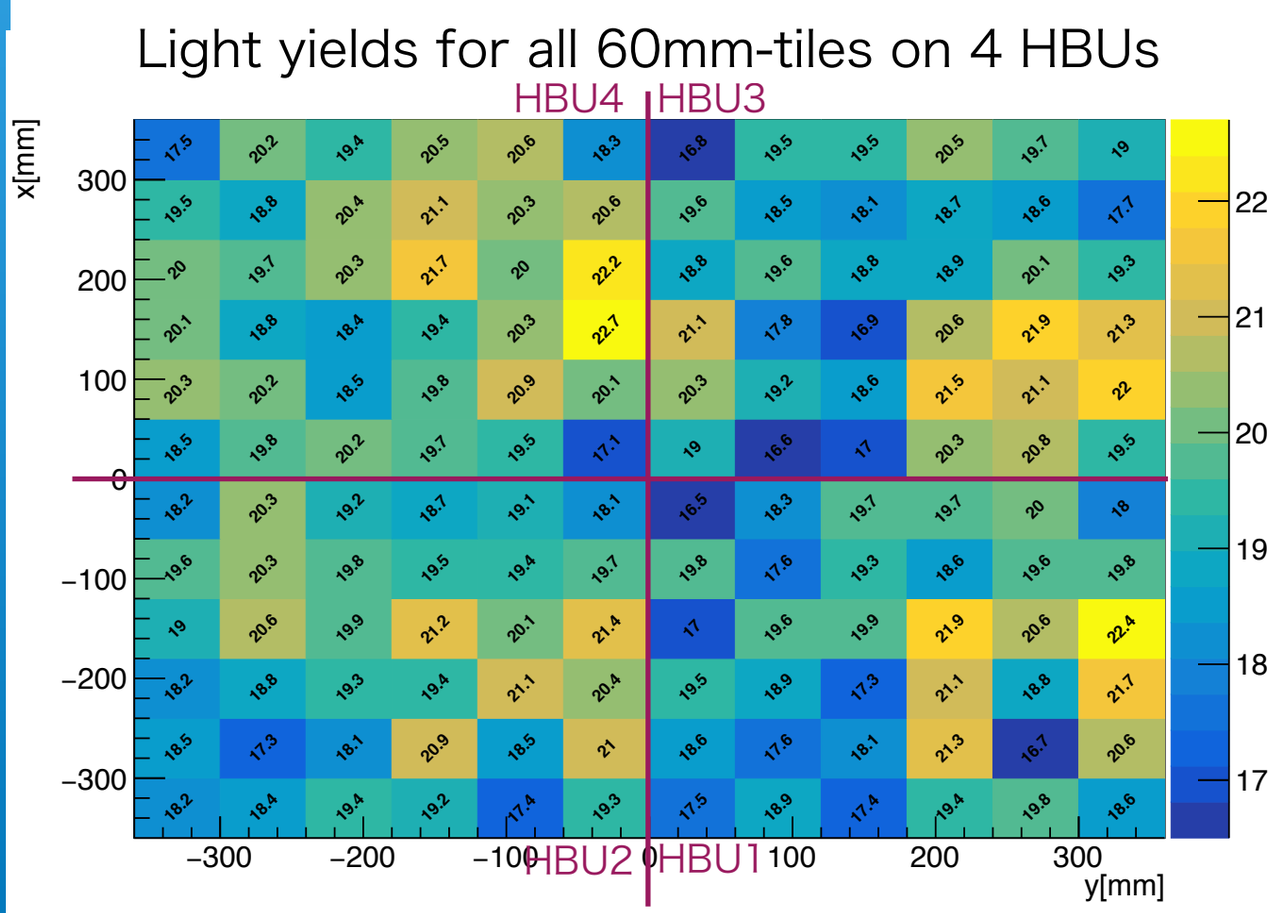
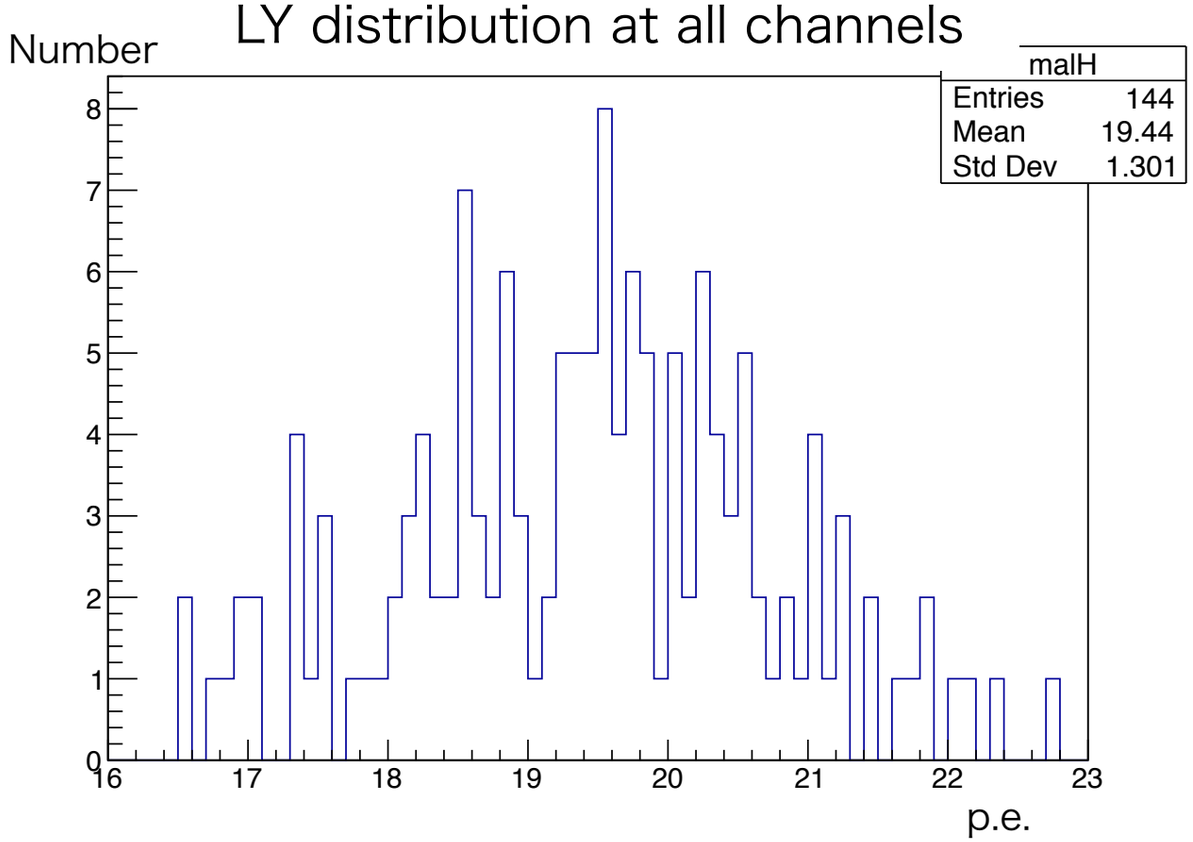
- Gain ranges between 15-20 ADC counts
  - Mean : **16.9**
- Showing slight ASIC dependence.
  - 9 tiles at the same ASIC have almost the same values.

Map of gain values at each channels at the same bias voltage



Gain distribution at each ASIC



MIP-equivalent Light Yield

- MIP value is **83%** at the peak value of Sr-90.
- Light yield ranges between 16-23 p.e. (converted into MIP)
- Mean value is **19.4 p.e.** (converted into MIP)
  - Typical 30mm-tile light yield is 14 p.e.
- No ASIC dependence