Electric field distortions with a GridPix Readout

Peter Kluit, **Kees Ligtenberg,**

Y. Bilevych, K. Desch, H. van der Graaf,

F. Hartjes, K. Heijhoff, J. Kaminski, G. Raven, T. Schiffer, J. Timmermans

LCTPC Analysis meeting – July 6 2018

Outline

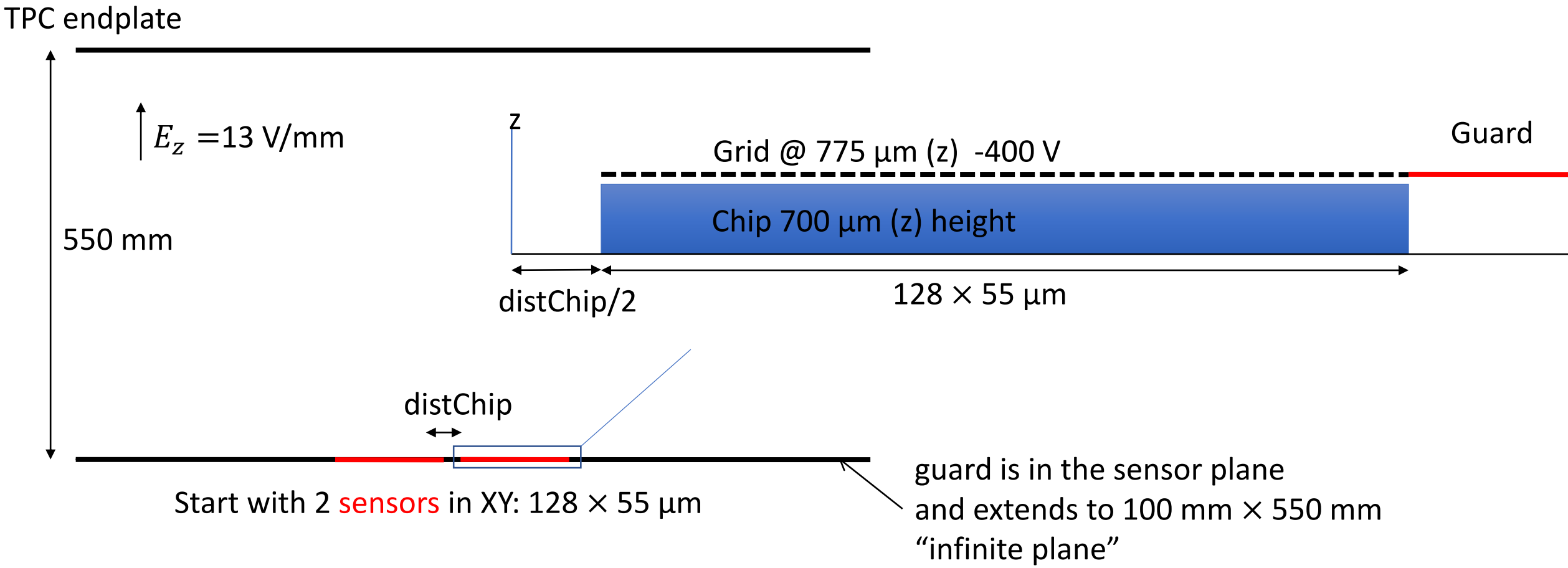
- Simulation of electric field distortions
  - At edges between chips
  - At edges with T-structure guard
  - From mechanical asymmetries
- Measurement of distortions in Gridpix detector with test beam
  - At edges with guard
  - In the pixel plane

Introduction to the simulation

- The read-out plane is covered by many GridPix chips ⇒ Edges
- Distortions at the edges are studied with simulations

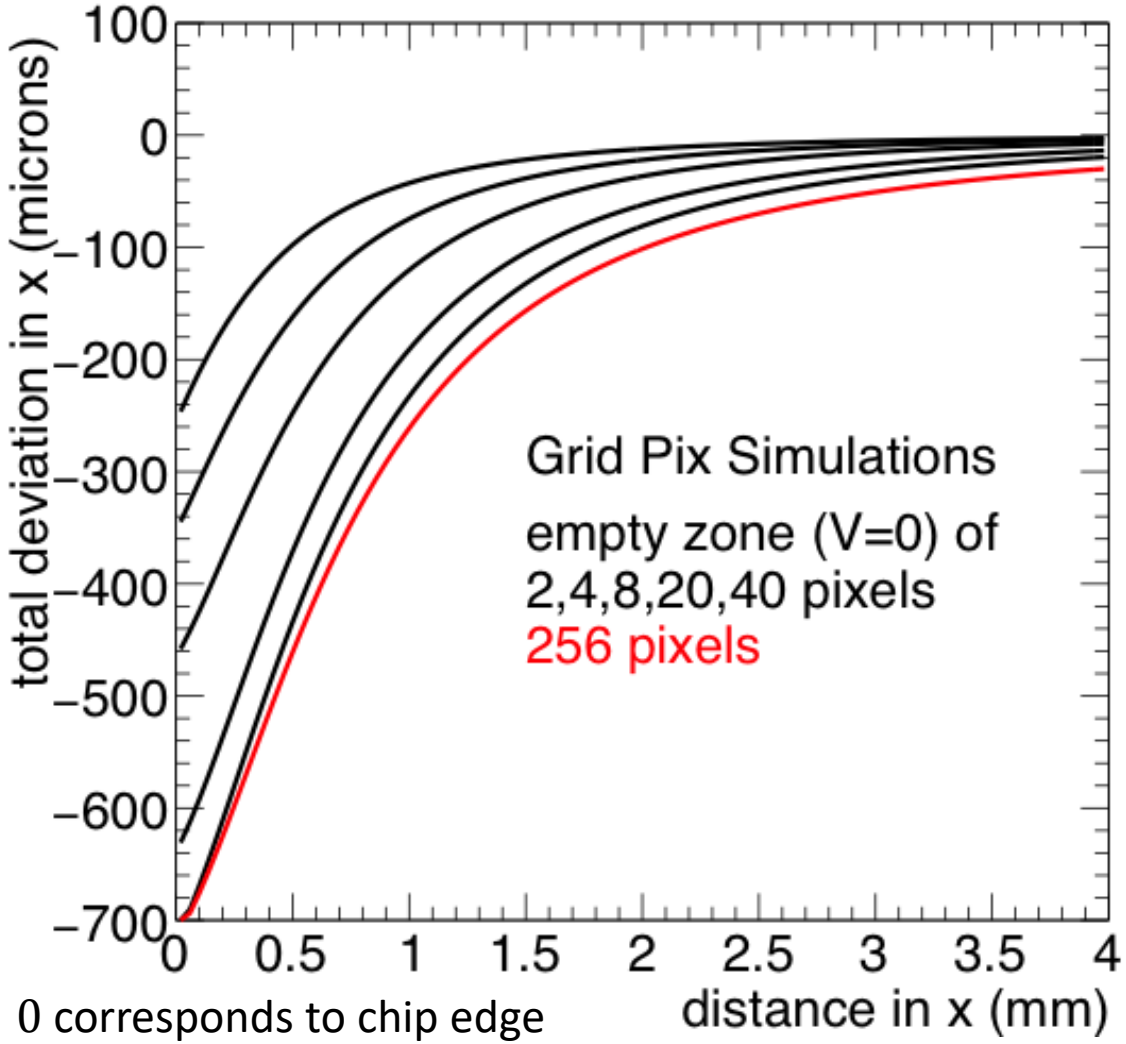
- Two Gridpix chips are simulated as rectangular plates with square holes
- Z is defined as the drift direction, X and Y are in the sensor plane

Geometry in simulation



Simulated electric field distortions

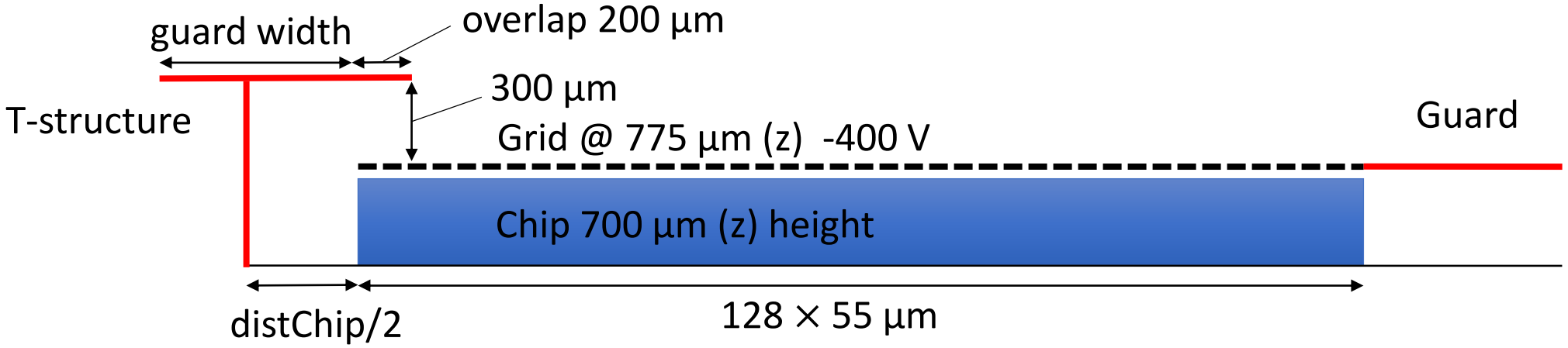
- Even for the top curve with 2 pixels (110 µm) distance there is a sizeable deformation
- Deviations smaller than 20 µm one are found more than 1 mm from the edge
- The absence of a functional chip (gap of 256 pixels) is similar to a large gap (40 pixels)



$x = 0$ corresponds to chip edge

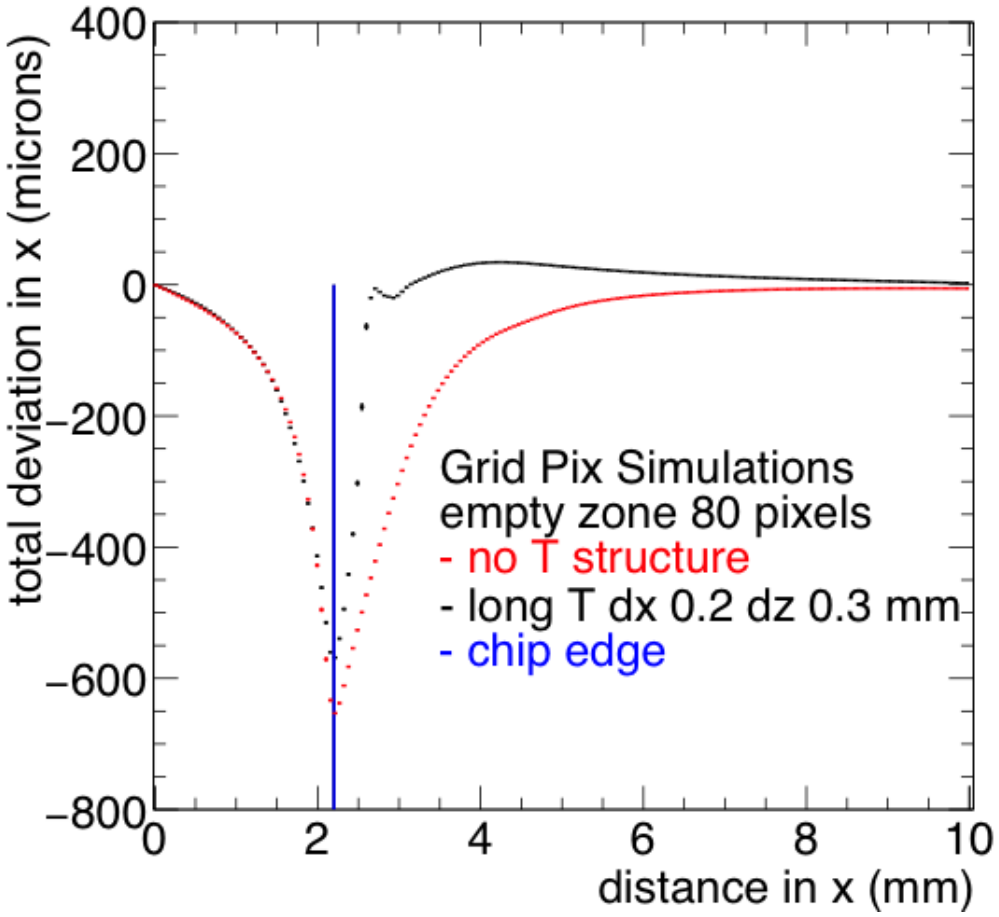
Long T-structure guard

- Special T-structure guard electrode is required to reduce distortions around large gaps
- T-structure extends over the grid
- Similar to guard in single chip Timepix3 GridPix Detector



A long T-structure extending over the grid

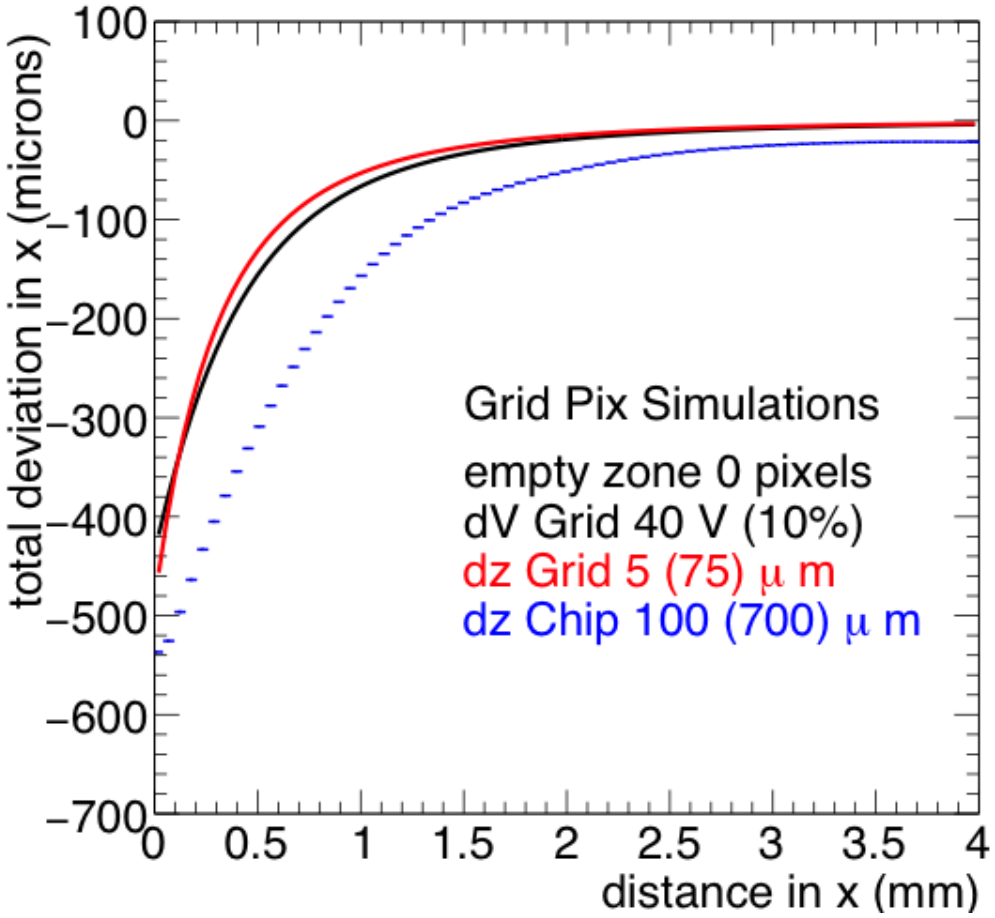
- A long T-structure can compensate the deviations
- However, the overlap will create a zone with large deformations near the edge
- This is OK, if this edge is in the inactive zone of the grid



Impact of asymmetries

With zero distance between the chips, the following asymmetries were introduced

- The voltage on the left chip is changed by 10% (40 V)
- The distance of the grid to the chip is changed from 75 to 70 µm on the left chip.
- The thickness of the left chip is changed from 700 to 800 µm



What precision do we need for a module?

Using the T-structures of 40 and 80 pixels the deformations at 5 pixels from the edge are max 50-70 µm. This puts requirements on the design:

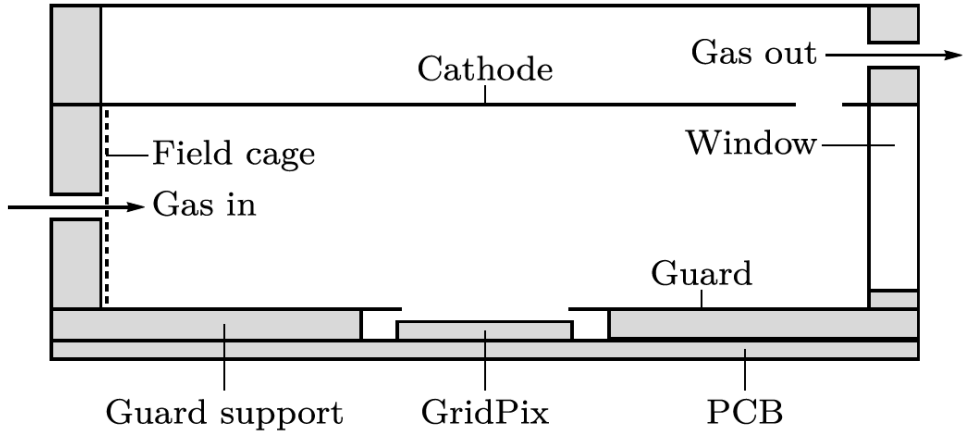
1. The chip height must be controlled at the 10-20 µm level
2. The distance of the grid wrt chip should be constant to better than 1 µm
3. The voltage must be regulated to better than 4 V (1%)
4. The height of the T-structure should be constant at the 10-20 µm level
5. The width of the T (top) and its placement wrt the chip should stay below 10 µm

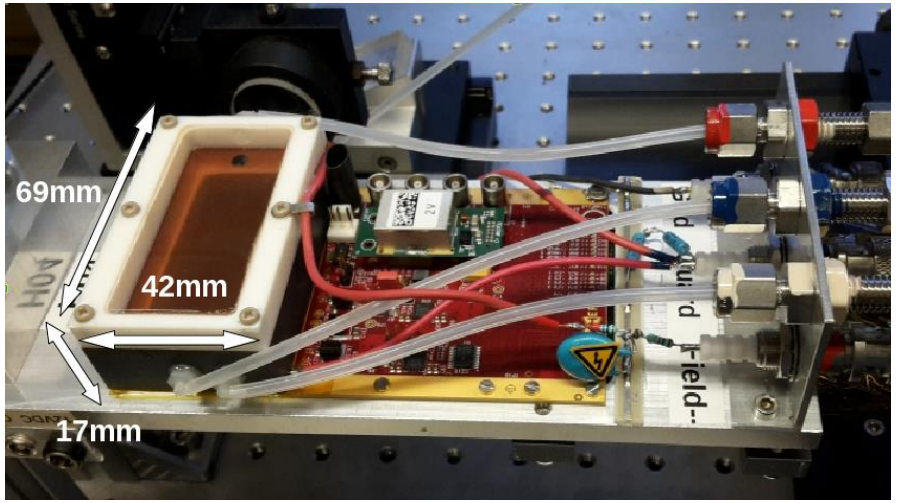
The first two items have to be ensured during the chip production process. Items 4,5 depend on the production of the T-structure and 2,4,5 on the assembling of the chips and T-structure on the module.

Timepix3 based GridPix detector

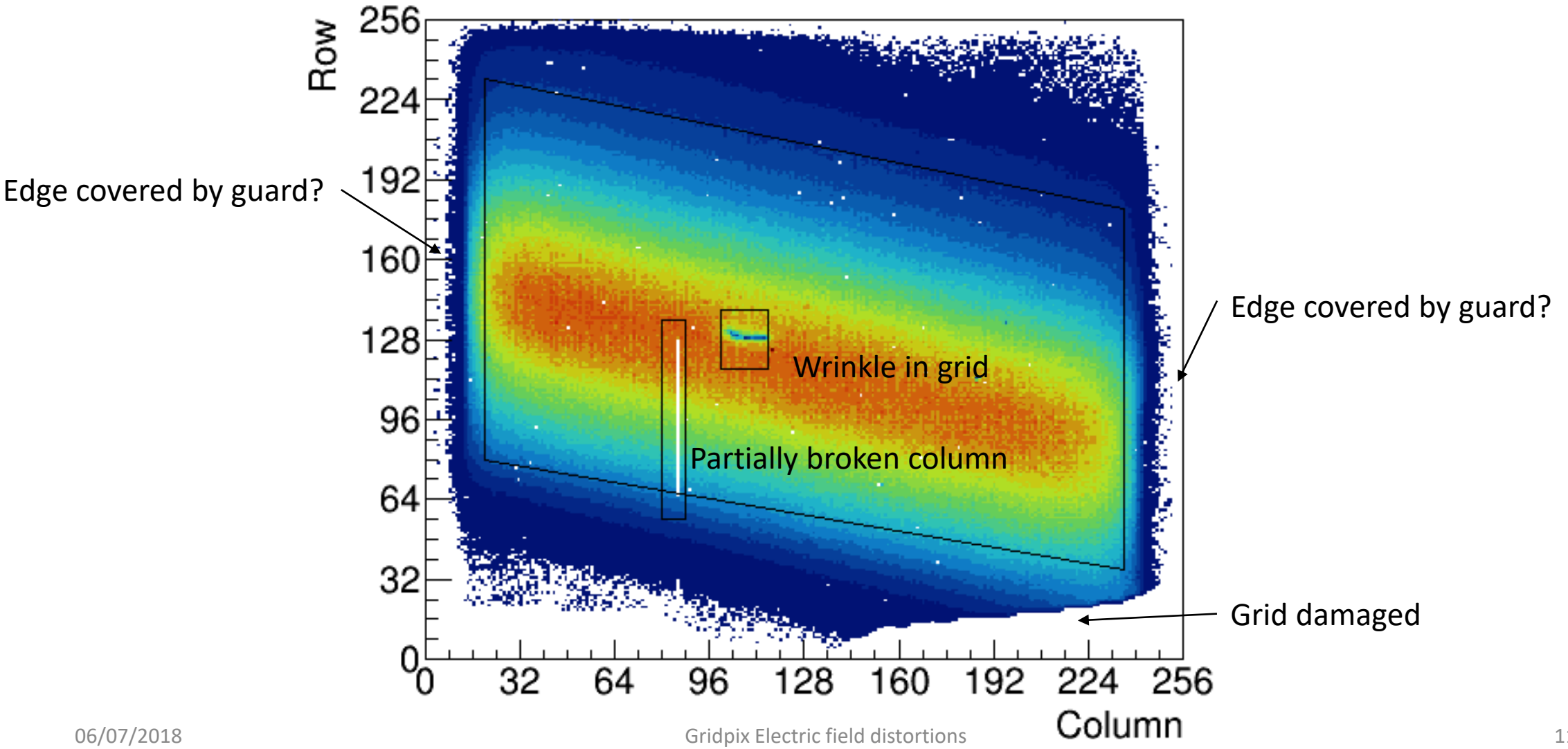
- Detector with single GridPix chip
- Guard at 4 sides above GridPix and extending to chip edge
- Drift field is 280 V/cm
- Grid at 350 V, Guard offset by 25 V

- Test beam with 2.5 GeV electrons at ELSA facility (Bonn)





Distortions in Gridpix detector

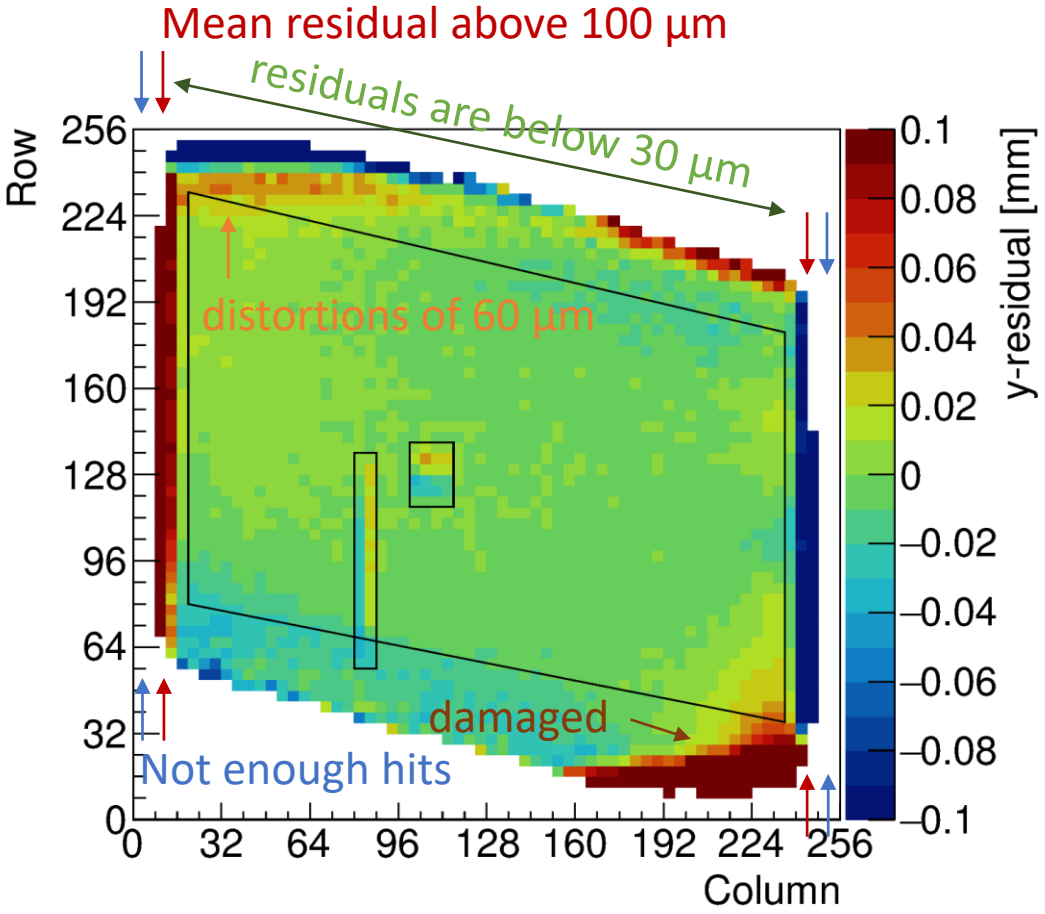


Mean residuals from test beam

Mean y-residual per 4 × 4 pixels

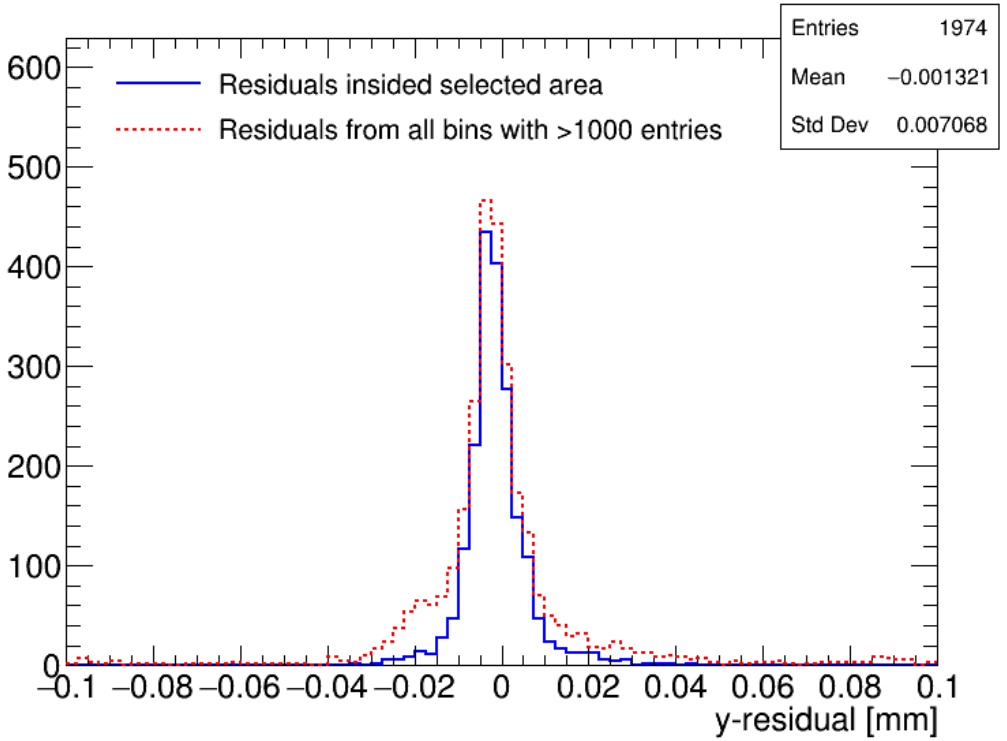
- Too small number of hits in first and last 8 columns (at edge)
- Mean residual above 100 µm for columns 8-16, 240-248
- From column 16-240, residuals are below 30 µm
- Bottom right is damaged
- Top left has distortions of 60 µm

1 mm from the edged distortions are below 30 µm



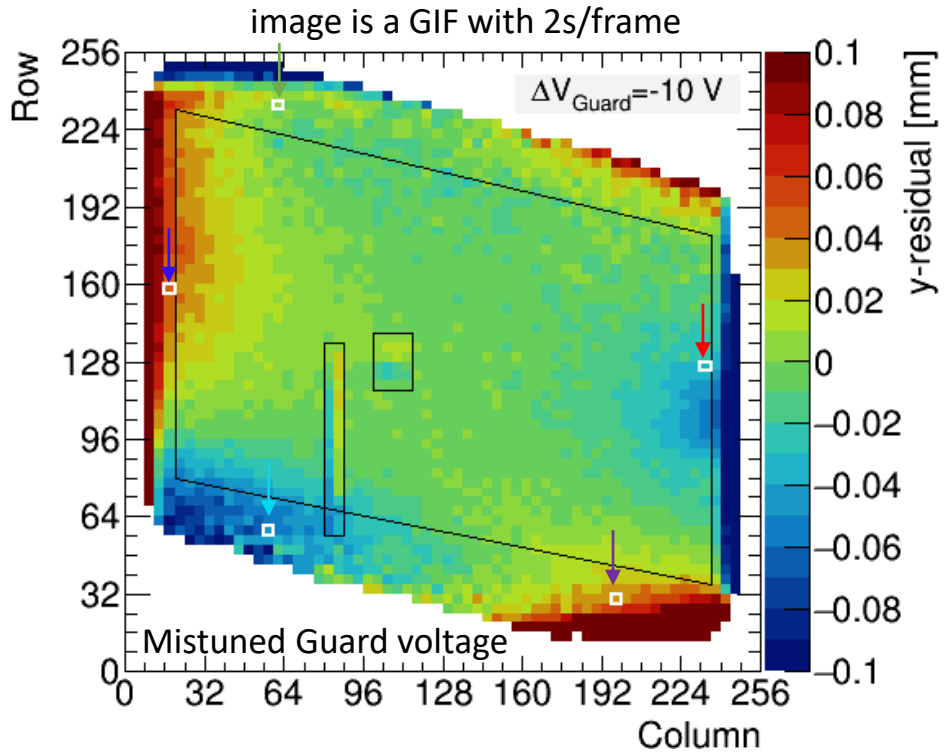
Systematics in selected area

- Within the selected area away from the edges, systematic deviation r.m.s. is 7 µm
- Overall grid quality is good

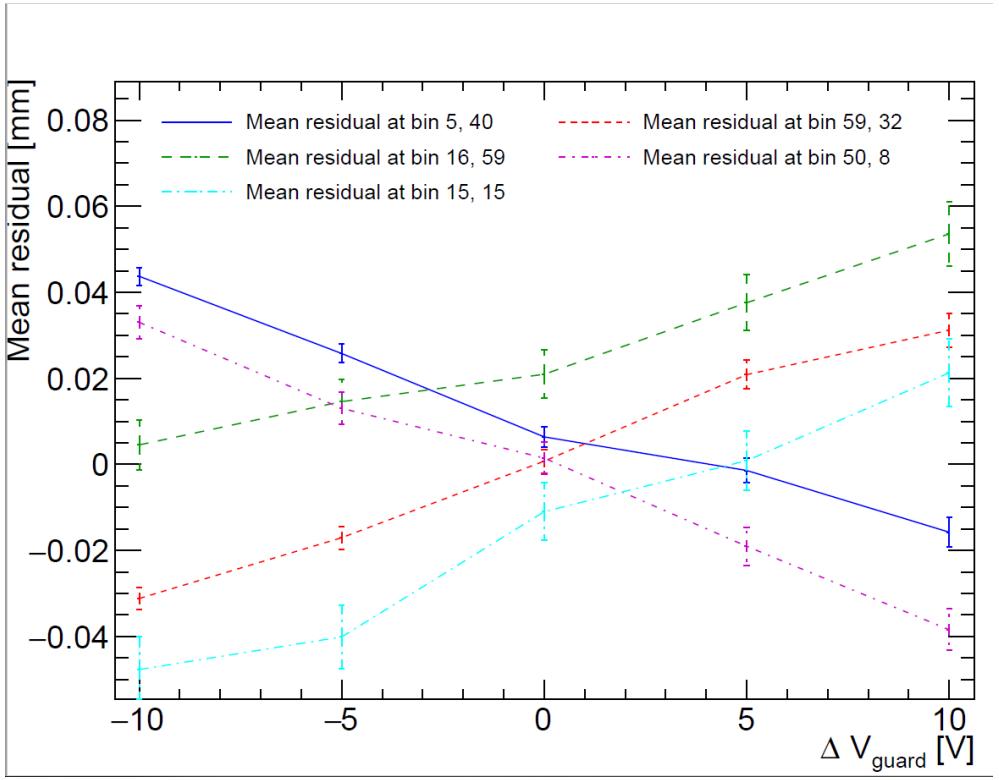


Distortions at the edges due to variation of guard voltage

In the deformation plot, the attraction of hits to the guard is visible near the edges



The Projection of selected bins 1-3.5 mm from the edge, shows that deformations are below +-50 µm for +- 10 V



Conclusions

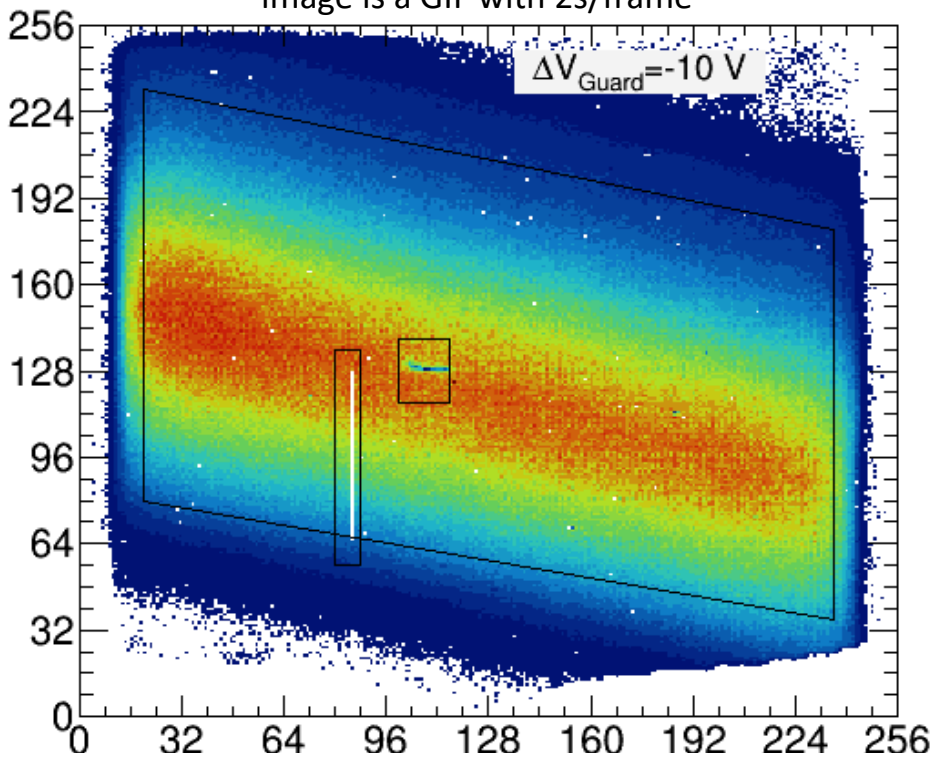
- From simulations requirements on module designs are identified to keep distortion below 100 µm
  - Chip-Chip distance should be smaller than 110 µm (2 pixels)
  - Larger gaps can be bridged with a T-structure
  - There are stringent requirements on chips and T-structure dimensions e.g. chip and T-structure height must be precise at the 10-20 µm level
- With the single chip detector
  - Effects at edges are assessed
  - The grid quality in the center of the chip is in good condition (the r.m.s. of the mean residuals is 7 µm)

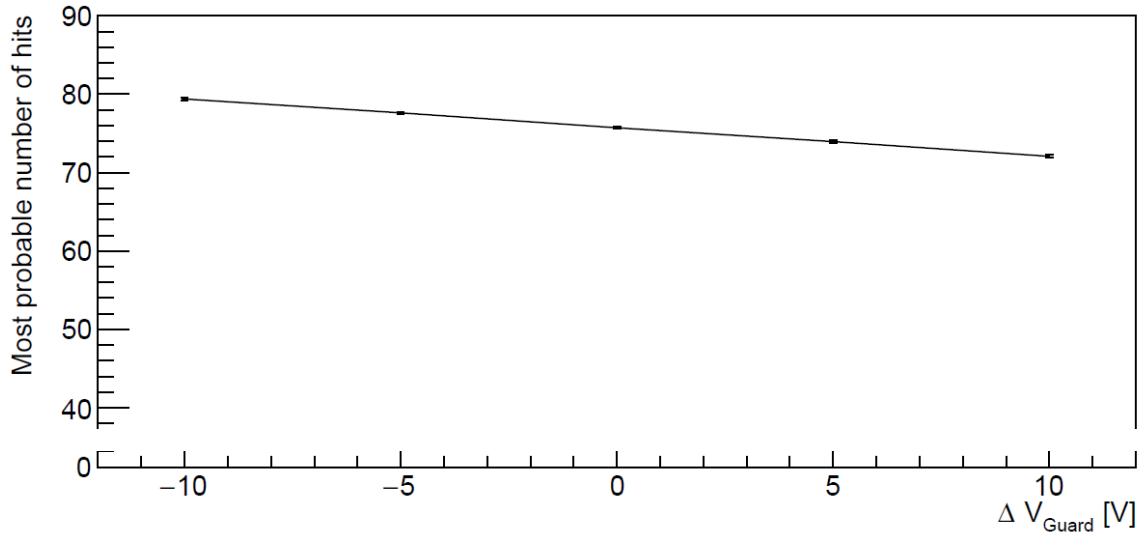
Backup

Variation of guard voltage

- Variation of guard voltage, allows to study a mismatch of guard voltage
- Increasing the guard voltage attracts hits from the border to the guard
- This causes a decreasing number of hits

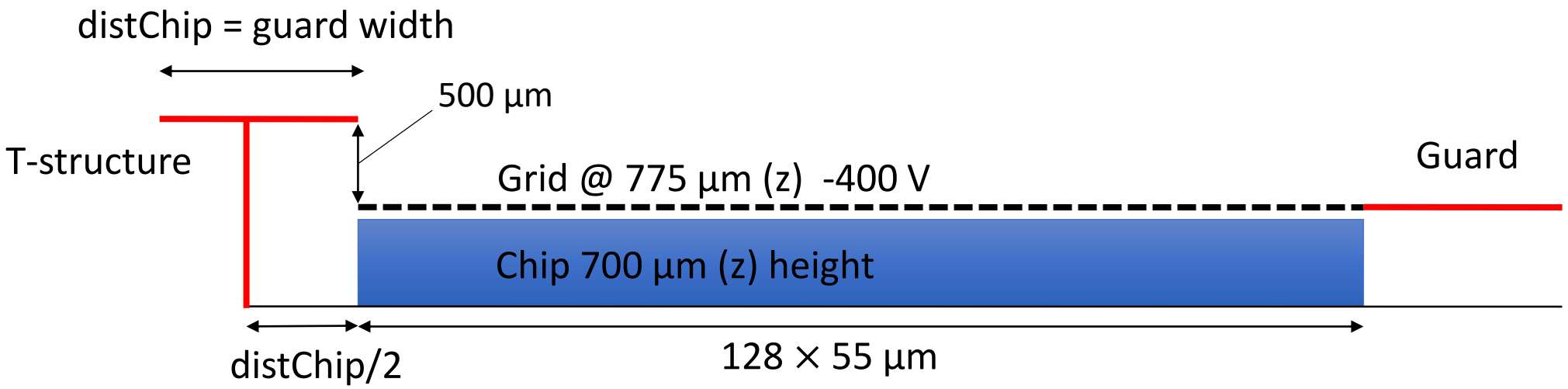
image is a GIF with 2s/frame





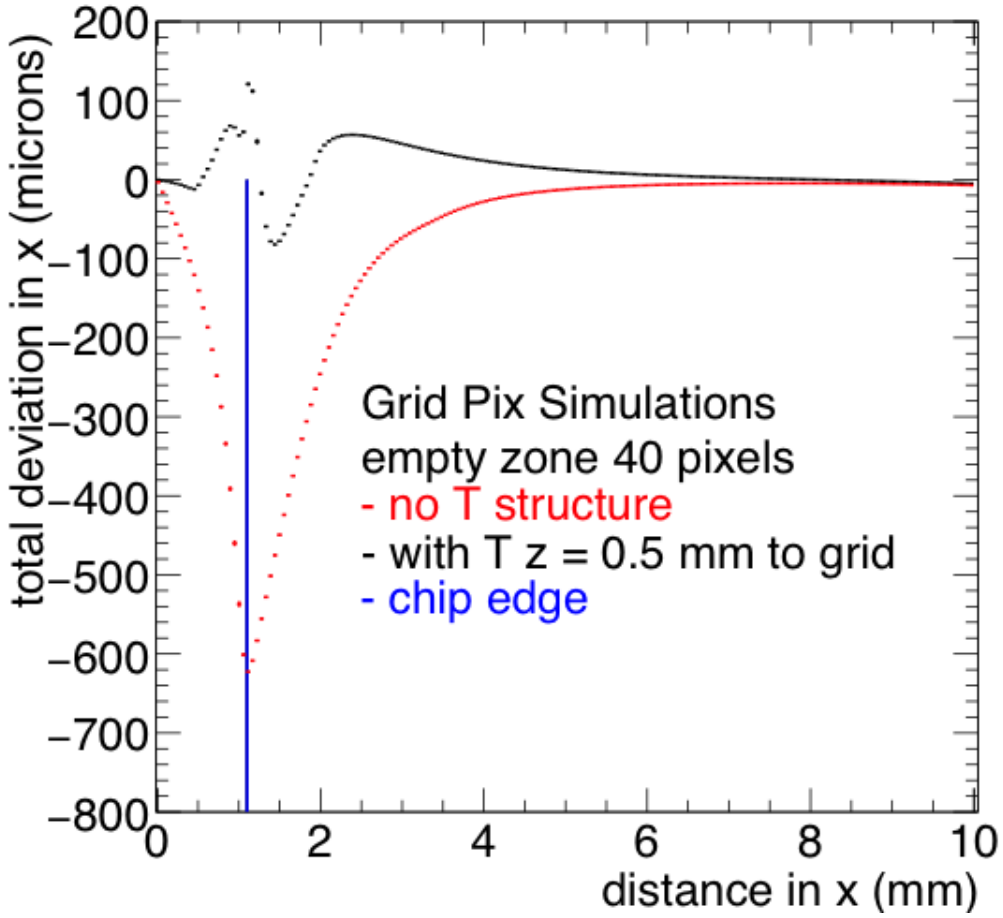
Special T-structure guard

- Special T-structure guard electrode is required to reduce distortions around large gaps
- Each chip has a side with a large gap required for the bond



A 40 pixel wide T-structure

- Voltage of guard is tuned to minimize distortions
- Distortions are reduced from 600 µm to below 100 µm
- Distortions at 1 mm from the edge are below 50 µm



An 80 pixel wide T-structure

- Voltage of guard is tuned to minimize distortions
- Distortions are reduced from 650 µm to below 140 µm
- Distortions at 1 mm from the edge are below 70 µm