What has happened with the development of the SALTRO readout system since the last CM?

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Leif Jönsson
Lund Univerisity
(on behhalf of the Lund group)

Status in June 2016 at Santander:

- Since the contract with the Swedish company was signed in April 2013 we had experienced 6 unsuccesful attempts to bond the SALTRO-chip to our carrier board. Further the quality of the epoxy layer covering the top side of the carrier board was not of suffiecient quality for efficient cooling.

- We decided to perform an X-ray investigation in order to find the cause of the problem.

- The design of the MCM-board (Multi Chip Module) in HDI-technology (High Density Interconnect) was essentially complete and a mechanical sample was produced to check the spatial constraints.

- The development of the firmware for the serial readout had started already in 2014. Yifan Yang from Brussels for the CPLD and Fan Zhang from Wuhan for the SRU. Unfortunately Brussel's engagement in LHC prevented them from continue and Fan had to leave the project due to emplyoment circumstances in the beginning of 2016.
A master student from the Faculty of Engineering at Lund University was engaged but before he could finish he was offered employment in industry.

- We presented ideas for cooling of the chips

- In the beginning of 2017 the X-ray investigations were finished and revealed that the loop of the bonding wires were in several cases not adequate. There were wires which rested on the edge of the die. The conclusion was that when the carrierboard was heated up in the process of applying the tin balls these wires were ripped off due to the different expansion of the PSB and the epoxy layer.

- The contract with the company was terminated on the 25.2.2017

- A new contract was signed on the 16.2.2017 with a company which was able to package our dies in small enough capsules.

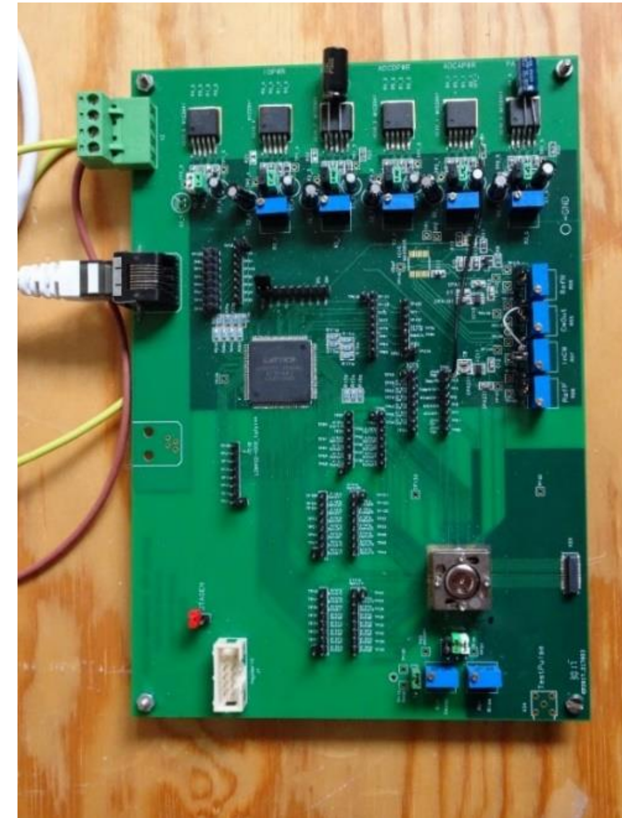
- The first ocular inspection of the dies revealed that some dies were of bad quality and the variation in size was bigger than expected. This presents a potential problem for succesful packaging.

A new test board

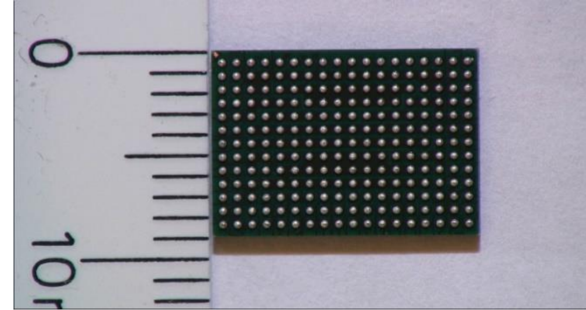
Since the BGA footprint is different for the packaged chips compared to the carrier board, the test board had to be modified and a new test socket had to be purchased.

The test board is read out via an SRU (Scalable Readout Unit).
The FPGA firmware on the SRU is using the ALICE and TOTEM systems.
However, this firmware has to be modified for full functionality in our application.

The firmware for the CPLD is adopted from the ALICE exp.



End of July 2017 we received the first pre-sample of 34 chips, which had a perfect surface quality and very precise dimensions.



- From the subsequent tests in Lund only 20 chips passed the requirements, which corresponds to a success rate of less than 60%.

- It was carefully tested that there was no bug in the test board.

- A procedure for selecting and positioning the dies was agreed on with the company and a second Pre-sample of 55 chips was ordered.

- At the end of May the second pre-sample was delivered and subsequent tests in Lund showed that 46 chips passed the requirements, corresponding to a yield of more than 80%.

- Packaging of the full sample was ordered and the delivery followed at the end of November 2018

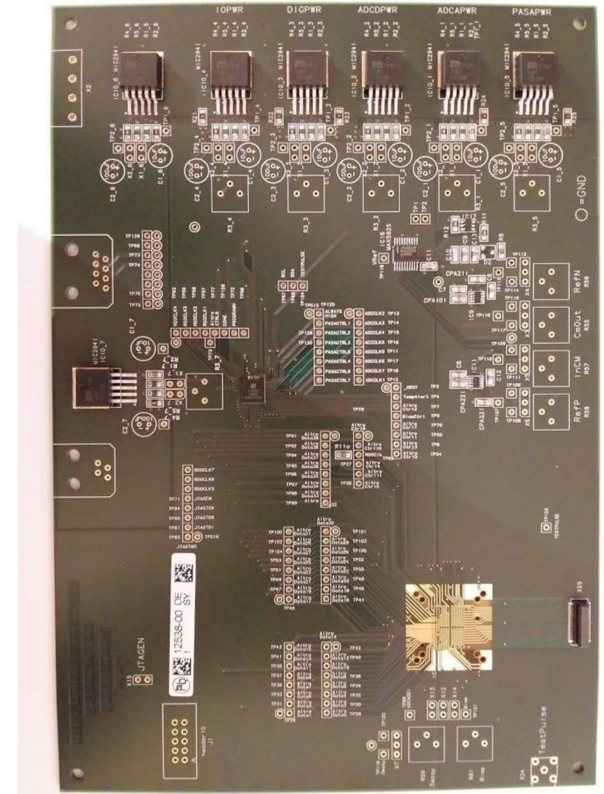
A new and somewhat smaller CPLD has been found, which helps in the deployment of the components on the MCM-board.

This led to a modification of the test board, in order to check the correct routing for the CPLD.

The PCB has been delivered and the components have been mounted by the Electronics Workshop at DESY.

The test socket and the various connectors will be mounted in Lund.

The aim is to test all the packaged chips with this test board but this can only happen when the firmware for the CPLD and the SRU has been finalized.



Status of the DAQ system

With the present DAQ-system we are limited to perform a full readout of 2 channels out of 16 alternatively to read out all channels but limited to 180 samples.
The CPLD: the firmware works with th old testboard. It has to be modified and tested for the new test board.
The SRU: re-arrangement of the memory management necessary for full readout of al 16 channels.
A bug which causes the system to hang has to be solved. This needs an FPGA programmer.
The PC: the firmware exits but has probably to be further developed.

The final MCM-board

- The design in HDI technology will start soon but will not be completed until we have got some test results from the new test board.
- Tests of a small sample SALTRO16 chips with the new test board, can be performed with the present firmware, in order to make sure that the routing for the CPLD is correct.
- As soon as this is established the design of the final MCM-board can be completed and the PCB can be ordered.
- Soldering tests with empty packages will be performed by the Electronics Workshop at DESY.
- After successful tests of the packaged chips, the MCM-boards will be mounted by the Electronics Workshop at DESY.

Cooling

Contact was established with Filippo Bosi, whose group in Pisa is working on micro channel cooling within the AIDA2020 project. He offered himself to develop a cooling system for our puprose.

A mockup board was sent to us by Takahiro Fusayasu and was forwarded to Pisa. This board simulates one SALTRO chip ladder with 5 chips providing a realistic simulation of the power dissipation and could thus be used to test the performance of the micro channel cooling.

On the 14.12.2017 I learnt that Filippo had suffered from serious heart problems.

Plans for the next future

- Mount the test socket and connectors to the test board.
- Test the funktionality of the test board with already tested SALTRO16 chips.
- When we are convinced that everything is ok, continue with the design of the final MCM board.
- Continue to look for a FPGA-programmer.