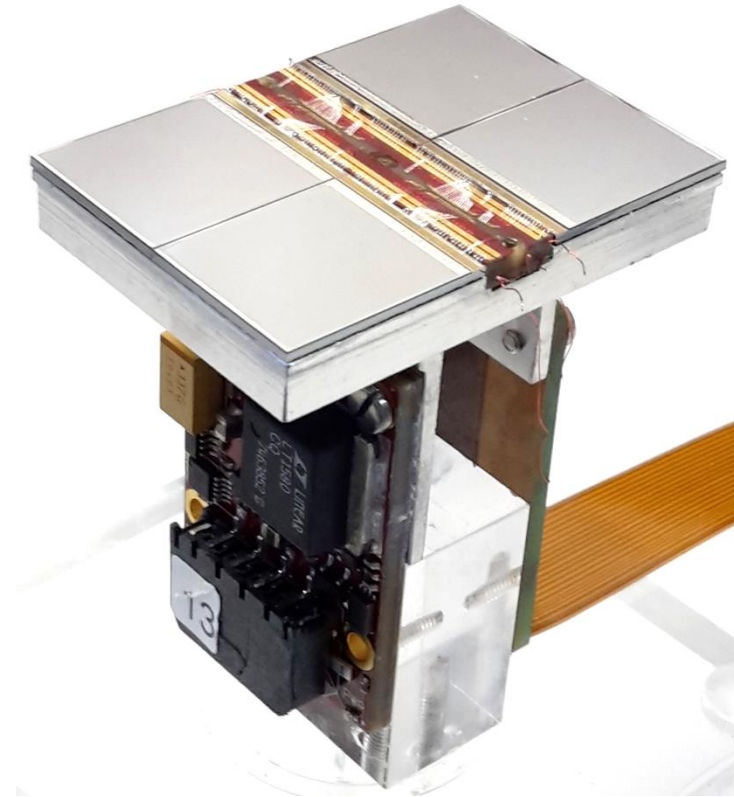


Fred Hartjes

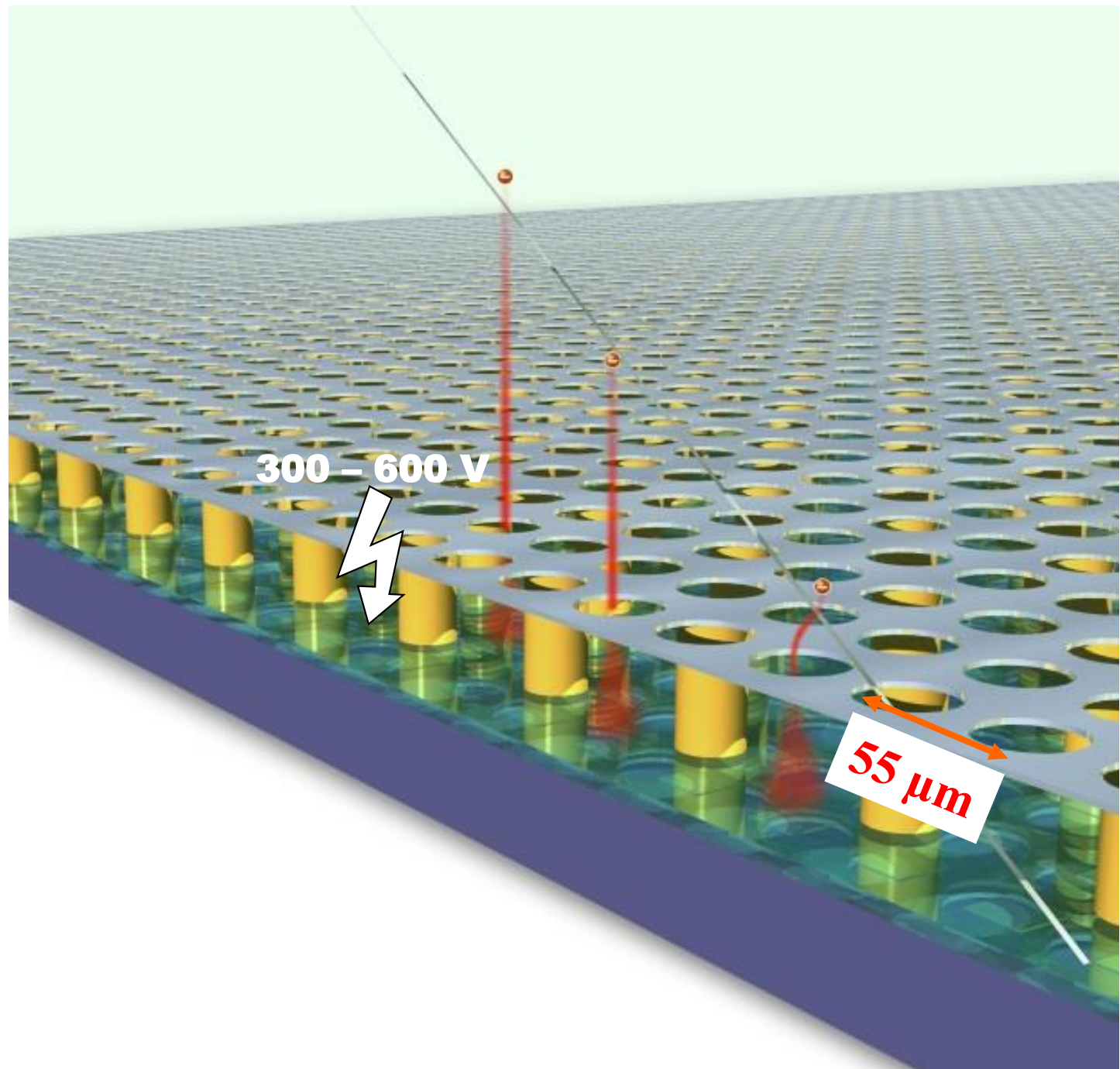
On behalf of  
Nikhef  
and  
Physikalisches Institut  
Universität Bonn



# GridPix technology

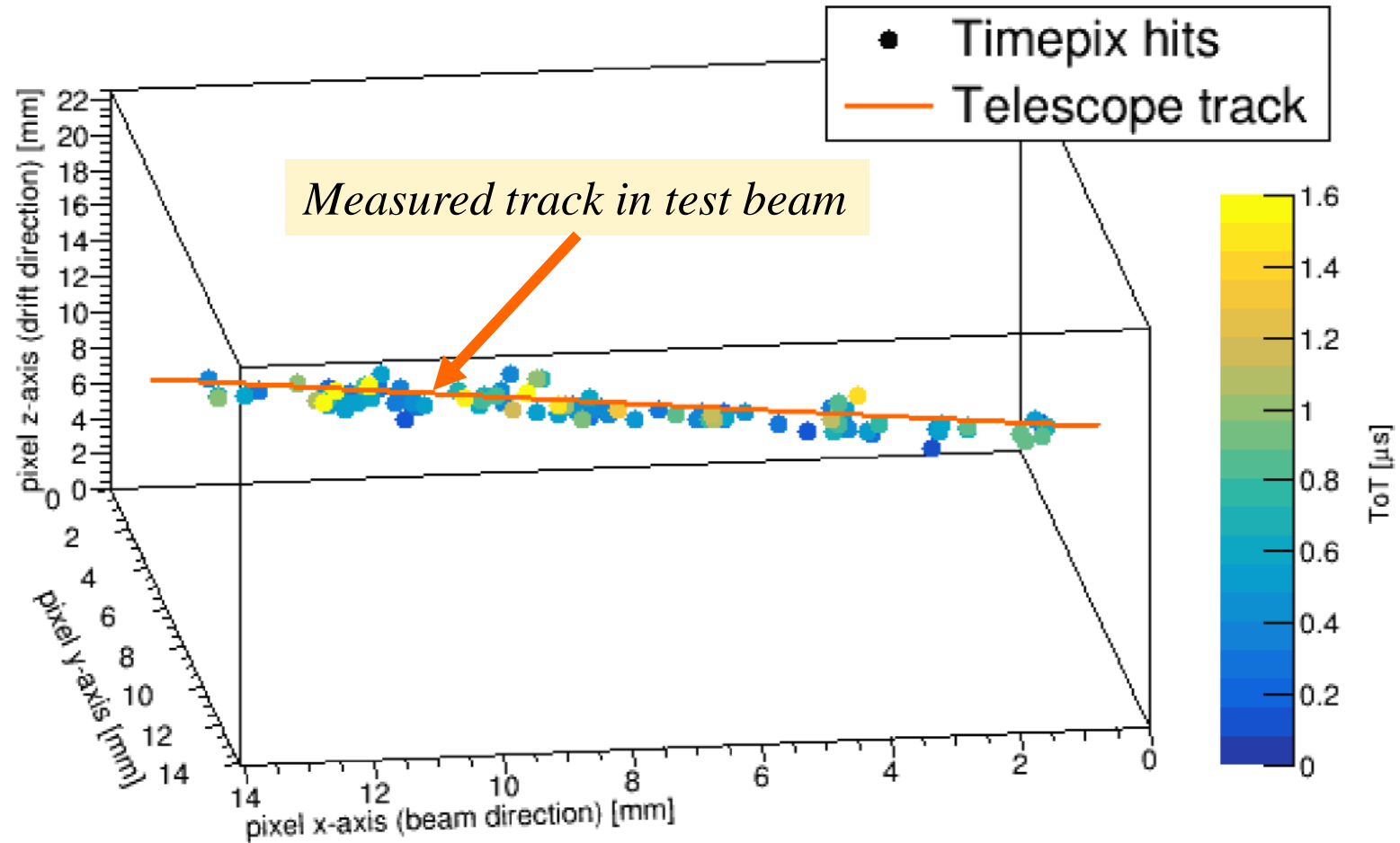
- Pixel chip with integrated Micromegas
- => **InGrid**
- Grid set at negative voltage (300 – 600 V) to provide gas amplification
- Very small pixel size (55  $\mu\text{m}$ )
- => mostly detecting **individual electrons**

*GridPix chip*



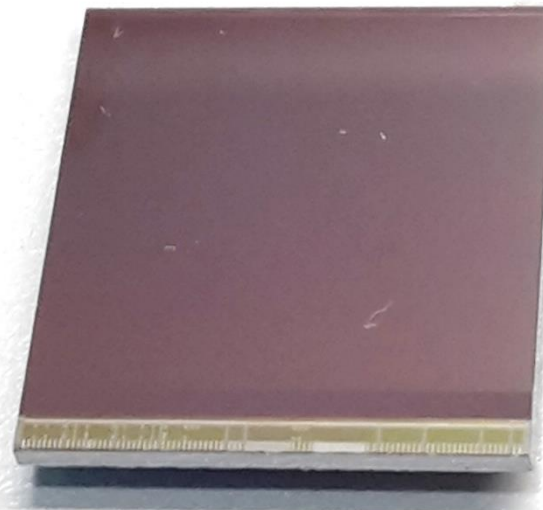
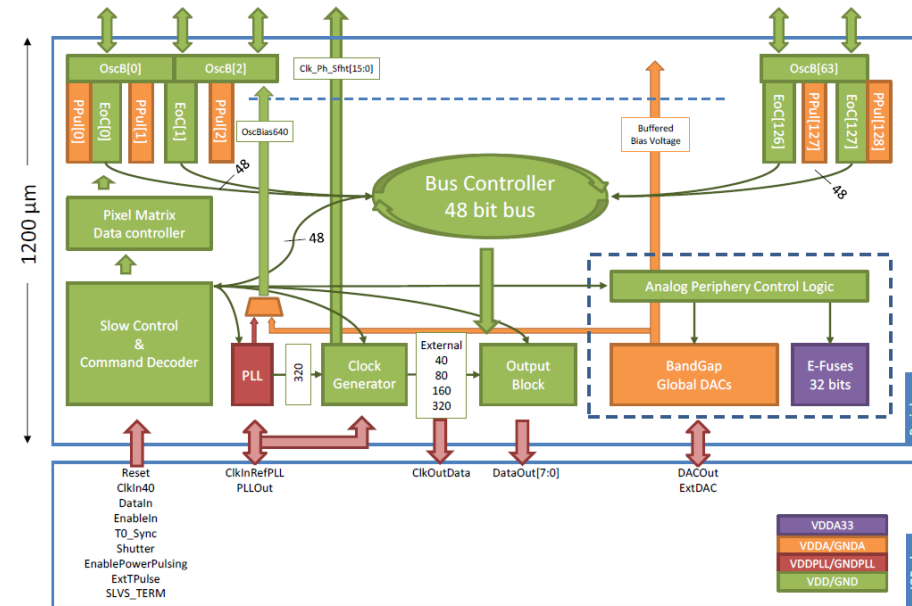
# GridPix: detecting individual electrons

- Uses the **complete information** of the ionization profile
- The **best resolution** that can be obtained with a gaseous detector
  - $dE/dx$  by single electron counting
- **Fine granularity** enables **rejecting background tracks** and **deltas** in offline analysis



# Pixel chip: TimePix3

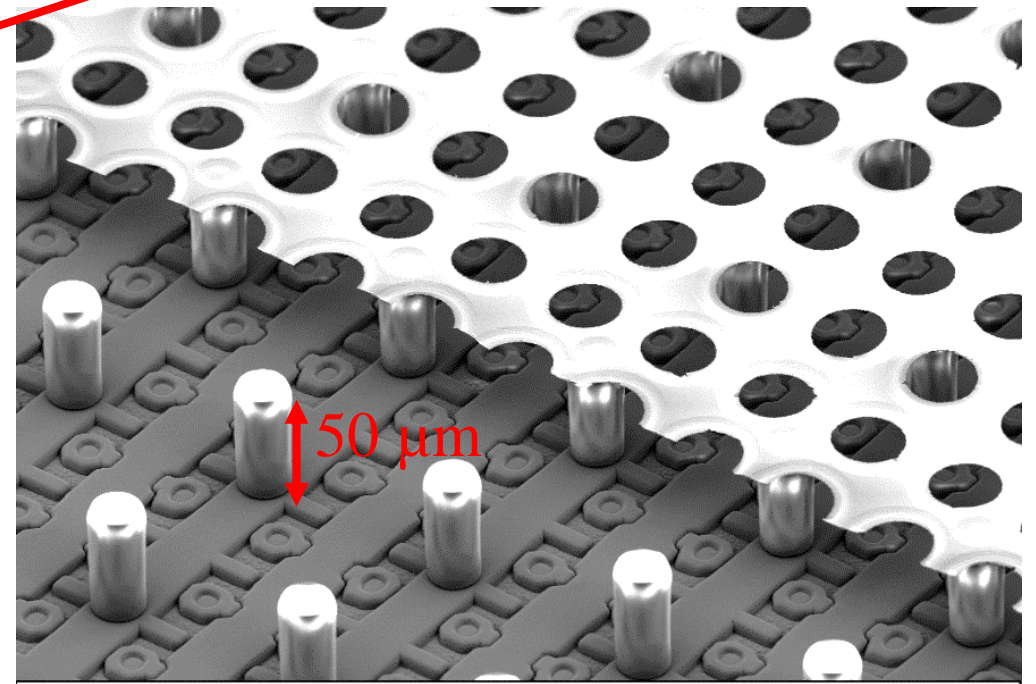
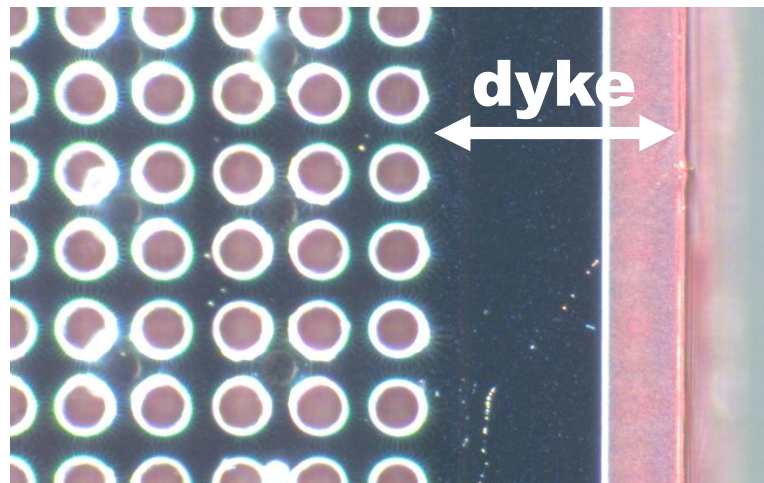
- 256 x 256 pixels
- 55 x 55  $\mu\text{m}$  pitch
- $\Rightarrow$  14.1 x 14.1 mm sensitive area
- TDC with **610 MHz clock (1.64 ns)**
- Used in the data driven mode
  - Each hit consists of the **pixel address** and **time stamp** of arrival time (ToA)
  - Time over threshold (ToT) is added to register the signal amplitude
  - $\Rightarrow$  **compensation for time walk**
  - **Trigger** (for  $t_0$ ) added to the data stream as an additional time stamp
- High power consumption
  - $\sim 1 \text{ A @ } 2 \text{ V}$  (2W), depending on hit rate
  - $\Rightarrow$  good cooling is important





# TimePix3 equipped with InGrid

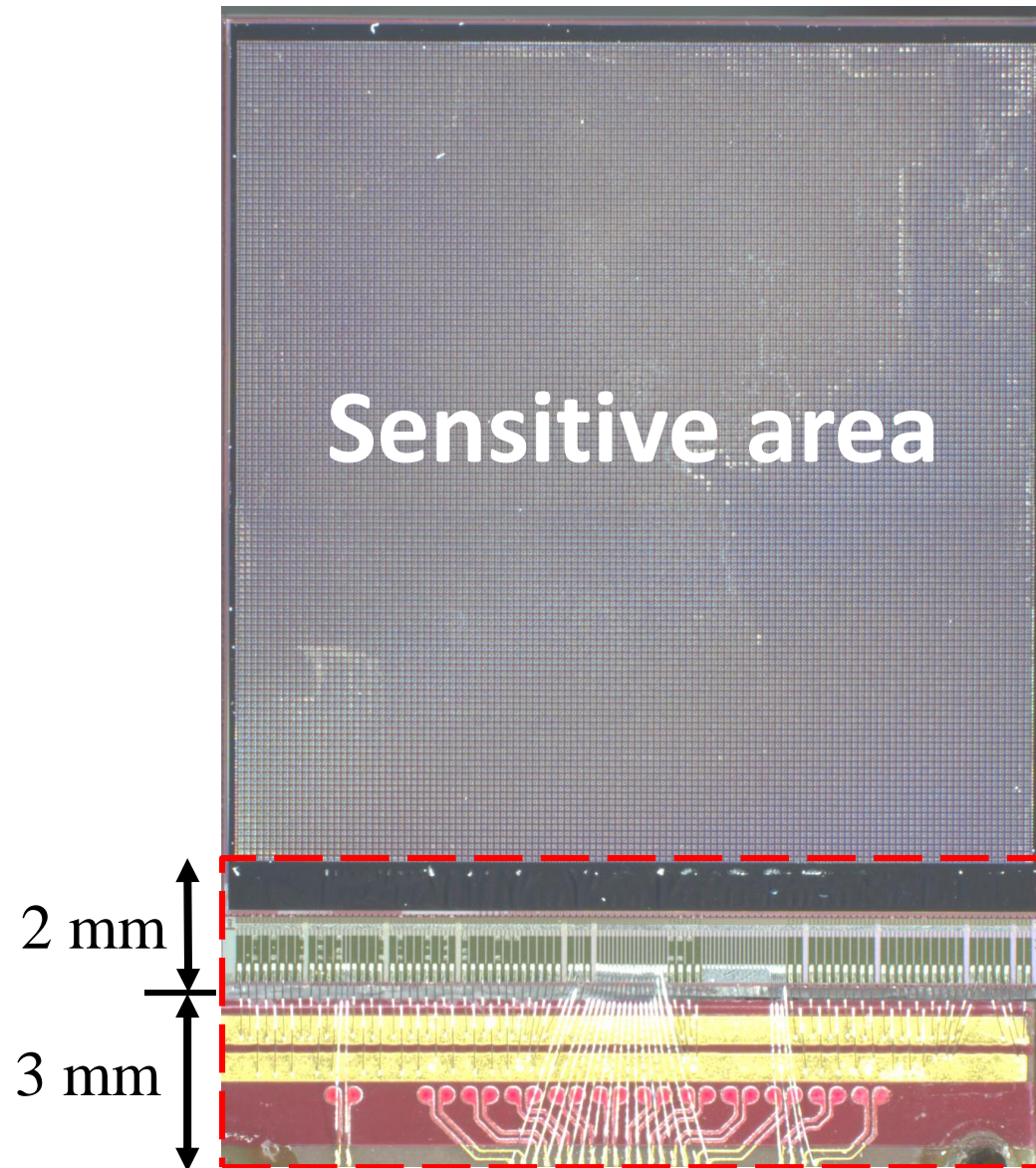
- Wafer post-processing at IZM Berlin
- Aluminium grid (1  $\mu\text{m}$  thick)
- 35  $\mu\text{m}$  wide holes, 55  $\mu\text{m}$  pitch
- Supported by SU8 pillars 50  $\mu\text{m}$  high
- Grid surrounded by SU8 dyke (150  $\mu\text{m}$  wide solid strip) for mechanical and HV stability



Mag = 250 X Signal A = SE2  
WD = 14.3 mm EHT = 10.00 kV  
20  $\mu\text{m}$   
Stage at T = 50.0 °  
Chamber = 6.64e-004 Pa  
Fraunhofer IZM

# Maximizing active area

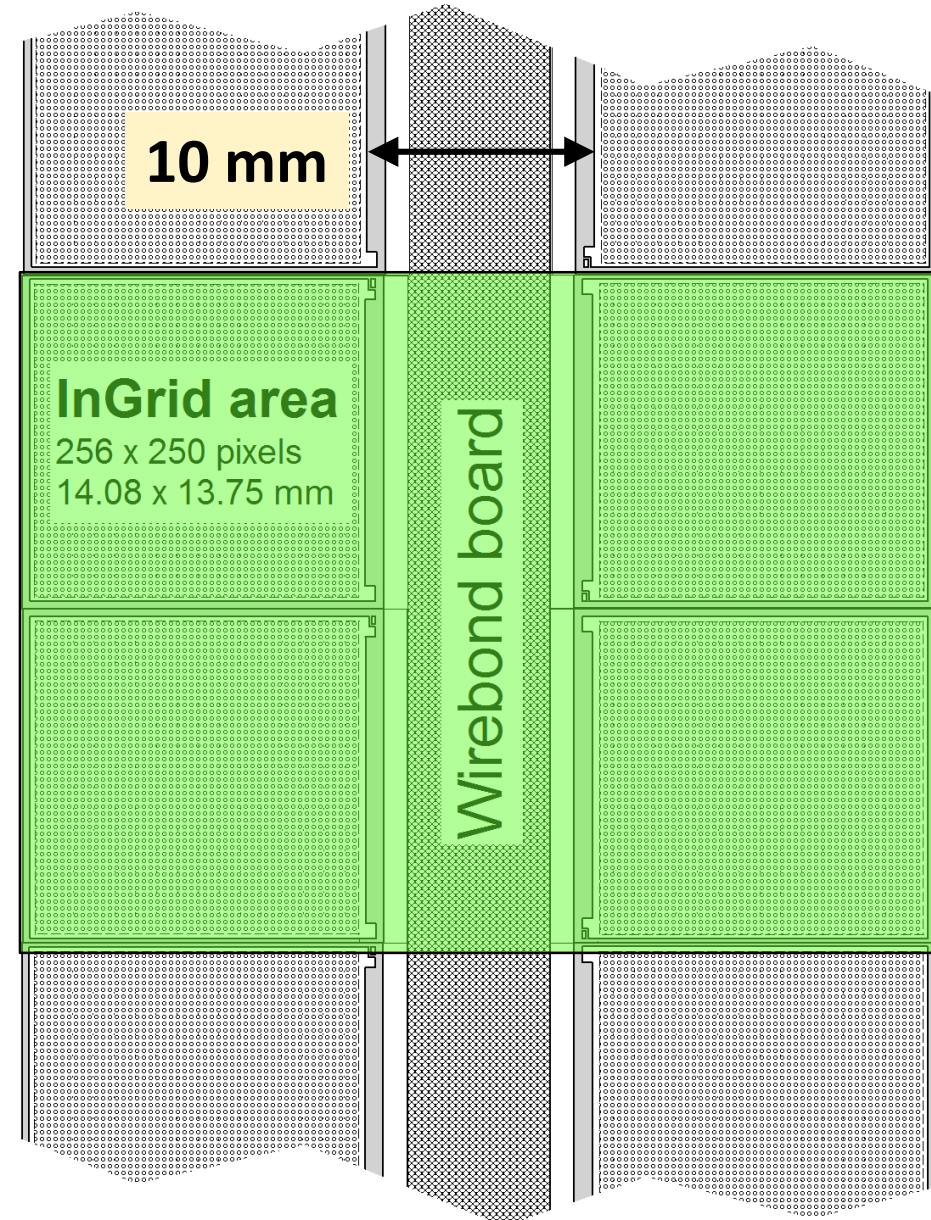
- Using TimePix3 chip
- Wirebond board squeezed to smallest width possible => **3 mm**
- Inactive zone (wirebond pads + electronics) => **2 mm**
- => we need a **5 mm wide inactive zone per chip for connection + electronics**
- (only applies when the connecting PCB is shared with an opposite chip)





# Getting the optimal detector size

- 1 x 2 chips
  - Not sufficient space (14 mm) for a LV stabilisation, chip control lines and a data RO
- **2 x 2 chips (QUAD)**
  - All fits
- $\geq 3 \times 2$  chips
  - Less flexible, lower yield, more handling risk



# Covering large detection areas: QUAD

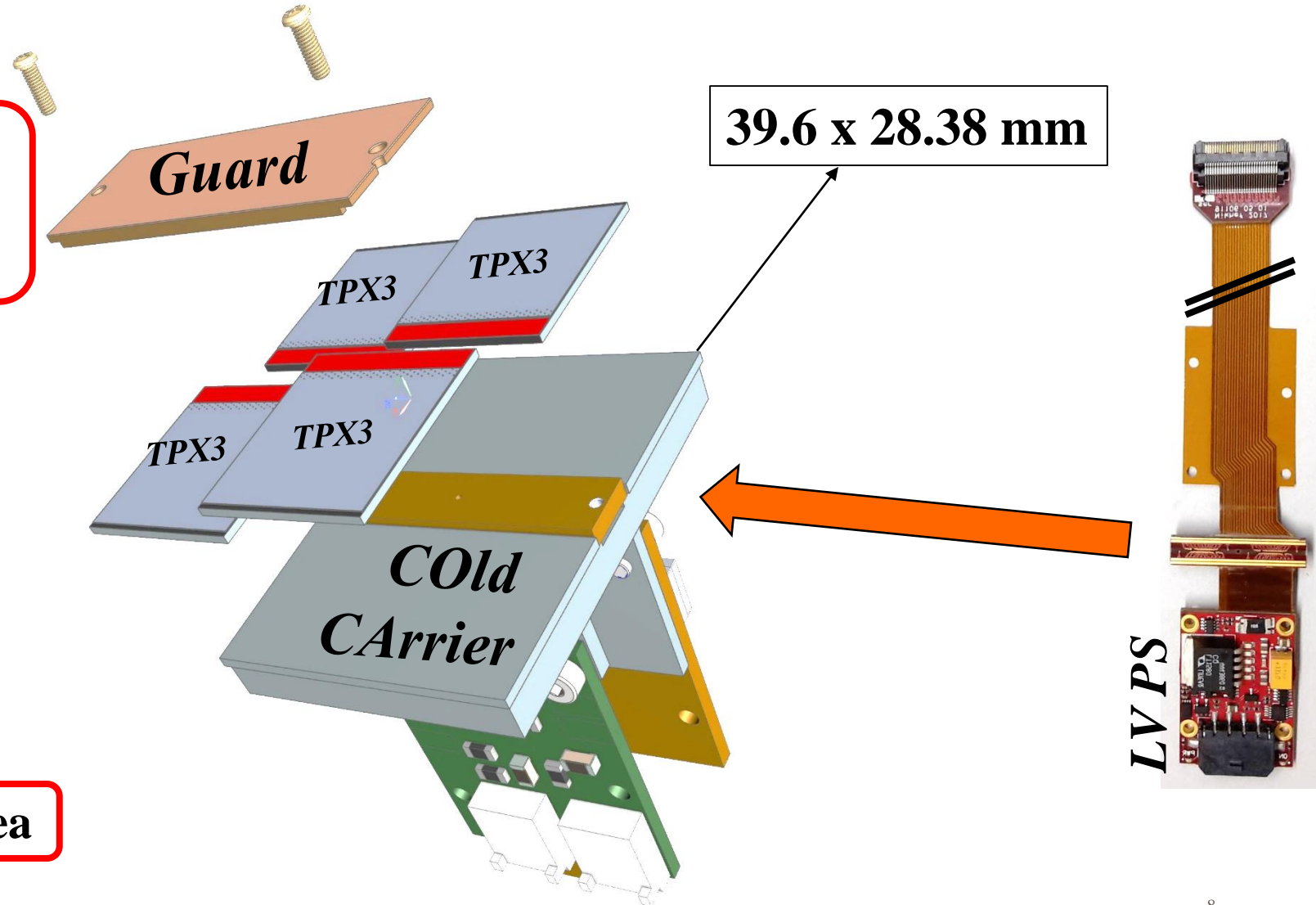
- Four-TimePix3 chips

■ All services (signal IO, LV power) are located **under** the detection surface

- The area for connections was squeezed to the minimum

- Detection surface can be extended by adding other QUADs at all 4 sides

■ => **no limit on detection area**





# Assembled QUAD

- QUAD has a sensitive area of 68.9%

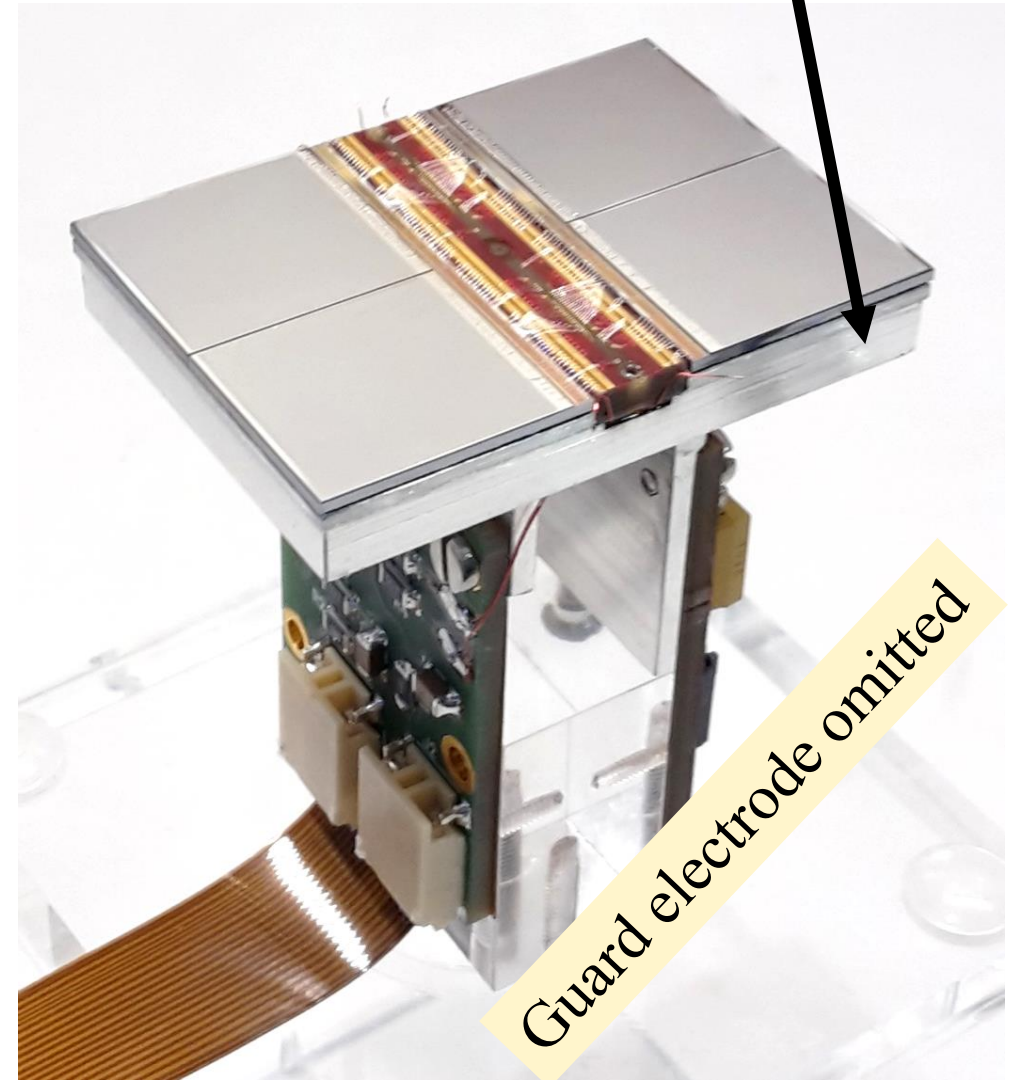
QUADs being produced in series  
(14 QUADs)



**Commercialization under study**

Contact us if you are interested

Cold Carrier  
(COCA)



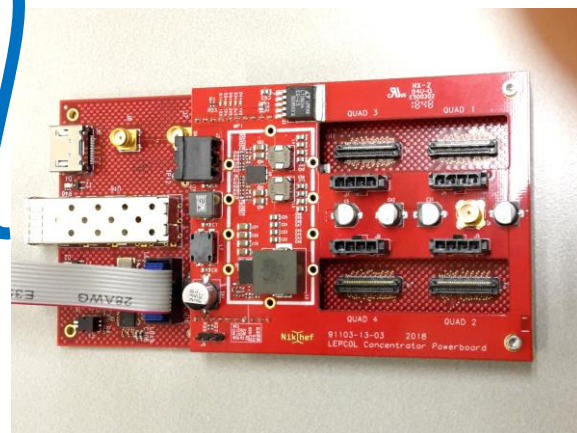
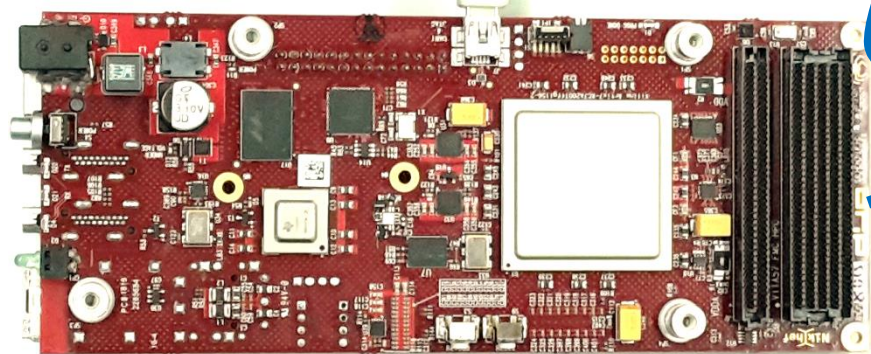
**Guard electrode omitted**

# DAQ

## SPIDR board

Optical link

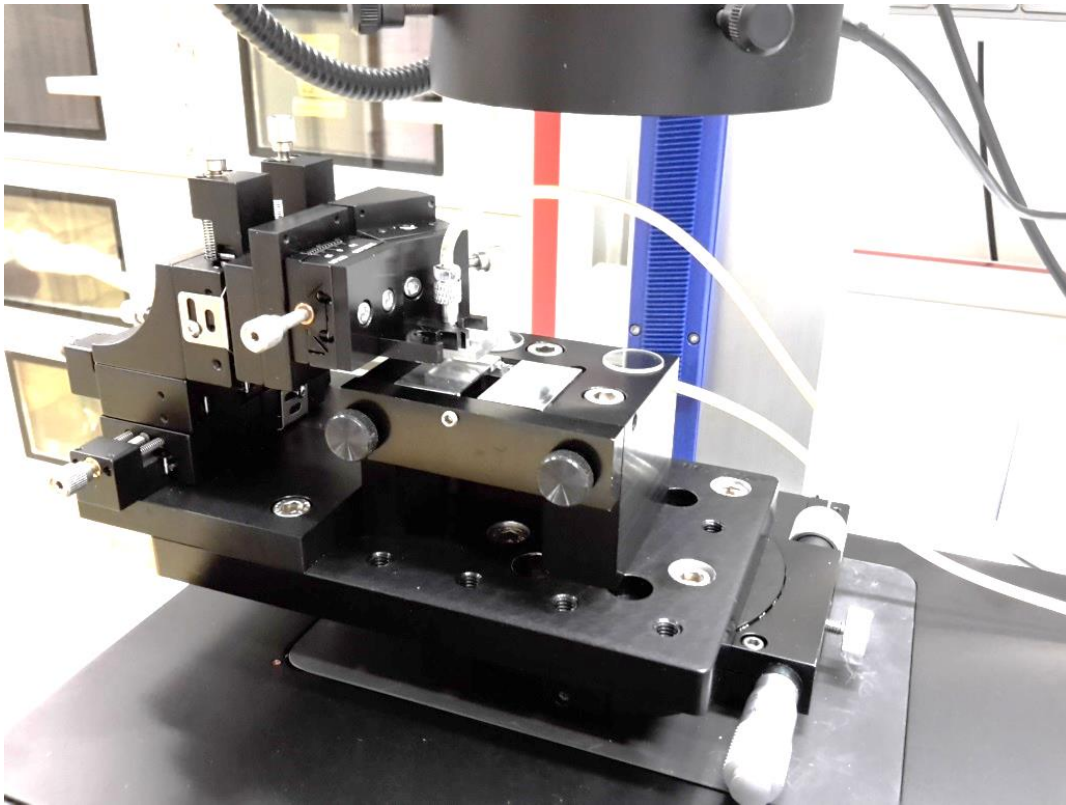
## Concentrator



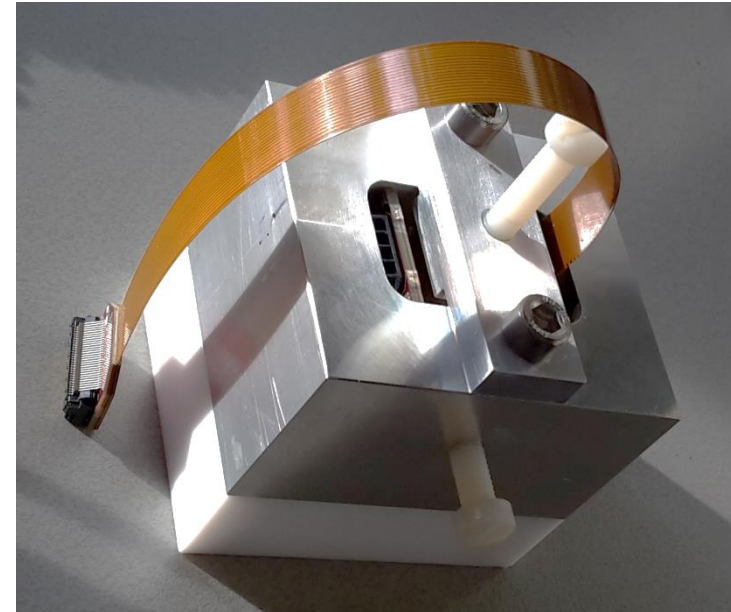
# QUAD's tooling

- Based on small production quantities (up to ~ 50)

## Chip alignment jig



## Gluing tool



## Pickup tool for chip with InGrid



# Chip alignment

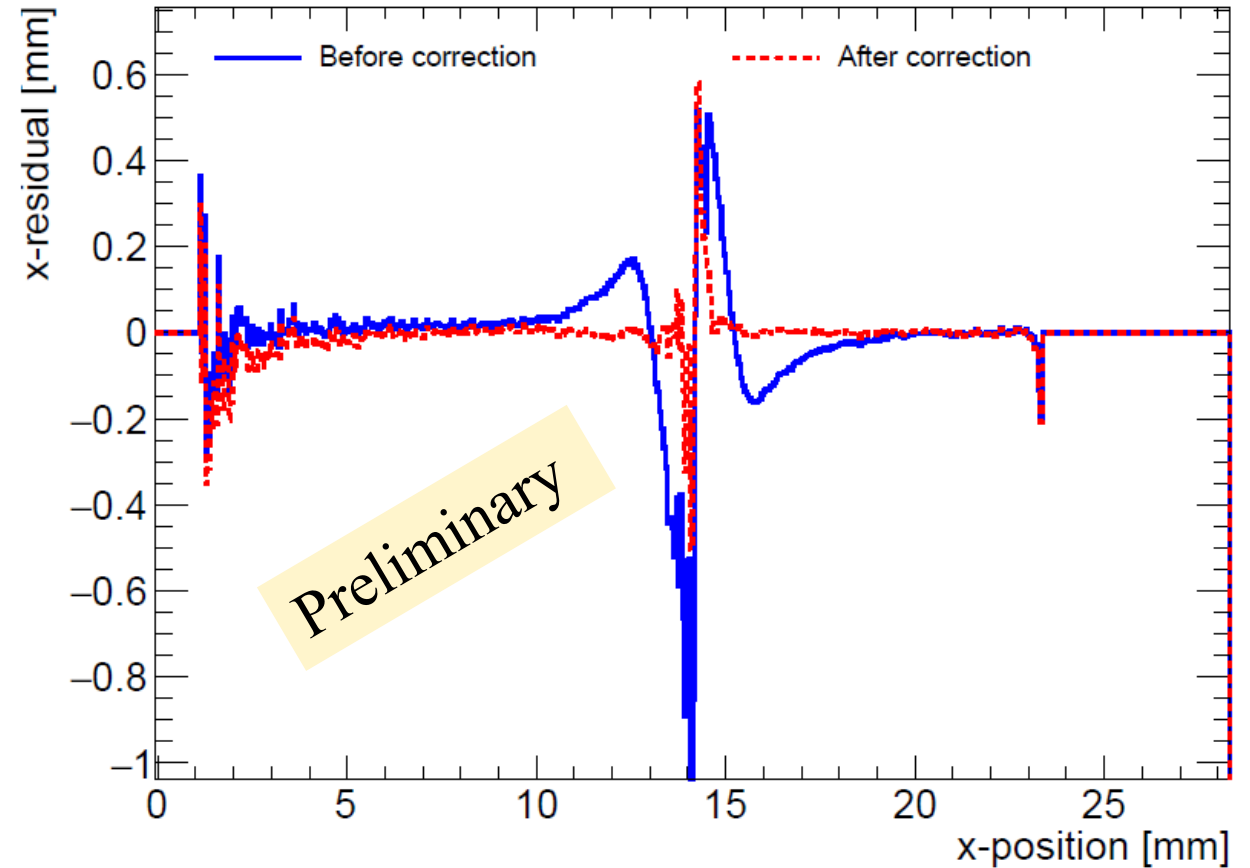
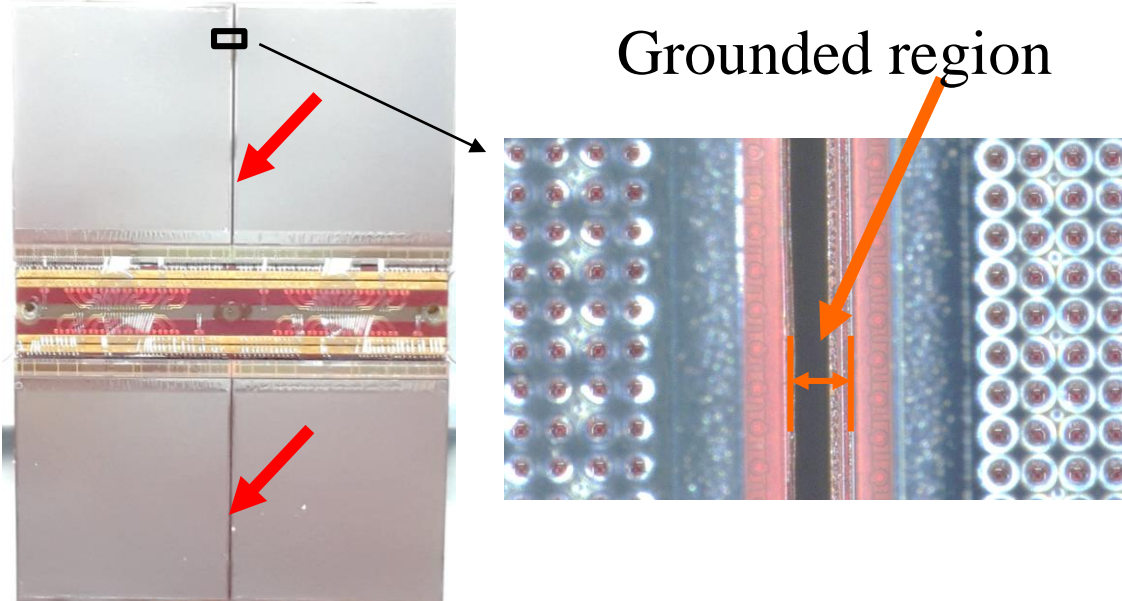
- Semi automatic under LabVIEW
- Referring the precise edges of the COCA to the bonding pads
- Aimed accuracy 20  $\mu\text{m}$  in X,Y and Z



# ■ Last testbeam: small deformations QUAD edge deformations

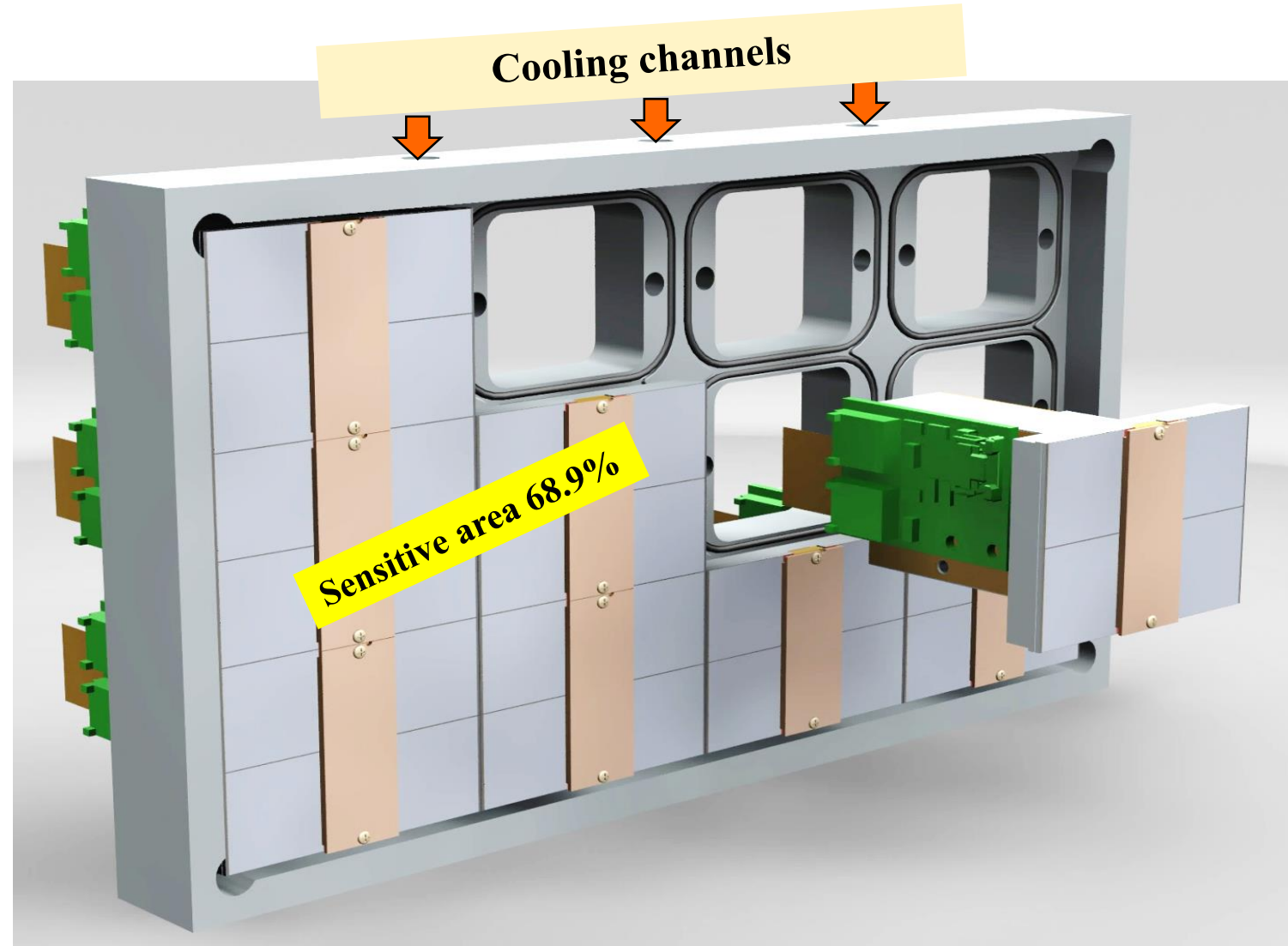
due to

- Dead zone between chips
  - Grounded region between chips
- May be corrected by fitted correction function or adding proper **guard electrode**



# QUAD as a building block

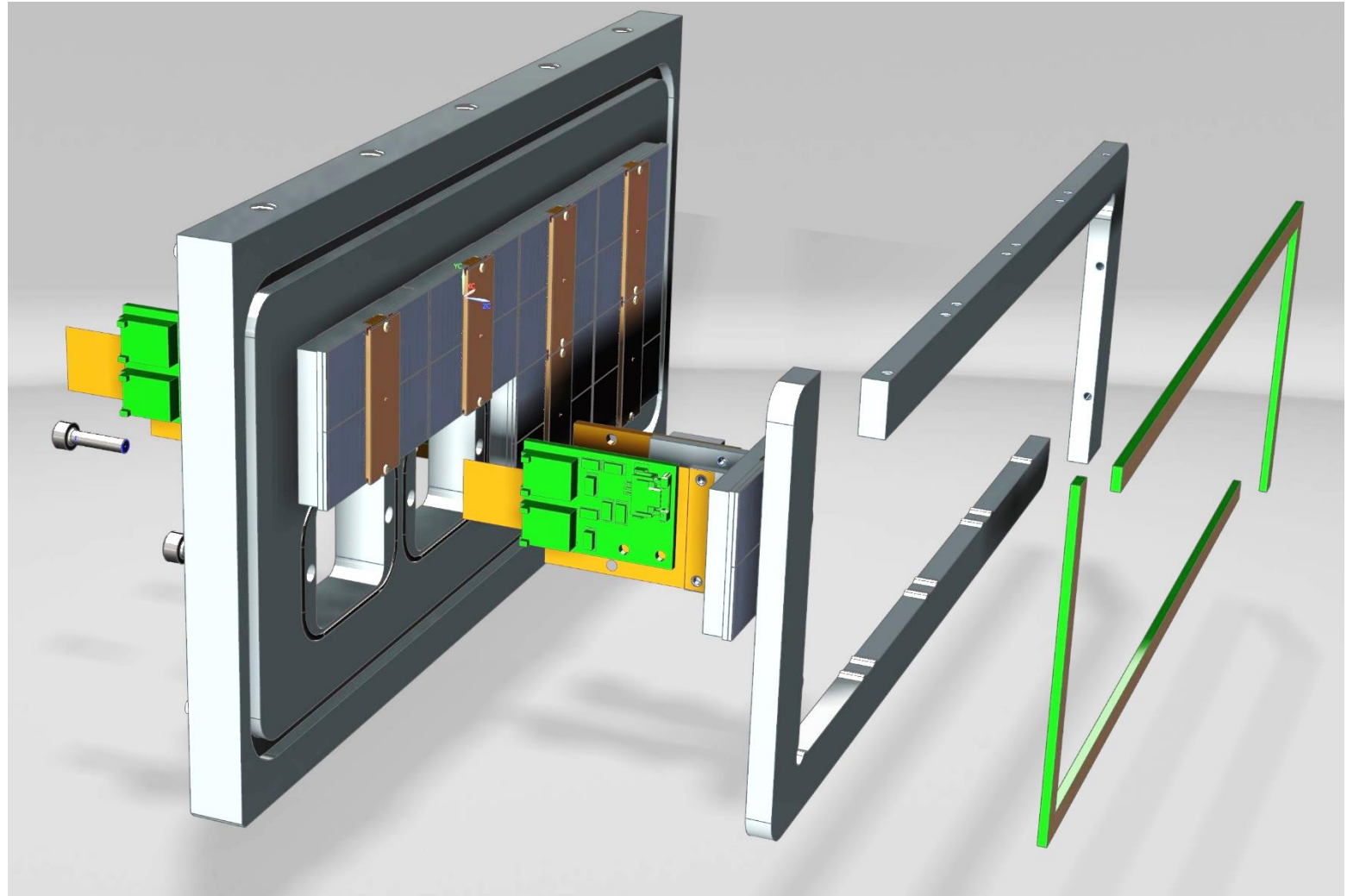
- Building blocks of **39.6 x 28.38 mm**
- Unlimited surface may be covered
- Plug in QUADs into a cooled gastight mounting plate
- Push them from two sides to a mechanical reference





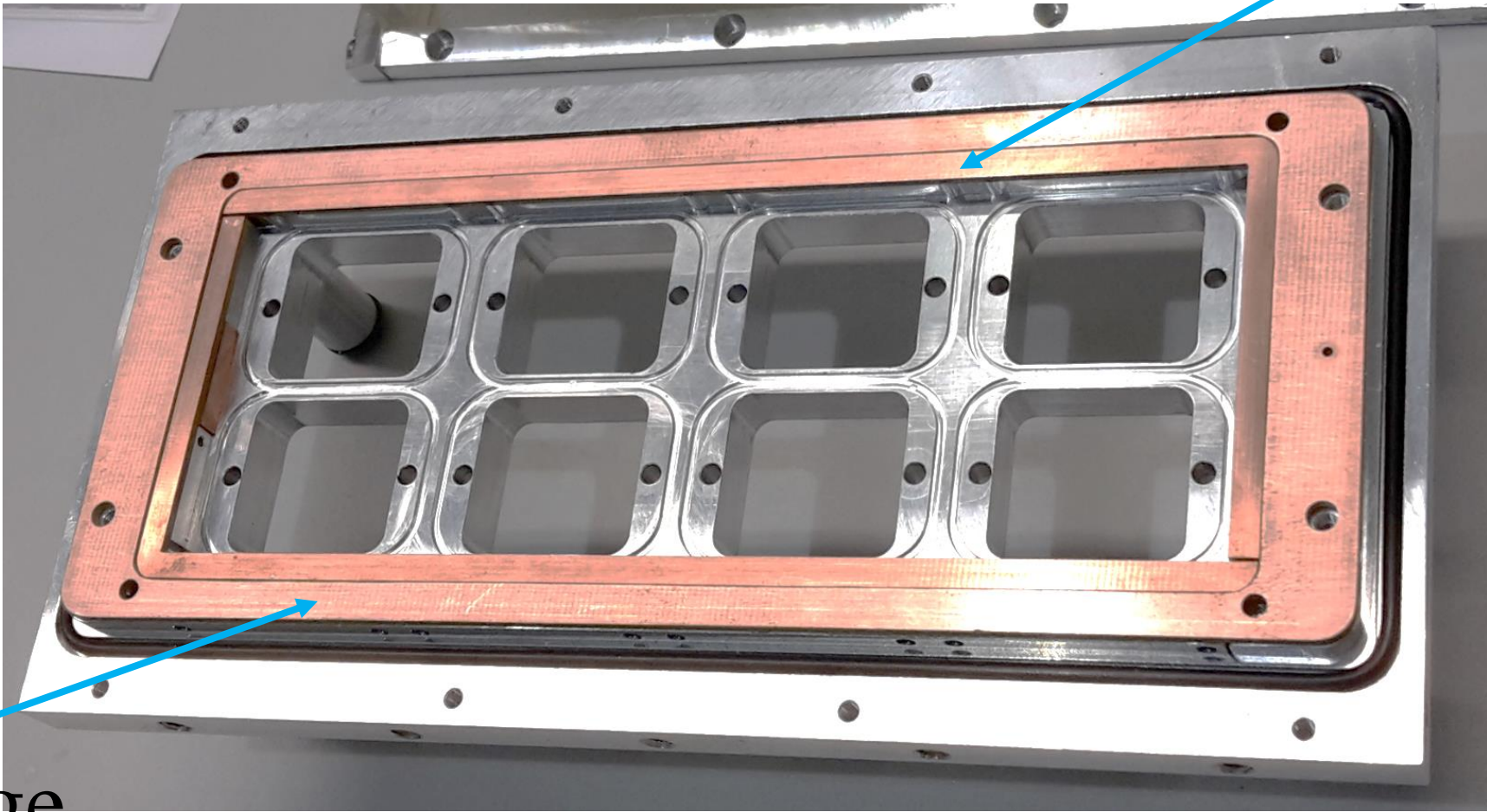
# Testbox for 2 x 4 QUADs

- Being assembled
- Presently liquid cooling
  - Glycol



# Guard structure around the QUADs

Guard

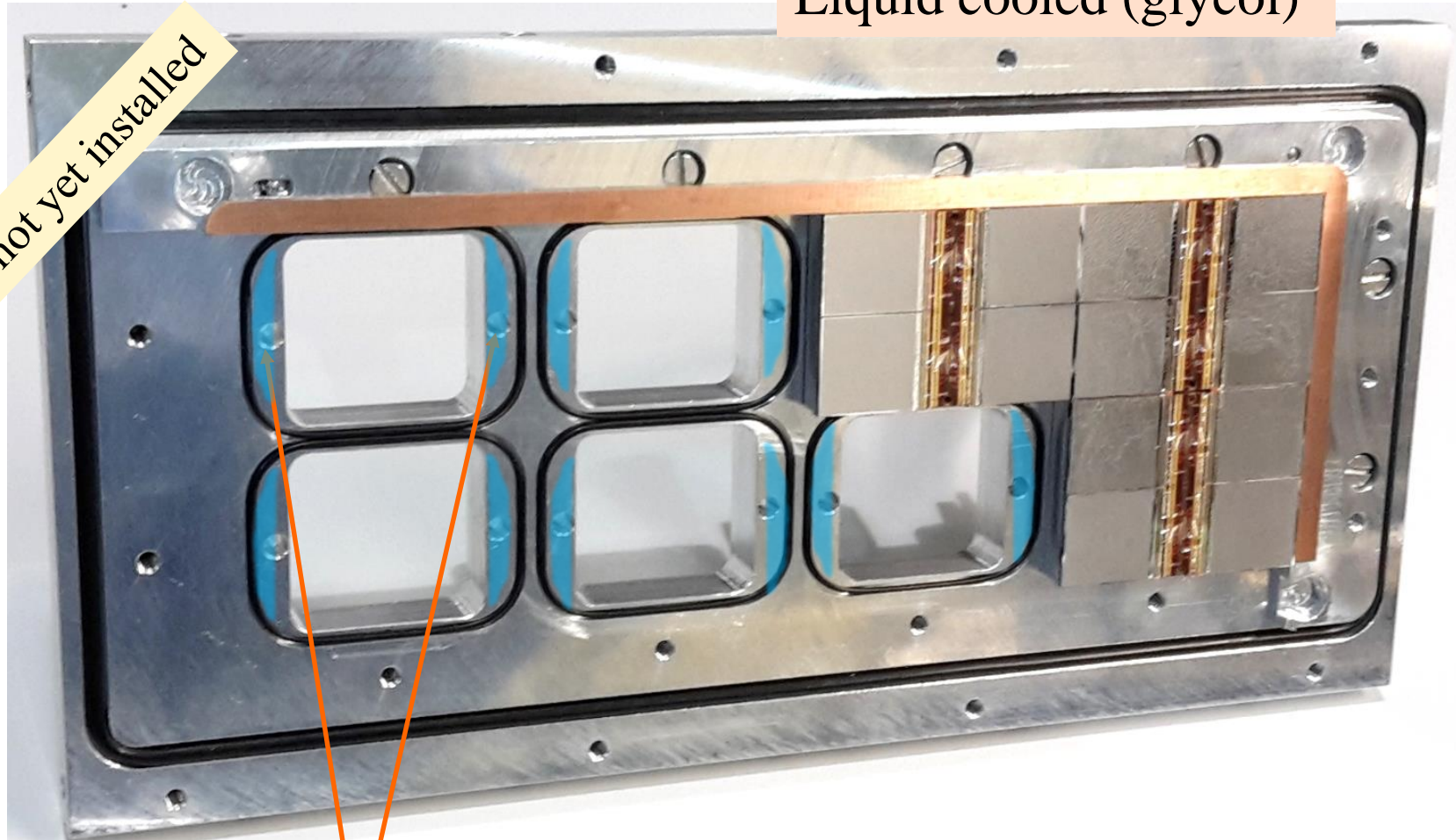


Base  
field cage

# Mounting plate for 8 QUADs being assembled

Liquid cooled (glycol)

Guard electrodes not yet installed

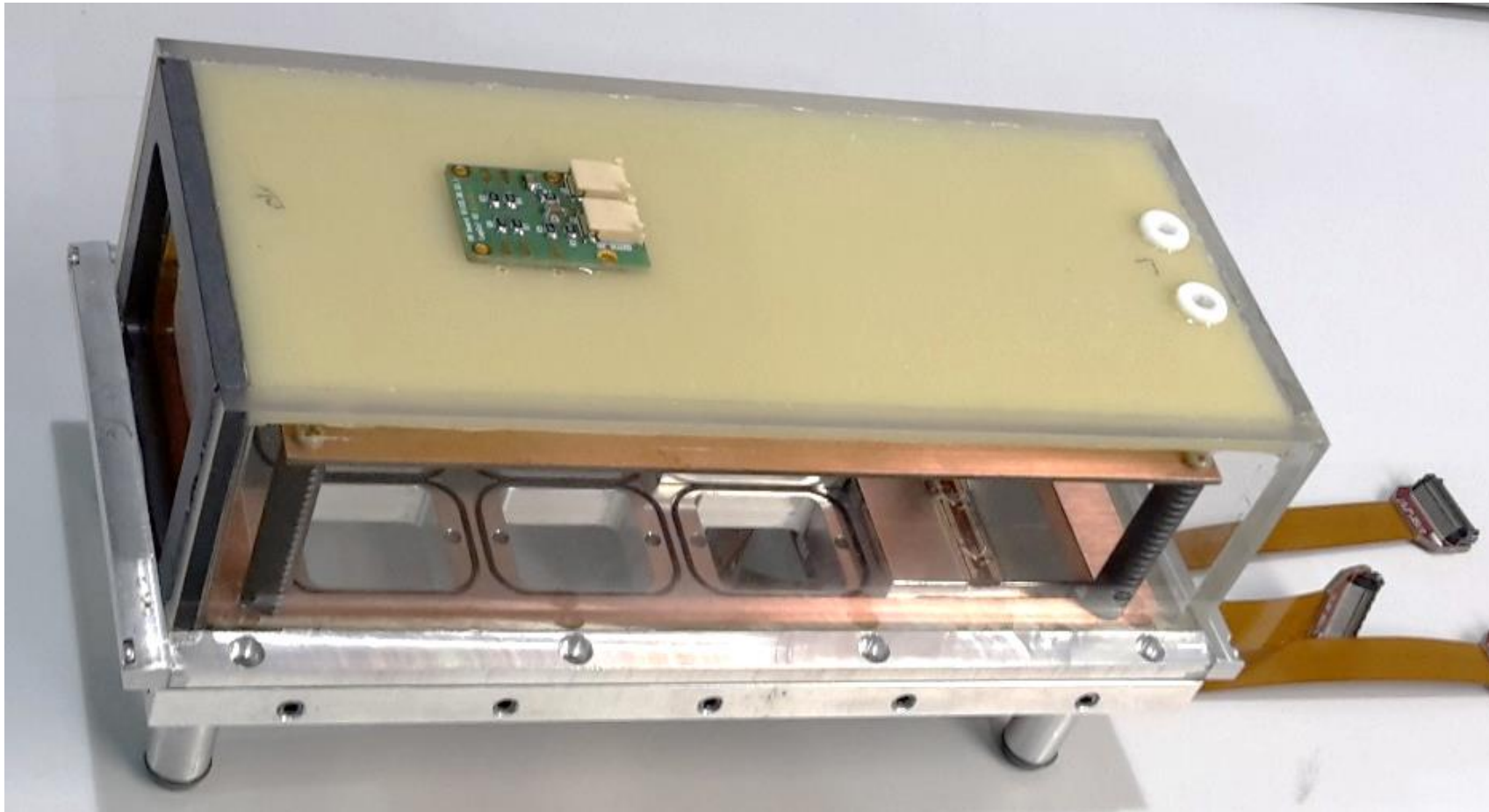


Thermal grease  
(outside gas volume)



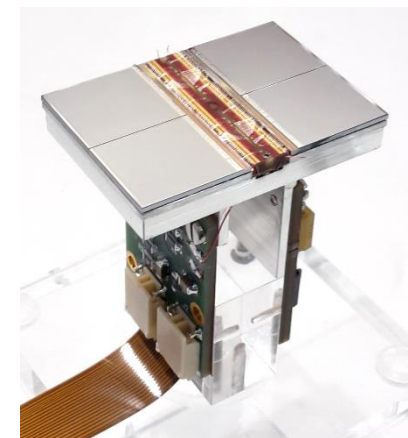
# Testbox in assembly

Windows of optical glass for UV laser measurements



# Conclusions

- Since 2017 three TimePix3 wafers were successfully equipped with an InGrid
  - Last two (low yield) wafers carried 88 electrically usable chips
  - Only a few were rejected because of grid problems
- The QUAD we present as a building block to populate an ILCTPC module
- A beam test showed the need for a narrow guard electrode structure covering the gap between the chips
- Presently the QUAD can be produced in limited quantities
  - One QUAD per two days can be achieved
  - A production of 14 QUAD modules is close to finish
- A testbox carrying 2 x 4 QUADs is being assembled
  - UV laser tests: focused and parallel beam (ionization in the gas)
  - Testbeam (Bonn)



This work is done by the effort of:

Yevgen Bilevych, Klaus Desch, Jean-Paul Fransen,  
Harry van der Graaf, Markus Gruber, Fred Hartjes, Bas  
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**Nikhef**

and

**Physikalisches Institut Universität Bonn**

