HG/LG Inter-Calibration and Gain Stability

12.12.2018

AHCAL Main Meeting at DESY

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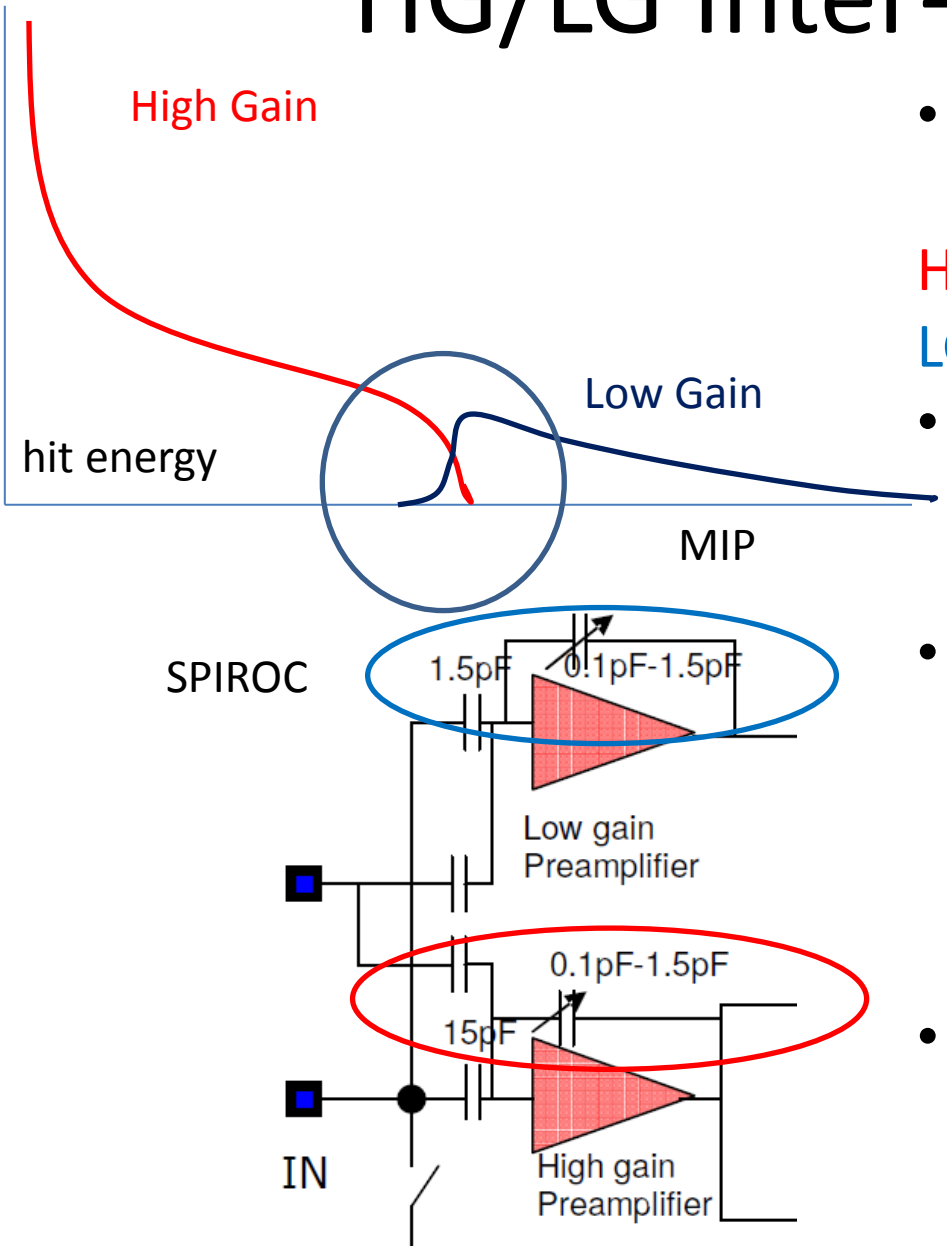
HG/LG Inter-Calibration



- SPIROC2B/2E has 2 signal output lines. High Gain and Low Gain

HG -- small deposited energy hits

LG -- large deposited energy hits

- In principle, IC factor is constant and just depends on ratio of capacitors. (IC ~20 for TB 2018)
- But IC factor is different for each channel due to an uneven quality of capacitance and parasitic capacitance.
  →measurement is important
- After inter-calibration, HG and LG output of hit energy should be connected smoothly

Methods to extract IC factor

LED runs

- slope of HG_ADC vs LG_ADC
- ΔHG_ADC/ Δ LG_ADC

Challenges

- Pedestal shift
- linear range selection
- IC factor extraction with beam runs

IC factor from LED runs dHG_ADC/dLG_ADC

- Small LED V step is required to cancel out or reduce impact of pedestal shift.

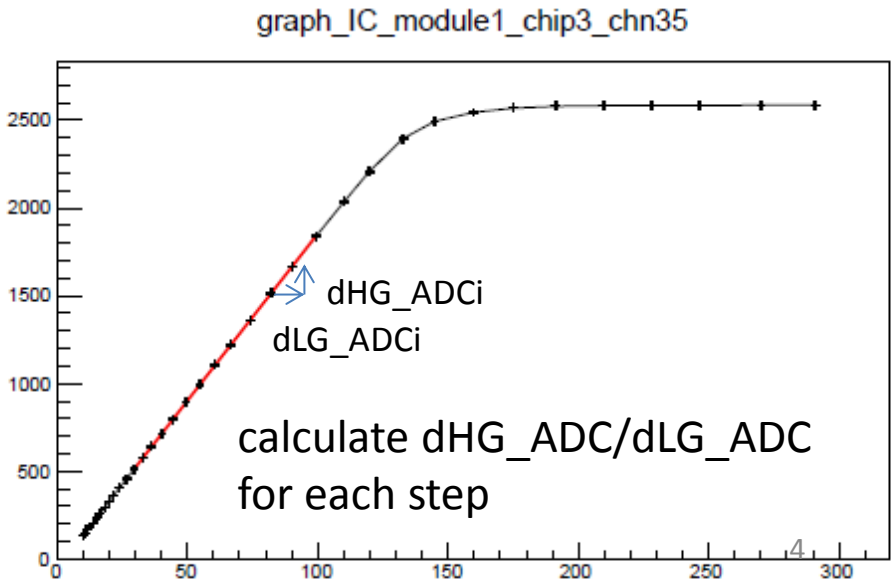
ΔLight yield * HG = $(HG\_ADC_{i+1} - HG\_ADC_i)$

ΔLight yield * LG = $(LG\_ADC_{i+1} - LG\_ADC_i)$

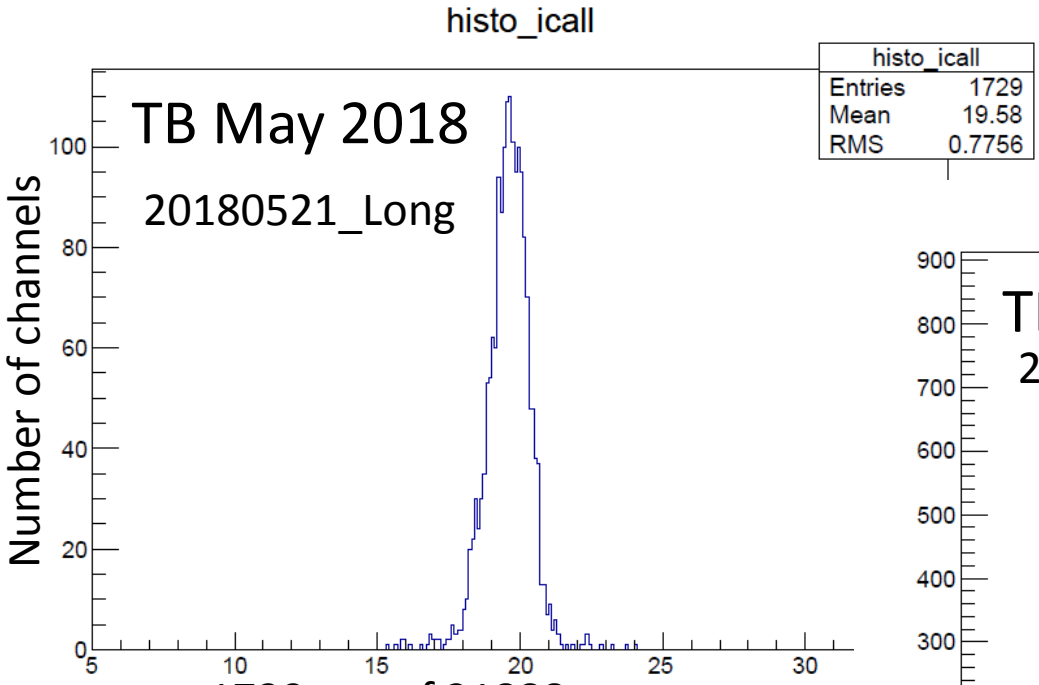
IC = HG/LG = $(HG\_ADC_{i+1} - HG\_ADC_i)/(LG\_ADC_{i+1} - LG\_ADC_i)$

constraints

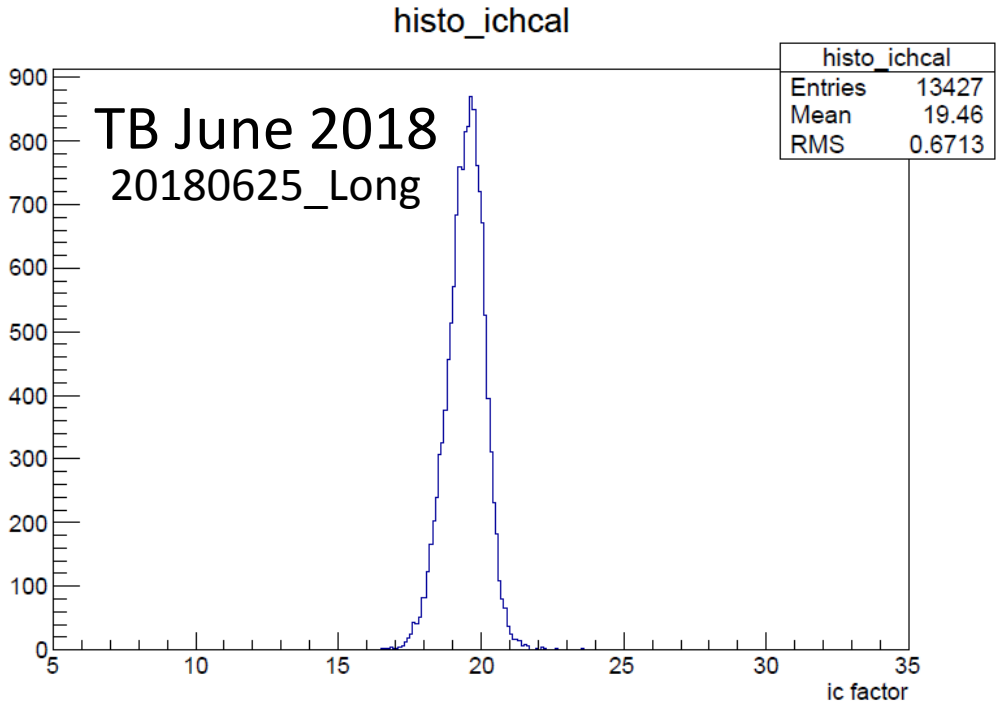
- reasonably large signal
- $HG\_ADC_{i+1} - HG\_ADC_i > 100$
- $30 < LG\_ADC_{i+1} - LG\_ADC_{ped} < 100$
- total amount of charge in a chip < 60000



LED Run May and June 2018 LG1200



1729 out of 21888
5 sets of LED run for IC
(10+1 runs)
Average of slopes and
memory cells per channel

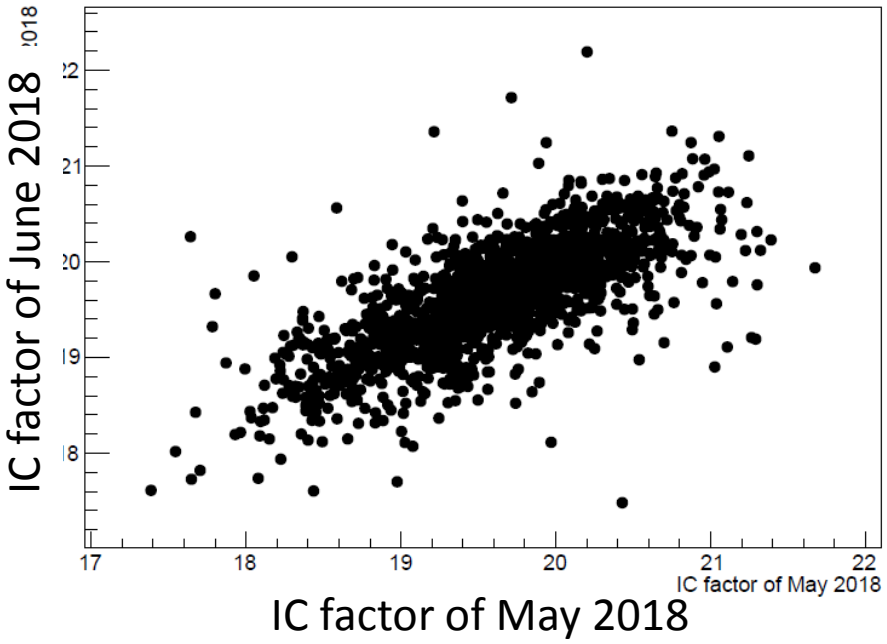


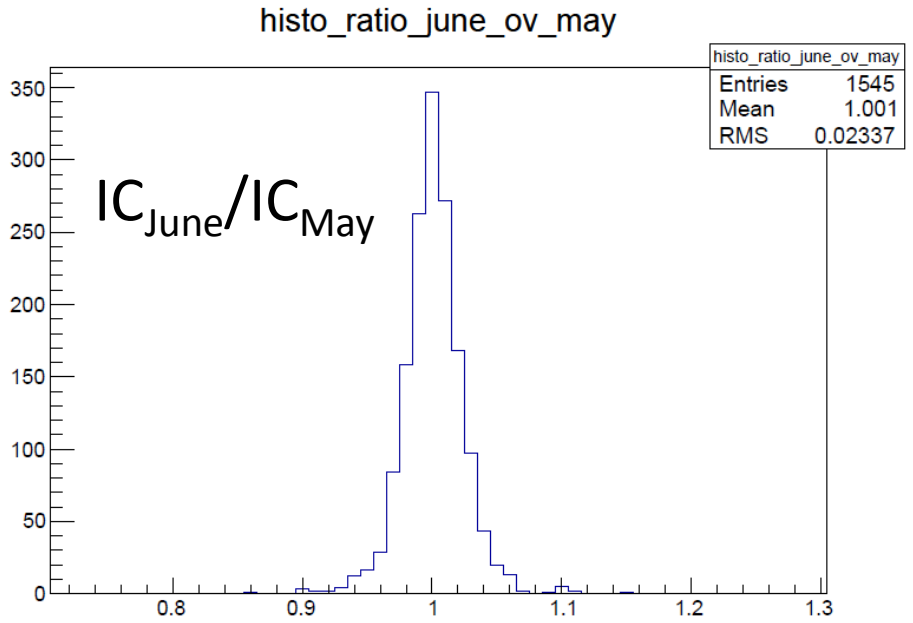
13427 out of 21888
101+1 runs

Channel-to-channel spread 3.5-4%

Comparing IC factor of June and May 2018

after reject outliers: range of plots is mean $\pm$ 3xRMS of IC histogram

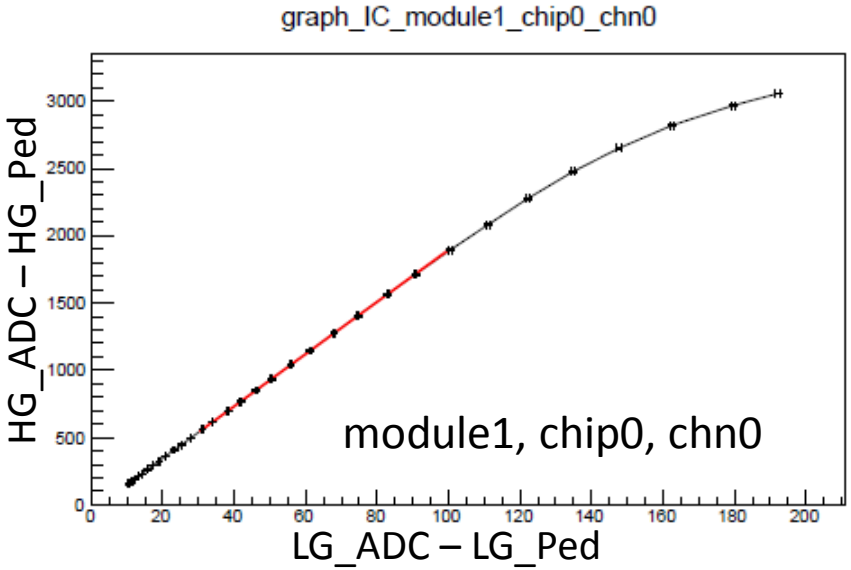


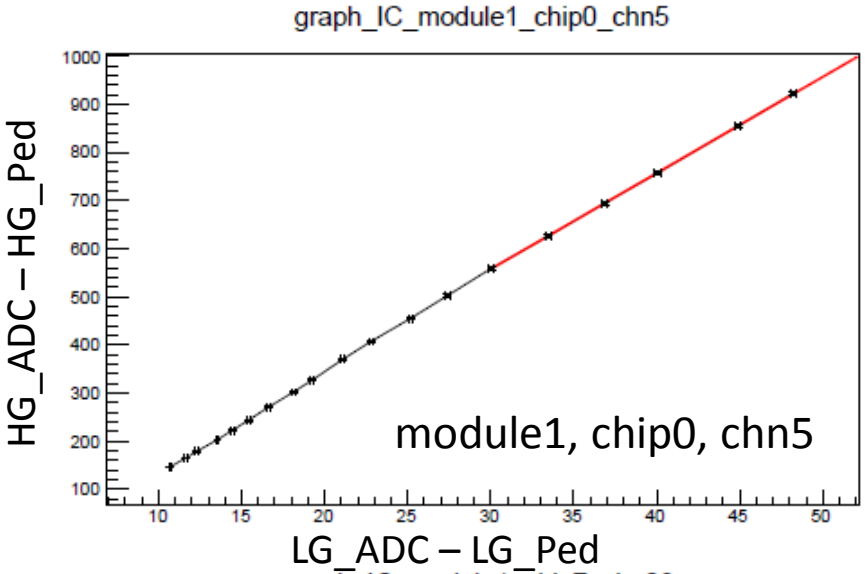


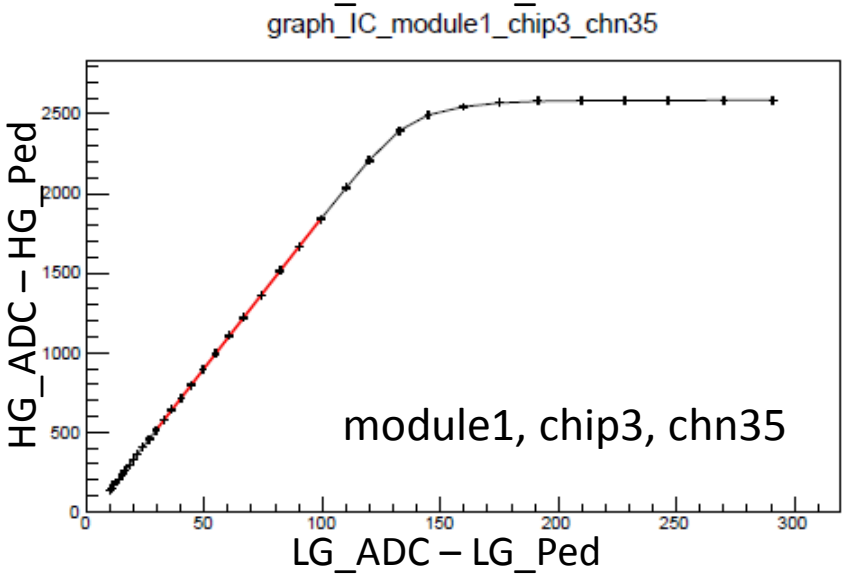
RMS of IC_{June}/IC_{May} is 2.3%, mean is 1.001 $\pm$ 0.0006

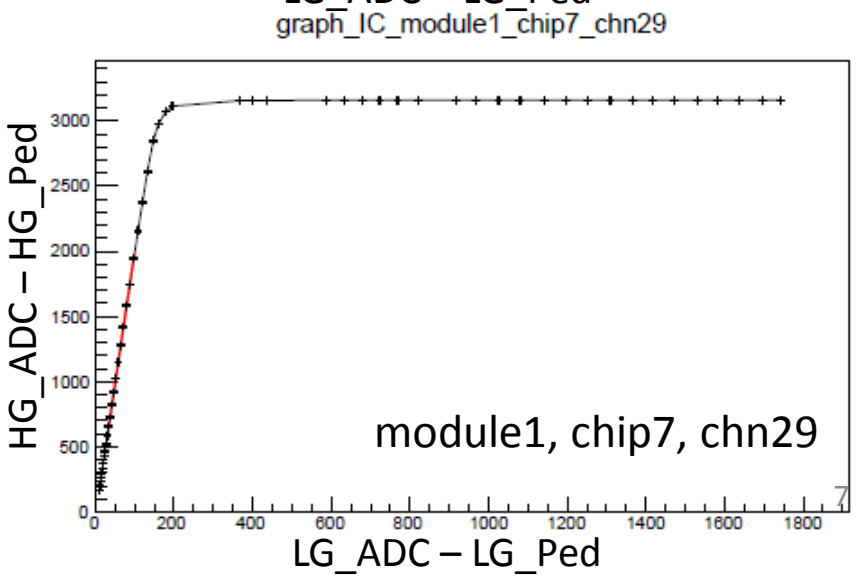
Slope of HG vs LG

- after pedestal subtraction
- fitting range 30 < LG < 100
- total amount of charge in a chip < 60000 ADC (HG)
- at least 5 points in the fitting range

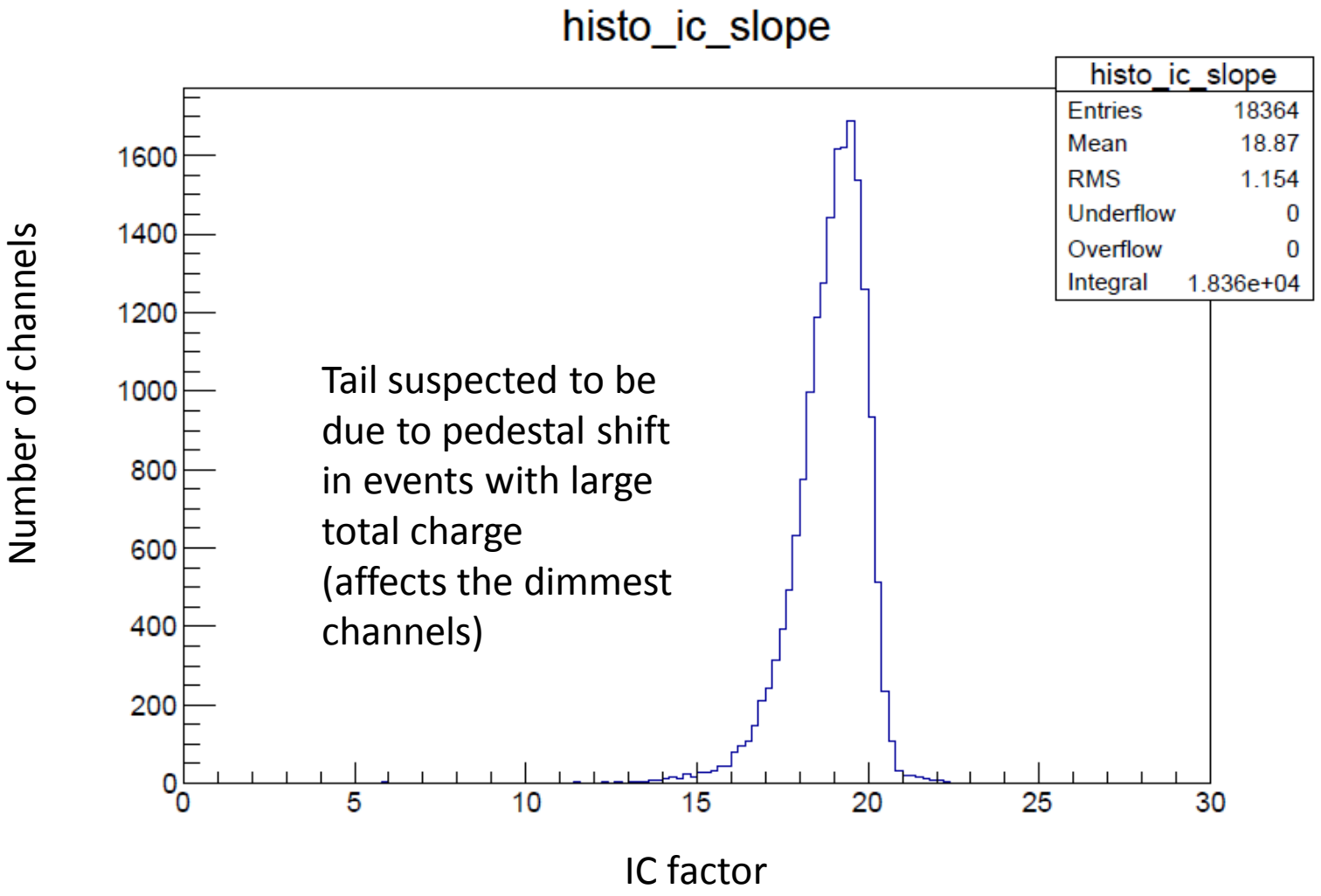






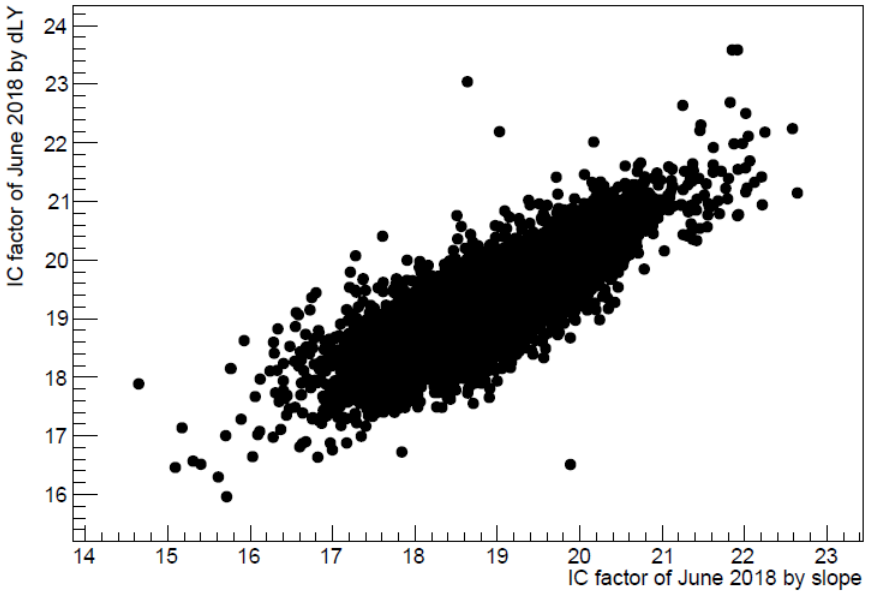


Slope of HG vs LG

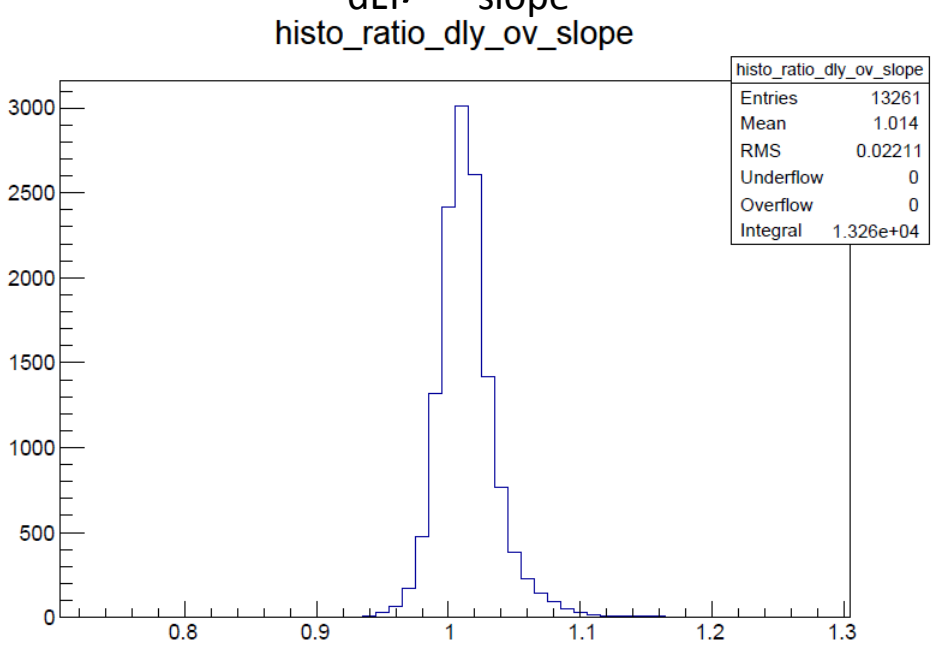


IC factor dLY vs Slope and IC_{dLY}/IC_{slope}

dLY vs Slope



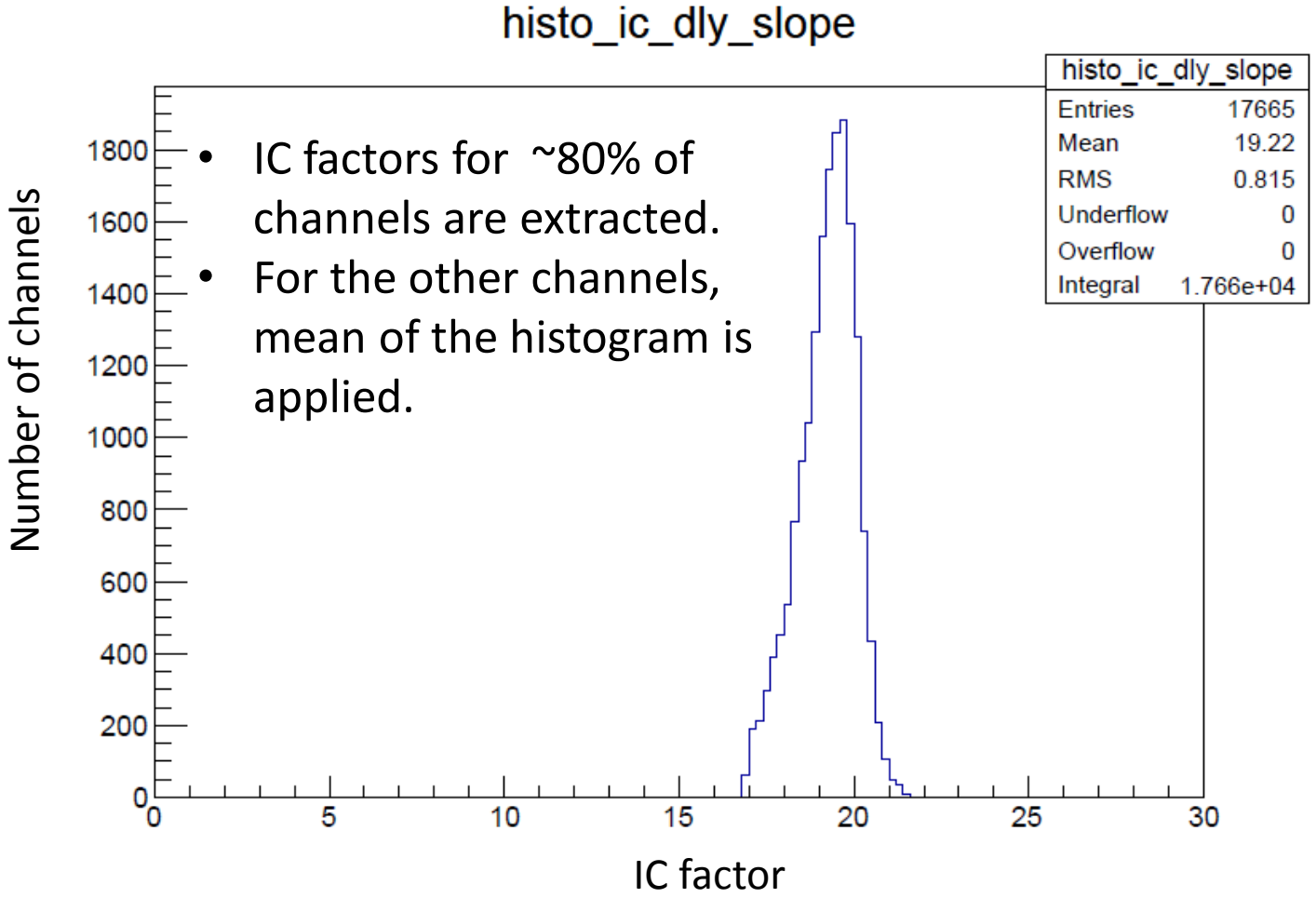
IC_{dLY}/IC_{slope}



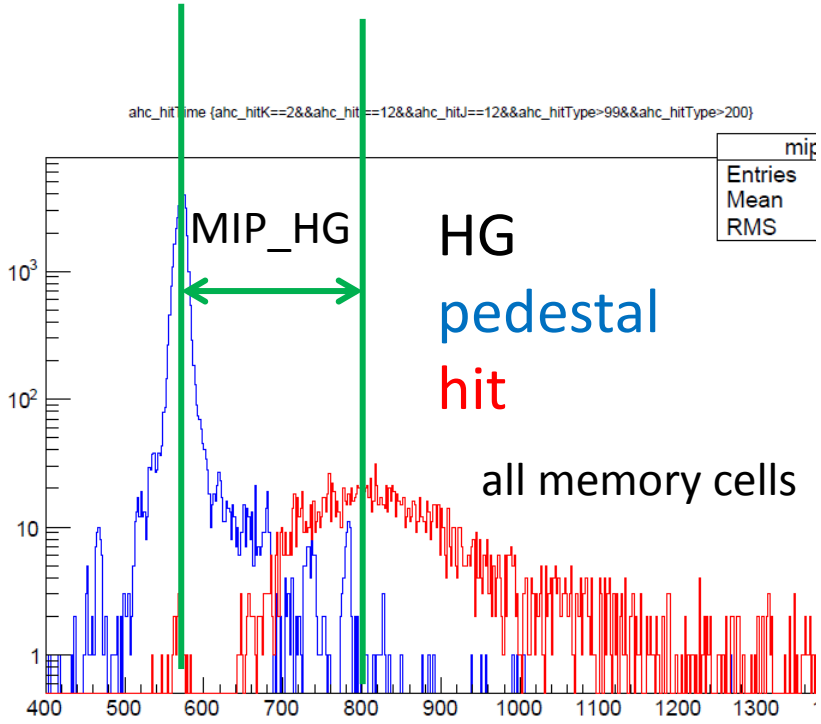
- Mean of IC_{dLY}/IC_{slope} 1.014 → 1.4% systematic shift
- RMS = 0.022

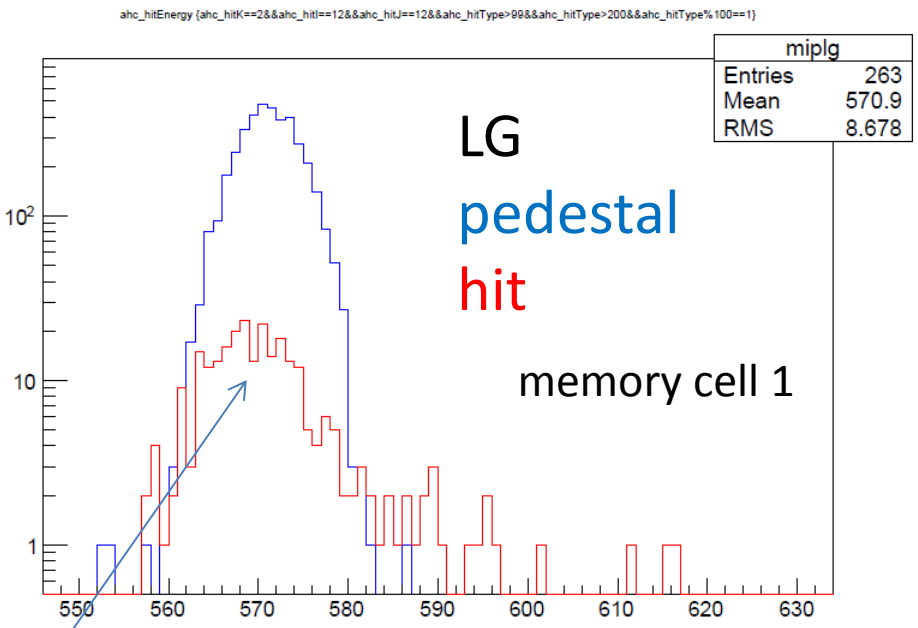
IC factor extracted by dLY and slope

1. fill IC values extracted by dLY within mean +/- 3*rms of IC histogram of dLY
2. fill IC values extracted by slope within mean +/- 3*rms of IC histogram of slope, if the IC values are not filled by first step.



Muon Run with IC mode (HG/LG)
Pedestal shift with hit?





AT run is not available to extract the IC factor due to a pedestal shift.
But this information is useful to correct the low gain pedestal.

- IC factor is obtained from LED runs (ETIC)

→ Pedestal_LG = (Peak_LG with hit) – (expected MIP_LG)

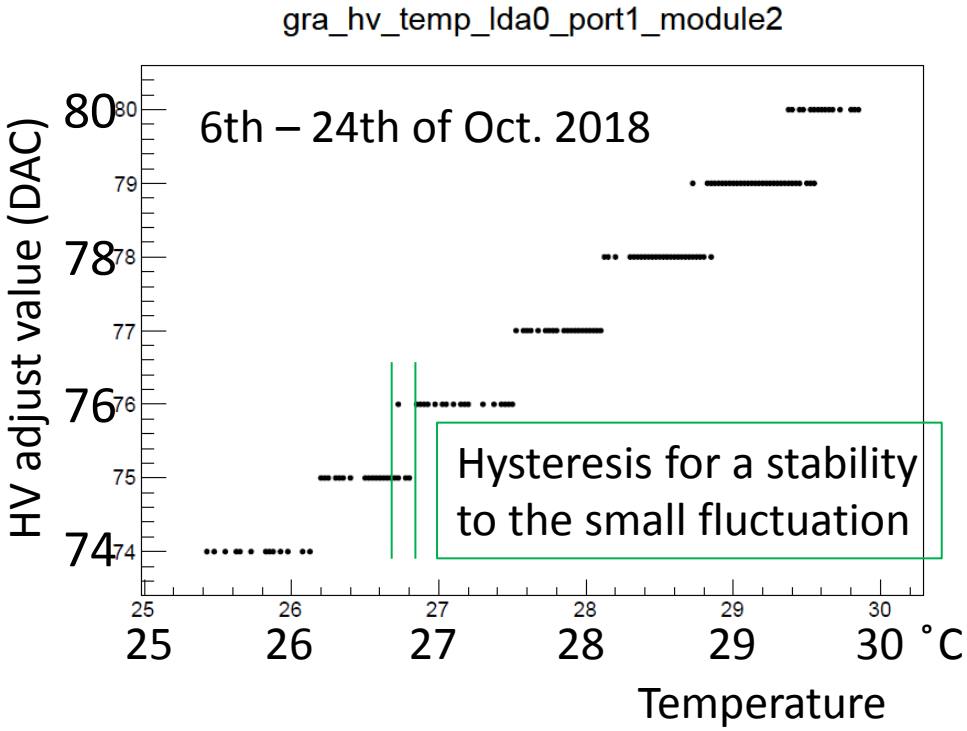
(expected MIP_LG) = MIP_HG/F_{IC}

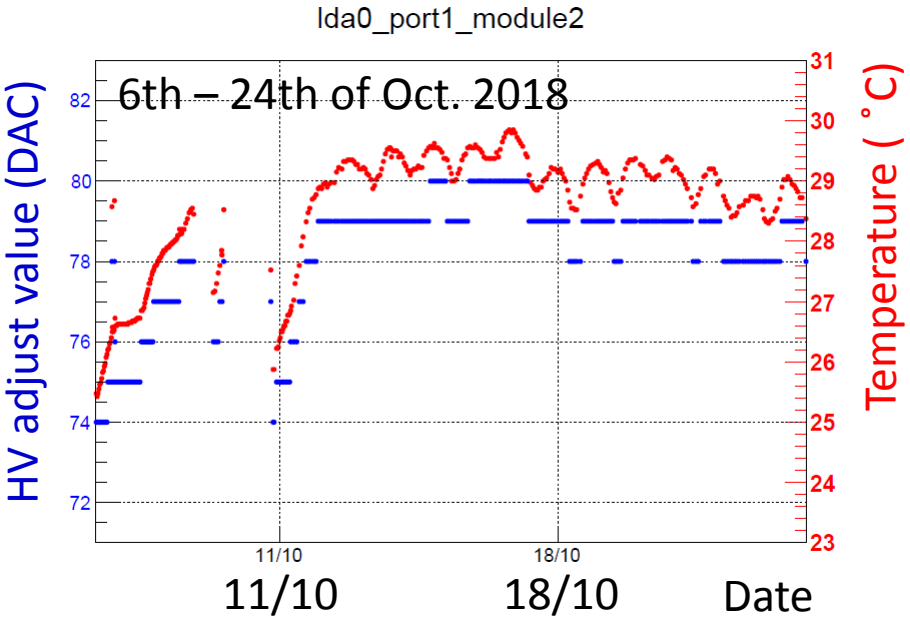
Gain Stability During TB

HV Adjustment

HV Adjust Value and Temperature vs Time

- Automatic HV adjustment on power board successfully works for Vop correction against temperature changes.
- Routinely running for TB in 2018

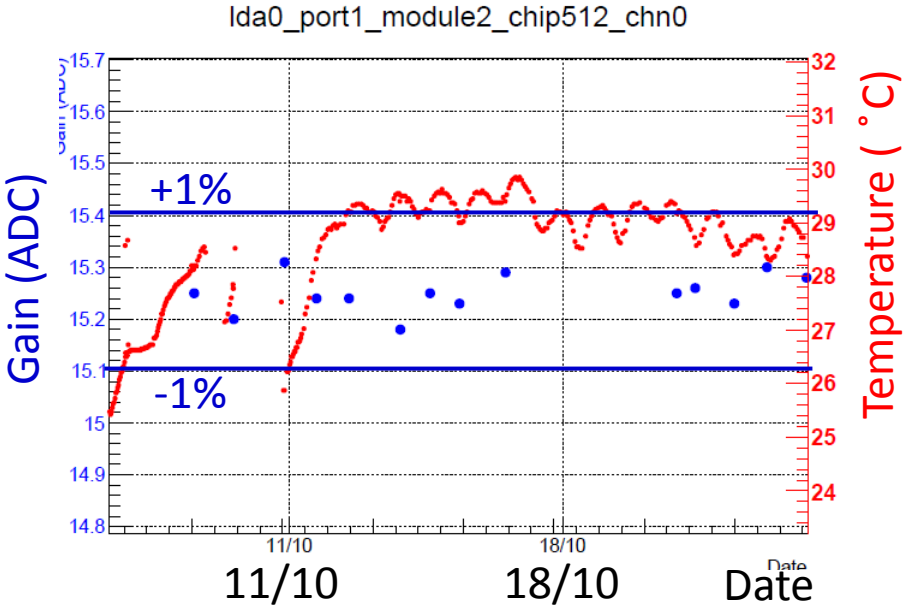


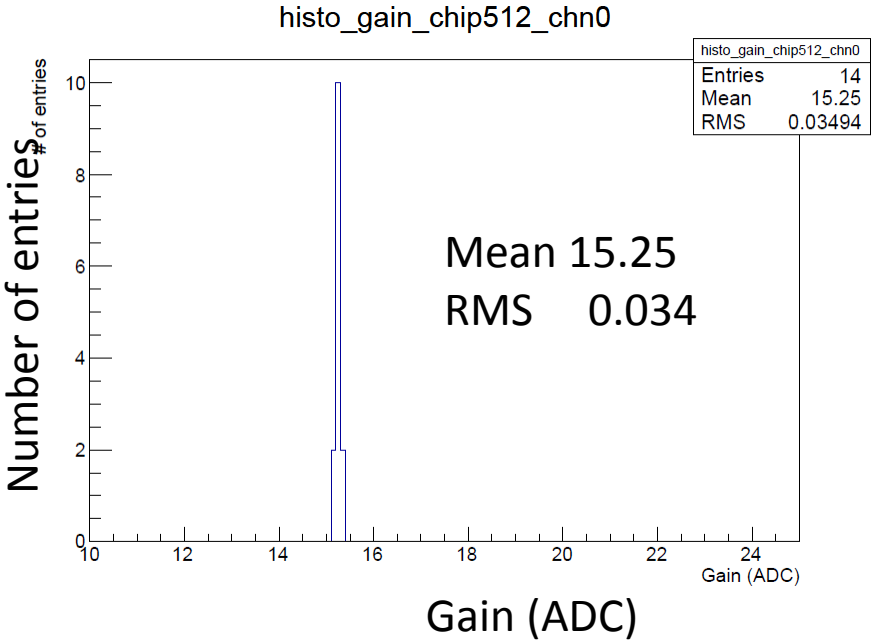


Gain Stability

Gain and Temperature vs Time

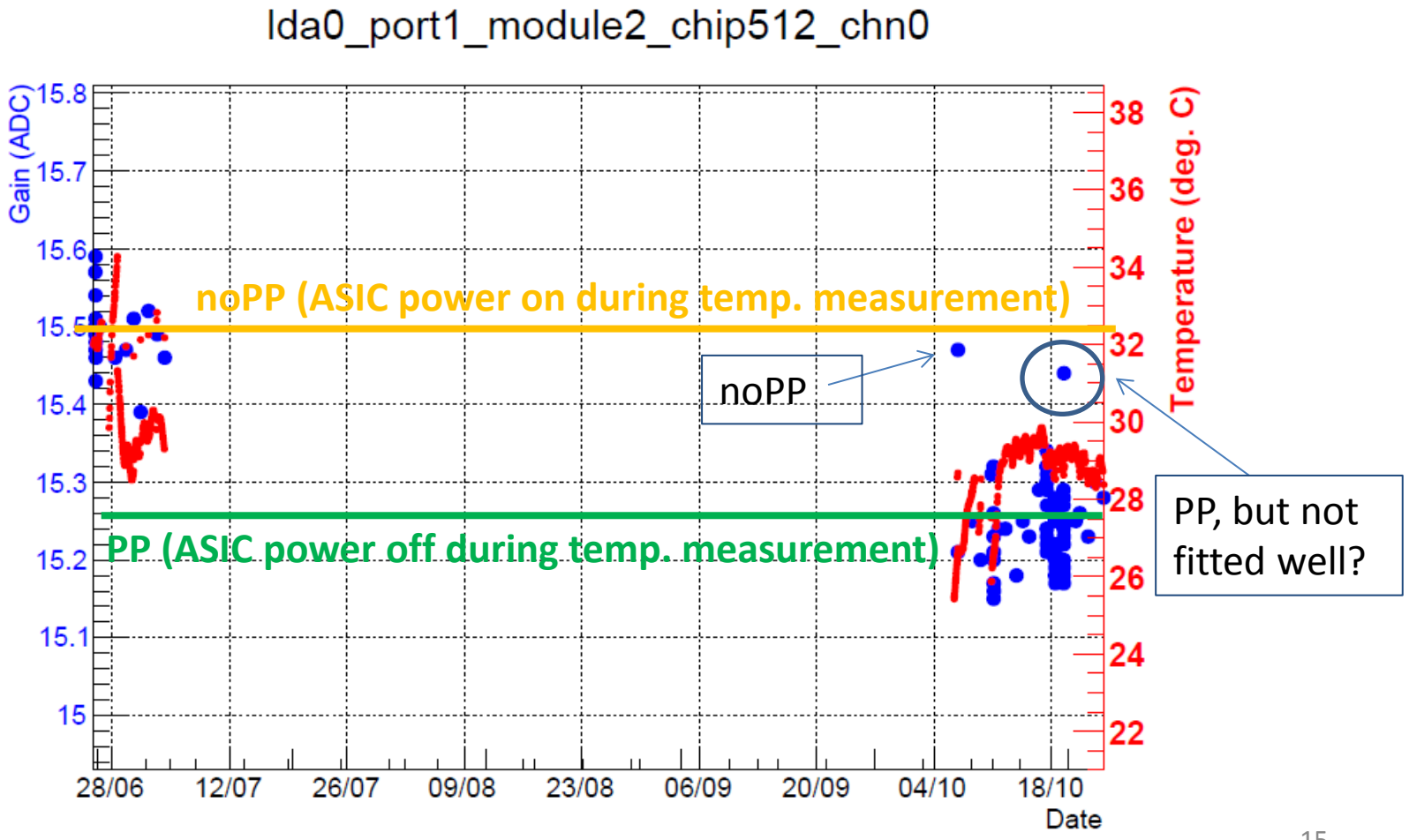
- Gain of MPPCs are successfully stabilized by automatic HV adjustment
- Dispersion of gain is within a precision of gain extraction by multi Gaussian fitting (<1%)





Gain Stability
Gain and Temperature vs Time

- short and long LED runs: June and October 2018



Summary

- HG/LG IC factor ~ 19.2
- Mean of IC_{June}/IC_{May} = 1, RMS ~2.3%
- no significant difference between slope and dLY methods
- IC factor is extracted for 17665 channels by 2 methods

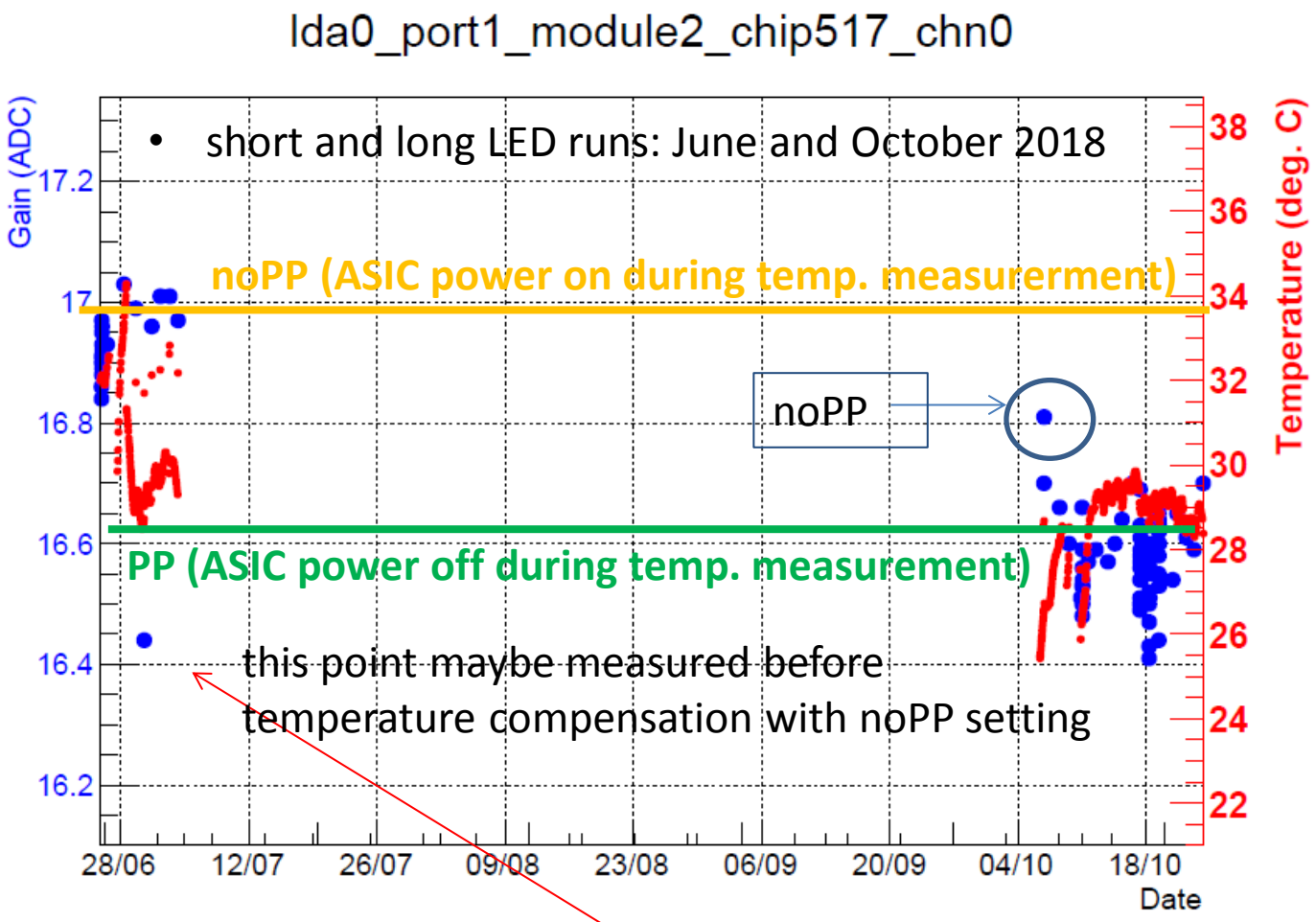
- Automatic adjustment of common bias voltage to compensate for temperature changes → stable gain within less than $\pm$ 1%

To do

- apply higher order correction for slope

Backup

Gain Stability



30.06.2018 15:51 Naoki, Lorenz, Katja, Jiri **LED run**

Run#	particle	ROCs	events	note	power	comment
61245	LED	2000	-	x=--, y=--	noPP	LED pedestal
61246	LED	2000	-	x=--, y=--	noPP	LED V=5400mV
61247	LED	2000	-	x=--, y=--	noPP	LED V=5700mV, HV adjustment just executed for this run
61248	LED	2000	-	x=--, y=--	noPP	LED V=6000mV
61249	LED	~20	-	x=--, y=--	noPP	LED pedestal

Temperature Compensation for MPPC

- MPPC gain depends on temperature. Because breakdown voltage depends on temperature.

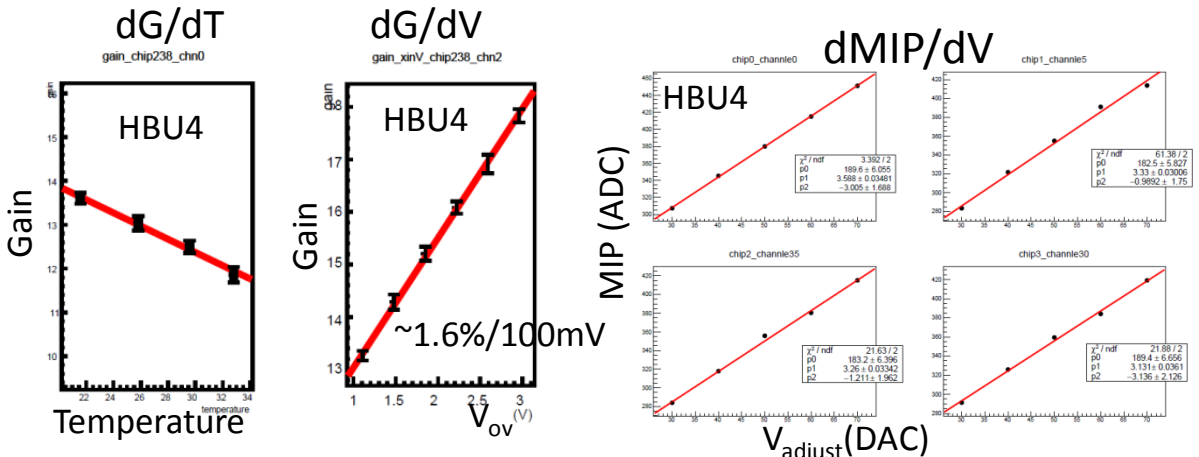
  complete discussion of temperature dependence on gain by HPK.
  https://hub.hamamatsu.com/sp/hc/resources/Temperature_Gain_SiPM.pdf

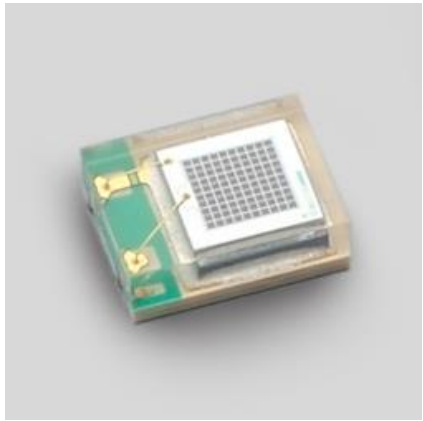
$\text{Gain} \propto V_{ov}$
$V_{ov} = V_{bias} - V_{break\ down}$

- We want to keep V_{ov} same as a value at a reference point. Adjust bias voltage against temperature changes.

→Automatic HV adjustment

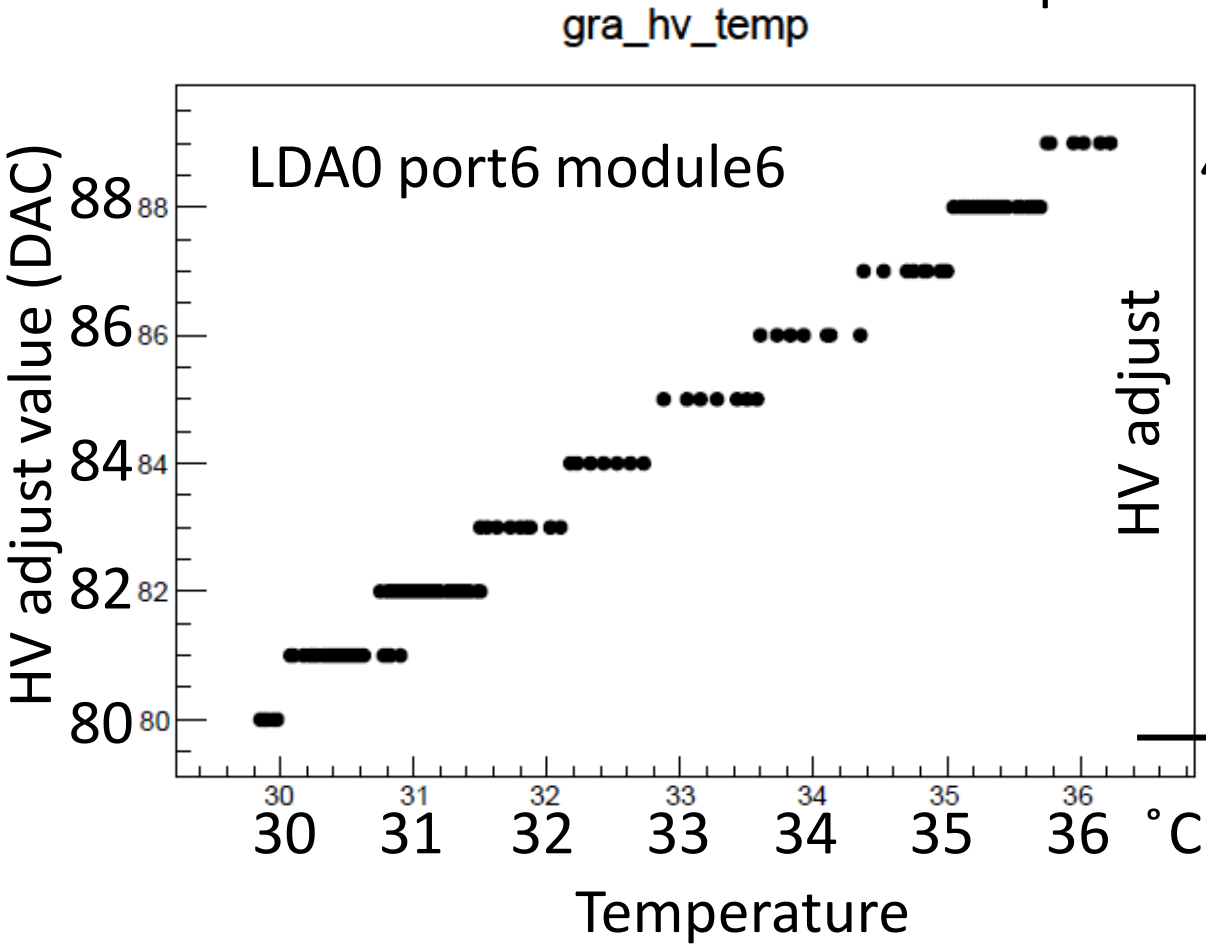
- HPK S13360-1325
- dMIP/dV is ~1.1%/DAC (1 DAC ~ 37mV)

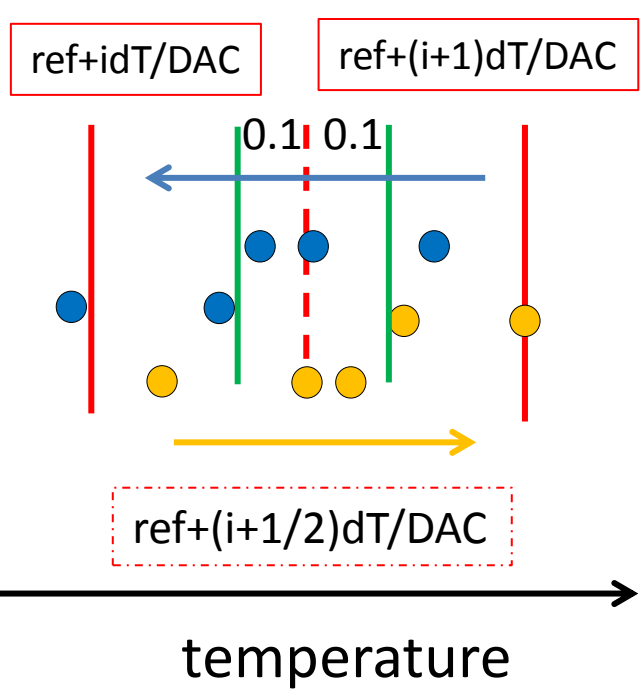




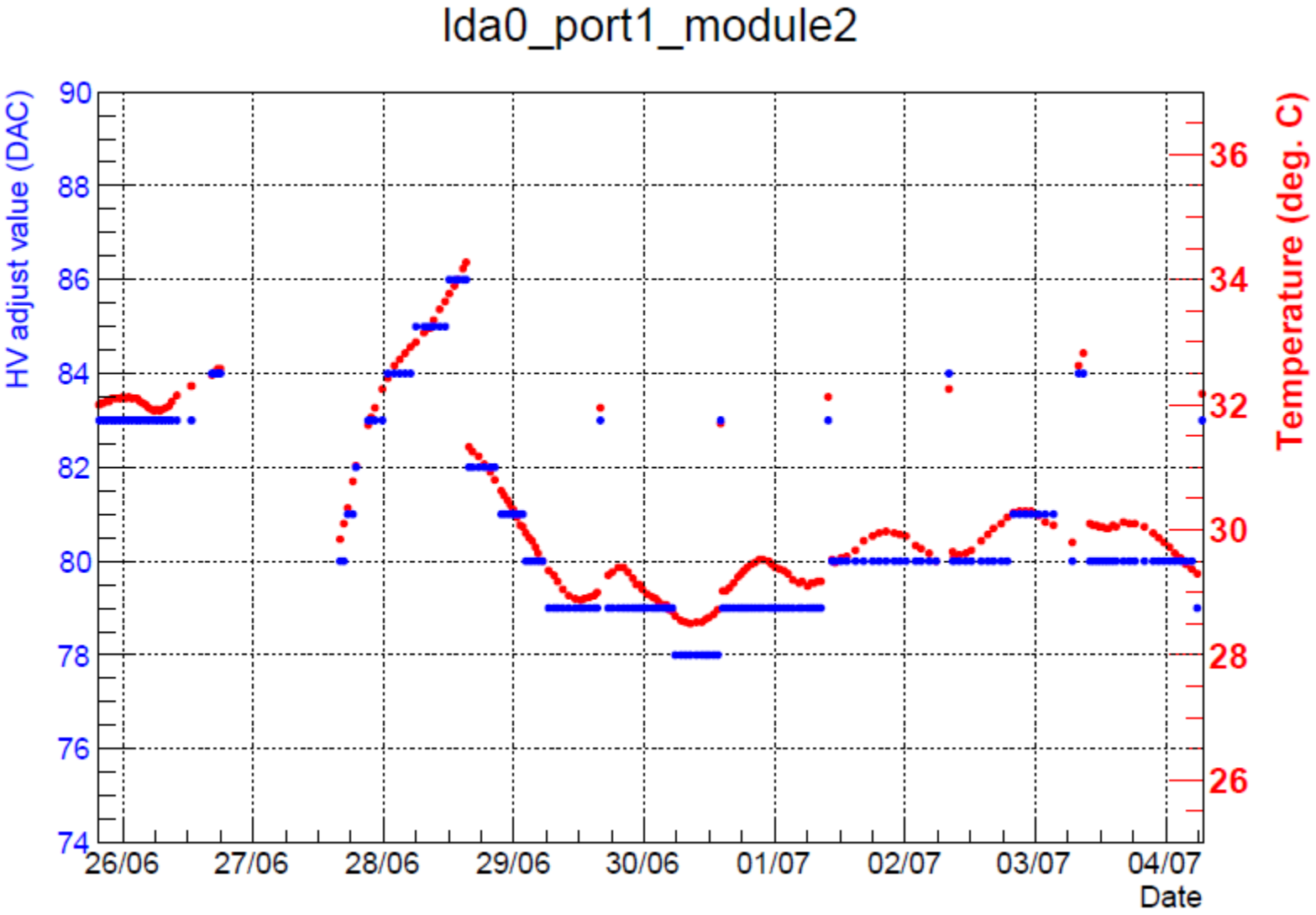
HV adjust vs Temperature

- 28th of June – 4th of July 2018
- There are over-lap of 0.2 degree C due to a hysteresis for stabilization around borders of temperature

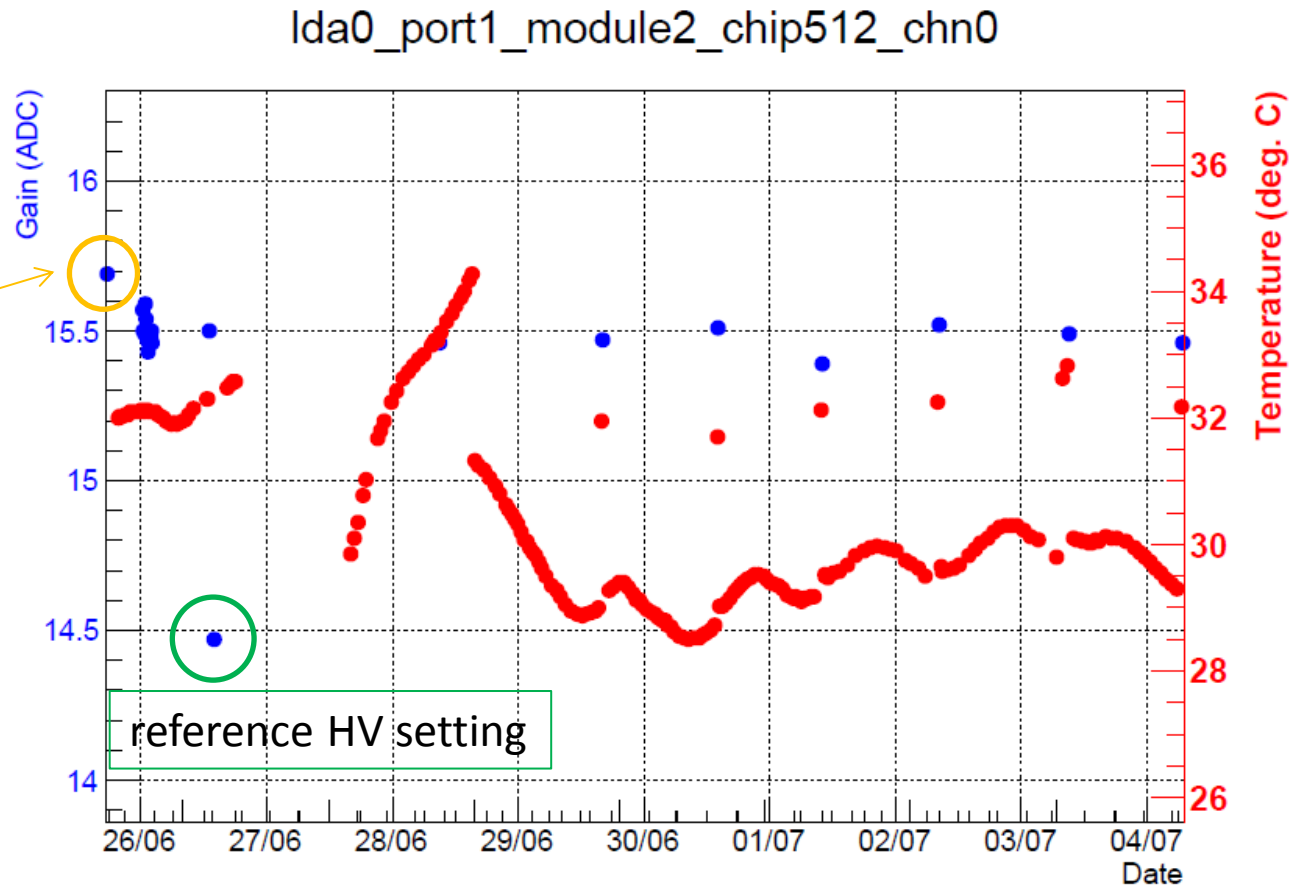




HV adjust value and Temperature vs Time



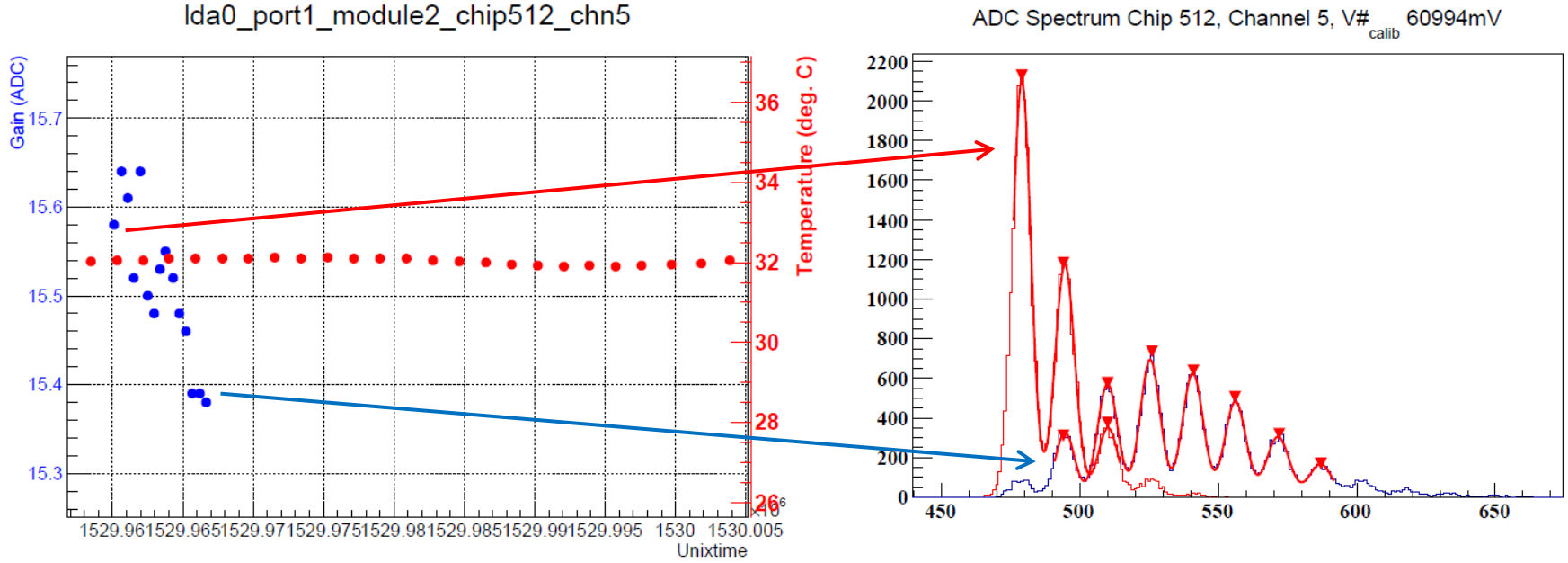
Gain and Temperature vs Time



no HV adjust (same setting as the last configuration)

- Automatic HV adjustment on power board successfully works for the temperature compensation.
- Automatic HV adjustment is included in DAQ chain for TB in 2018.

LED V dependence on Gain?



- Is there LED V (total amount of charge) dependence of Gain?
- same trend on many channels
- SPS looks O.K. for the first and the last measurement of point.

peak has a tail on lower side
→ later peaks affected by after pulsing
→ dependence on number of peaks
→ Systematic shift caused by a fitting method?

IC factor from LED runs
dHG_ADC/dLG_ADC

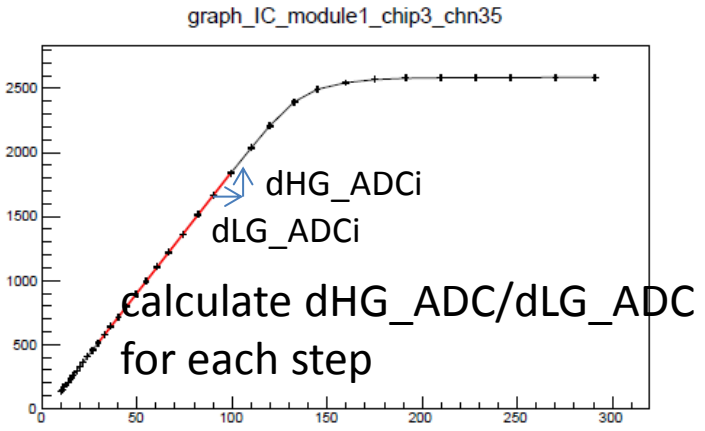
ΔLigit yield * HG = $(HG\_ADC_{i+1} - HG\_ADC_i)$

ΔLigit yield * LG = $(LG\_ADC_{i+1} - LG\_ADC_i)$

IC = HG/LG = $(HG\_ADC_{i+1} - HG\_ADC_i)/(LG\_ADC_{i+1} - LG\_ADC_i)$

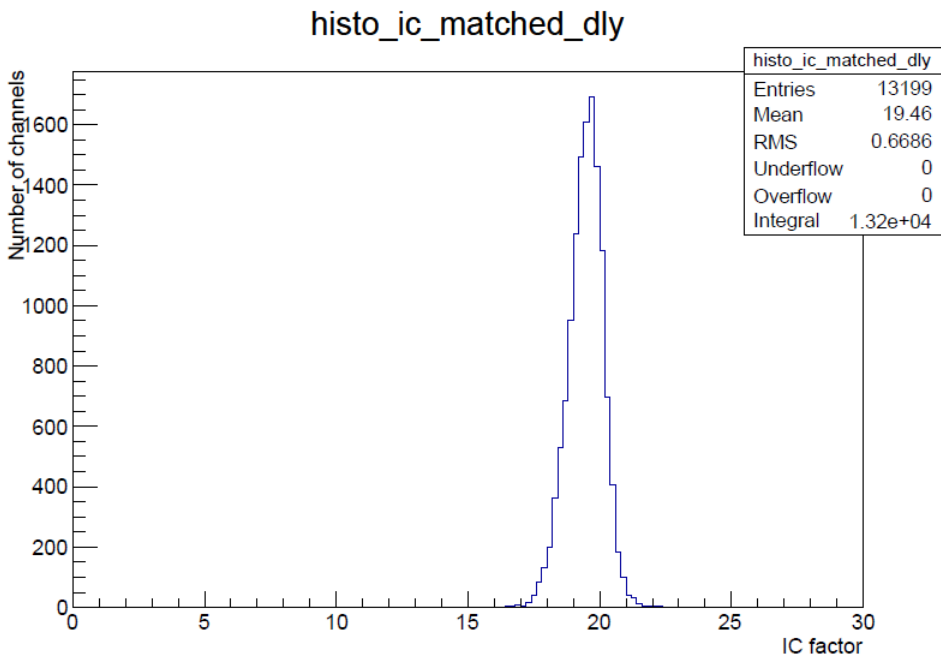
constraints

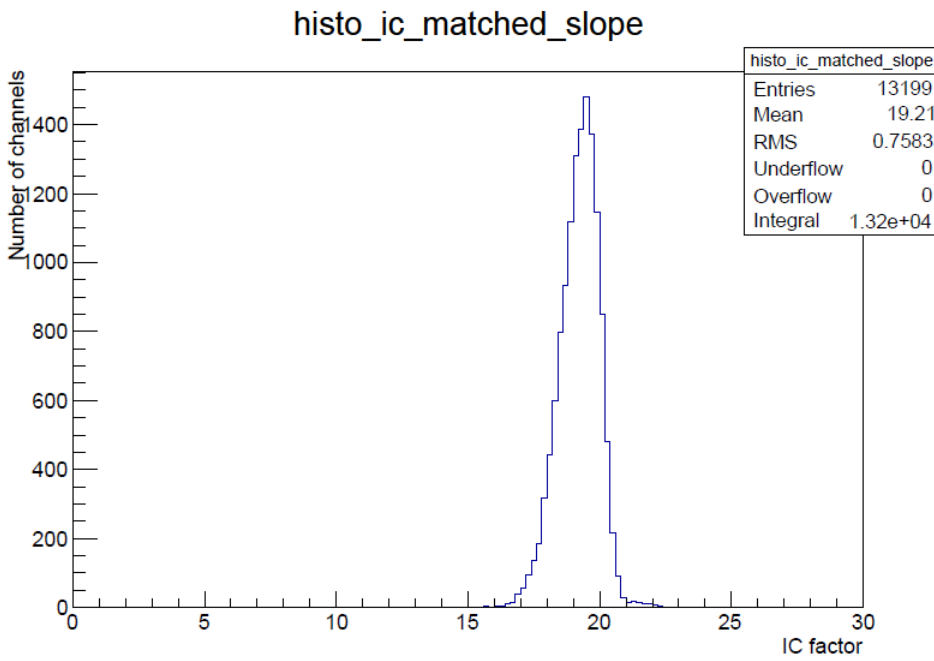
- $HG\_ADC_i > HG\_ADC_{ped}$
- HG_ADC_i and $HG\_ADC_{i+1} > 10$
- HG_ADC_i and $HG\_ADC_{i+1} < 1500$
- $30 < LG\_ADC_{i+1} - LG\_ADC_{ped} < 100$
- total amount of charge in a chip < 60000
- $HG\_ADC_{i+1} - HG\_ADC_i > 100$
- HG_RMS_{i+1}-HG_RMS_i >0
- LG_RMS_{i+1}-LG_RMS_i >0



IC factor dLY and slope

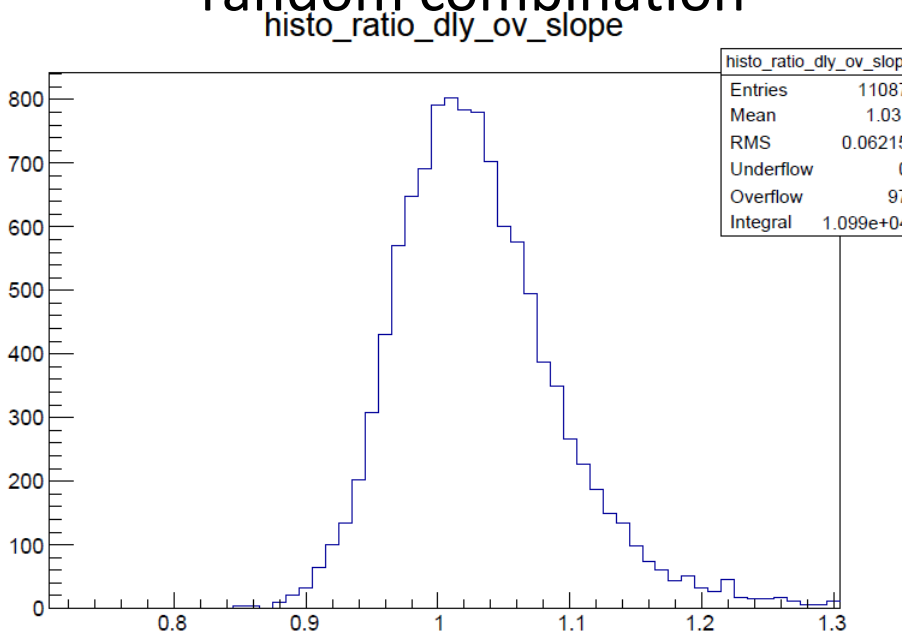
$0.9 < IC_{dLY}/Ic_{slope} < 1.1$



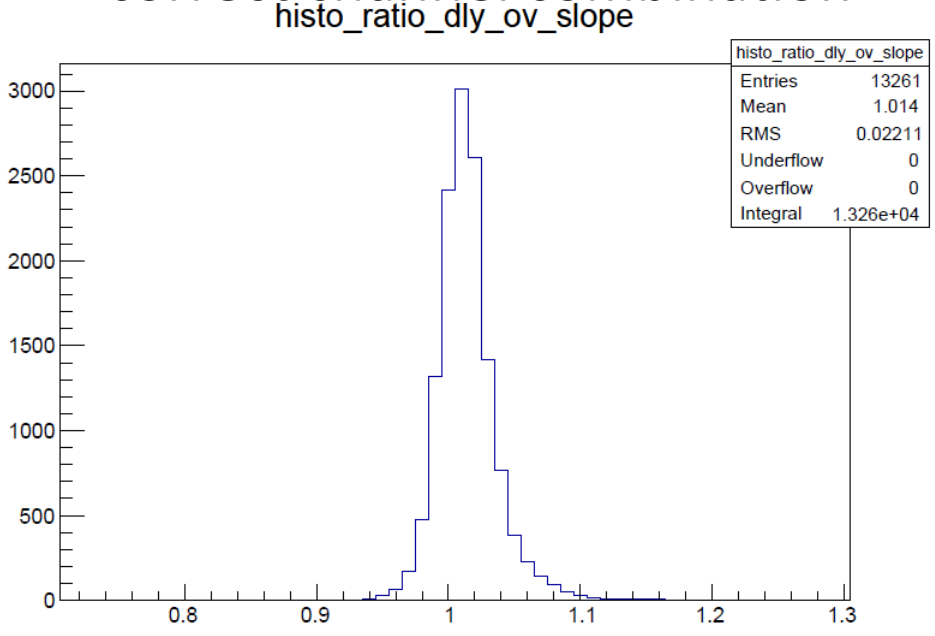


IC factor dLY vs Slope and IC_{dLY}/IC_{slope}

IC_{dLY}/IC_{slope}
random combination



IC_{dLY}/IC_{slope}
correct channel combination



- RMS of IC_{dLY}/IC_{slope} with random combination ~6%
- channel by channel variation ~6%