

HG/LG Inter-Calibration and LG Pedestal position with Hit

18.12.2018

AHCAL Analysis Workshop at DESY

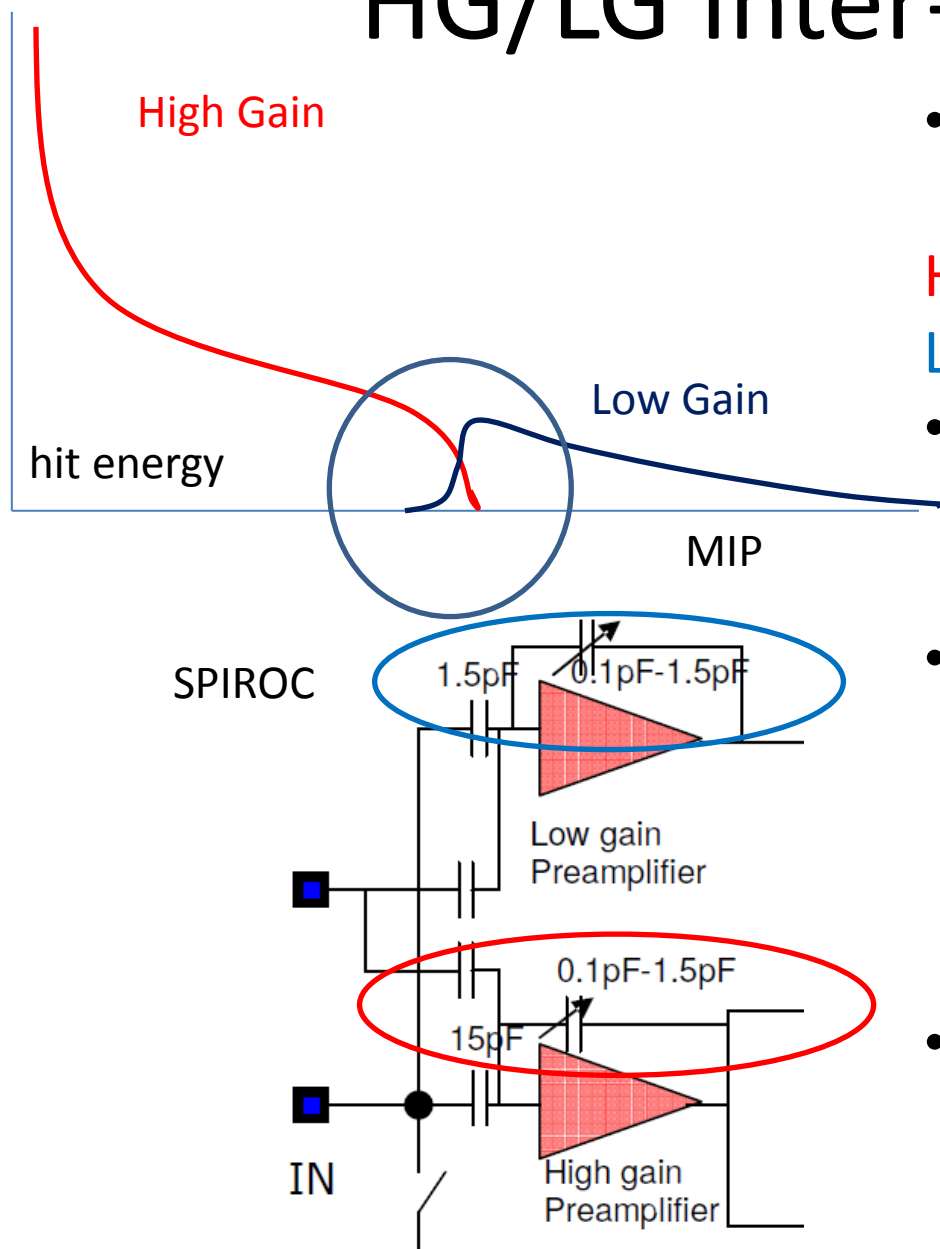
Yuji Sudo (DESY)



AIDA²⁰²⁰



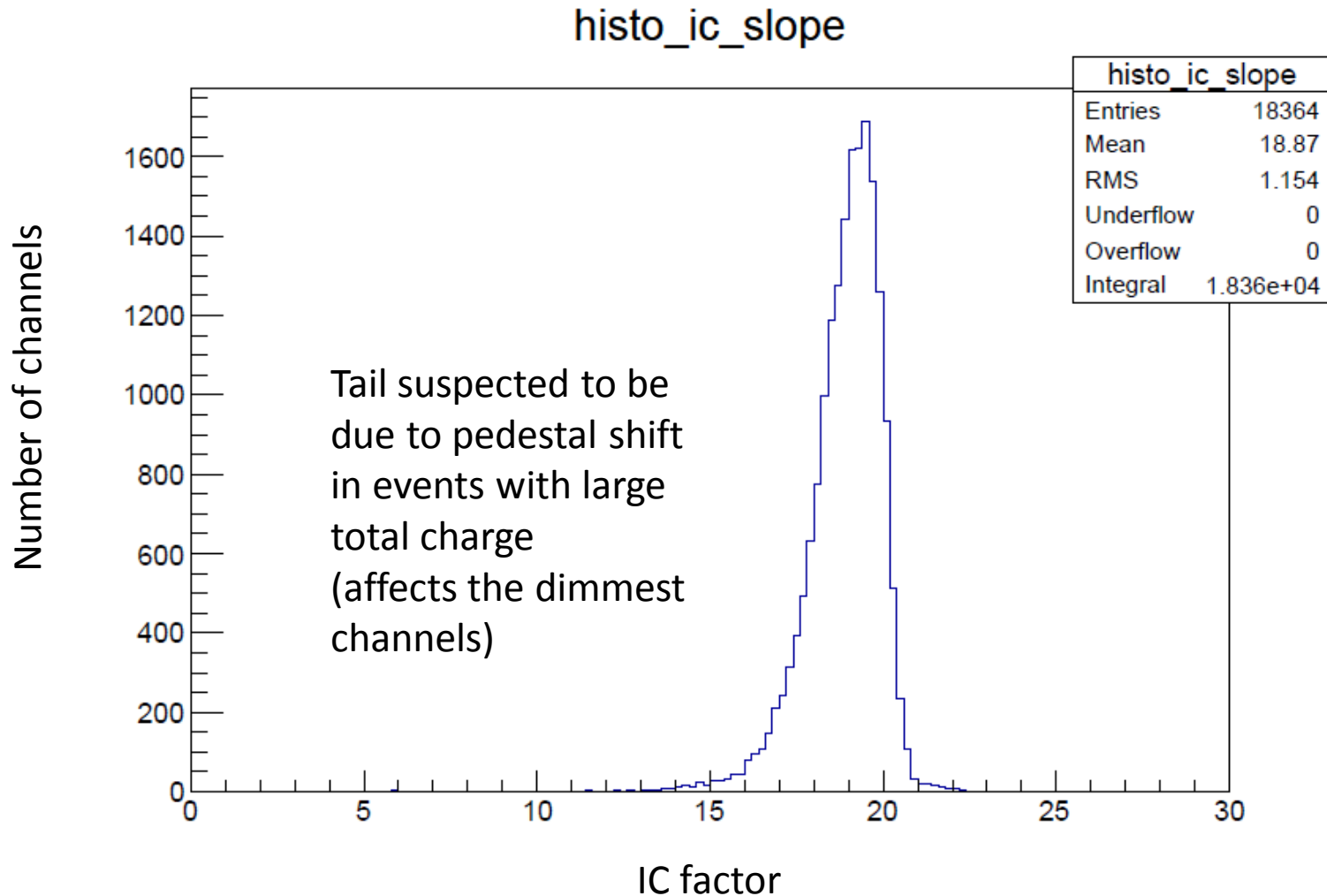
HG/LG Inter-Calibration



- SPIROC2B/2E has 2 signal output lines. High Gain and Low Gain
HG -- small deposited energy hits
LG -- large deposited energy hits
- In principle, IC factor is constant and just depends on ratio of capacitors. (IC ~20 for TB 2018)
- But IC factor is different for each channel due to an uneven quality of capacitance and parasitic capacitance.
→ measurement is important
- After inter-calibration, HG and LG output of hit energy should be connected smoothly

Slope of HG vs LG without correction

- need to apply higher order correction for slope

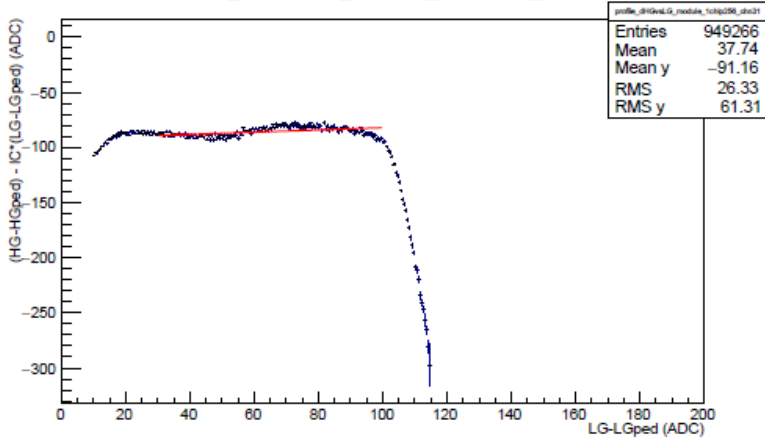


correction value

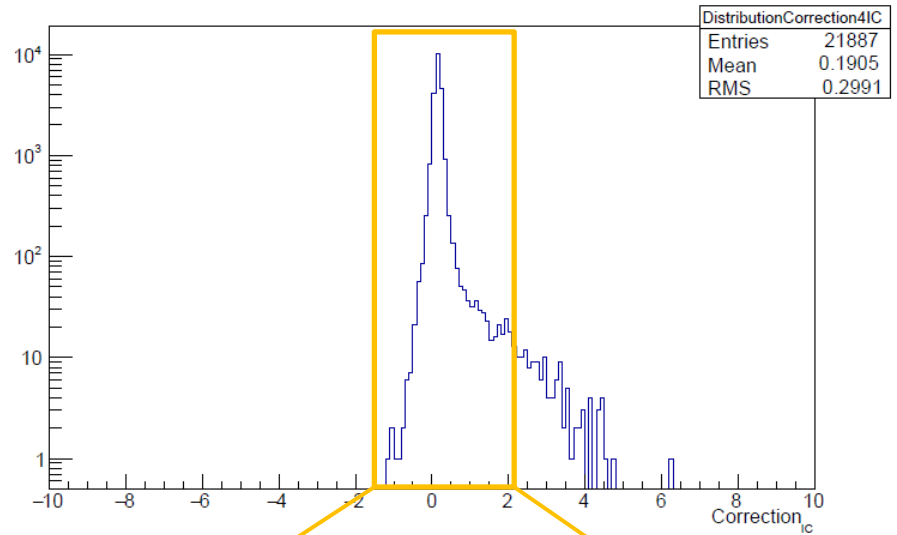
- higher order correction for slope

fit profile of dHGvsLG
 $30 < \text{LG ADC} < 100$

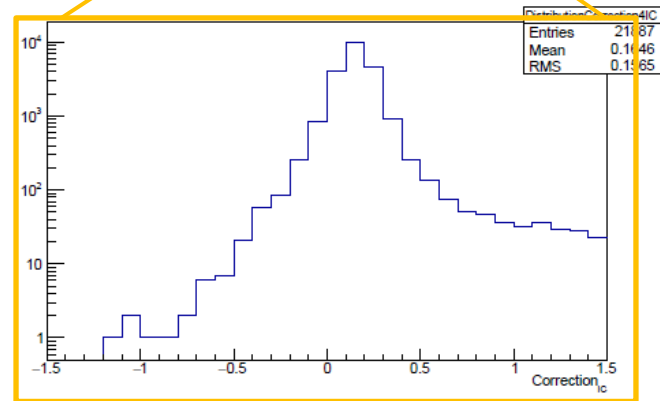
profile_dHGvsLG_module_1chip256_chn31



number of channels

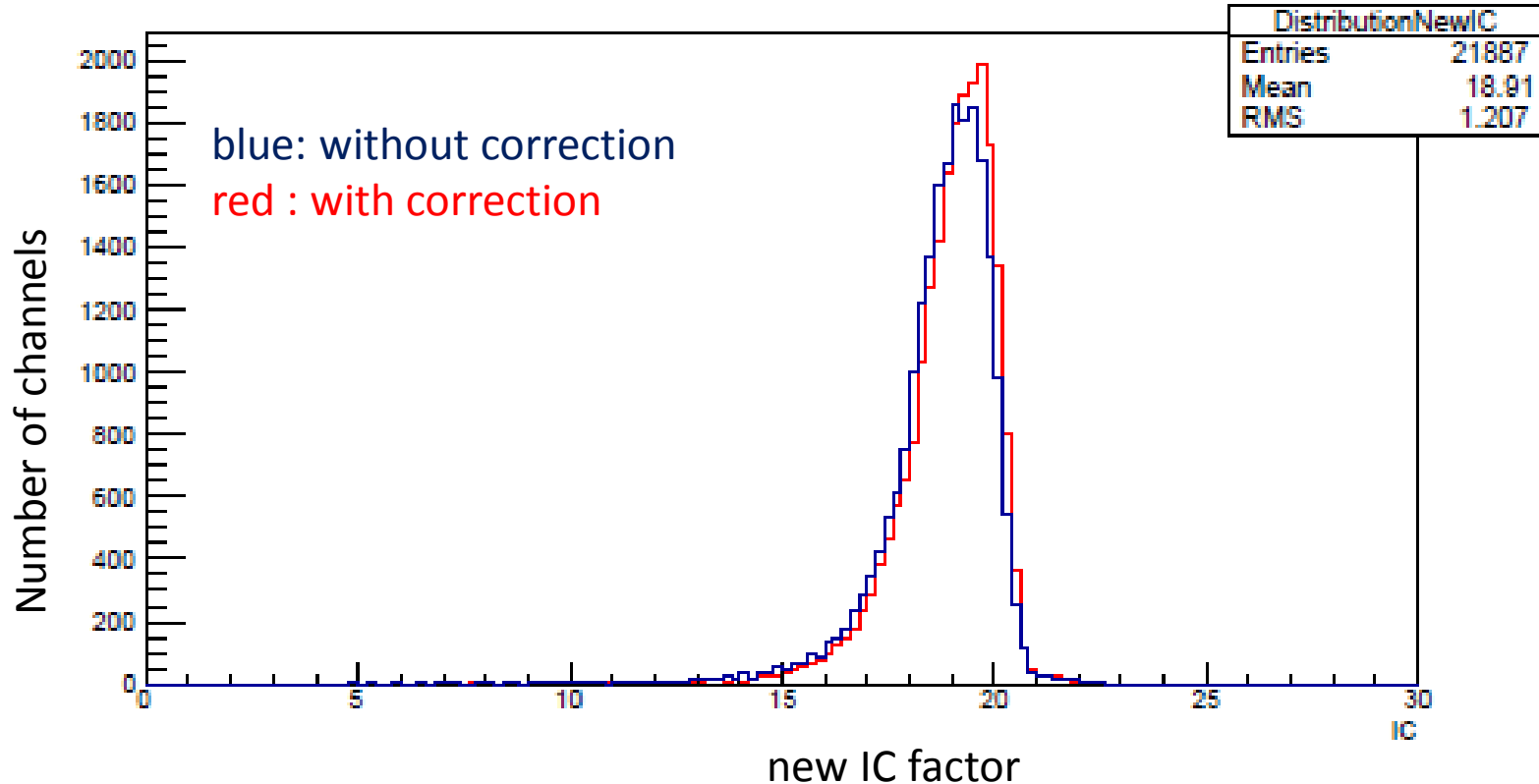


correction for IC factor



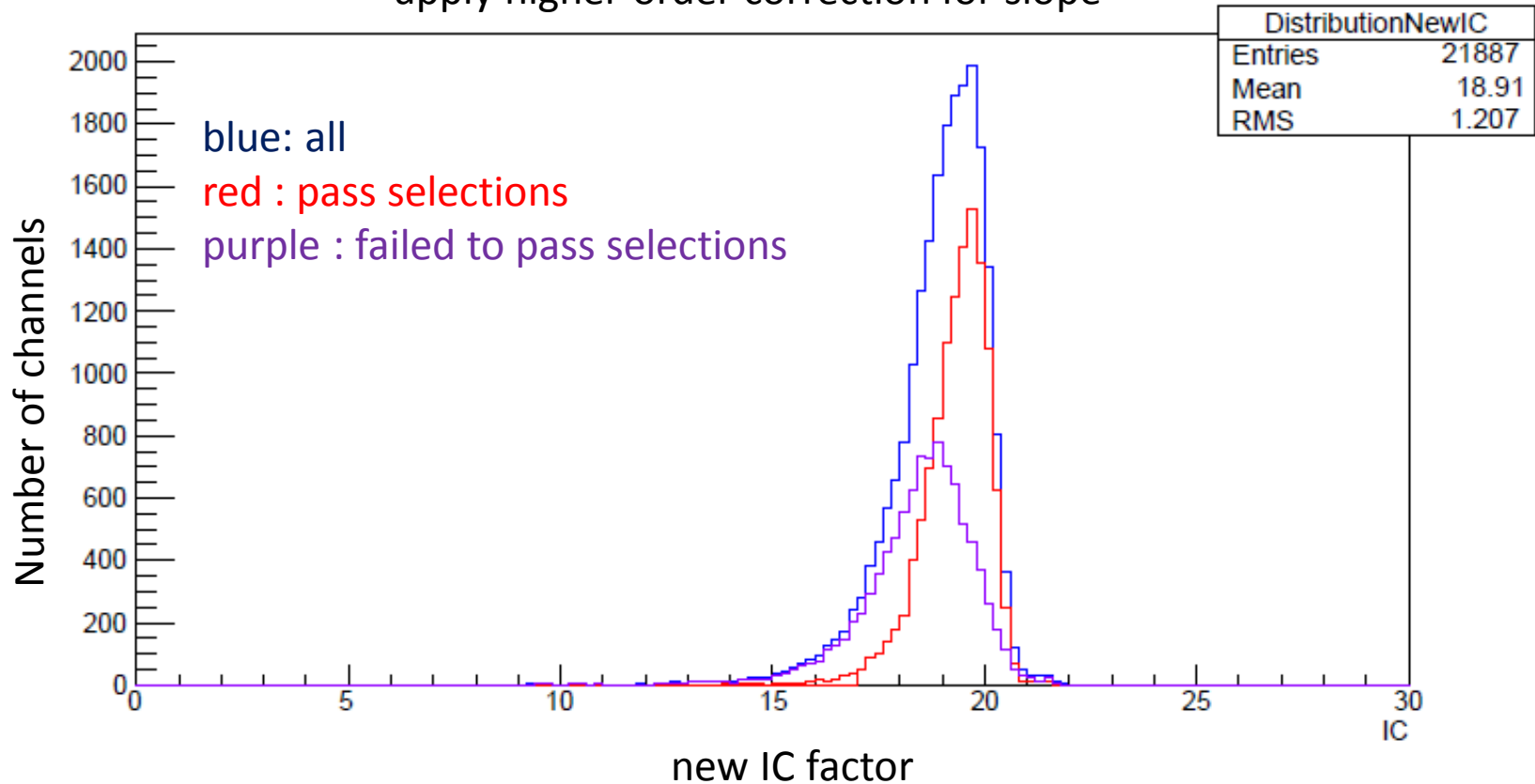
Slope of HG vs LG with correction

- apply higher order correction for slope



Slope of HG vs LG with correction

- apply higher order correction for slope



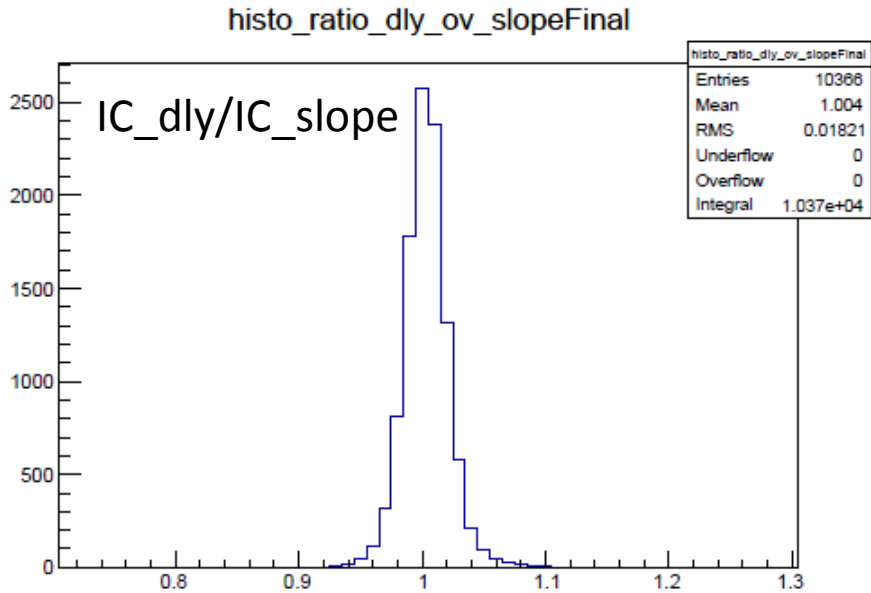
selection

no measured point with a total amount of charge in a chip >60000 in fitting region

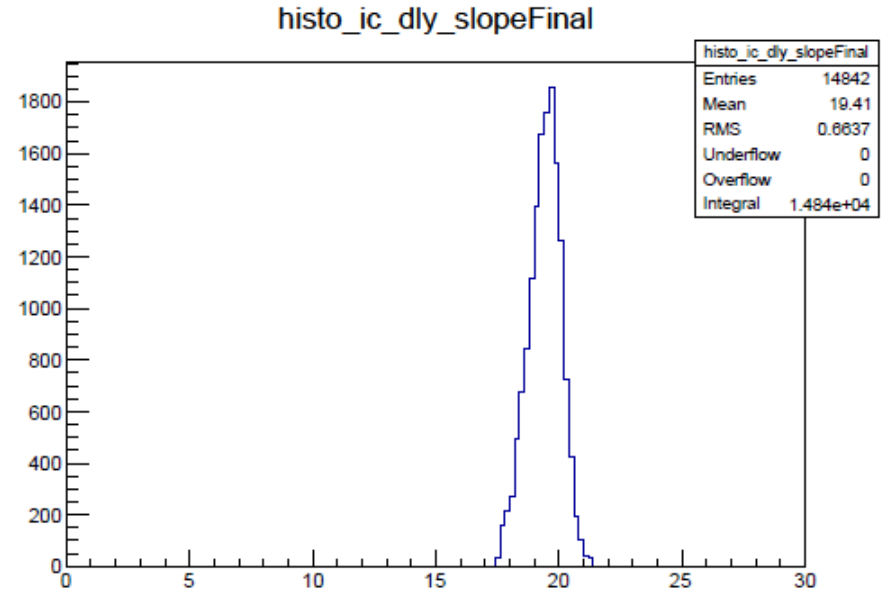
IC > 15 and get RMS

mean ± 3 *RMS

Inter-Calibration Factor



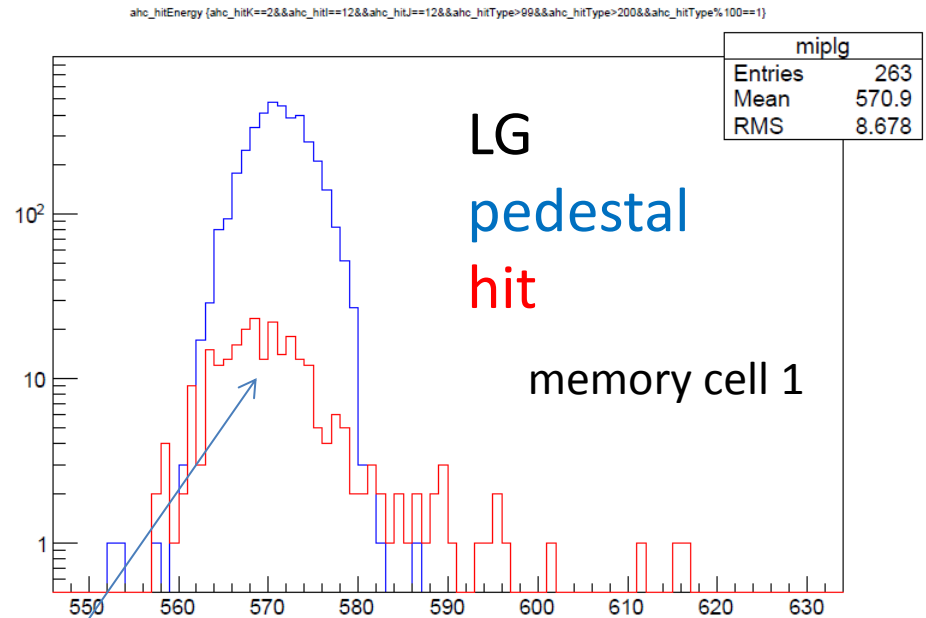
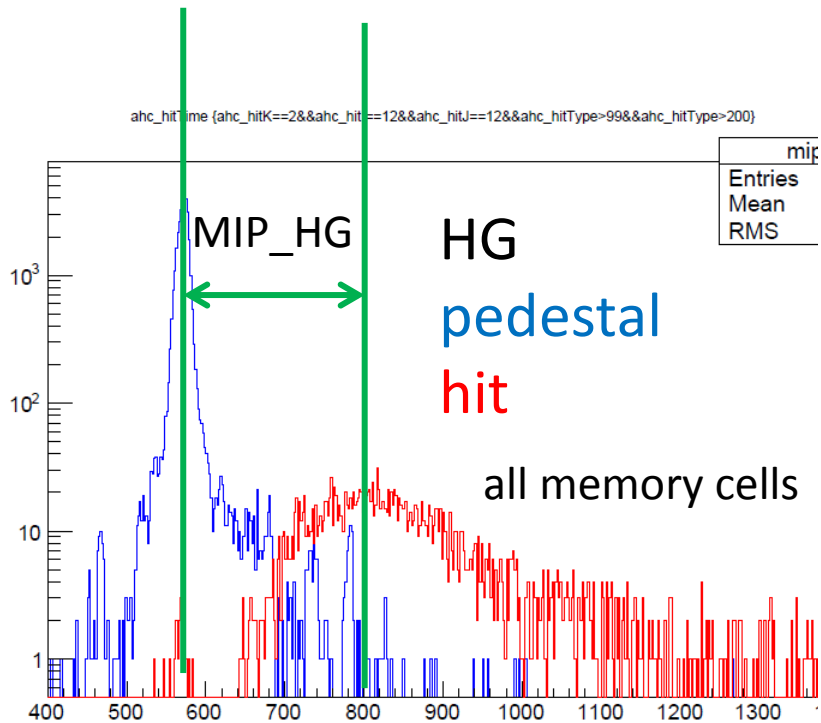
0.4% systematic shift
RMS = 0.018 (previous result 0.022)



loose selection :17665, mean=19.22
tight selection :14842, mean=19.44 (new)

Muon Run with IC mode (HG/LG)

Pedestal shift with hit?



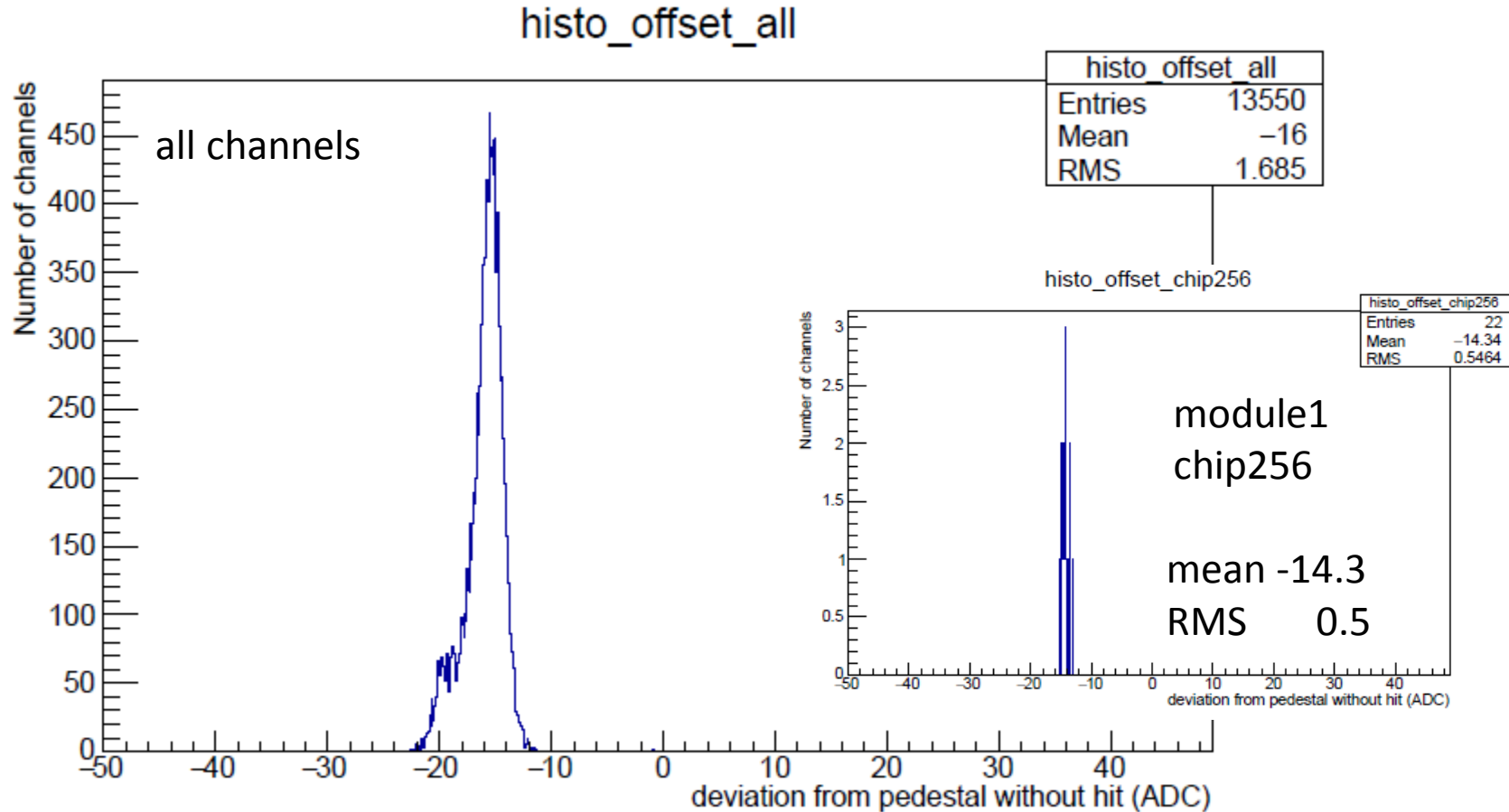
AT run is not available to extract the IC factor due to a pedestal shift.
But this information is useful to correct the low gain pedestal.

- IC factor is obtained from LED runs (ETIC)

$$\rightarrow \text{Pedestal_LG} = (\text{Peak_LG with hit}) - (\text{expected MIP_LG})$$

$$(\text{expected MIP_LG}) = \text{MIP_HG}/F_{IC}$$

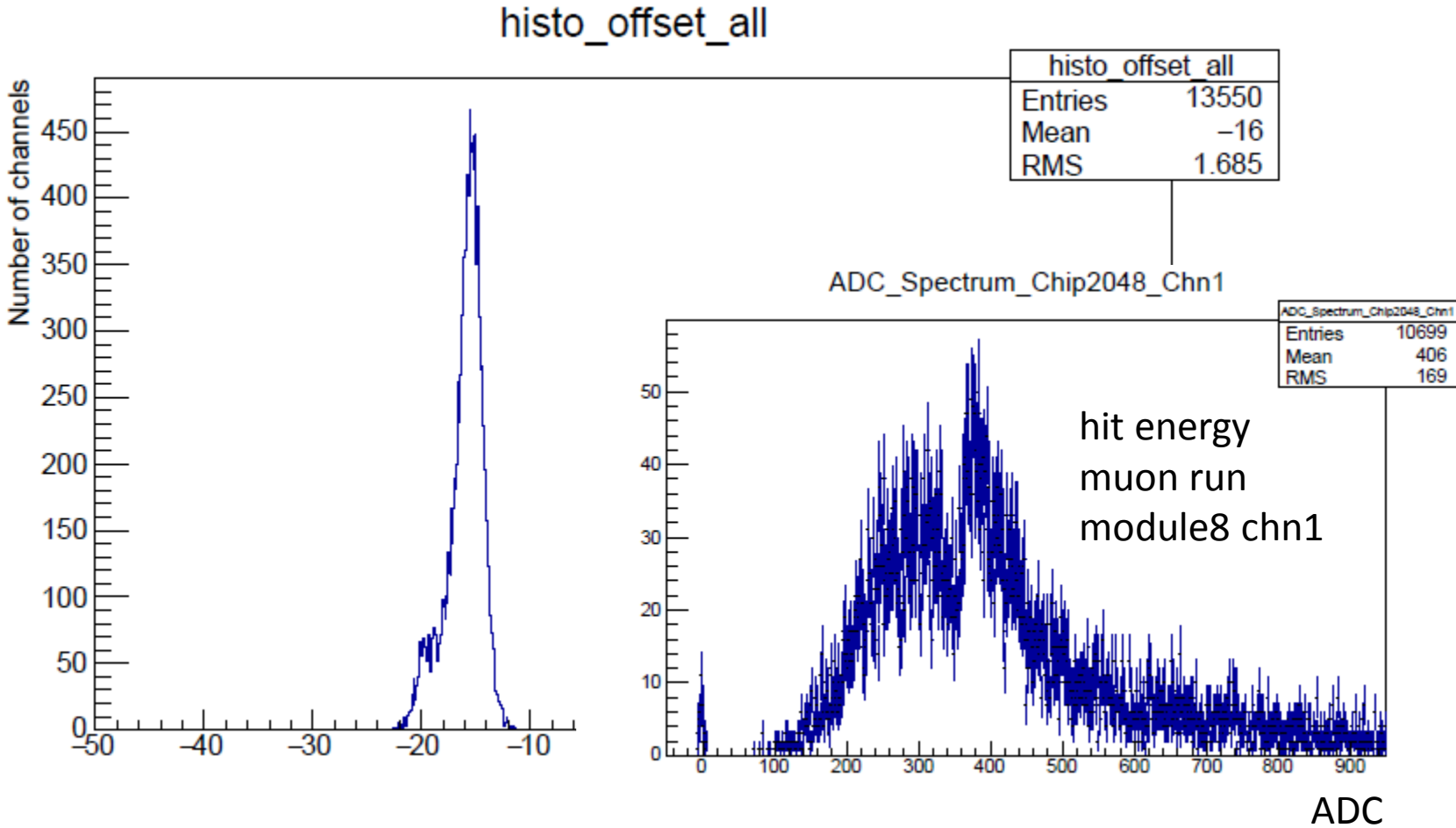
LG Pedestal Offset for hitbit1



$\text{offset} = \text{LG_Pedestal_wHit} - \text{LG_Pedestal_woHit}$

$\text{LG_Pedestal_wHit} = \text{LG_MIP_MPV} - \text{HG_MIP_MPV}/\text{ICfactor}$

LG Pedestal Offset for hitbit1



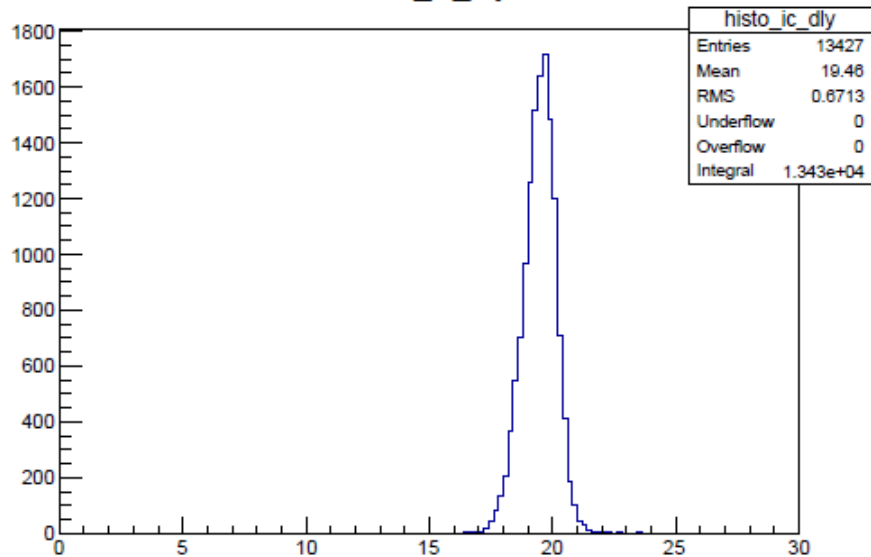
Summary

IC factor: higher order correction is applied to IC factor extracted from slope of HG vs LG output

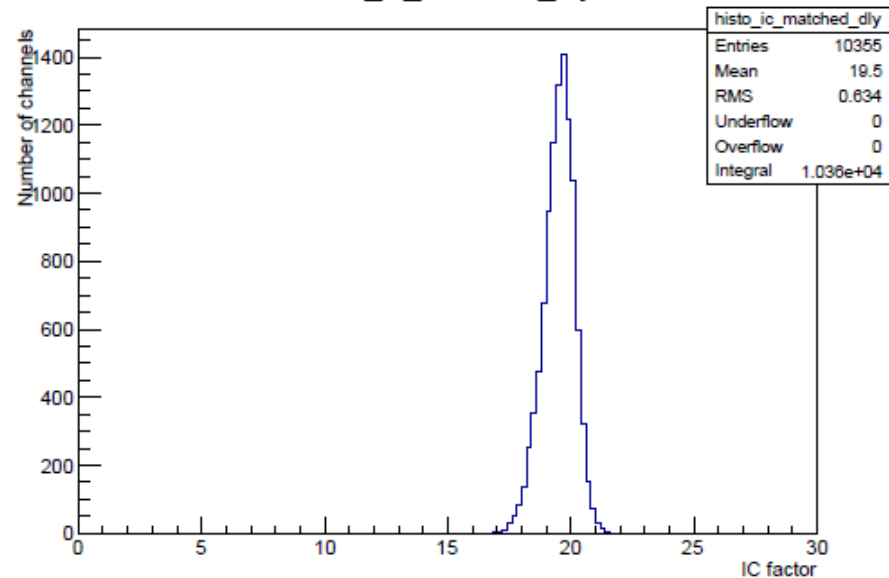
LG pedestal: need to figure out the strange peak on MIP spectrum

Backup

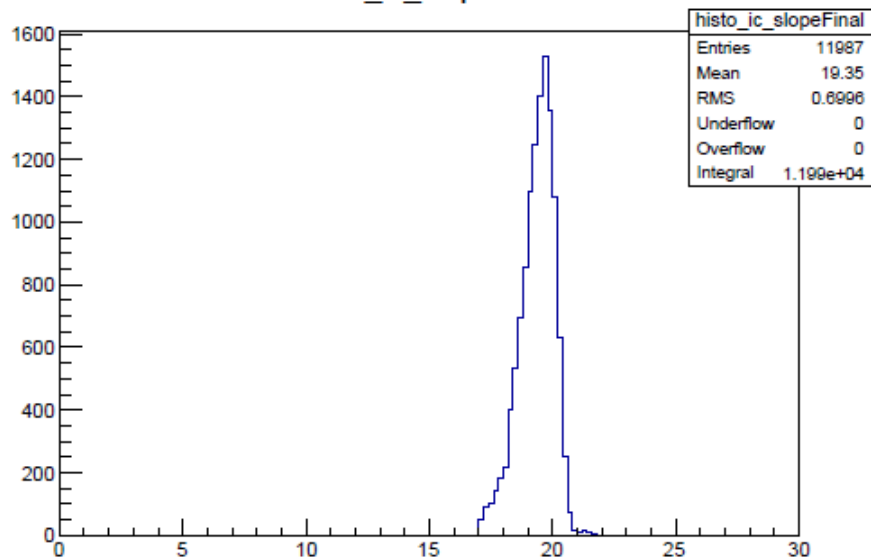
histo_ic_dly



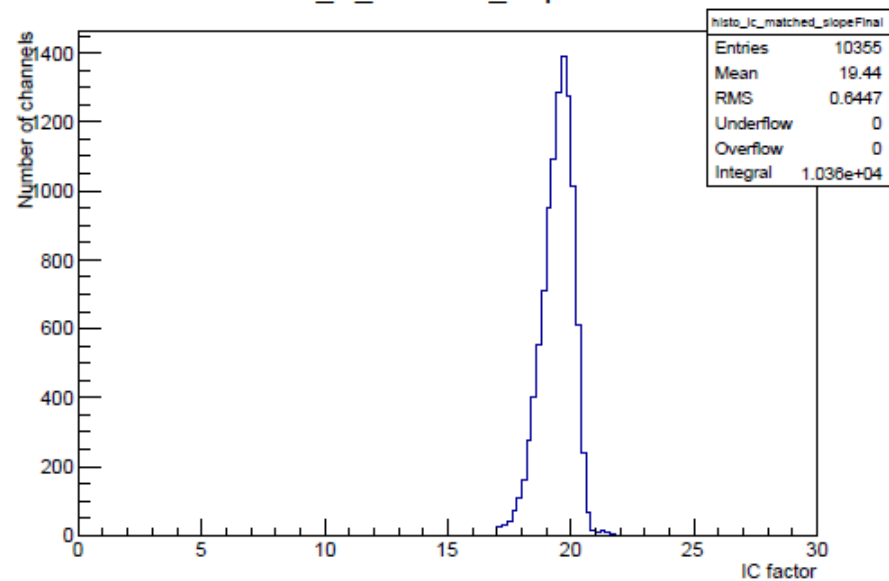
histo_ic_matched_dly



histo_ic_slopeFinal



histo_ic_matched_slopeFinal



IC factor from LED runs

dHG_ADC/dLG_ADC

- Small LED V step is required to cancel out or reduce impact of pedestal shift.

$$\Delta\text{Light yield} * \text{HG} = (\text{HG_ADC}_{i+1} - \text{HG_ADC}_i)$$

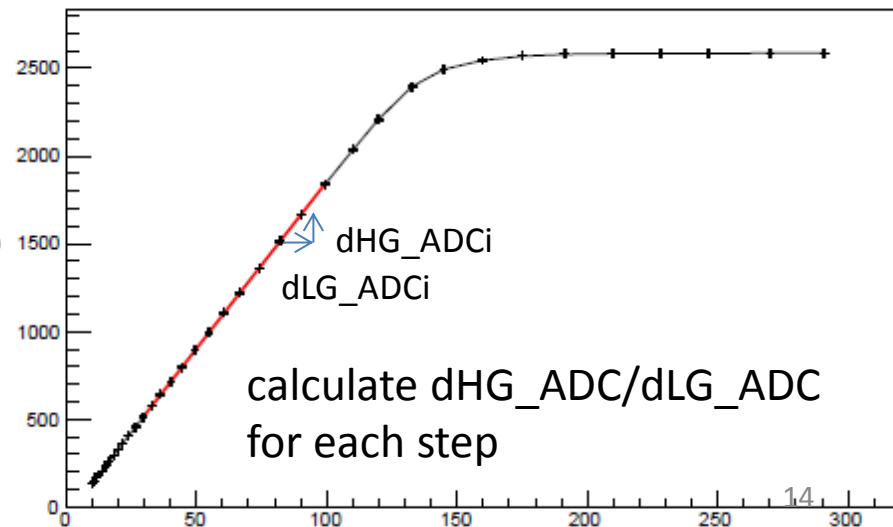
$$\Delta\text{Light yield} * \text{LG} = (\text{LG_ADC}_{i+1} - \text{LG_ADC}_i)$$

$$\text{IC} = \text{HG}/\text{LG} = (\text{HG_ADC}_{i+1} - \text{HG_ADC}_i)/(\text{LG_ADC}_{i+1} - \text{LG_ADC}_i)$$

constraints

- reasonably large signal
- $\text{HG_ADC}_{i+1} - \text{HG_ADC}_i > 100$
- $30 < \text{LG_ADC}_{i+1} - \text{LG_ADC}_{\text{ped}} < 100$
- **total amount of charge in a chip < 60000**

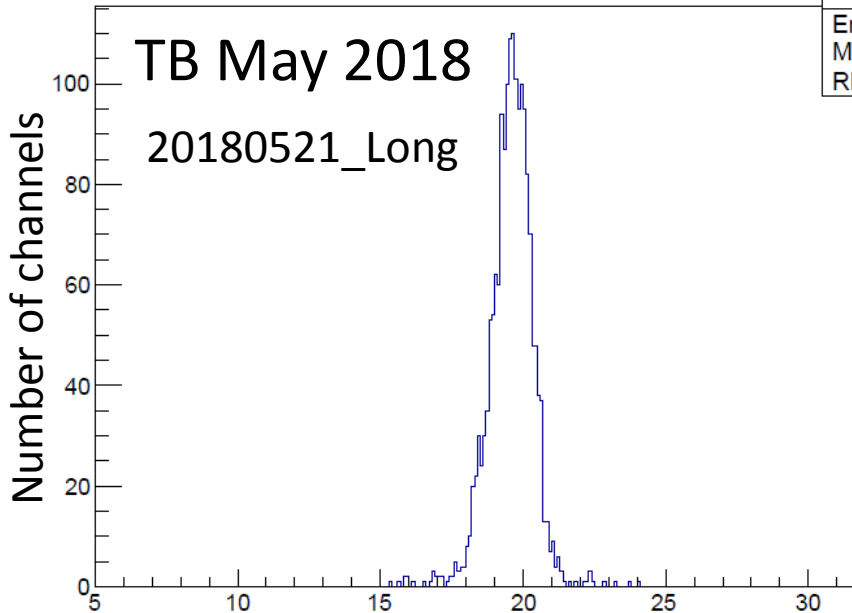
graph_IC_module1_chip3_chn35



LED Run May and June 2018 LG1200

histo_icall

histo_icall	
Entries	1729
Mean	19.58
RMS	0.7756



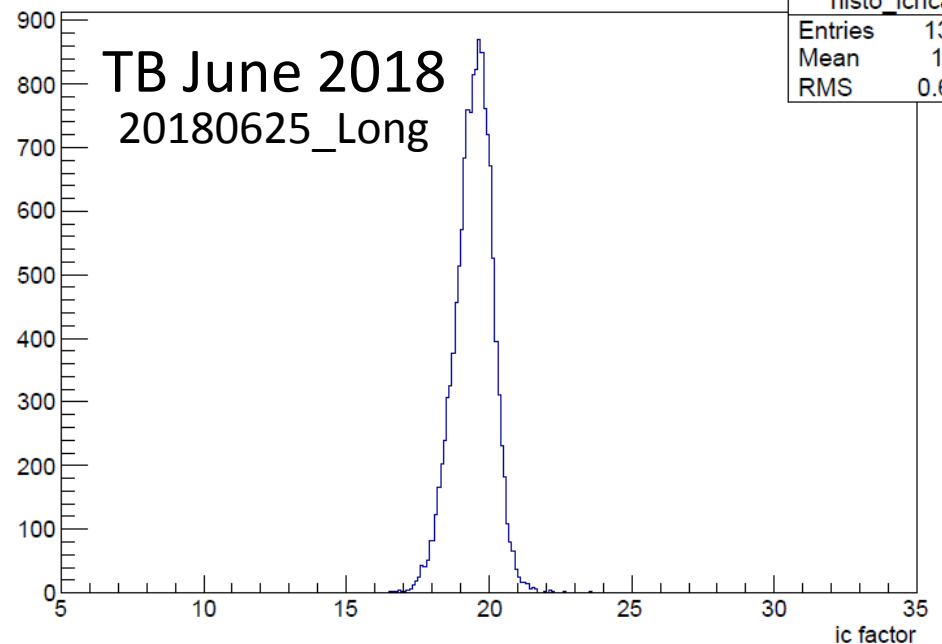
1729 out of 21888

5 sets of LED run for IC
(10+1 runs)

Average of slopes and
memory cells per channel

histo_ichcal

histo_ichcal	
Entries	13427
Mean	19.46
RMS	0.6713



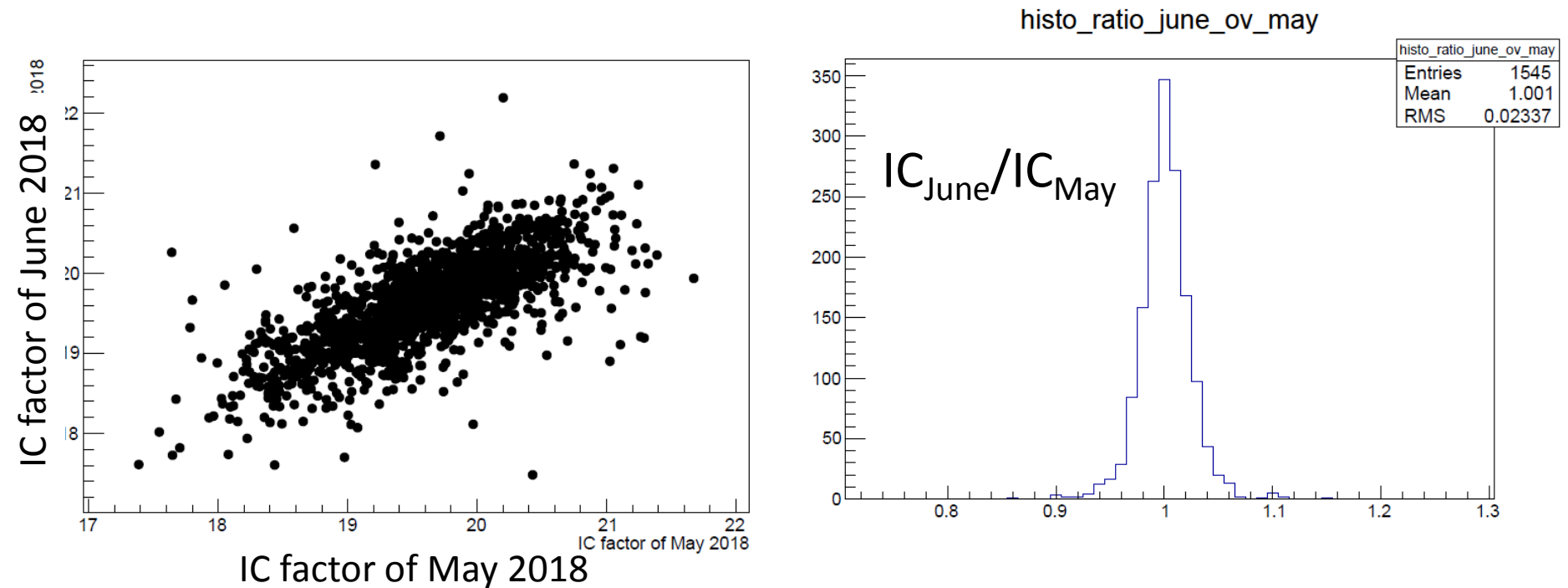
13427 out of 21888

101+1 runs

Channel-to-channel spread 3.5-4%

Comparing IC factor of June and May 2018

after reject outliers: range of plots is mean ± 3 xRMS of IC histogram

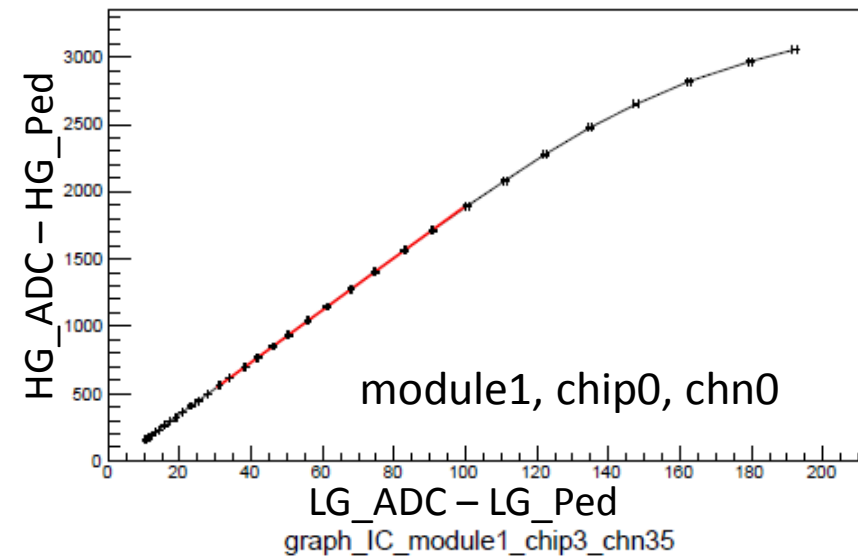


RMS of $IC_{\text{June}}/IC_{\text{May}}$ is 2.3%, mean is 1.001 ± 0.0006

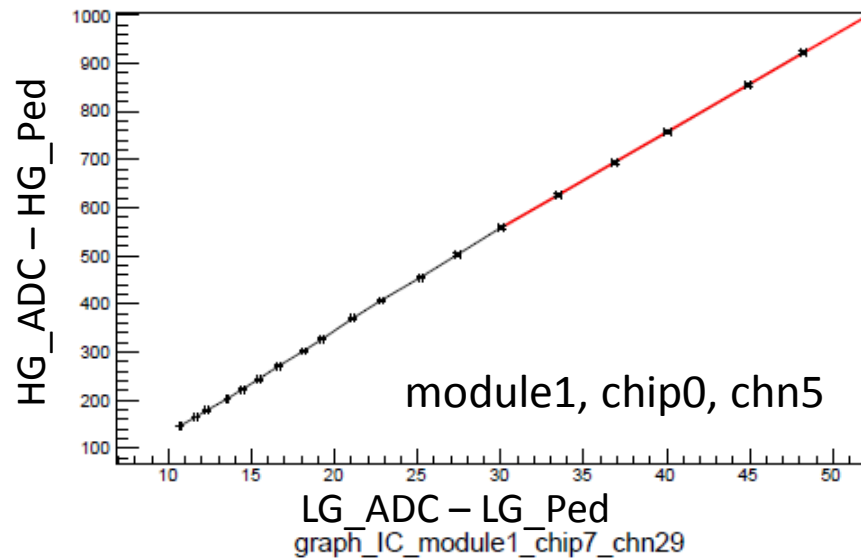
Slope of HG vs LG

- after pedestal subtraction
- fitting range $30 < LG < 100$
- total amount of charge in a chip < 60000 ADC (HG)
- at least 5 points in the fitting range

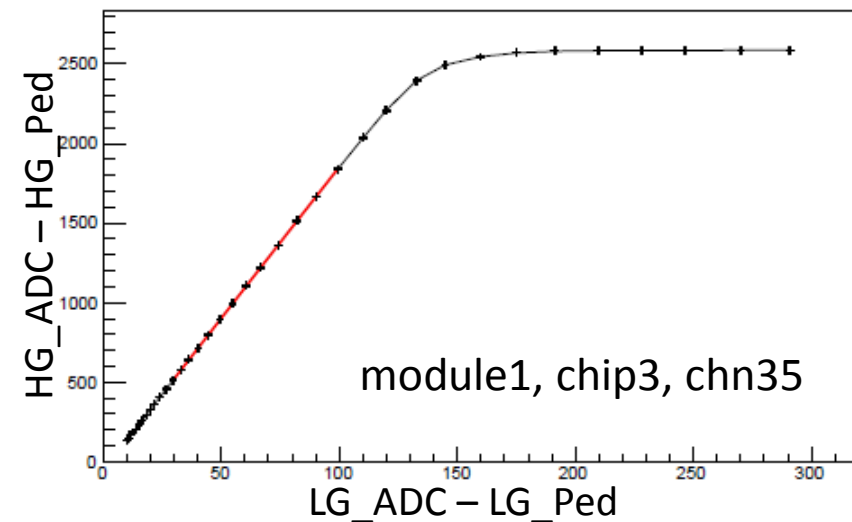
graph_IC_module1_chip0_chn0



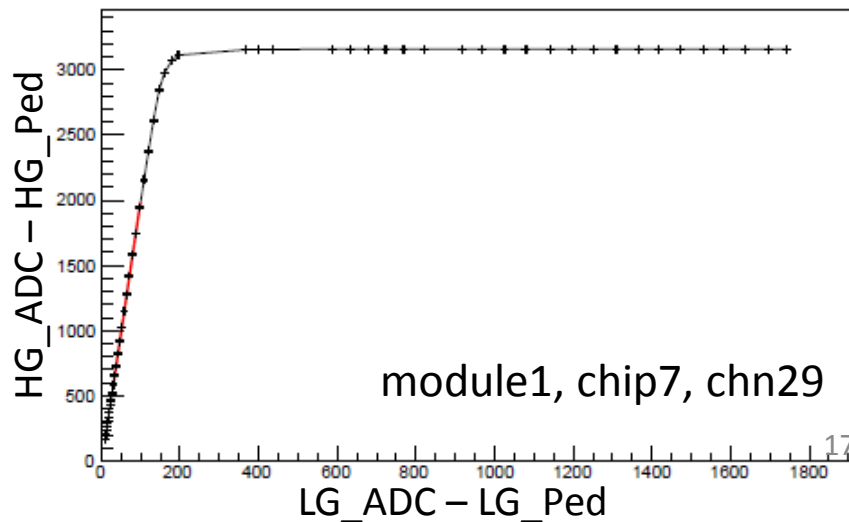
graph_IC_module1_chip0_chn5



graph_IC_module1_chip3_chn35

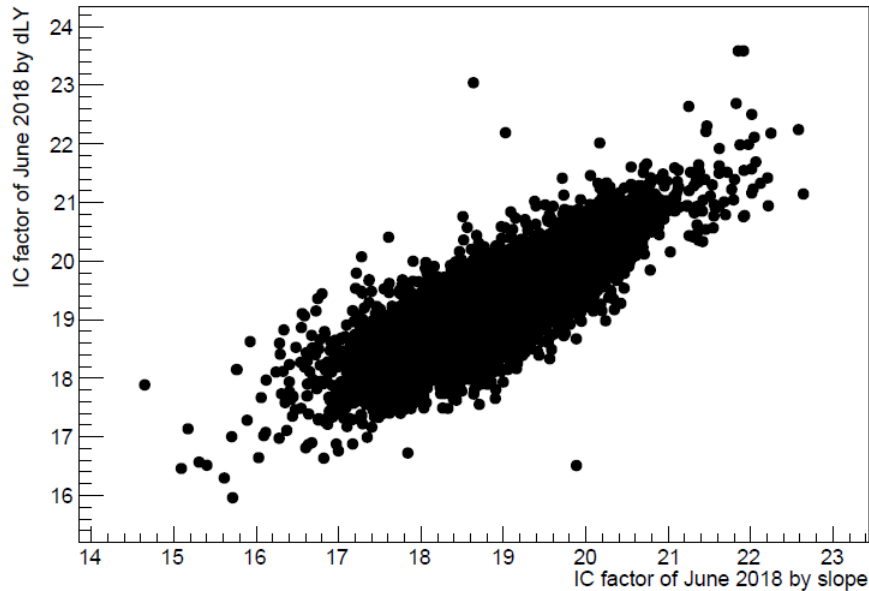


graph_IC_module1_chip7_chn29

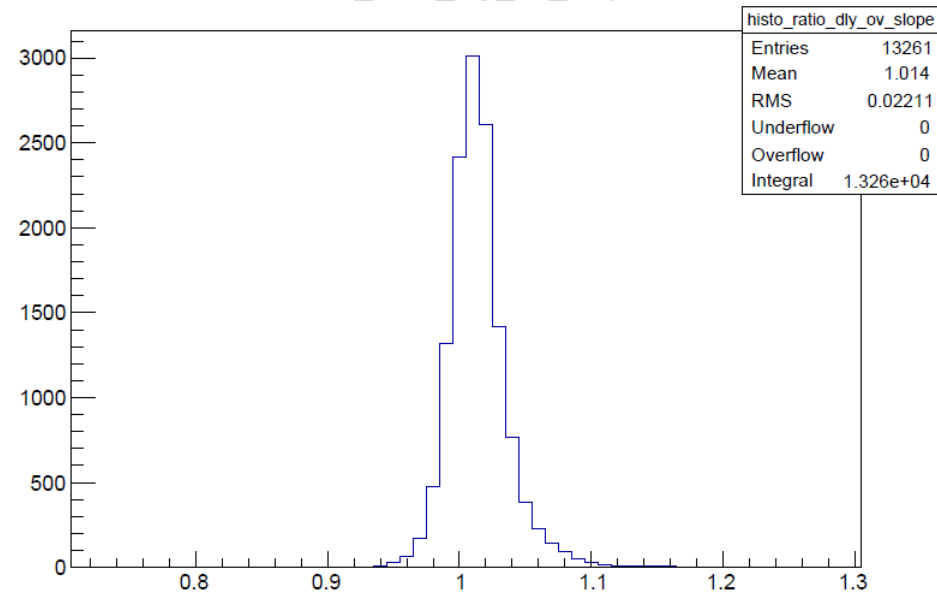


IC factor dLY vs Slope and IC_{dLY}/IC_{slope}

dLY vs Slope



IC_{dLY}/IC_{slope} histo_ratio_dly_ov_slope



- Mean of IC_{dLY}/IC_{slope} 1.014 \rightarrow 1.4% systematic shift
- RMS = 0.022

IC factor extracted by dLY and slope

1. fill IC values extracted by dLY within mean $\pm 3 \times \text{rms}$ of IC histogram of dLY
2. fill IC values extracted by slope within mean $\pm 3 \times \text{rms}$ of IC histogram of slope, if the IC values are not filled by first step.

