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Facing the challenges:

- 5 bunch trains per second (5 Hz)
- 3000 bunches within one train
- one bunch every 300 ns, 150 ns possible
- each bunch to be registered
- high dynamic range (better 1:10k)
- more than 10k channels, depending on design
- Fast, low power, rad hardness to be considered

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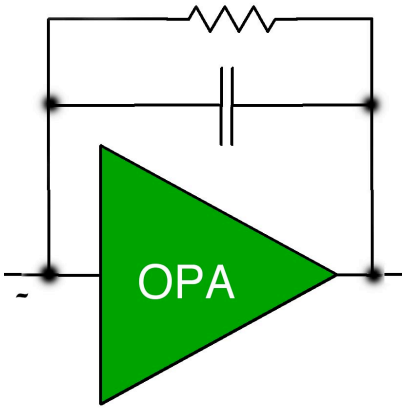
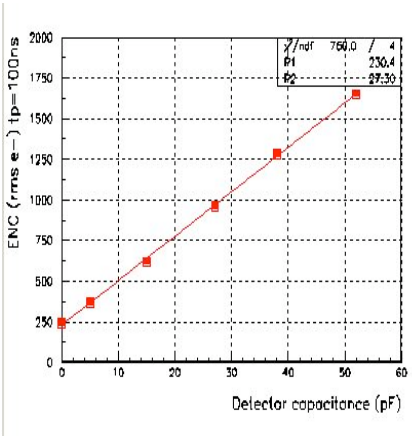
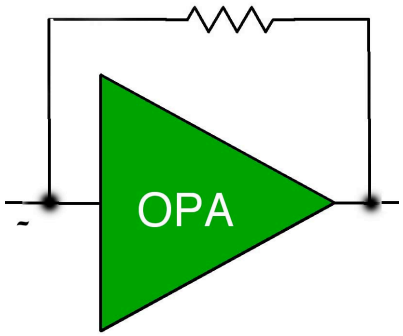
Basic Concepts:

- charge sensitive frontend





- current sensitive frontend



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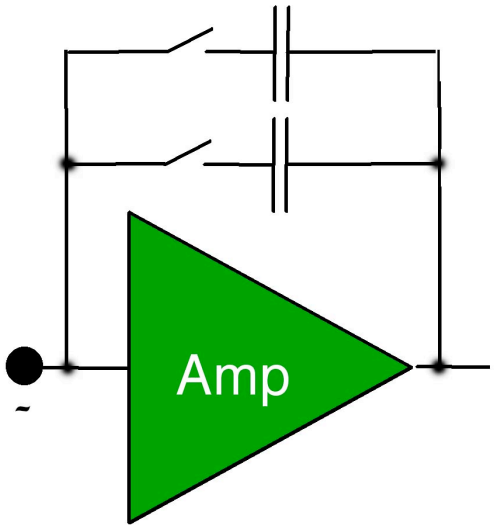
Dynamic Range:

- operation with two (more) scales:



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Analog or Digital Storage:

- 3000 bunches within one train
- one bunch every 300 ns, 150 ns possible

→ analog storage nearly impossible

(depth, decay of charge, switching noise)

→ Digitization with ADC, staggering?

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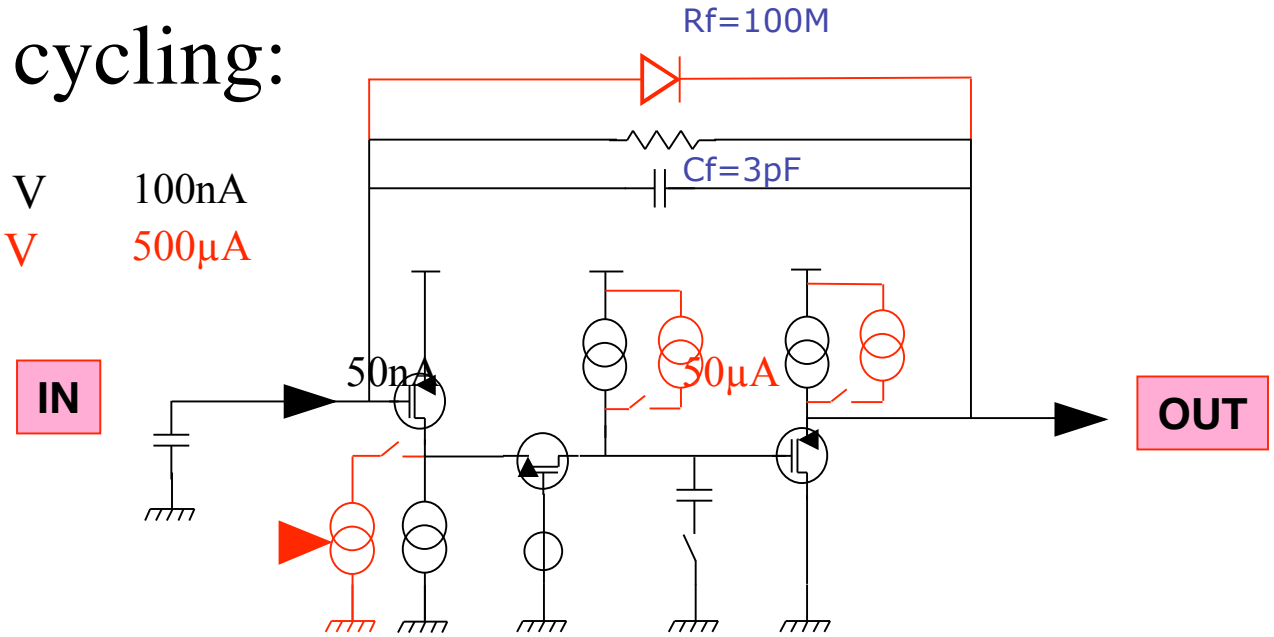
Power Consumption:

- more than 10k channels, depending on design

→ power cycling:

Low current : - 0.5 V 100nA

Hi current : - 0.85 V 500µA



PICTURE:
CH. DE LA TAILLE

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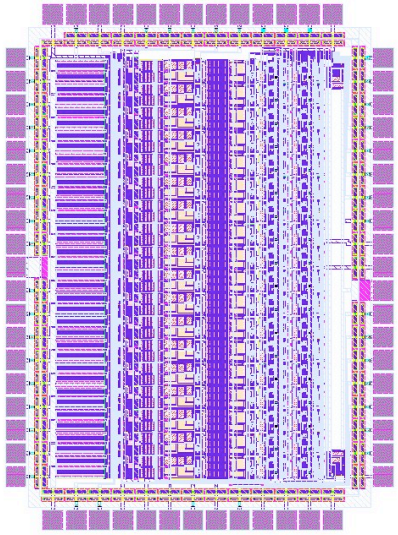
The Way To Go:

- Integrated solution after testing concepts



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The Price To Be Payed:

- About 5 man-years **+** (electronics engineer)
- Several chip submissions (collaboration?)
- And, and, and

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Next Steps:

- Investigation of preamp principles
- Feasibility studies of digitization
- Investigation of known r/o systems
  (FLC Calice (Orsay))
- developing and refining of building blocks