Detector InterFace (DIF) board status for CALICE SDHCAL

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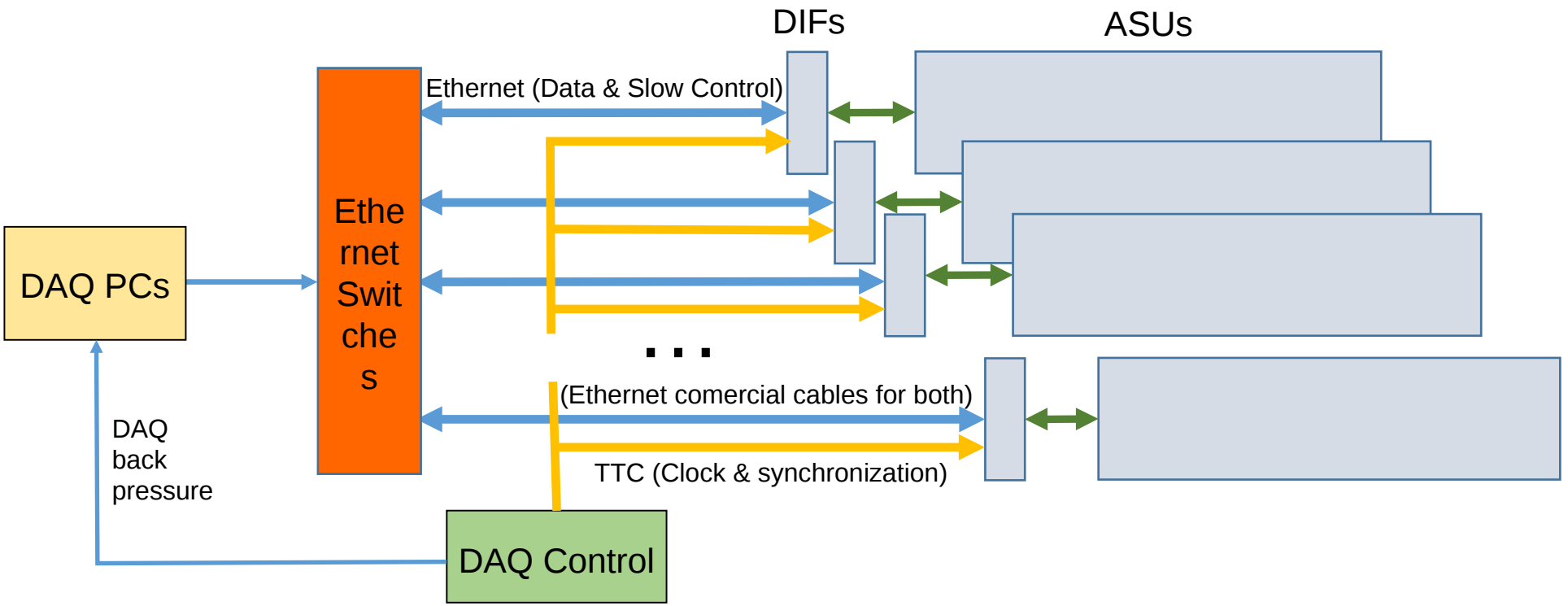
Outline

- SDHCAL DAQ architecture.
- DIF main characteristics and architecture.
- DIF to plane interface.
- DIF PCB. Power distribution plane and circuits.
- DIF + ASU tests: Java application.
- DIF status.
- Summary.

SDHCAL DAQ architecture



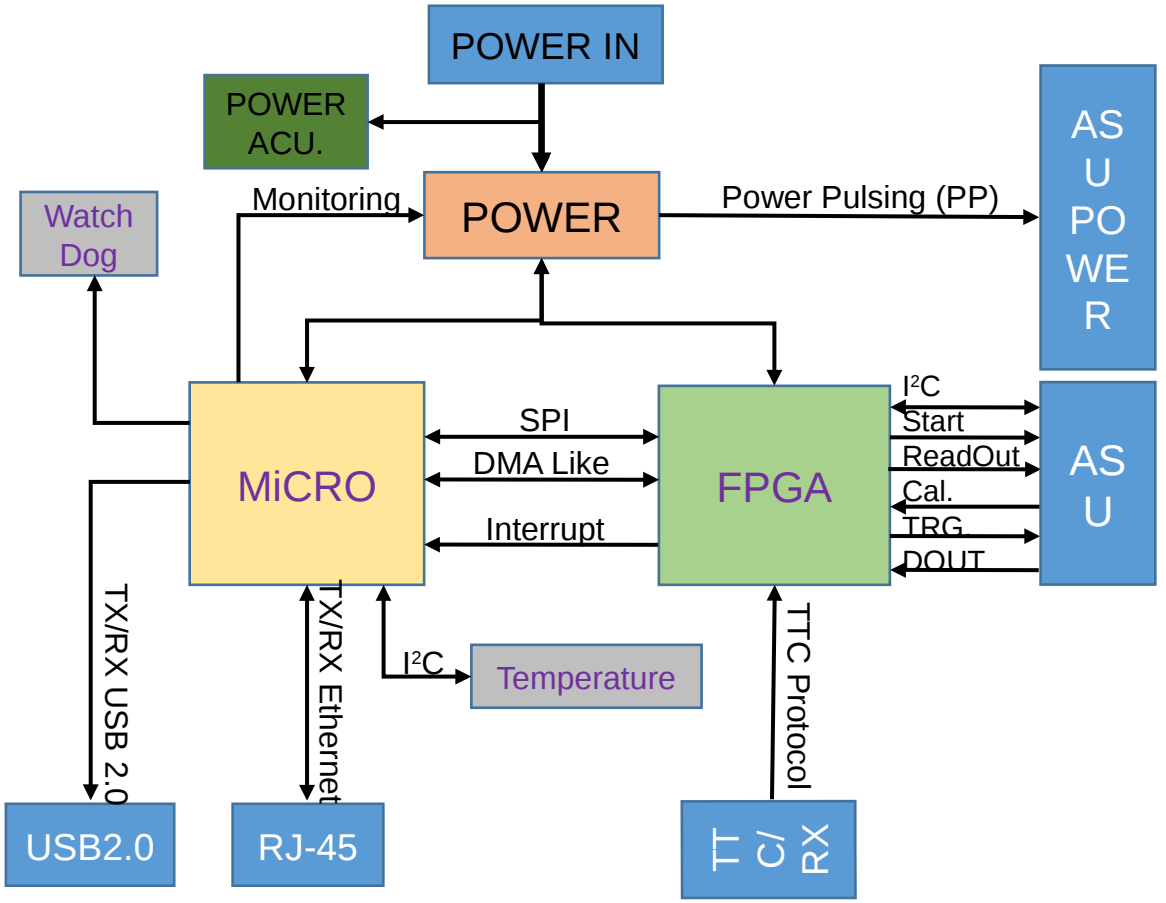
- One DIF per plane, including 3 ASUs (Active Sensors Units).
- Slow control & readout by Ethernet using commercial switches.
- Clock & synchronization (time & trigger) by the TTC system used in the LHC.

DIF main characteristics

- The DIF is the interface board between the ASU board with all HARDROC3 (HR3) ASICs and the DAQ software. It can handle up to 432 HR3 (1 x 3 m detector).
  - ASU interface → Kyocera connectors (80 pins for signals and supply).
  - DAQ interfaces.

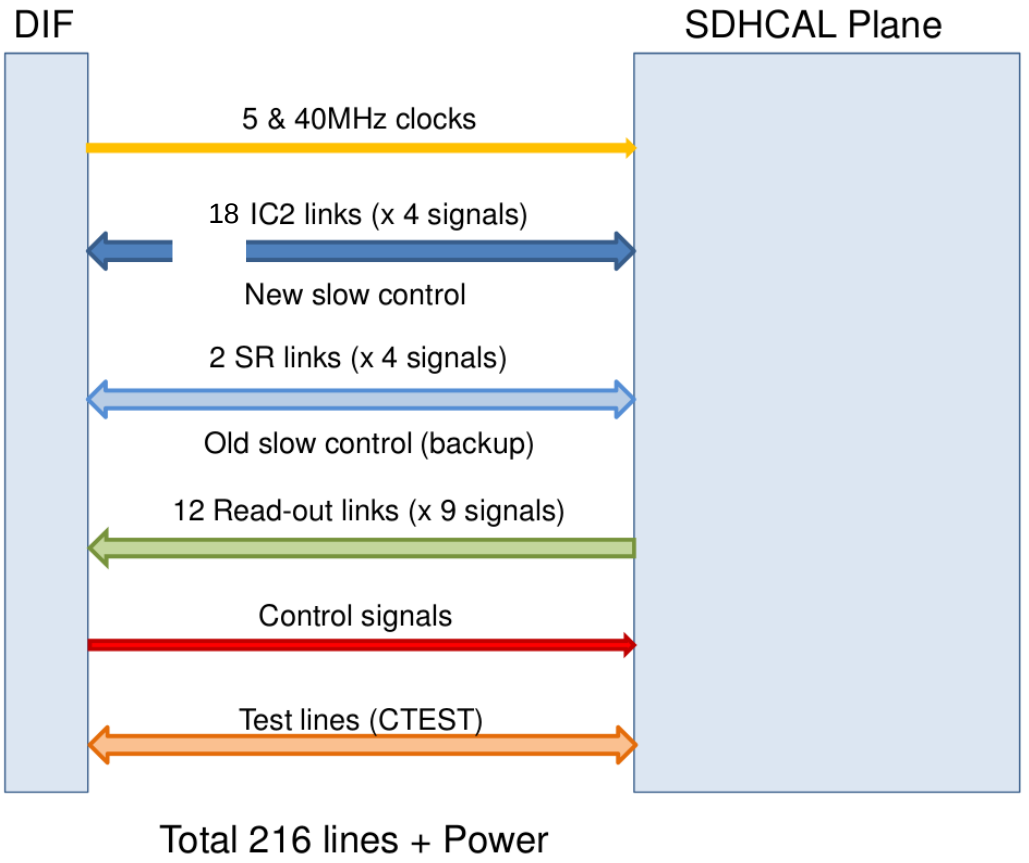
    1. TTC link (sends both the clock and synchronous commands to the ASIC).
    2. Ethernet (UDP) → to receive all ASIC data.
- It is developed with a FPGA and a MCU to ensure communication with both ASICs and DAQ software (using Ethernet link).
- The DIF controls the HR3 configuration through redundant I2C, performs readout and sends data to the DAQ software.
- It receives all ASICs configuration data and local DAQ commands and sends data to the DAQ software through a local Ethernet interface.

DIF architecture



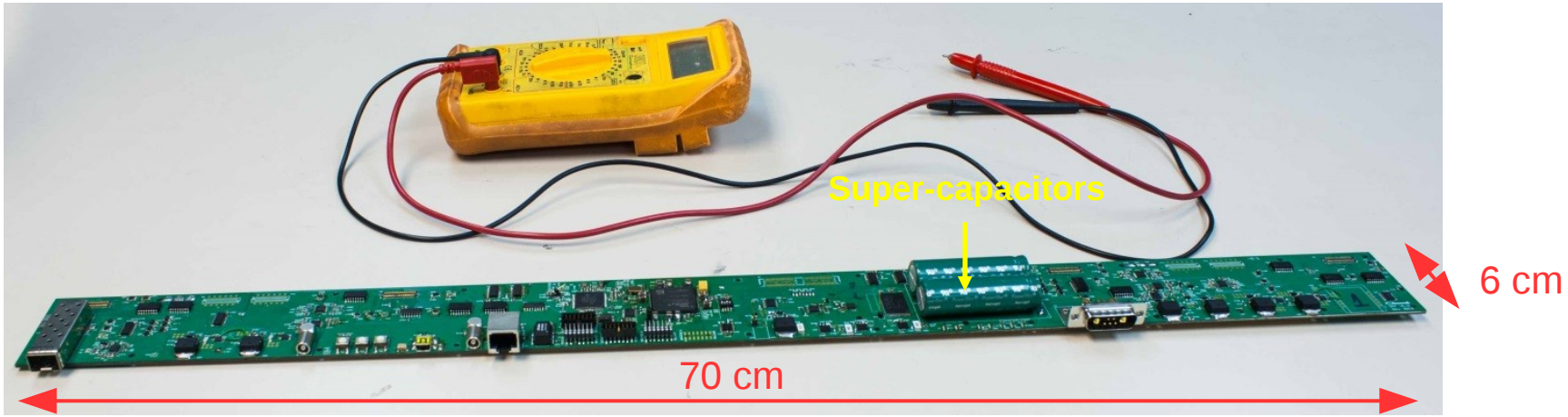
- HR3 slow control through I2C bus (two of the old slow control buses only as backup)
- Data transmission to/from DAQ by Ethernet. USB 2.0 (for debugging).
- 93 W Peak power supply with super-capacitors.

DIF to plane interface



- HR3 communication:
  - 18 I2C lines → 12 parallel lines + 6 redundant shared between two adjacent lines of maximum 36 ASICs (for speed and reliability reasons).
  - For each line ASIC, configuration (one I2C line + 1 redundant) and ASIC readout (two open collector serial links) are on separated doubled lines.

DIF PCB (I)



- **Design**: it must be as close as possible to each ASIC line, filling the narrowest space.
- **Super-capacitors**: the global power supply can provide the average power (not the maximum). These capacitors are the local storage for the current needed during the detector active period. Requirements → 30 A at 3.7 V. Solution → 2 x 100 F / 2.7 V.
- **TM4C1294NCPDT MCU** (120 MHz, 10124 KB flash memory):
  - Update FPGA configuration. Receive and execute DAQ commands.
  - Receive, store locally and send HR3 readout data (via Ethernet).
  - The selection of I2C lines through 1-Wire.
  - Control the power supply of the plane. Read the power and temperature sensors.

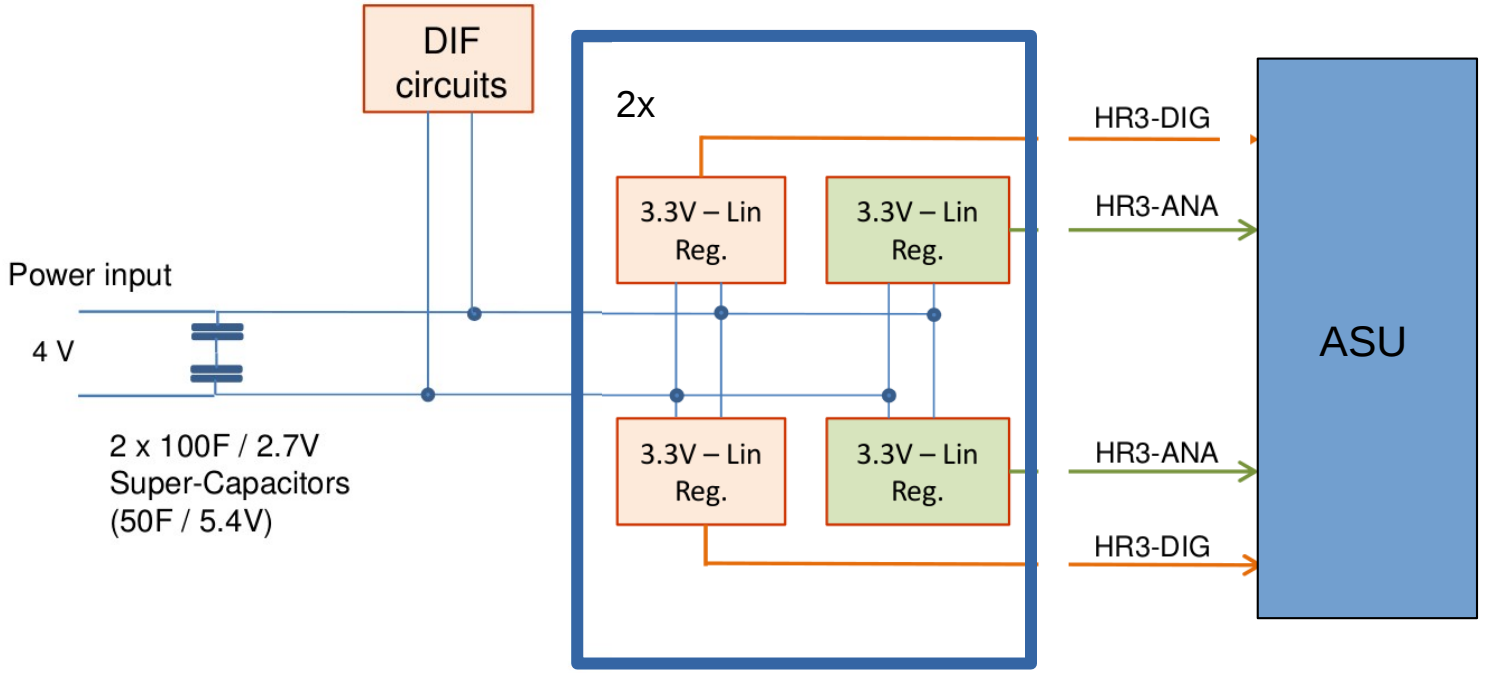
DIF PCB (II)

- **Xilinx Artix–7 FPGA** (pins 3.3 V compatible, RAM from 1800 to 13140 kb):
  - FPGA and MCU exchange the HR3 configuration through SPI and FPGA generates 18 independent I2C lines which can work in parallel.
  - Readout information is transferred using a DMA Like.
  - Synchronization and transmission of TTC clock to the plane.
  - Transform fast commands coming from TTC into signals for the detector plane (*Reset, Start_Acq, Triger_ext*) and informs the processor about the new state.
- **Digital readout**:

  1. Trigger mode → the ASICs are active after the *StartAcquisition* signal.

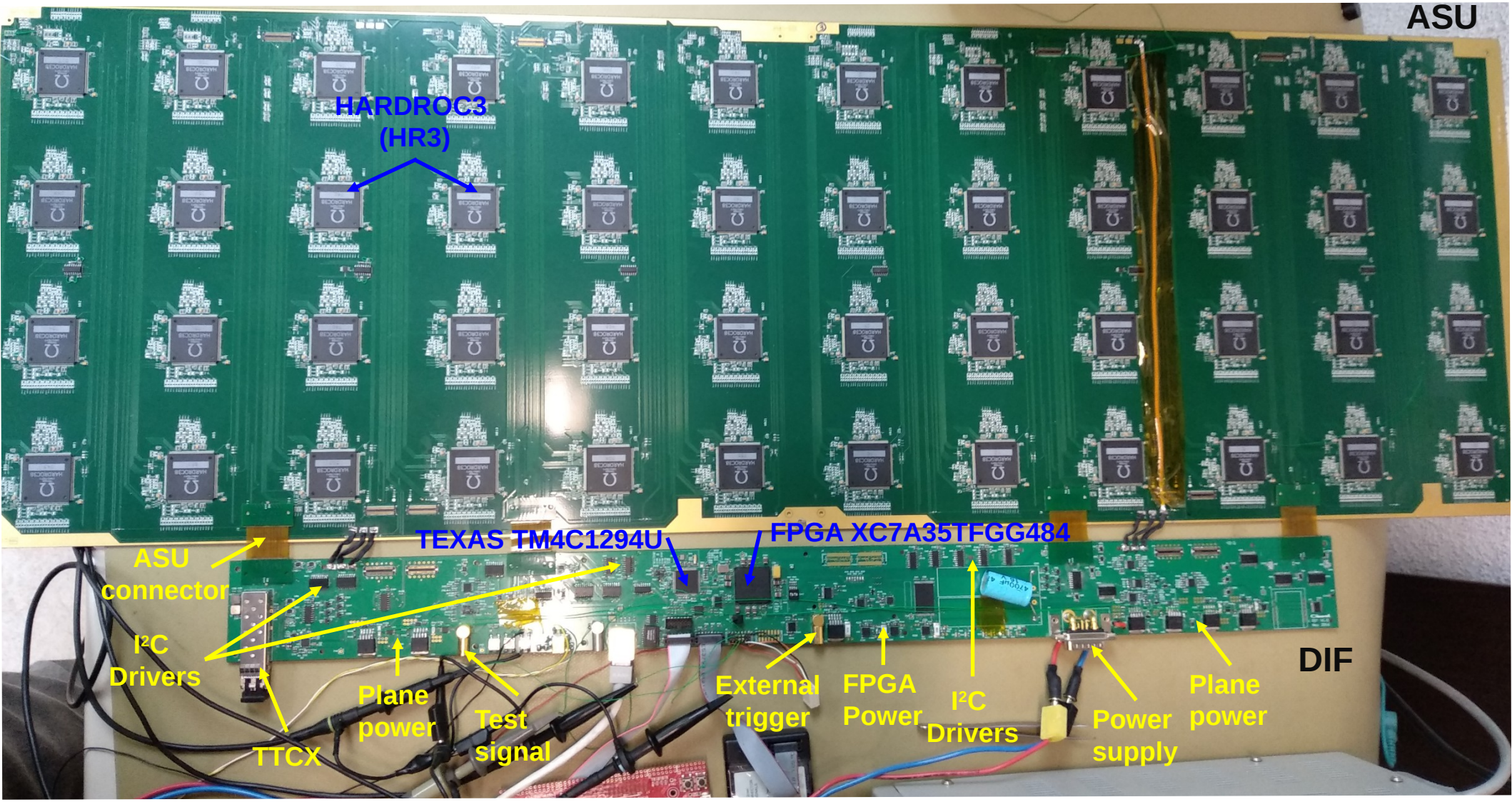
  2. Triggerless mode → the ASICs are put into acquisition state at the start of a Spill signal (the accelerator clock).
- **Power pulsing**: during the inactive period, ASICs can be switched off to reduce the power consumption of the electronics and thus the heat dissipation in the calorimeter.
- **Data format**: to make easy the reconstruction and analysis of the data, additional information are added to the data stream (the ASIC data are encapsulated in a specified format by the DIF's FPGA with a header, a trailer and some information).

Power distribution: plane and circuits

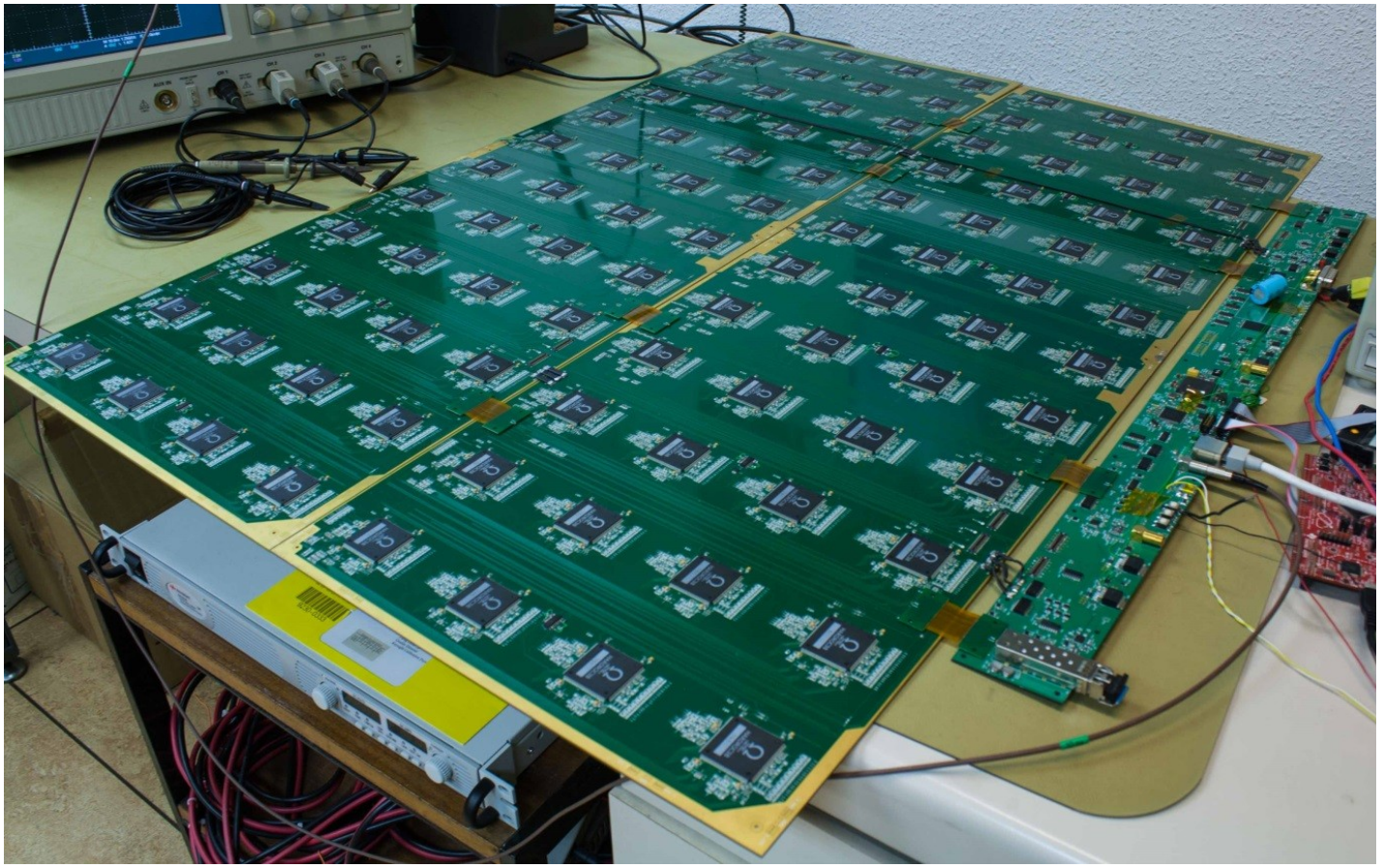


- **Plane**: two analog and two digital voltage regulators.
  - Regulators low dropout type (about 500 mV max) needed to power the plane.
  - Current monitoring and over-current protection per output voltage and slab.
- **Circuits**: FPGA and MCU can be also set to low power mode.
  - Switching regulators for lower voltages (1.0 and 1.8 V) to reduce dissipation.
  - FPGA power ON sequencing is done from the MCU.

DIF + ASU tests (I)

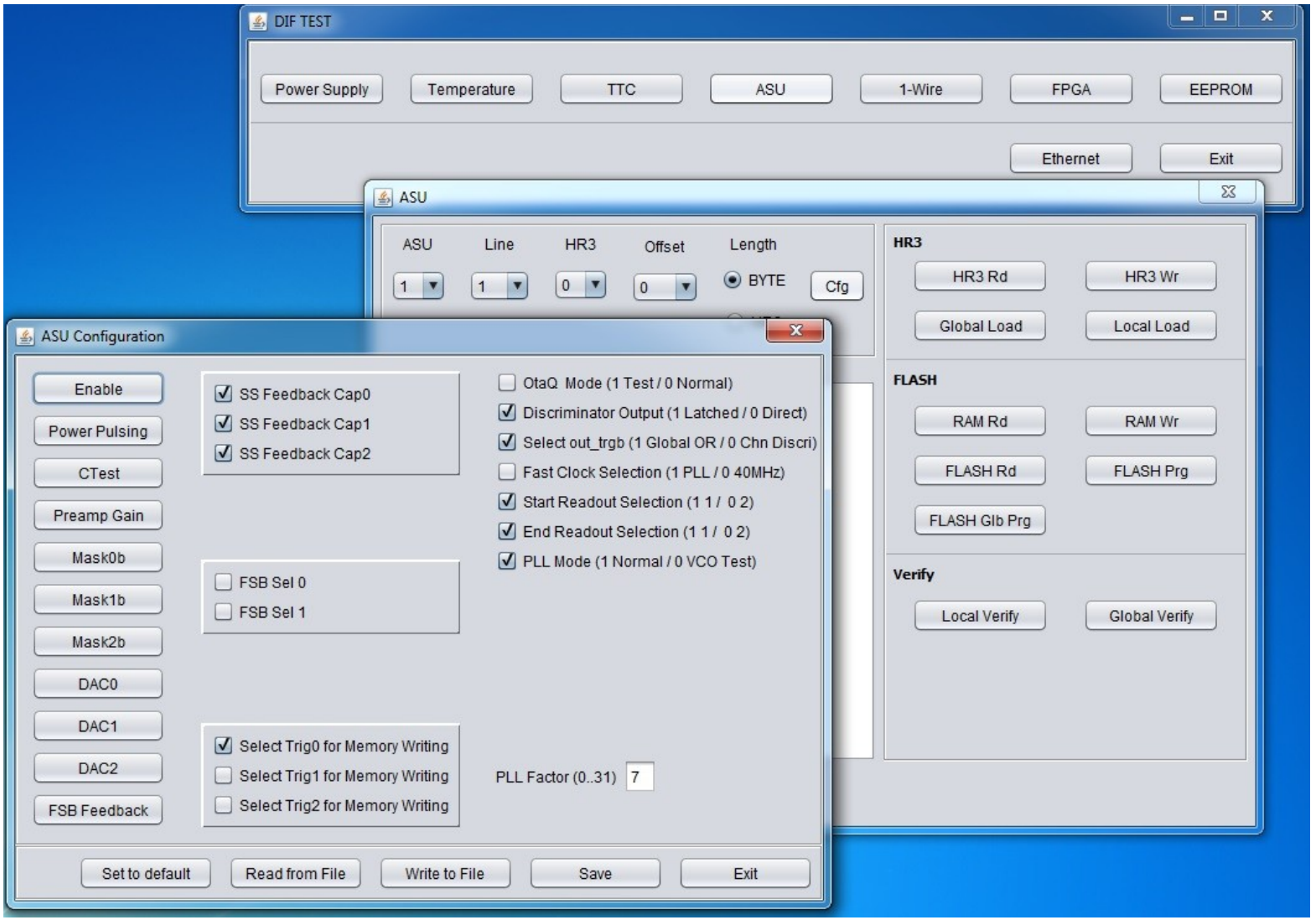


DIF + ASU tests (II)



- Tests done with an individual DIF, DIF + 1 ASU and DIF + 2 ASUs connected.
- A last test with 3 ASUS will be also done.

Java application



A Java application designed to test the different functionalities of the DIF and ASU.

DIF status

- **Documentation:** Schematics and Layout √
- **Fabrication & Assembly:** 4 DIFs fully assembled and operational √
- **Firmware development:**
  Micro-processor
  - Ethernet communication √
  - FPGA communication √
  - Data acquisition √

  FPGA
  - I2C √
  - Synchronization √
  - Power Pulsing χ
  - Data acquisition √
- **Functional tests:**
  - Power √
  - FPGA √
  - Micro-Processor √
  - TTC Synchronization / commands √ / χ
  - Power Pulsing (super-cap) / ASU √ / χ
  - Old slow control test with ASU √
  - I2C slow control test with ASU √
  - Data acquisition test with ASU χ

Summary

- 4 DIF boards fully assembled.
- Most of the performances of the DIF are completely tested.
- DIF remaining tests:

  1. Power Pulsing (PP) mode → PP will be tested using one ASU and simulating powering ON the ASICs (beam) and OFF (the rest of the time).

  The super-capacitors were tested with an active load simulating real conditions (5 ms of every 200 ms). Both a resitive and a capacitive loads were used.

  2. Data acquisition → it will be tested the data transmission from HR3 to the DIF and sending data to the DAQ using Ethernet (UDP).

  3. TTC commands → in the synchronization part.