SiW-ECAL overview

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CALICE Meeting
Utrecht Uni
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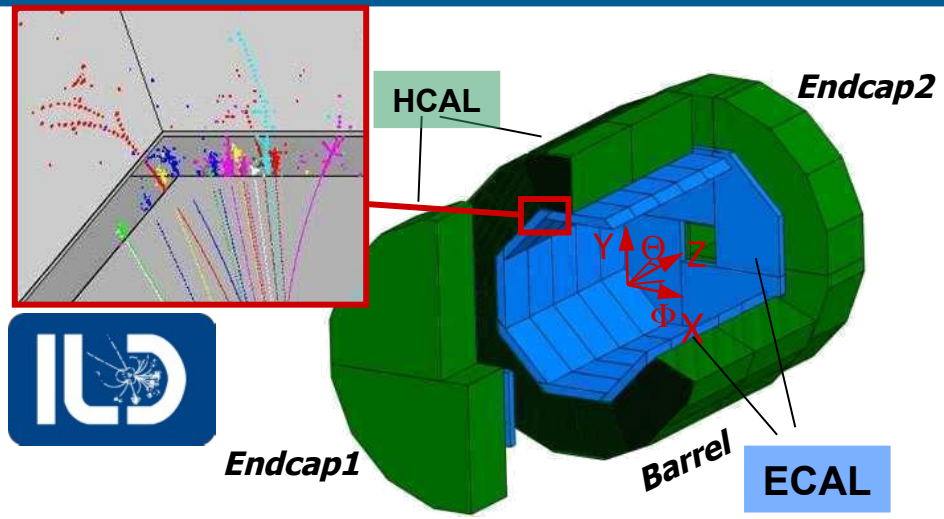
TNA support + WP14

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (E, (θ,φ), t)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)

SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material

  X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm

  Narrow showers

  Assures compact design

- Silicon as active material

  Support compact design: Sensor+RO≤2mm

  Allows for ~any pixelisation

  Robust technology

  Excellent signal/noise ratio: ≥10

  Intrinsic stability (vs environment, aging)

  Albeit expensive…

- Tungsten–Carbon alveolar structure

  Minimal structural dead-spaces

  Scalability

To be assessed by prototypes

Not included: general services

SiW-ECAL Building blocks: SLAB's & ASU's

R&D for "mass production" and QA

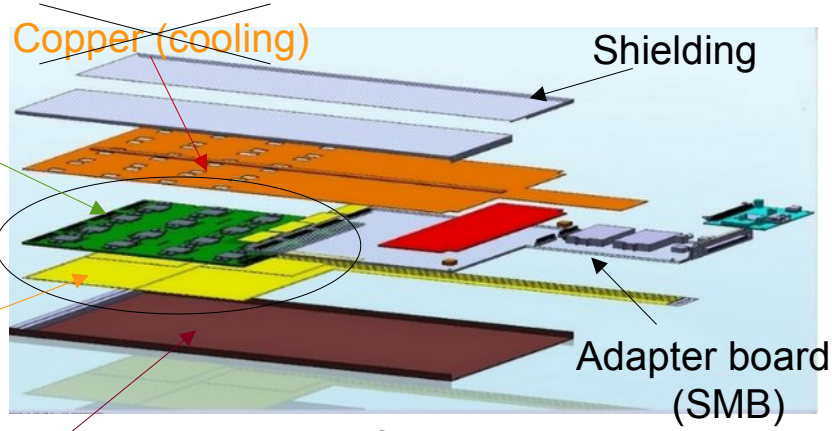
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
- Choice of square wafers
  - (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m)
(likely to be reduced by 30–40%)

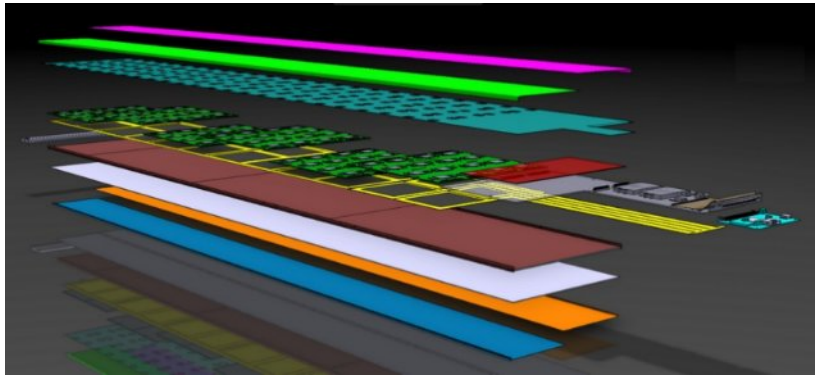
- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m²)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - ≠ lengths and endings

Tests of producibility (15)

Tests of feasability (1/4)



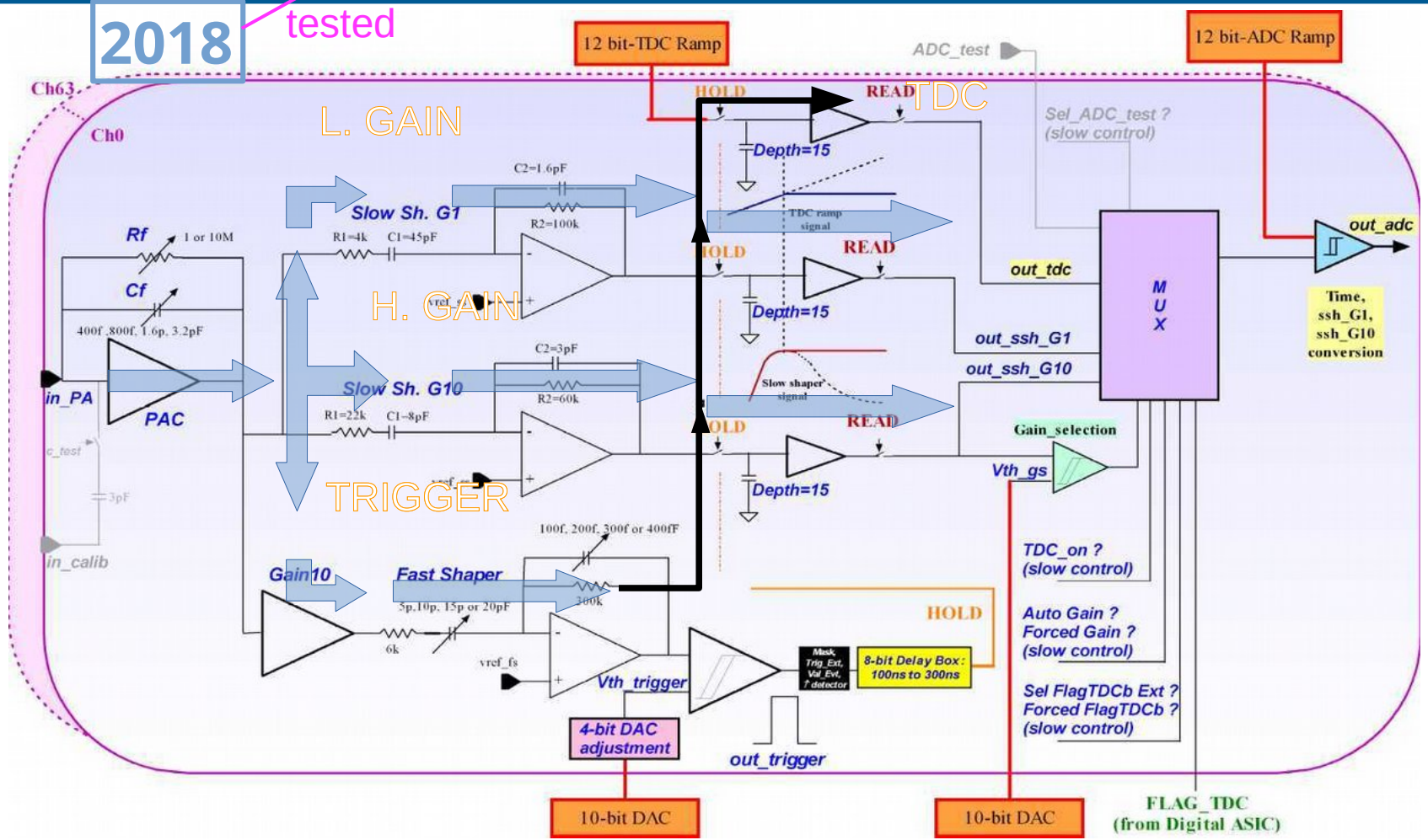
U layout of a **short slab**



U layout of a **long slab**

SKIROC2 / 2A Analogue core

2018 tested



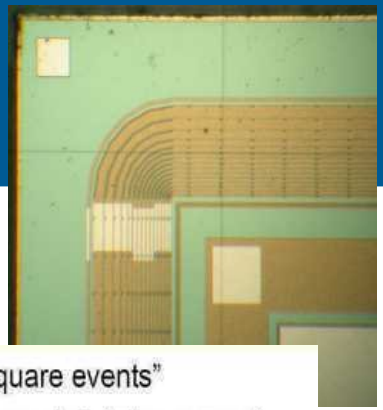
Similar to SiD Kpix

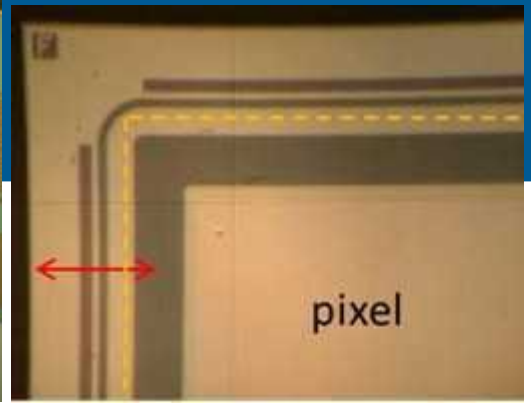
- 64 channels
- Preamp
  + 2 (auto)Gains
  + **TDC** (~1.4ns)
- Auto-triggered
  - **per cell adj.**
- 15 (×2) analogue memories
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-pulsed

Main default: Re-triggering

Not final chip (full 0-suppr.)

Silicon Sensors





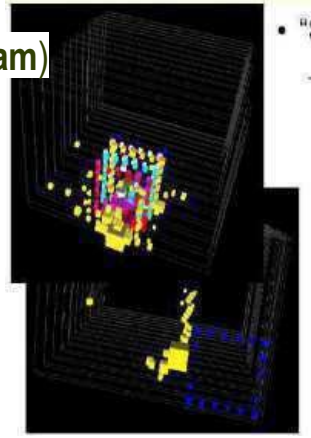
Cost driver

- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction(**CALIIMAX ANR program**)
- Decoupling of Guard Ring (Square Events).
- new design of ILD detector

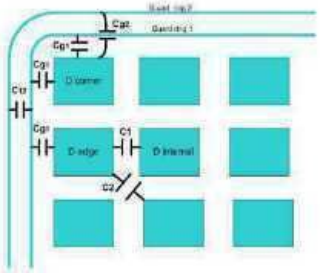
Command Sensors (@ Hamamatsu)

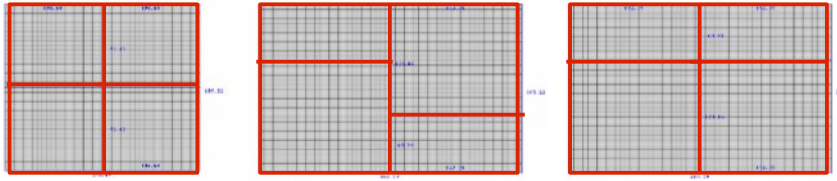
- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8'' in 186mm alveola
  320, 550, 650 → 725 µm ?

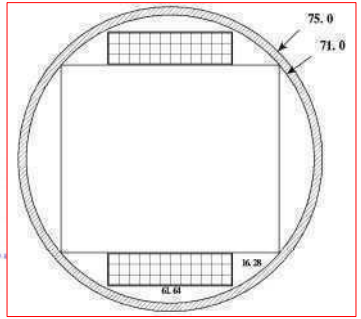
Wafers glued onto PCB's



- "Square events"
  - cross talk between guard rings and pixels

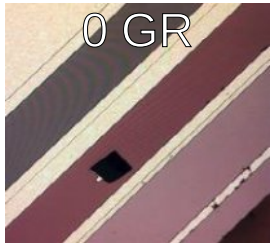


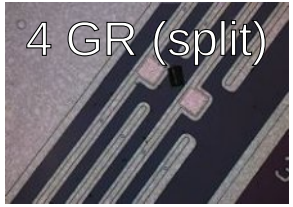


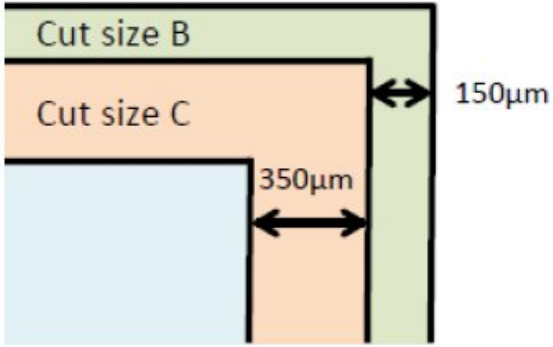


'quantum unit' of ILD dimensions (here 6'' wafer)

Guard Ring Studies (HPK)







Baby wafers: contig. & segmented Guard ring - 0, 1, 2, 4

- Floating 1 GR ⇒ 'square events'
- Addit'l GR ⇒ higher BD voltage

Cuts size ~ insensitive edge

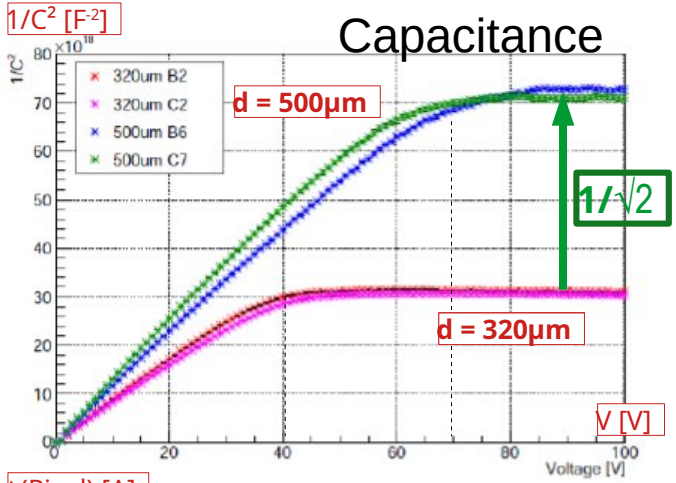
- Cut size B = 500 µm
- Cut size C = 350 µm

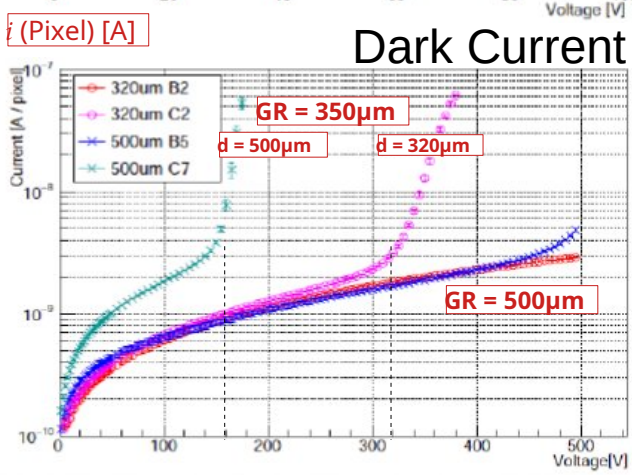
Prelim Conclusions:

- 320µm cut size C ✔
- 500 µm cut size B preferable

new 2018: 550 & **650** µm wafers

but HPK capacity for 8" ≥2020

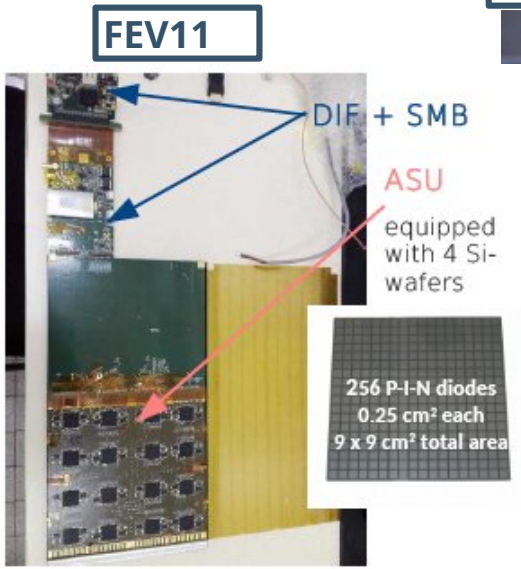


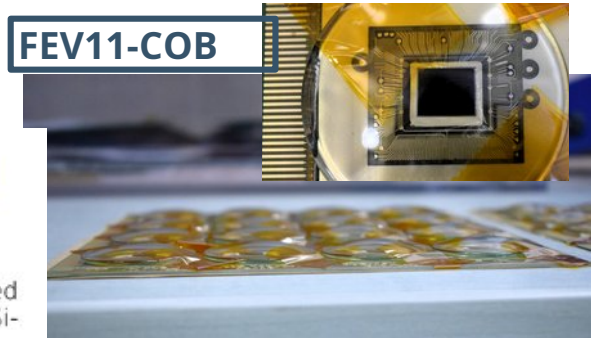


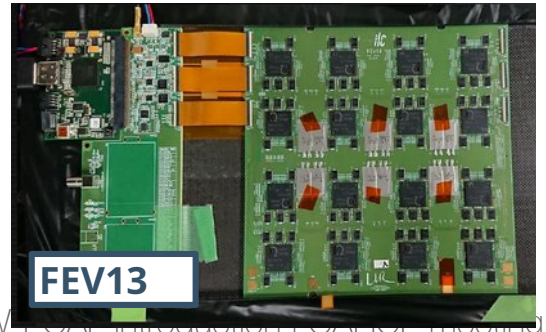
ASU: 12 years of R&D

Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints



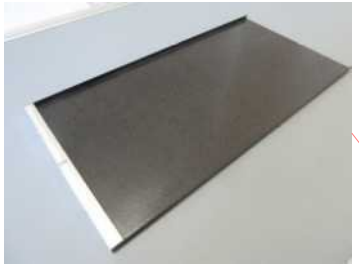


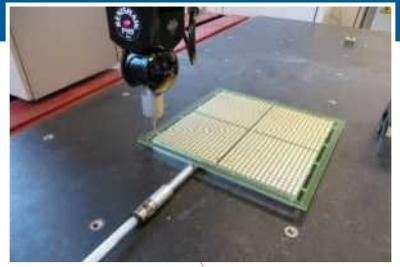


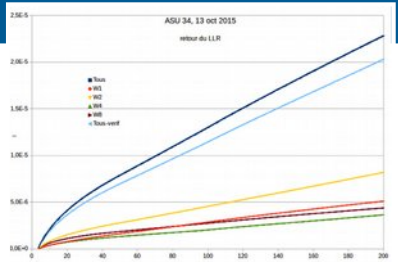
Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	7 units	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	SLABvFEV11 & FEV13 SK2a+ Compact stack	SK2 & SK2a (⊃timing)	Improved S/N Timing...

Assembly chain Paris

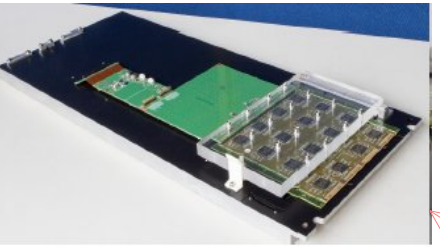
To be improved and extended

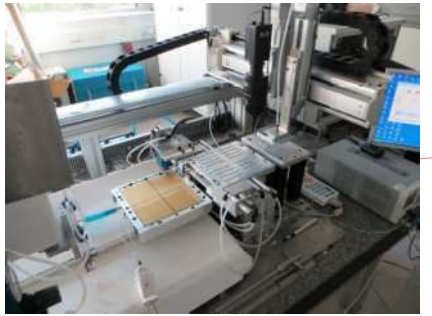


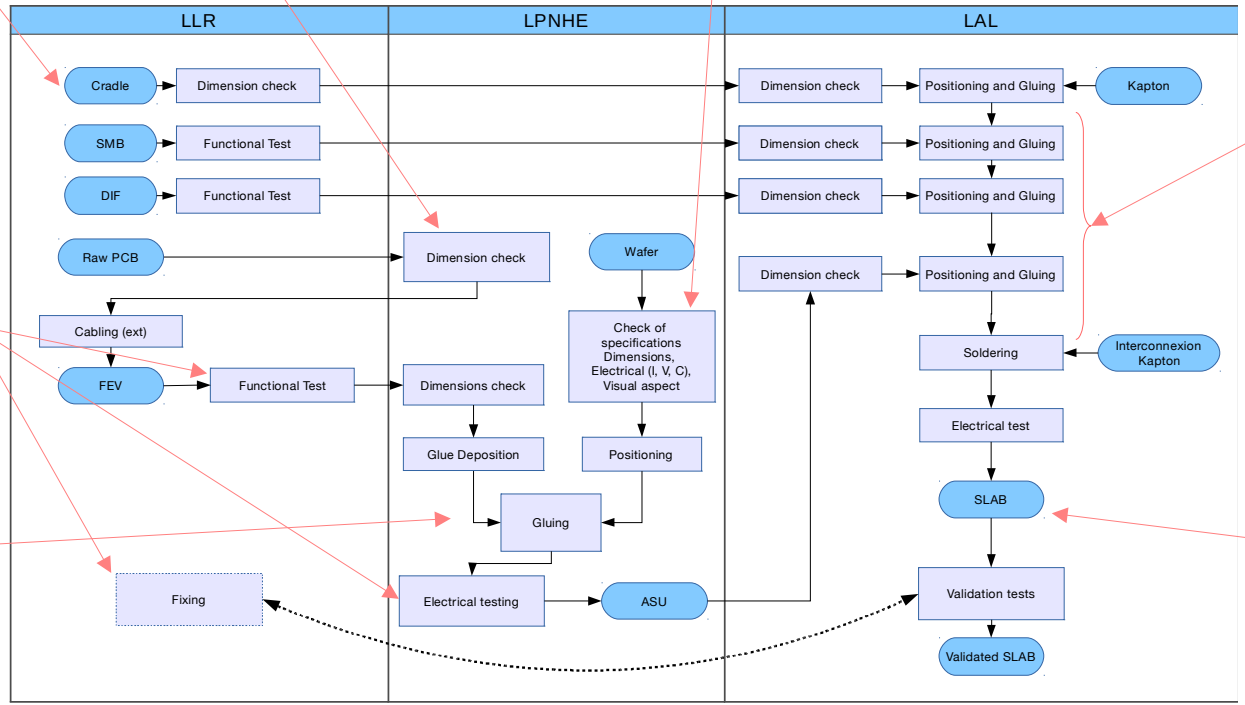


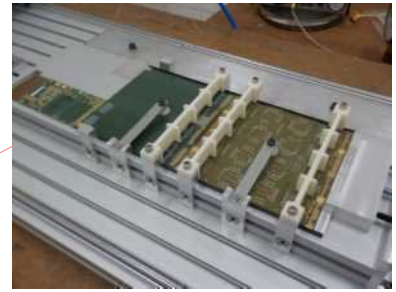


'Simplified view'







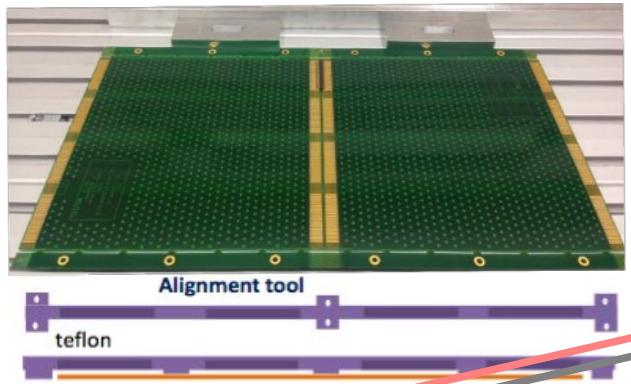


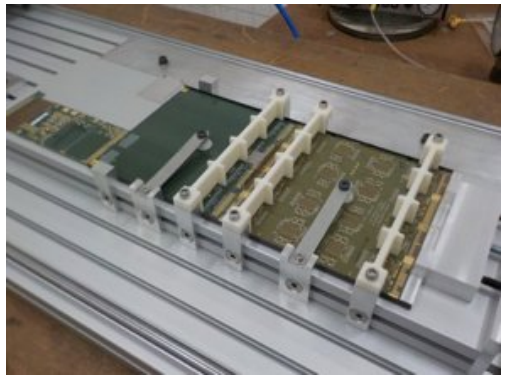
Mechanical Assembly for SLABs

Assembly bench for:

- Fragile Wafer
- Precision of PCB's ~ 50µm

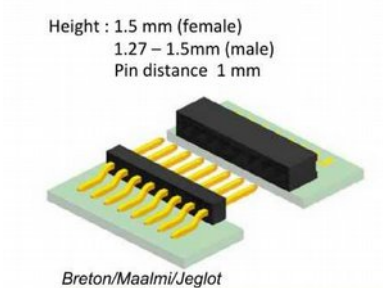
  ⇒ precision of 100µm on SLAB
- Interconnection

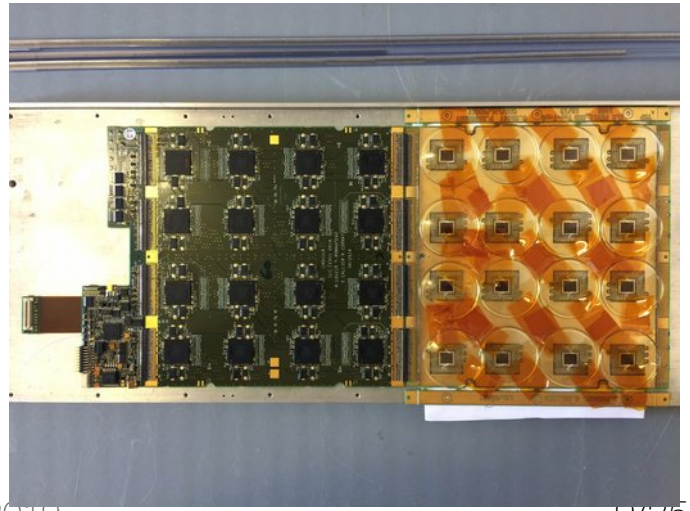




Connections to be handled by industry

- Dedicated Kaptons ✘
- Connectors
  - Grad-Conn
  - Antalec (near Orsay)



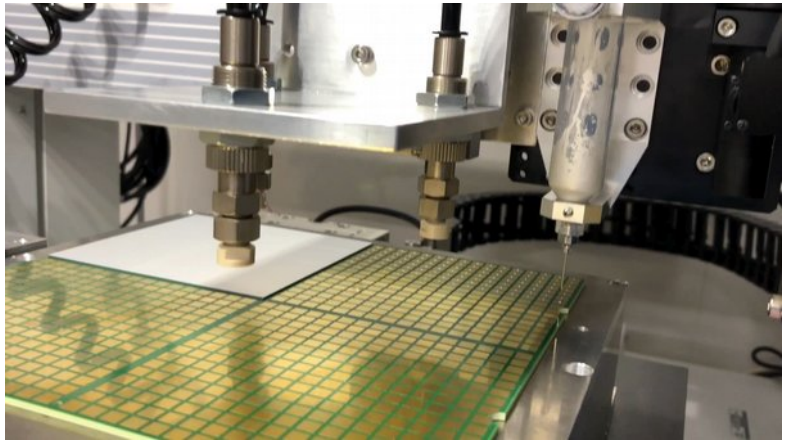


End of Slab and DAQ R&D

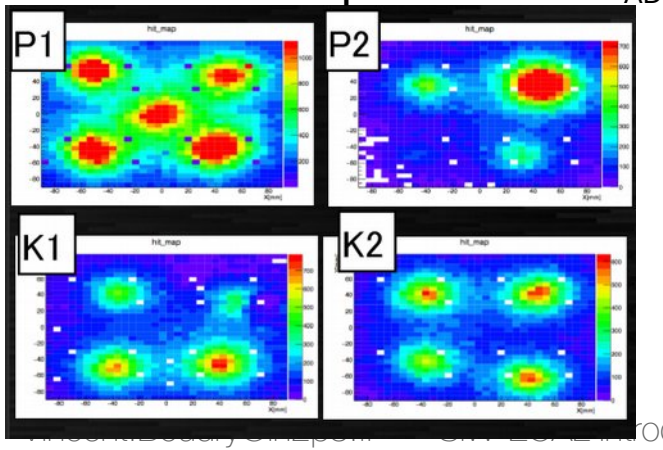
Jimmy

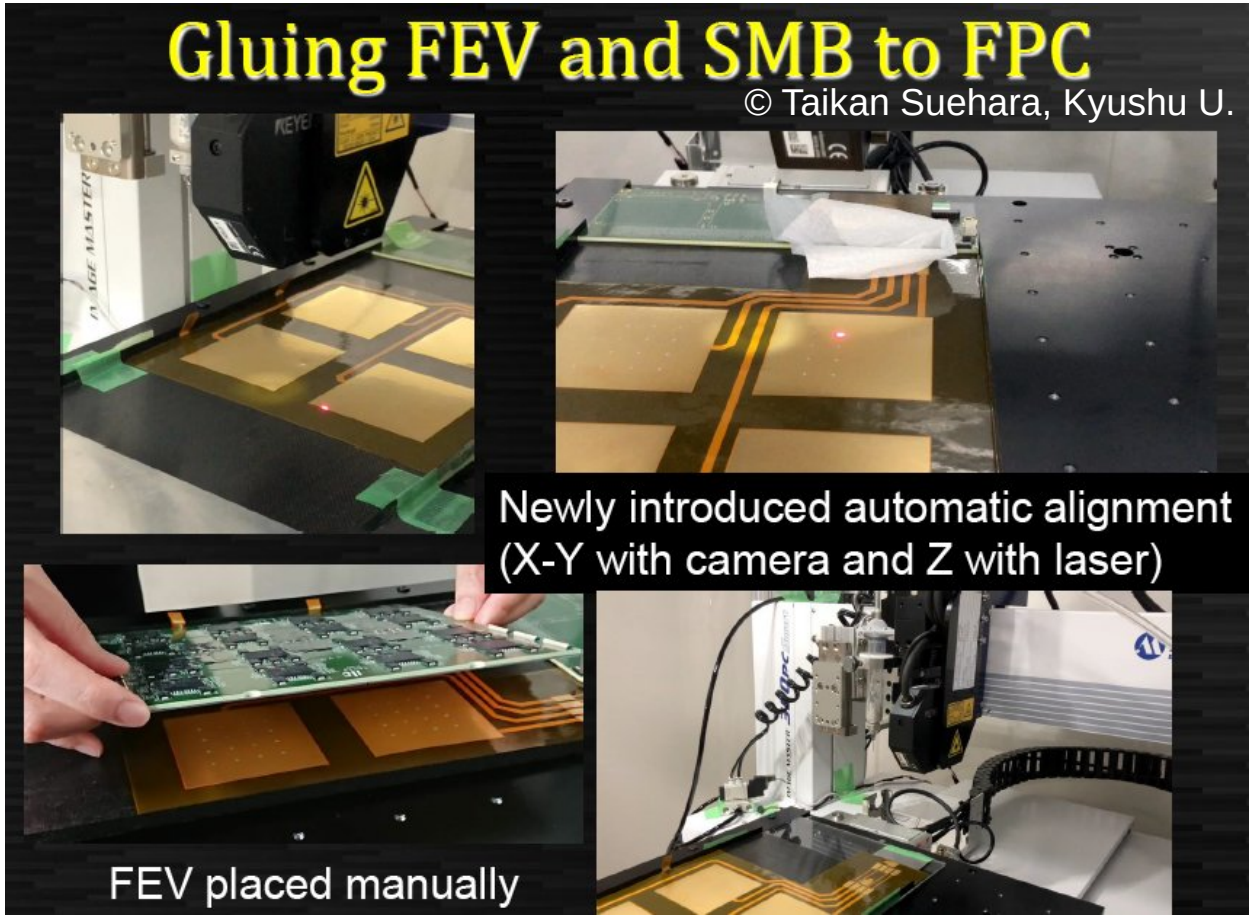
Second assembly bench (FEV13) @ Kyushu

Taikan



^{57}Co response $S/N_{ADC} \sim 30$

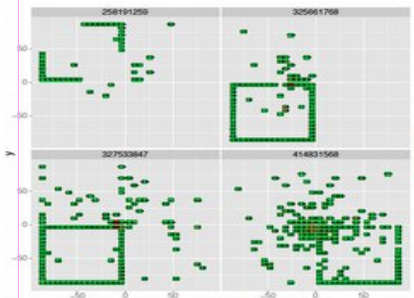


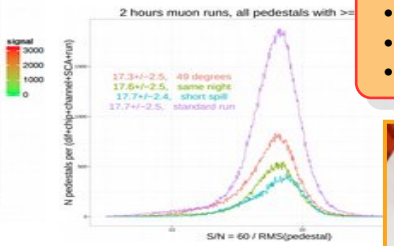


Beam-test 2015–2018

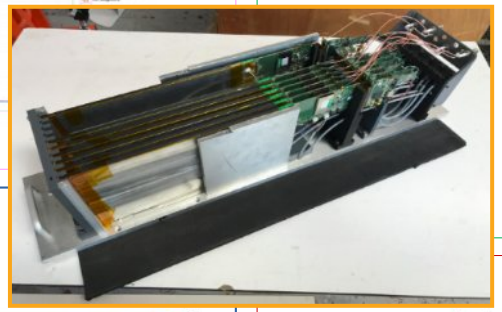
CERN 2015

"Naked FEV11"





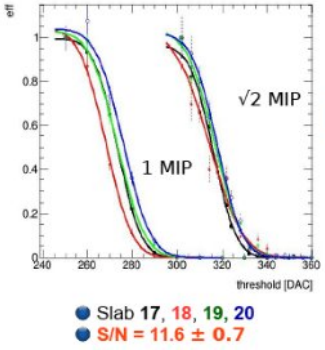
S/N_{ADC} = 16–17
(MIP – ped) / σ_{ped}
Defaults cataract :
- Negative signals
- re-triggers
- ~ high thr.
- sq events / 10

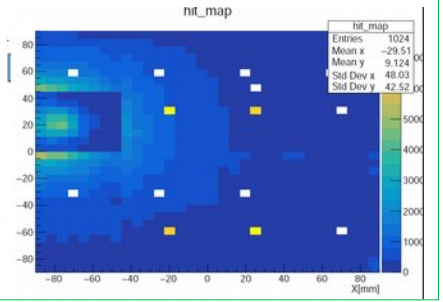


DESY 2018

7 FEV11 + 1 FEV13(650µm)

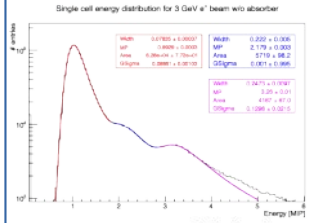
S/N_{Trig} ~ 11.6.±0.7
Trigger → ~1/3 mip (est.)
First comm. of FEV13

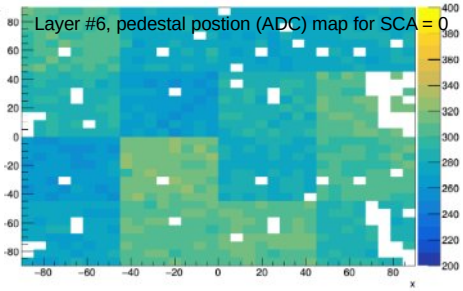


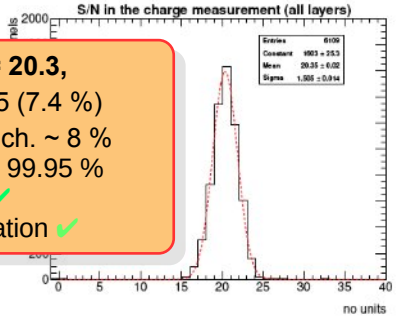


DESY 2017

7 FEV11





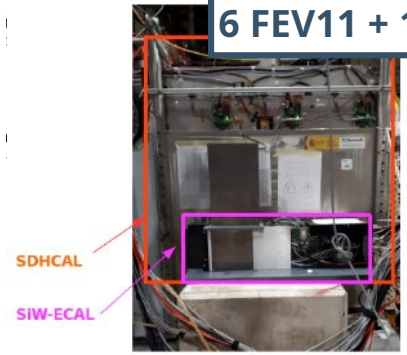


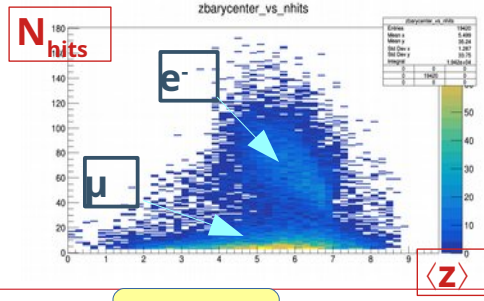
S/N_{ADC} = 20.3,
$\sigma_{S/N}$ = 1.5 (7.4 %)
masked ch. ~ 8 %
Hit eff. ~ 99.95 %
0°, 45° ✔
1T operation ✔

CERN 2018

Masked ch (FEV11) ~ 4 %

6 FEV11 + 1(4) FEV13(320 & 650µm) + 24X_0 W





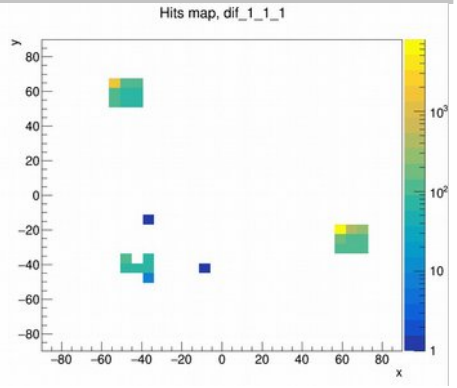
COB SLABs for BT2019

Adrian

Roman

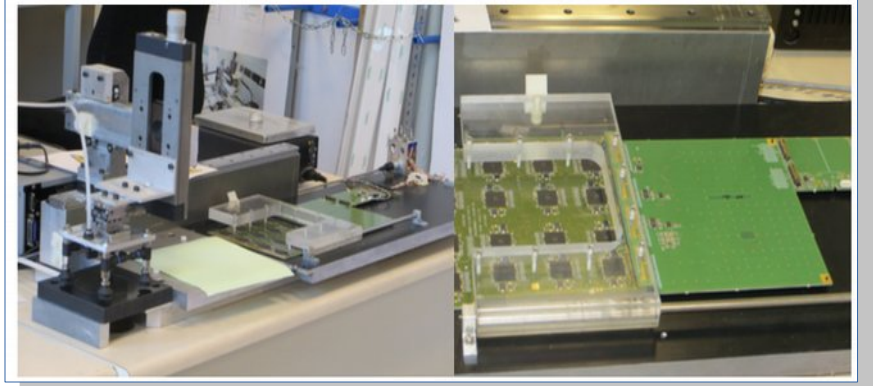
COB adaptations → for June BT

- Gluing of wafer(s) on COB PCB's [@LPNHE]
  - requires the adaptation of the gluing bench
- Testing of boards [@LAL]
  - requires the adaptation of the "versatile bench":
    - for GradConn Connectors



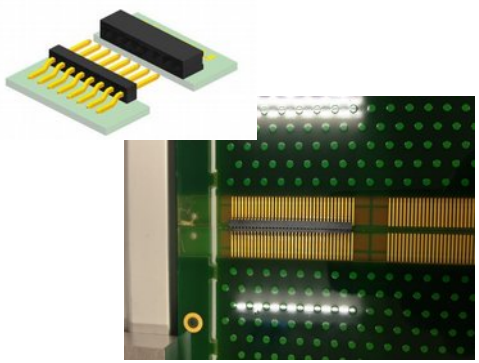
Electrical tests bench

- A dedicated electrical test system is used
  - to control the wafers before gluing
  - to check the short cuts immediately after gluing
  - to measure the I(V) curves of each wafer and all 4 wafers
- sourcemeter Keithley 2450 + LLR Bench

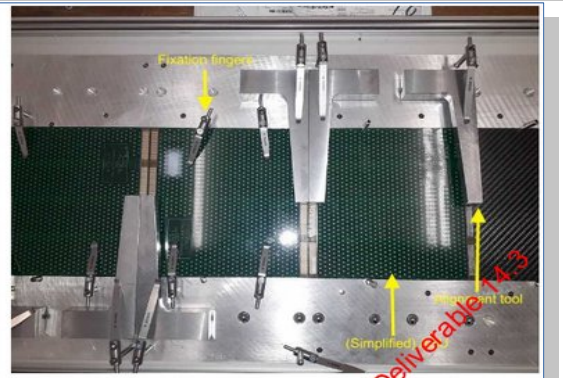


Work on assembly bench

- Check alignment option with connectors (was Kaptons)
- 2 producers:
  - GradConn
  - Antalec (near Orsay)

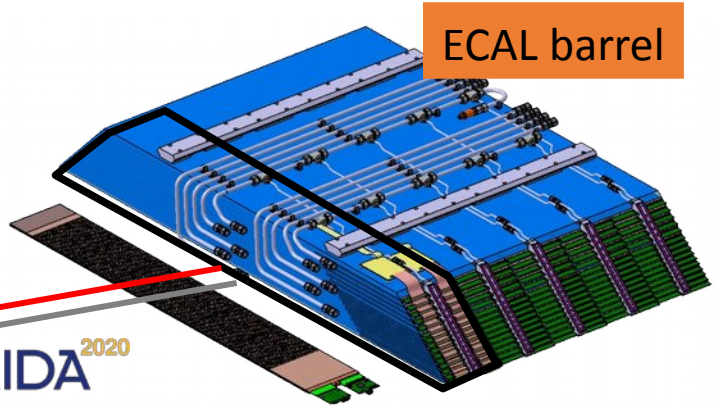


- Gluing on HV Kapton & Soldering of
  - 8 ASU's of 180.3 or 180.5 mm.
  - in U-shape carbon-fibre cradle *or* on simple carbon plate. (181.4 ± 0.3 mm)
- Alignment of two ASU wrt each other :±0.1 mm, Straightness deviation of 0.1 mm.
- In test phase with simplified ASU's
- using pick-and-place manipulator

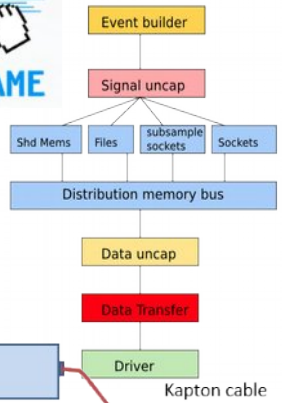


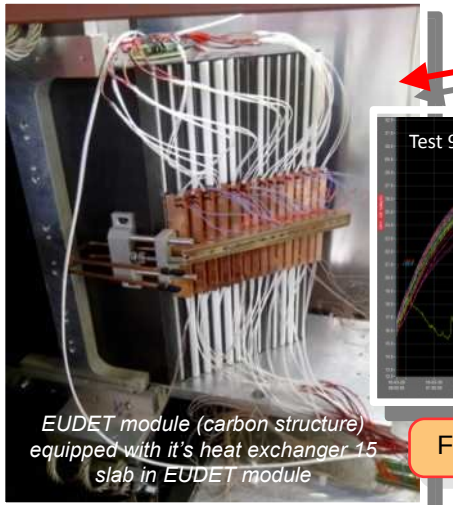
Improve testing procedures

Rails, Cables & Pipes (Services)



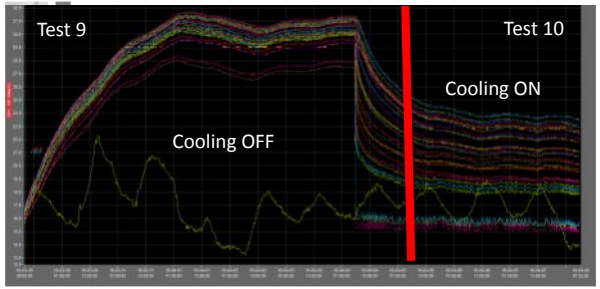
DAQ





EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module

AIDA 2020



First tests results in line with simulations

Side view

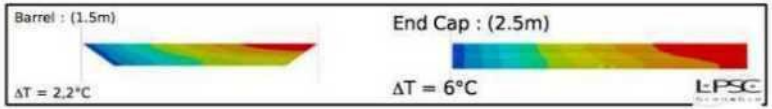
HDMI from CCC

Kapton cable Rigid+Flexible

Existing CORE MOTHER

SL-Board

Jimmy

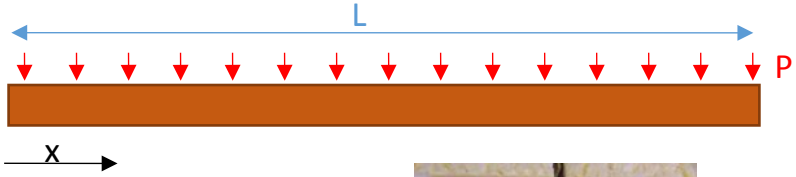


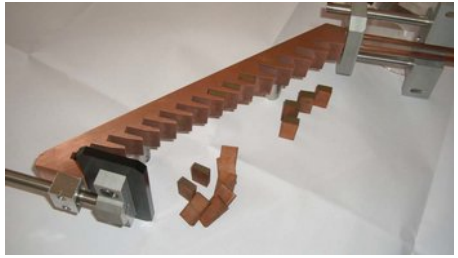
on going...

Active cooling

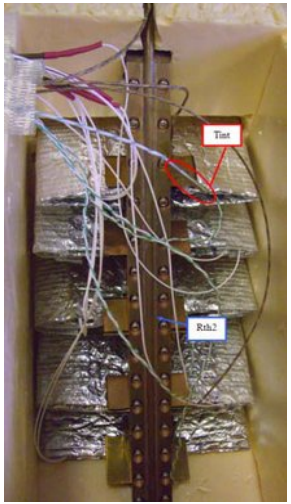
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

Passive cooling



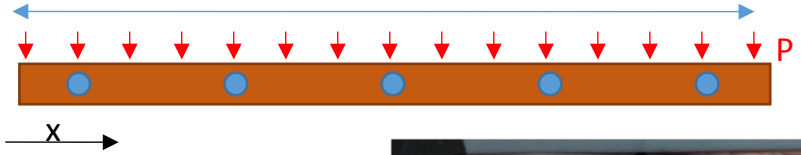


Passive cooling ramp example



Passive cooling ramp set up test

Active cooling

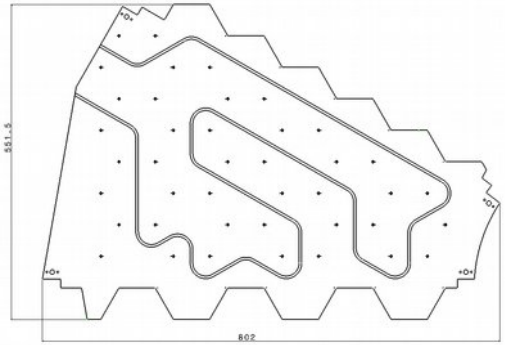


Active cooling set up test with water at room temperature

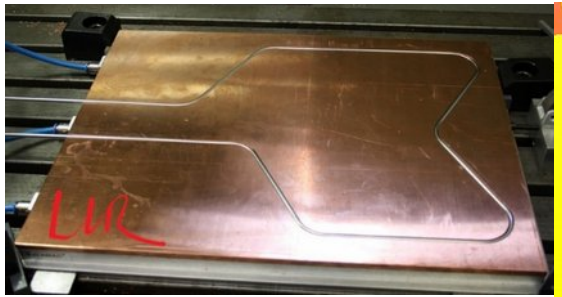
Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,8OD pipes embedded)

Active cooling

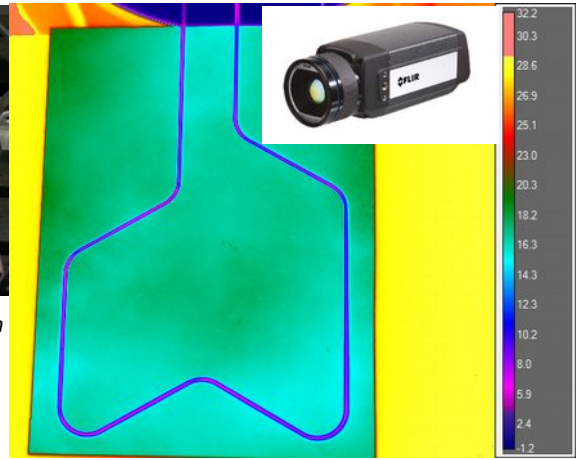
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

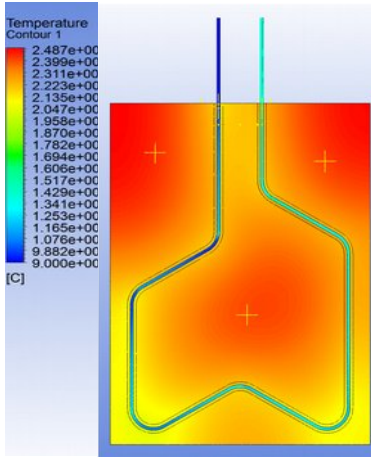


Copper plate prototype dimensions information



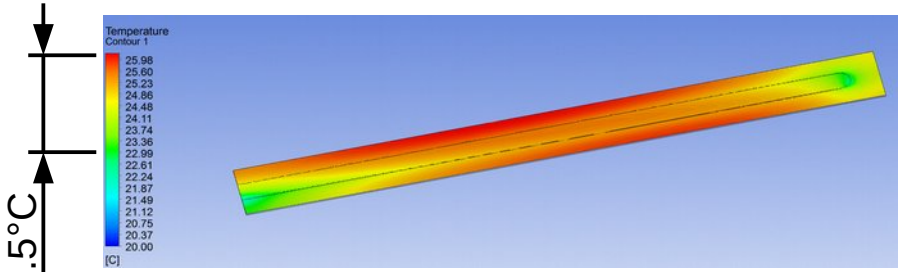
Pipe insertion on a cooling prototype for FEA correlation





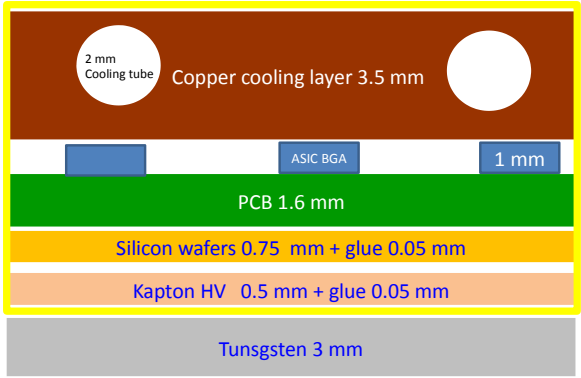
Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling



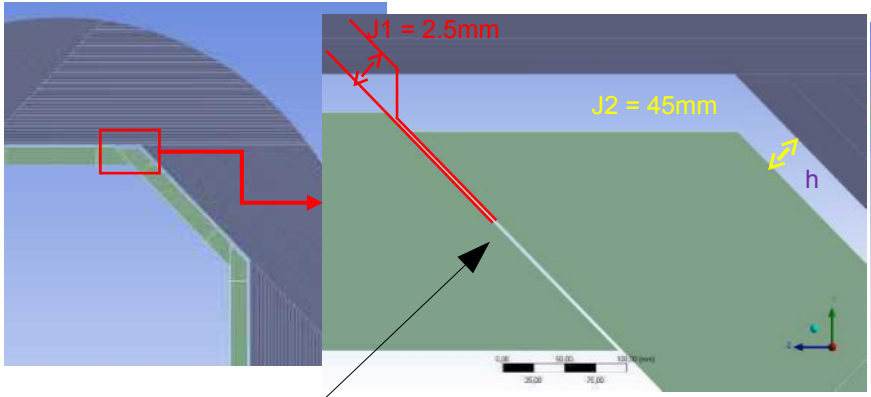
$\Delta T = 2.5°C$

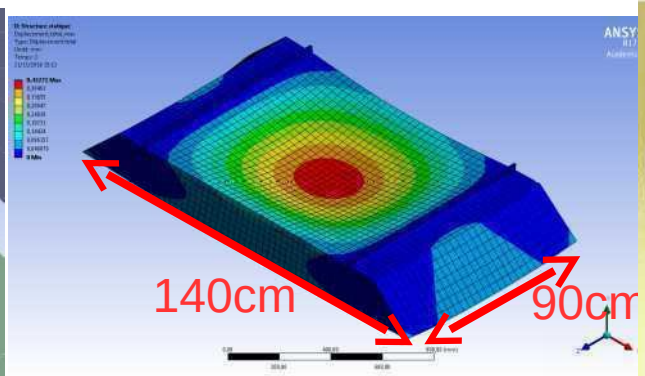
Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

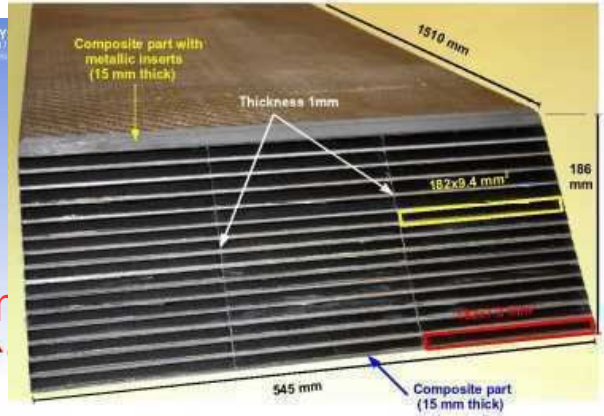


⇒ 9 mm / layer

CFRP+W Structures



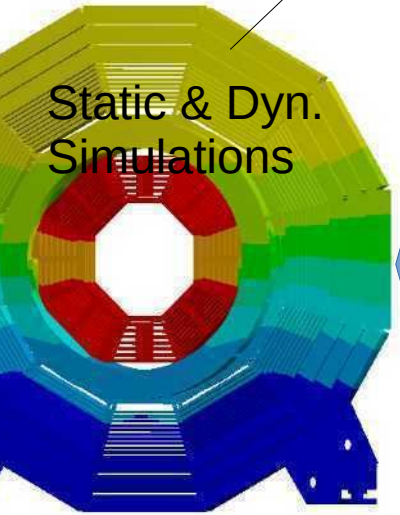




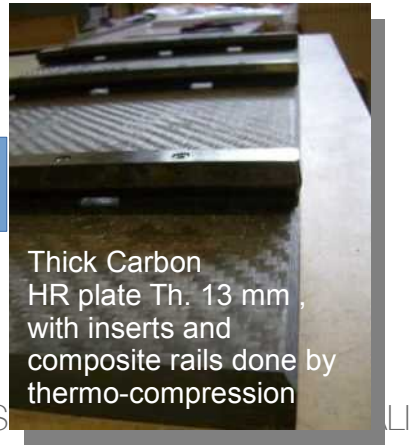
J1 = clearance between modules for the ECAL

J2 = Clearance at ECAL edges between ECAL and HCAL

h = height of the rails 30mm

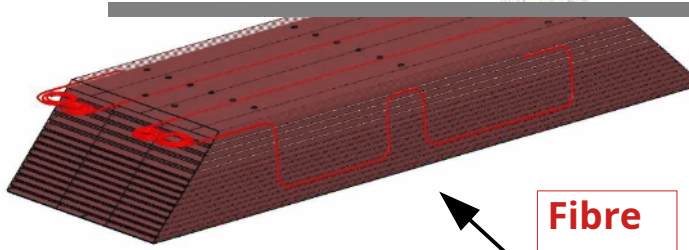


Static & Dyn. Simulations

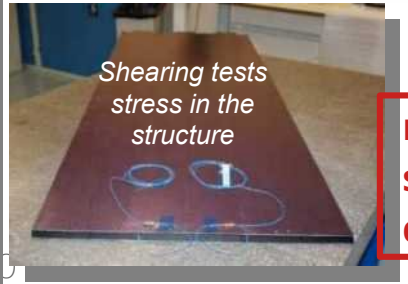


Thick Carbon HR plate Th. 13 mm , with inserts and composite rails done by thermo-compression

Moulding of one layer of 3 alveoli
L = 2.490 m wall thick. = 0.5mm



Fibre Bragg-Grated



Shearing tests stress in the structure

measurements still to be done…

Publications

DESY-2017 Beam Test

7 SLAB's FEV11 ⊃ 325 µm Wafers

"Commissioning paper"

Editor: **Adrián Irles**

- submitted NIM + 2 ArXiv for openness:
  - short (~NIM) + long (arxiv only)
- Limited to «low energy» response: mip and noises
- Submitted to NIM (Jan. 2019):
  - Rebuttal from 2nd referee:
    - understood as already submitted to JINST (due to format of long arxiv paper and conf. paper).
    - ~clarified: goes through corrections → June
  - Both ref for shower data as well
    - to be discussed

Beam test performance of the highly granular SiW-ECAL technological prototype for the ILC.

K. Kawagoe[a], Y. Miura[a], I. Sekiya[a], T. Suehara[a], T. Yoshioka[a], S. Bilokin[b,*], J. Bonis[b], P. Cornebise[b], A. Gallas[b], A. Irles[b,**], R. Pöschl[b], F. Richard[b], A. Thiebault[b], D. Zerwas[b], M. Anduze[c], V. Balagura[c], V. Boudry[c], J-C. Brient[c], E. Edy[c], G. Fayolle[c], M. Frotin[c], F. Gastaldi[c], R. Guillaumat[c], A. Lobanov[c], M. Louzir[c], F. Magniette[c], J. Nanni[c], M. Rubio-Roy[c,*], K. Shpak[c], H. Videau[c], D. Yu[c,d], S. Callier[e], F. Dulucq[e], Ch. de la Taille[e], N. Seguin-Moreau[e], J.E. Augustin[f], R. Cornat[f], J. David[f], P. Ghislain[f], D. Lacour[f], L. Lavergne[f,*], J.M. Parraud[f], J. S. Chai[g], D. Jeans[h]

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Abstract

The technological prototype of the CALICE highly granular silicon-tungsten electromagnetic calorimeter (SiW-ECAL) tested in beam at DESY in 2017. In this test the setup comprised seven layers of 1024 channels and a size of 18×18 cm^2 each. This article presents key performance results in terms of signal over noise ratios at different levels of the readout chain and a study of the uniformity of the detector response.

Keywords: Calorimeter methods, calorimeters, Si and pad detectors

arxiv.org/abs/1902.00110

Conclusions & perspectives

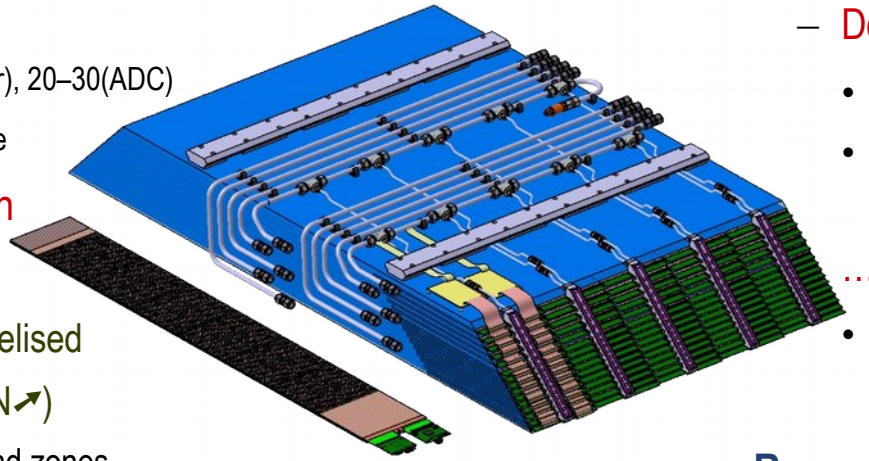
Technical Milestones:

At hand on CALICE prototype:

- Workable, scalable design
- Reduced GR event rates
- ASU with 1024 channel
  - » Signal/Noise > 10 (trigger), 20–30(ADC)
  - » on-going: HE e- response

On-going on ILD-like design

- Connection over 8 ASU's
- Mechanics & Cooling modelised
- Thicker & larger wafer (S/N↗)
  - – red. number of layers, dead zones
- Compact DAQ



Next steps

- – Final chips (SK3-like): full 0-suppr …
  - machine dependant (duty cycle, timing)
- – Industrial aspects (components, aging, …)
- – Double Layered Long Slab Prototype
  - Design with larger wafers
  - Demonstrator for industry
    - – Estimated cost ~160k€ / piece

… Build a module-0 …

- ~13 DL-Long Slabs × 3–5

… build a SIW-ECAL.

Ressources

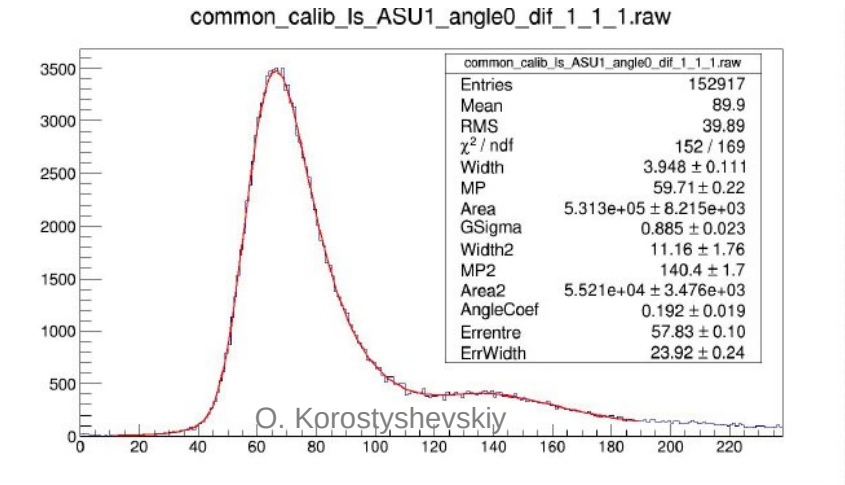
… political dependant …

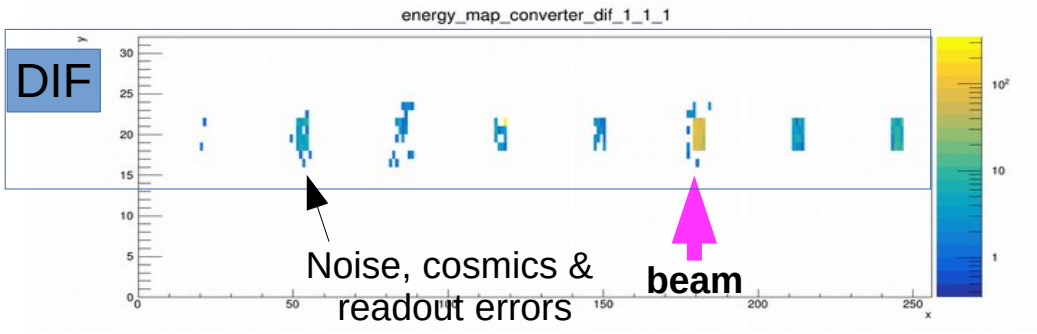
Lessons from e-Long SLAB

Electric “long slab”

2 weeks beg of July: full test of all prototypes:

- Electric long slab: **8** FEV12 + baby-wafers (320µm 2×2cm²):
- RC Filtering of HV between (every second) boards required
- Very clean response to “mip” (punch through e-)



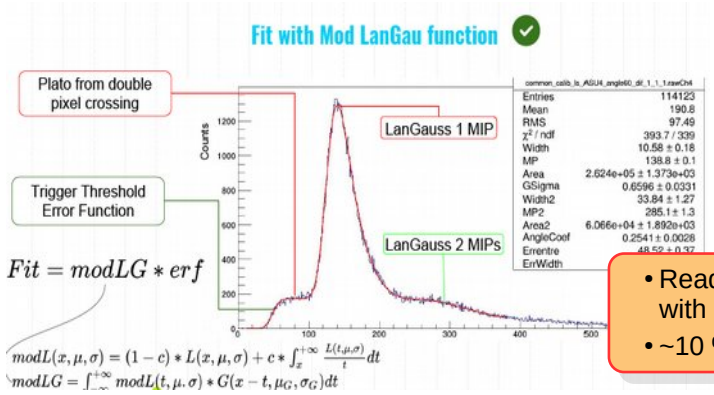


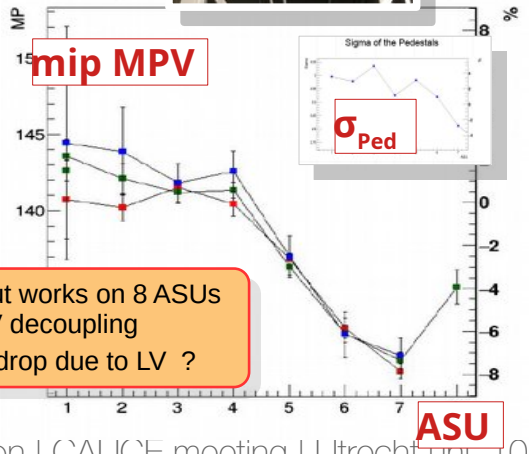
1st ‘electric long slab’ (2018)

Support of interface boards + 12 ASUs (DBD)

- 2+6+4 ASUs = ~3.2 m
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm per ASU
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom



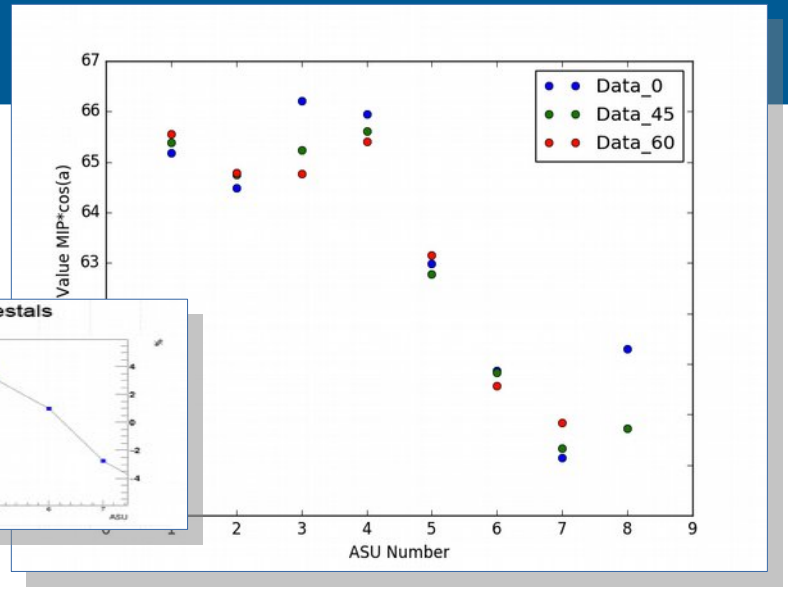


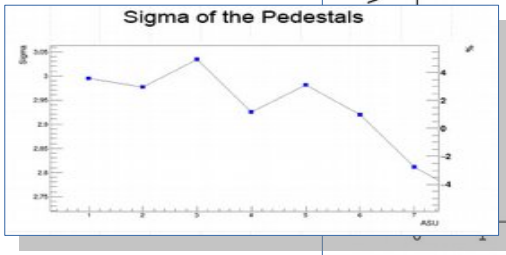
- Readout works on 8 ASUs with HV decoupling
- ~10 % drop due to LV ?

MIP response vs position

mip MPV *cos(θ) vs ASU#

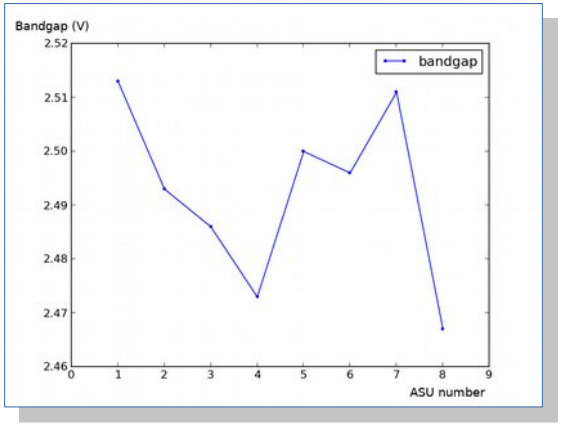
- OK for 4 1st ASU's + Small drop ~of signal ~2%/ASU for ≥ ASU#5
- Also hints similar drop on σ_{ped}

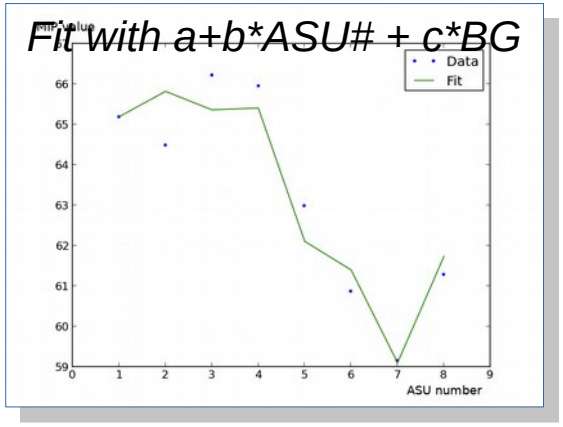




⇒ Voltage or Gain drop ?
Power pulsed mode with ballast et end of slab
or just random build-up effect from chip variability ?

- Answer: Voltage↘ + Band-gap variability
  Data fitted with
  - linear voltage drop (vs distance)
  - BG variability





Presented @ VCI'2019; paper submitted march 2019

⊃ ack't of support from AIDA-2020 and P2IO

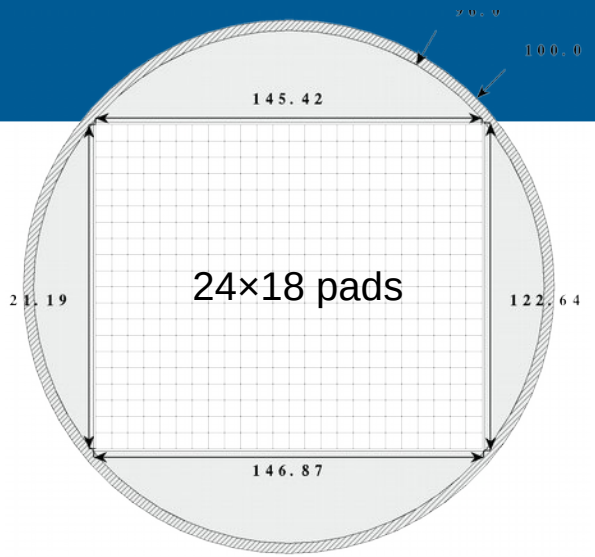
Going to 200mm Wafers…

From CMS HGCAL development & Hamamatsu contacts
future is 200mm (8'') ingots, 725µm thickness

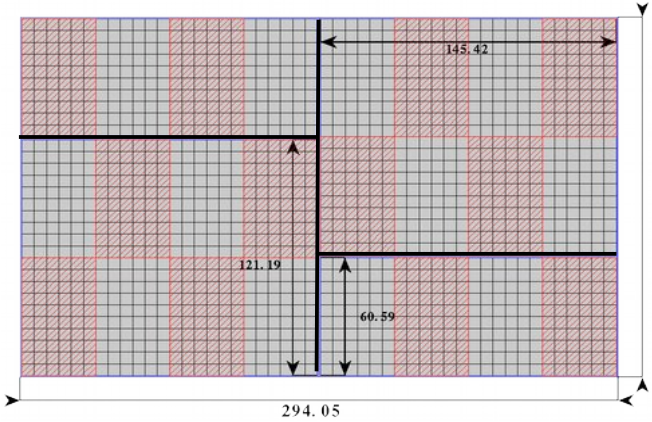
Mechanical constraints → ~187 mm alveoli, ~12 cm wafer

→ 1.5 Wafers ⊗ cell # mult. of 3 ⊗ cell width ~5 mm ⊗ paving with ~64ch ASICs

→ **30** or 36 cells in width



wafers on 200mm ingot ; 63 % use of surface



Optimised ReadOut electronics

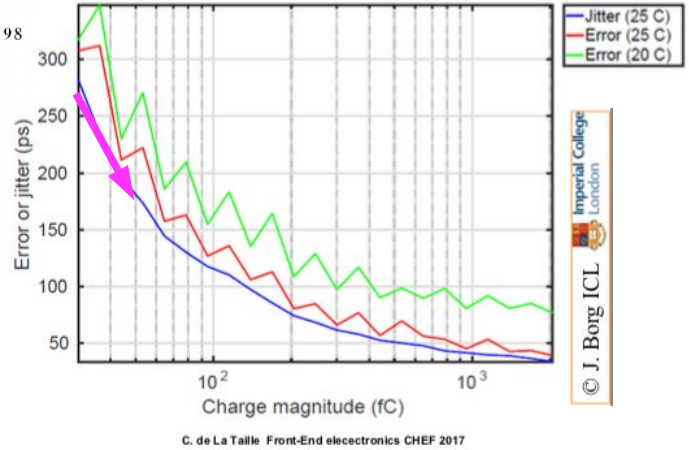
- 6×6mm² , ASICs of 60ch.

  wrt 5×5mm² (⚠ ≠5.5² of prototypes)

  30% less electronics
  consumption
  cost

- ASU: 1440 pads, 24 ASICs

- Noise ~ C ~ width²/th. ~ cst, Signal ~ th ↗, S/N ~ ×1.5; depl. Voltage ~ th² (×2)
  ⇒ Improved timing perf (esp. for mips)



BACK-UP

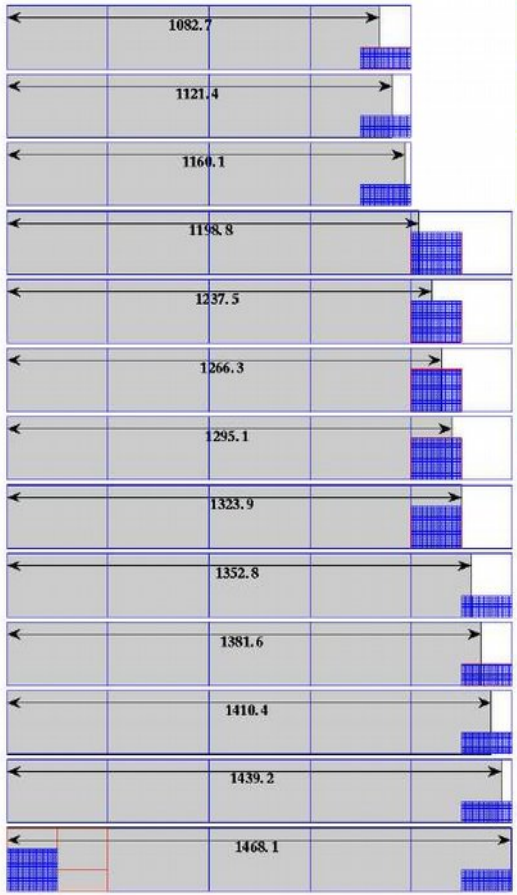
Redefinition of dimensions

- Full costing (hardware and man-power) and integration planning done by Henri Videau
- 3 designs looked at

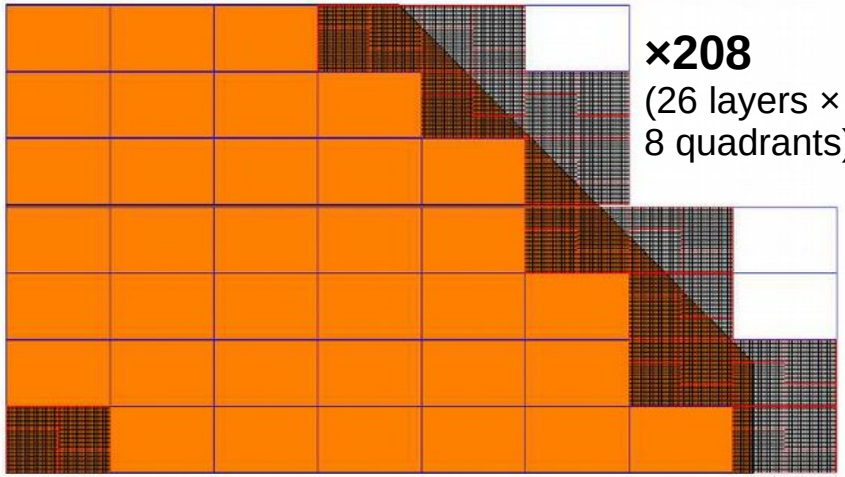
  under work version of **ECal Technical Design Document** (TDD, ~100 pages)
  by Henri Videau (LLR), Marc Anduze (LLR) and Denis Grondin (LPSC)

  – a “baseline” (or “large”) with inner ECal radius at RECal =1804mm, (model close to the DBD) with 30 layers
  – a “small ILD” model RECal ~1500 mm (all related quantities adapted ↔ $R_{outer}^{Endcaps}$)
  – a model with slightly reduced number of layers = 26 layers
- 725µm thickness with 200mm (8”) wafers ; 5.08 → 6mm cell size
  - ~ identical photon resolution expected
  - 13% gain cost on Silicon surface, PCB, and 40% on electronics (and power consumption) wrt DBD
  - Improved S/N ratio & timing, less channeling @ 90°

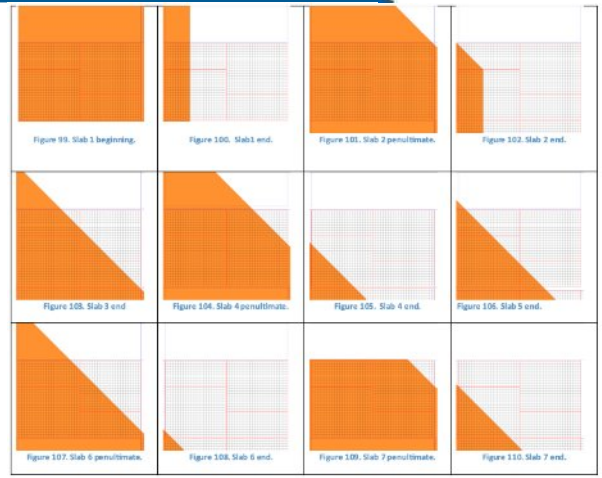
Tiling



×400
(2 sides × 5 columns ×40 modules)

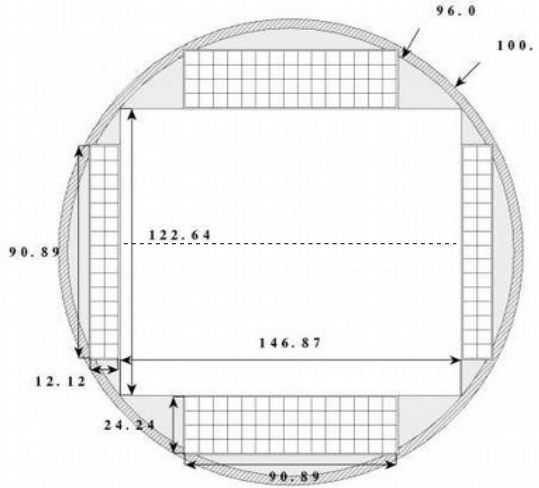


×208
(26 layers × 8 quadrants)



Matching of large and small rectangles, triangles and diamonds to be detailed for optimal use

add'l small rectangles:
87 % use of surface
(83 % for an hexagonal shape)



FEV13

Only a few masked channels!

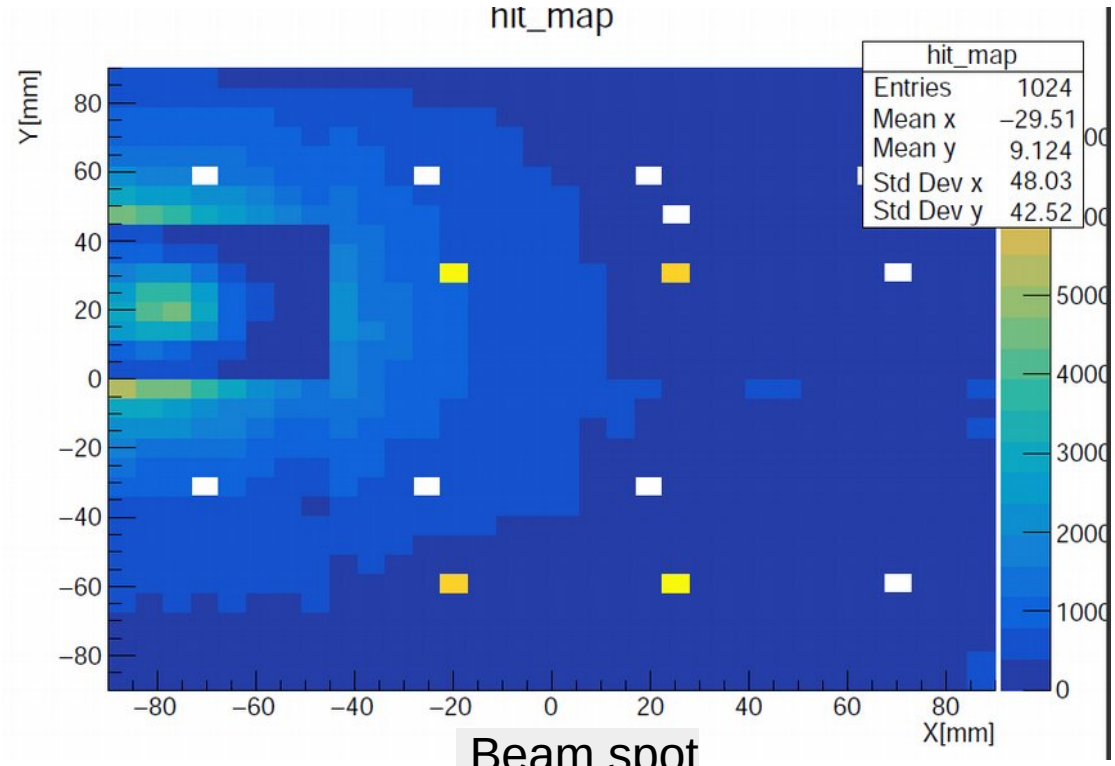
- worked «out of box»

but instabilities after a couple of days

- 4 new layers produced in Kyushu.
  - 3× 650 µm + 1 × 320 µm wafers

improved S/N handling, TDC enabling

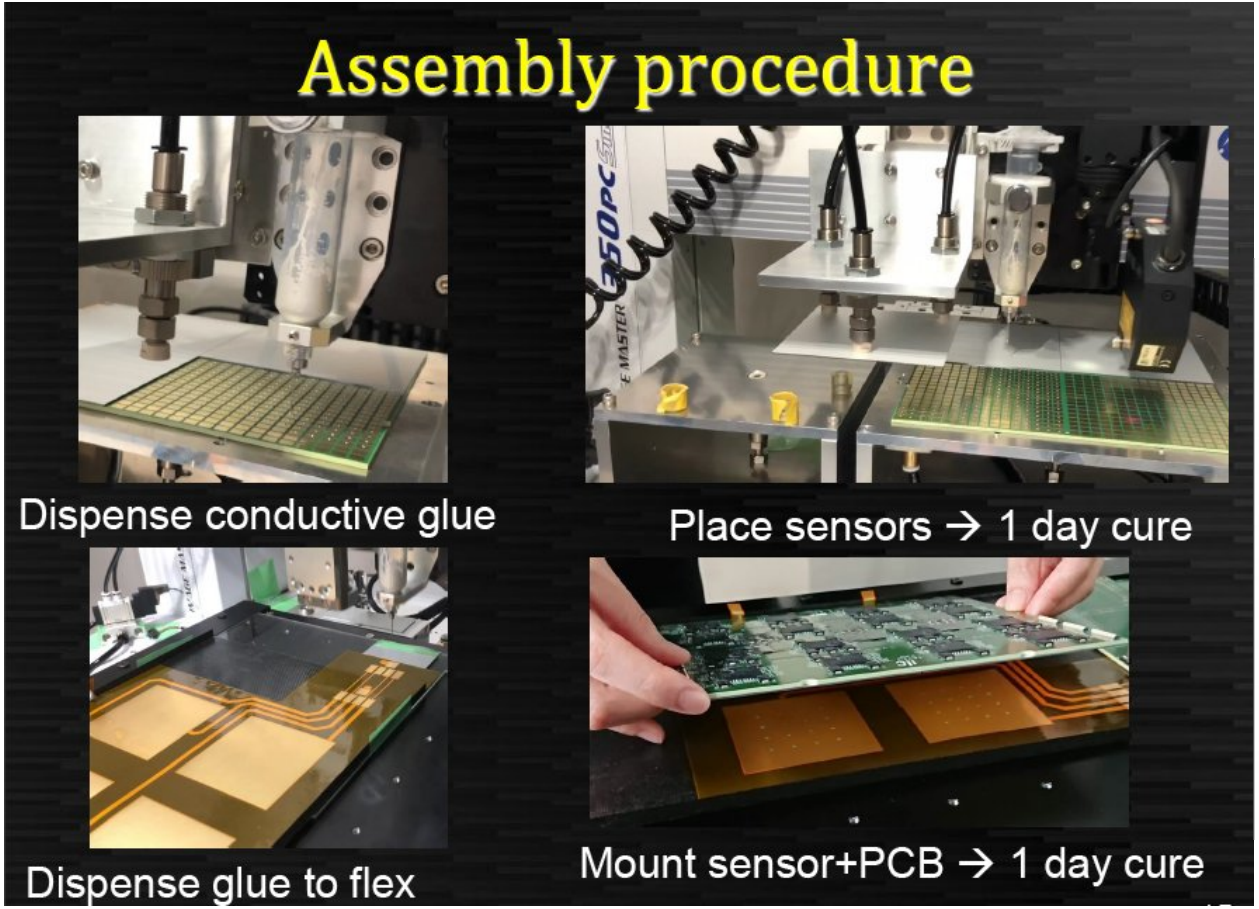
- individual thr adj.
- better noise adjustment → ~ only ch 37 excluded



Beam spot

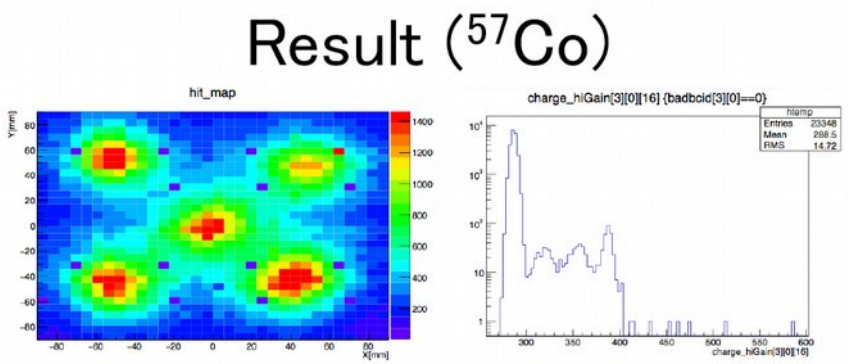
(not corrected to memory fill-up)

FEV13 assembly in Japan



Similar to production in Paris region

(AIDA-2020 benches)

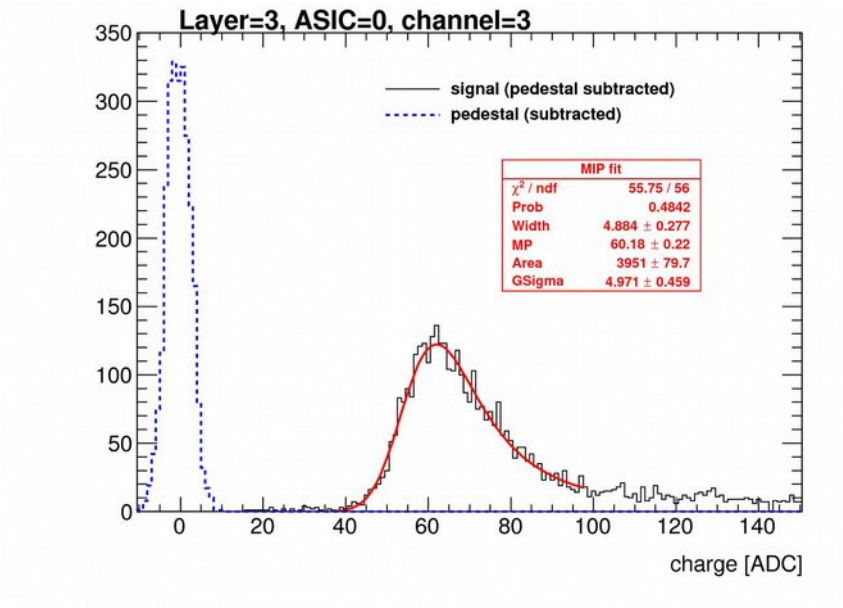


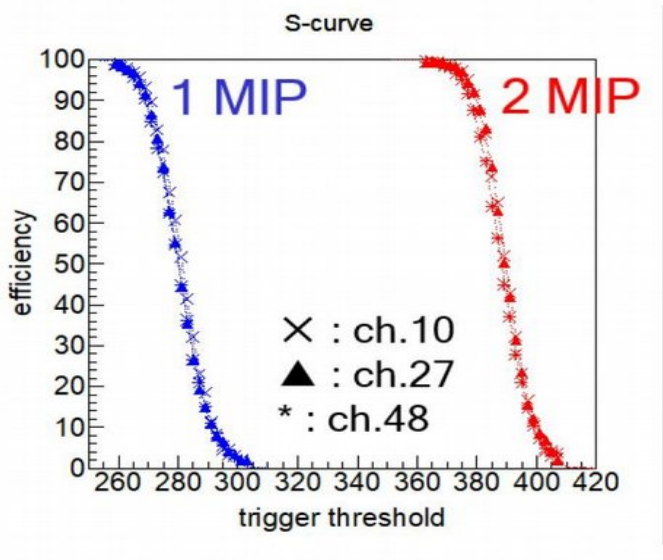
- We can get data now !
  But we have to finish to acquire datas in 4 times, because we have to test 5 SLABs. We already finished only the SLAB.

S/N ratio is about 30.

Improved to 40 in some cases

Stack: S/N on the trigger line from thr. scan





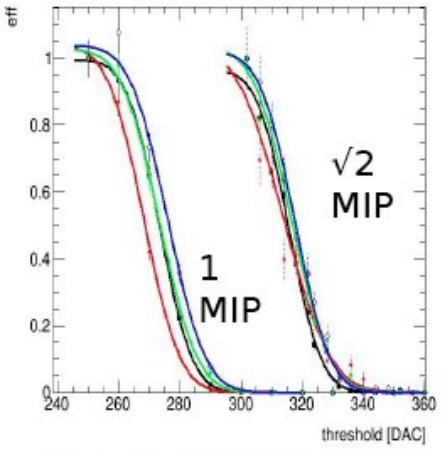
Injected signal → MIP

S/N ~ 20 in ADC branch

S/N ~ 12 in Trigger Branch.
Trigger at 50% mip with 6σ
or 1/3 mip with 4σ

S/N in the trigger line

- For autotrigger data taking, a S/N is to be defined by the study of the trigger line (fast shaper in Skiroc) → threshold scans with different signals
  - The threshold scan curve is interpreted as the integral of the gaussian distribution of the noise.

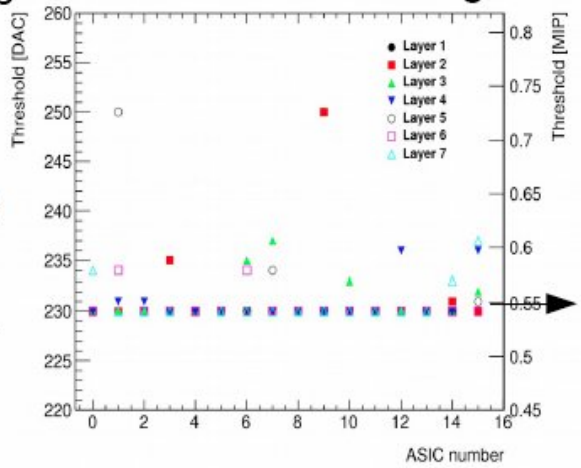


Slab 17, 18, 19, 20
(FEV11)

These curves
are used
for trigger calibration

and S/N
calculation

Trigger thresholds used in DESY@2017&2018



230DAC
≈ 5σ
distance
of the MIP

S/N = 11.6 ± 0.7 (ILD baseline requirements: S/N=10)

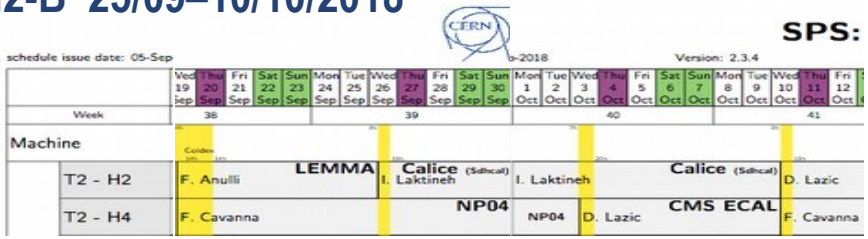
Trigger threshold at ~0.5 MIP

First S/N (trigger) measurements in beam test.

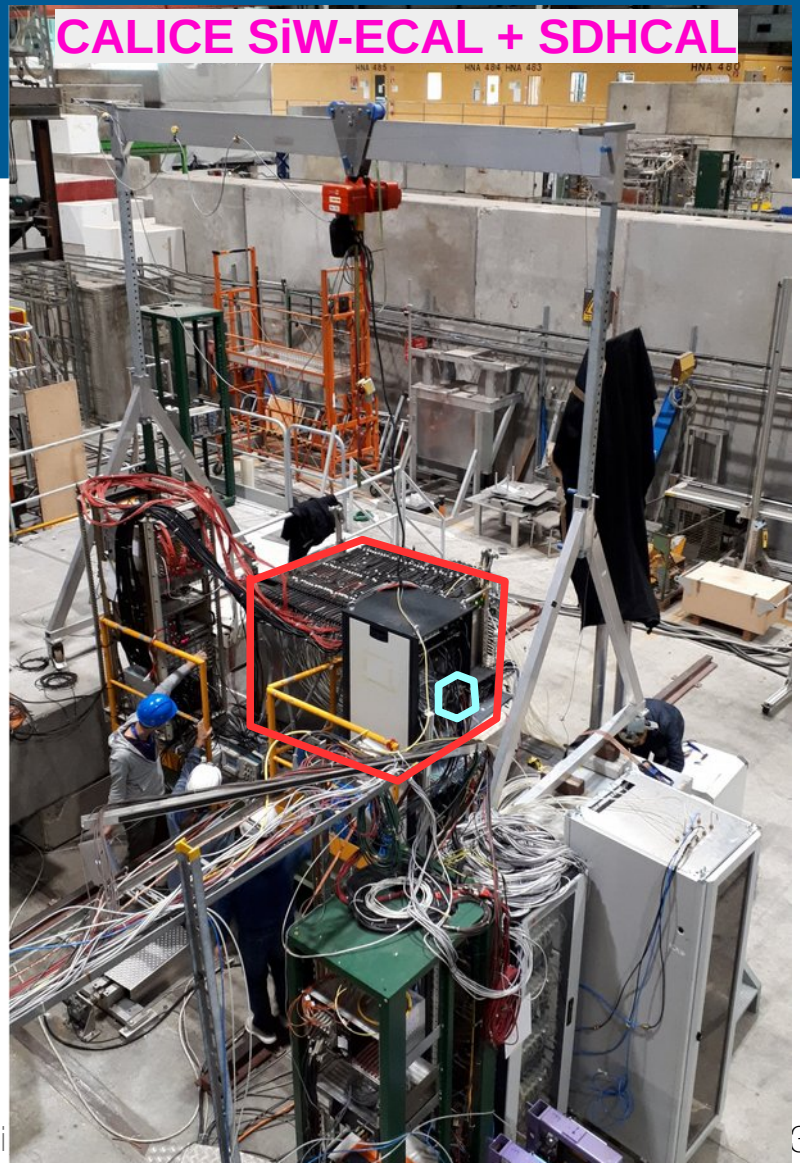
© A. Irles, at P2IO day

Combined BT at CERN 2018

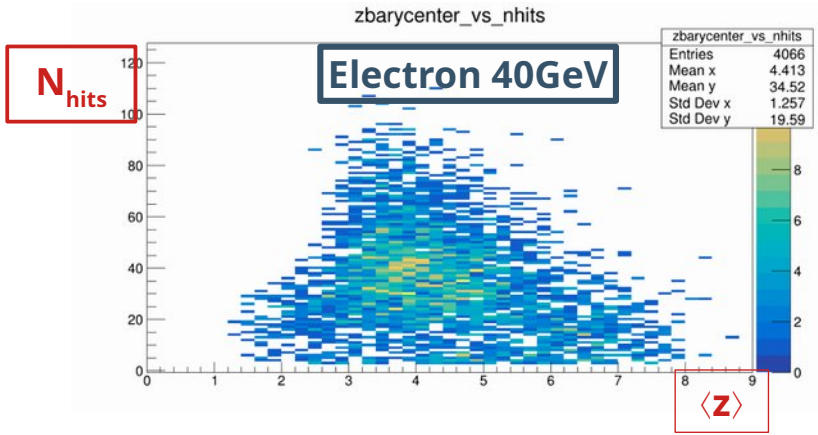
2 weeks on H2-B 25/09–10/10/2018

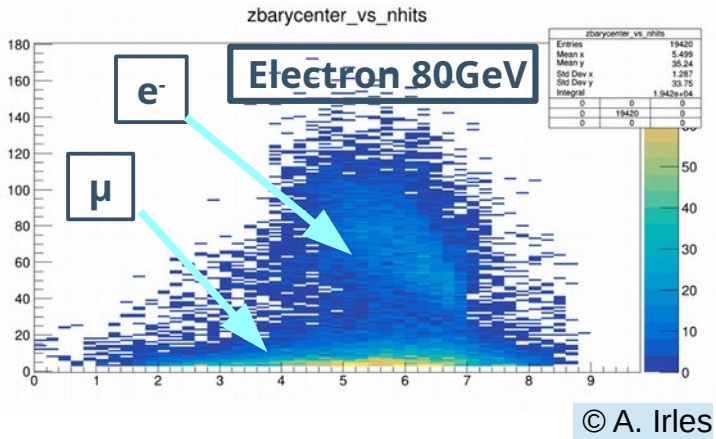


- 37 layers of SDHCAL RPC, 5MHz clock
- 10 layer of SiW-ECAL : 6 FEV11 and 4 FEV13.
  - 2.5 MHz (all FEV11 but 1) and 5.0 MHz (FEV13+1FEV11)
  - many issues with FEV13:
    - partial commissioning at LLR bef. BT
    - insecure transport (in plane) → repair on-site, esp. HV connections
  - 1 FEV13 has been working reliably



Standalone runs





Muons and electrons run

- low contamination, except @ High E.
- shower analysis still to be done (also for DESY tests)

These are the statistics for electron data. Obtained from the zbarycenter vs nhits plots.

energy	total events	electrons shower like events
10 GeV	630	~630 (very low contamination)
20 GeV	4060	~3480
40 GeV	2023	~1800
80 GeV	19420	~8000
150 GeV	8474	~1000

CERN-2018 Combined runs

Required some work on DAQ:

- HW and SW synchronisation
- Solution of CERN-2016 + 40 MHz clock on both
- first combined test this week (since 2016) but very limited manpower availability
  - shared Spills (and event number), separate clocks

Reconstruction:

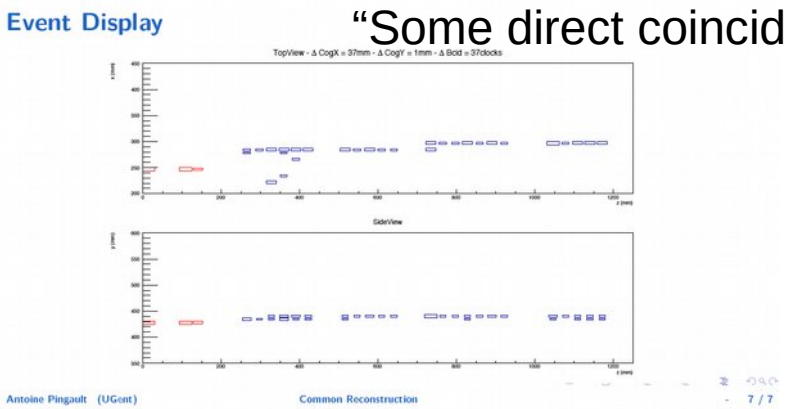
- Data:
  - ECAL = #sp, #bx_e
  - SDHCAL = cc (absolute bx@sp_start), #sp, #bx_h
- Procedure (to be done)
  - 1. Extract cc form SDHCAL event
  - 2. rec. times in ECAL and HCAL
    - time_in_sp = cc + f_freq * #bx_i + Δs
  - 3. check linarities (Δf + Δsyst.)
  - 4. rec. ECAL + HCAL

1st common meet 18/12/18

- Selection: nslabs_with_hit≥3
- Plot for PiPlus_50GeV (offset from e-log)

VERY PRELIMINARY

Common runs (selection = nslabs with hit >3)		
run	events (offsets elog)	events (offsets twiki)
PiPlus_40GeV	28299	not calculated
PiPlus_50GeV	3241	not calculated
PiPlus_60GeV	2365	not calculated
PiPlus_70GeV	12727	not calculated
PiPlus_80GeV	5484	not calculated
Muon_200GeV	108729	89506
Electron 150 GeV	not copied to the cern eos	
Standalone last muon ruon	not copied to the cern eos	

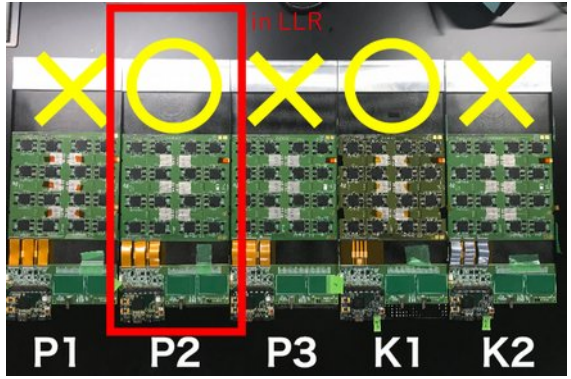


"Some direct coincidences"

Other news

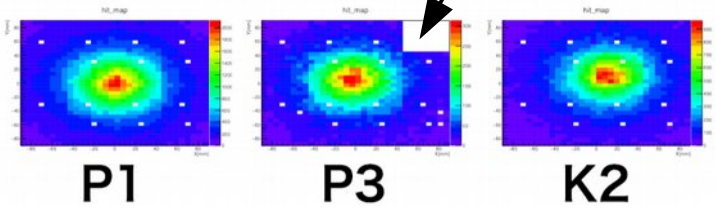
FEV13 with improved mechanics
(FEV13 slab dismounted and repaired in Kyushu)

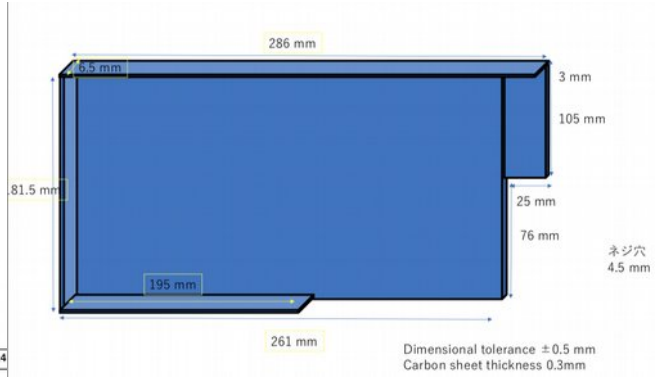
- all HV faults due to repairs



Ba133 source

Noisy chip





2 weeks of BT at DESY in 2019:

- 24/06 – 07/07/2019
  - COB tests
  - FEV13

DESY TEST BEAM.

DESY Test Beam Schedule 2019 - Version 2 15/11/2018

Ralf Diener, Norbert Meyners, Marcel Stanitzki - DESY Test Beam Coordinators

	Week		TB21		TB22		TB24/1		TB24	
				DATURA		DURANTA	PCMAG	Telescope in PCMAG		AGNES
10-Jun-19	24		CLIC PIXEL	X	ATLAS-ITk-Strips	X	T2K			
17-Jun-19	25		TBMST	X	ATLAS-ITk-Strips	X	T2K			
24-Jun-19	26		CMS-Pixel-Phase2	X	AFP-TOF	X	CALICE-SiW-ECAL			
1-Jul-19	27		CMS-Pixel-Phase2	X	Mu3e	X	CALICE-SiW-ECAL			
8-Jul-19	28		GammaMeV	X					CALICE AHCAL	
15-Jul-19	29		CLIC PIXEL	X					CALICE AHCAL	
22-Jul-19	30		X-Ray-Crystal-Rad	X						