# Compact Digital Electronics for SiW Ecal and other applications

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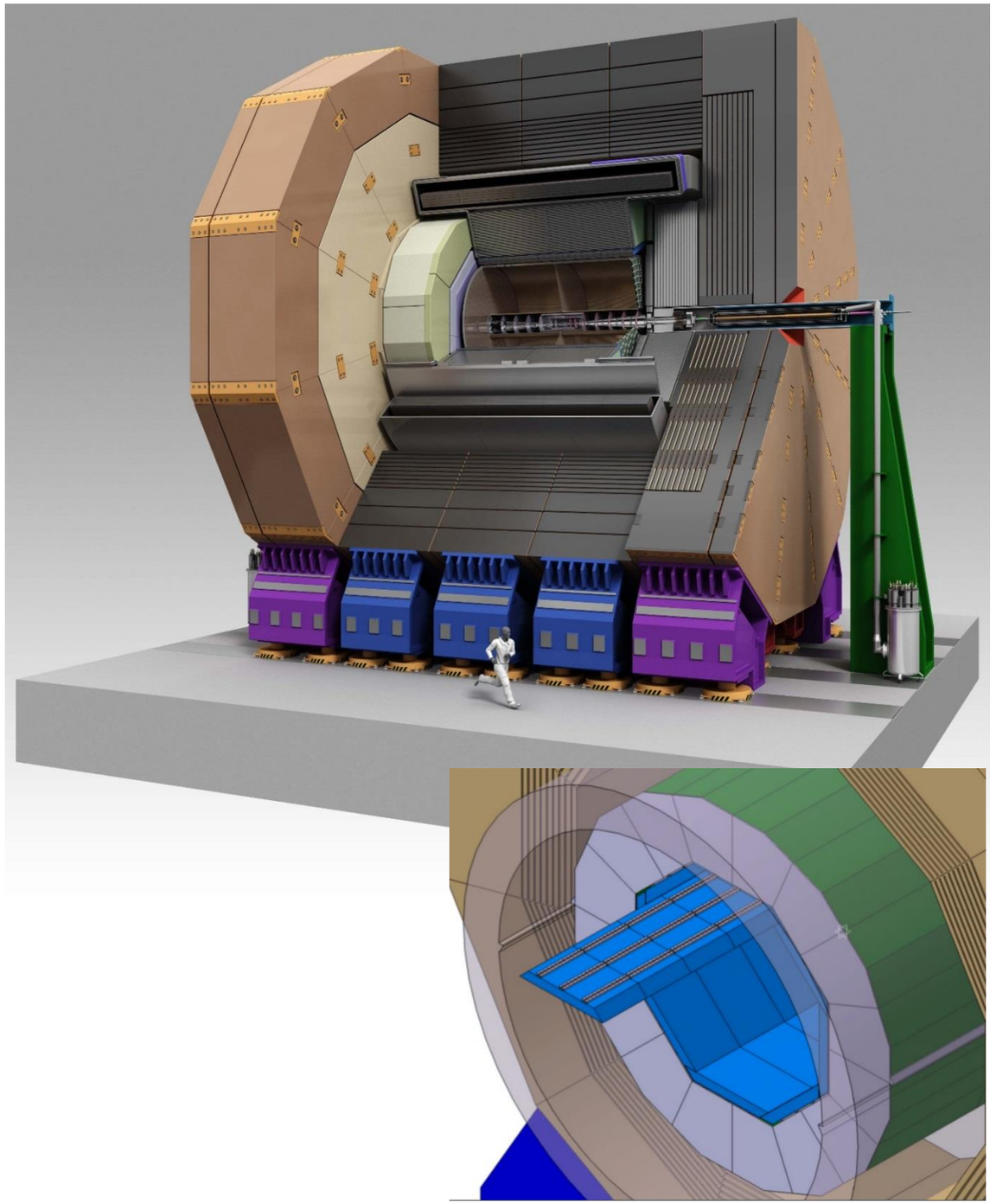
# Introduction

- Latest status of developments proposed by LAL group for a Silicon-Tungsten electromagnetic Calorimeter DAQ in ILD.

- Electronics developments is done by:
D. Breton, J.Maalmi, J.Jeglot.

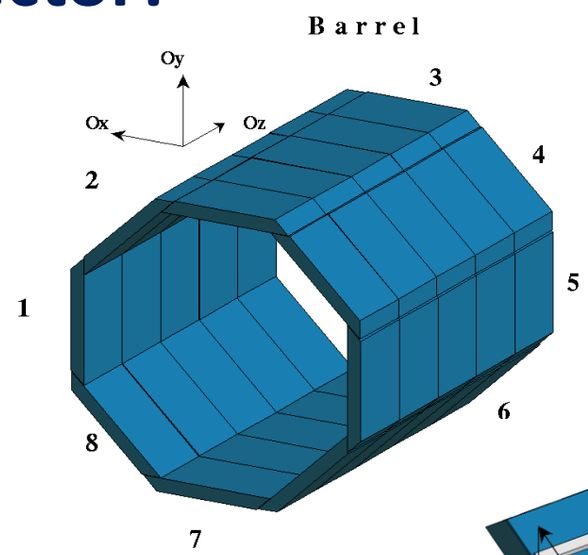
1. Power Pulsing: Proposal to use new ultra-flat super-capacitors on all ASUs of the Slab (order 10 ASUs per slab).

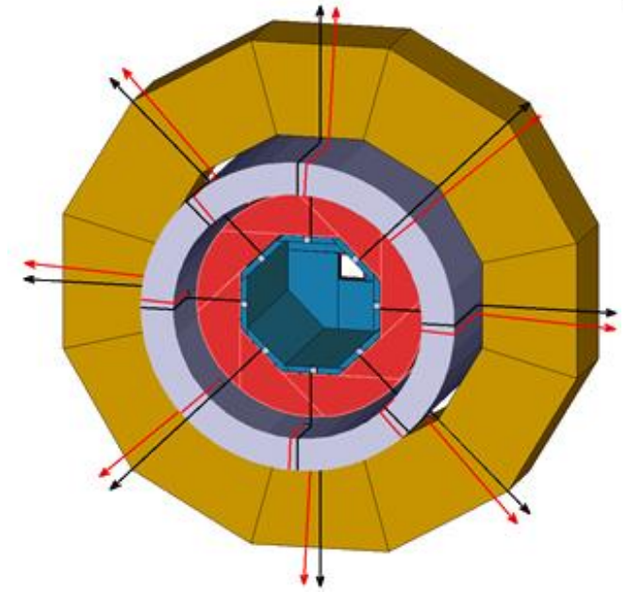
2. Control and Readout Electronics: Proposal for a compact Slab digital interface board and Control & Readout module.

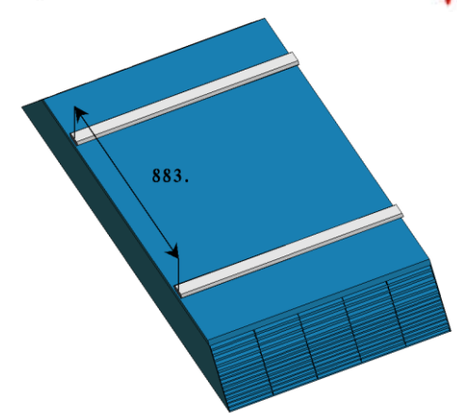


# Ecal Constraints

## The Challenge: a very Compact Detector!

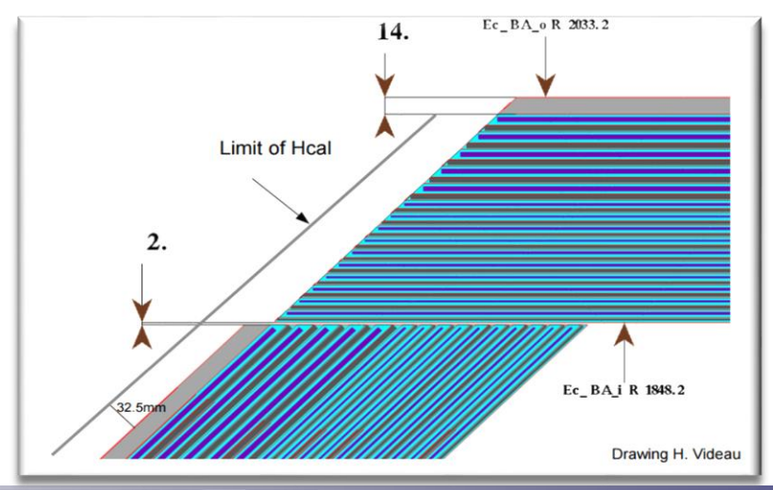





Constraints:

- Spatial constraints:
  - limited space between layers
  - Limited space at the end of a slab
  - Control & Readout electronics at the extremity of the Slab
  - Signal Integrity over the Slab
- Low power consumption: power pulsing
- Thermal uniformity
- Mechanical Assembly process



# Ecal Electronics
# Space Constraints

**Space constraints for the Active Sensor Units (ASUs):**

- Maximum Height for Electronics (including PCB): depends on number of layers (20-30)
  - For prototype: (PCB + components for the **SKIROC-2 BGA option**) : **~ 3mm**

Current ASU Electronic board design:

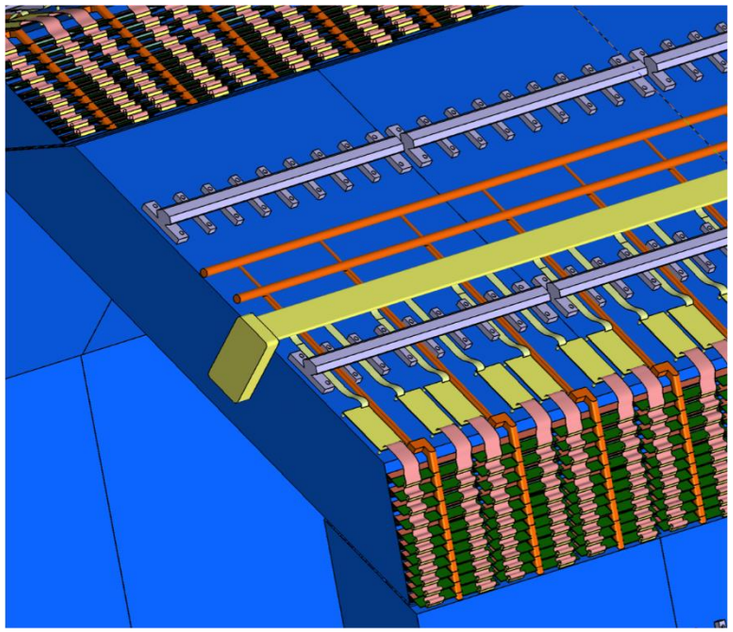
- PCB thickness (FEV 12): 1.6 mm
- SKIROC BGA height: 1.4 mm

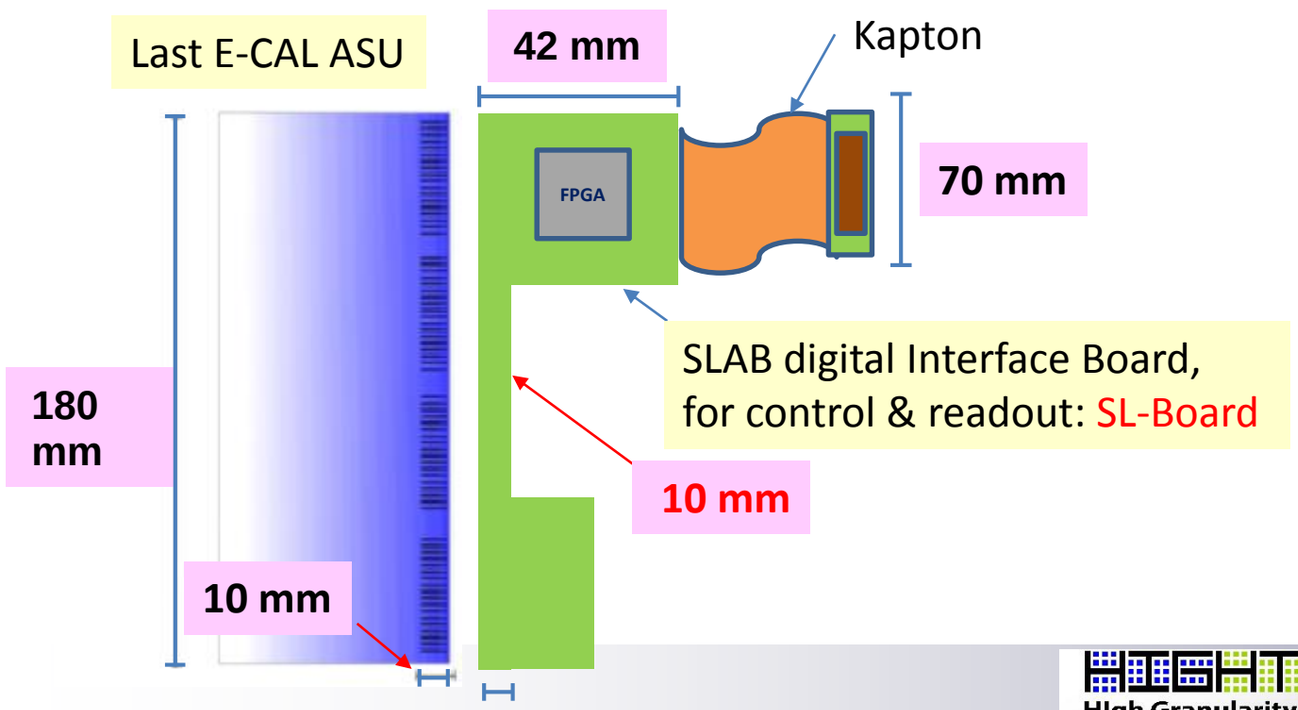
- ASU Chip on Board (total): 1,2 mm

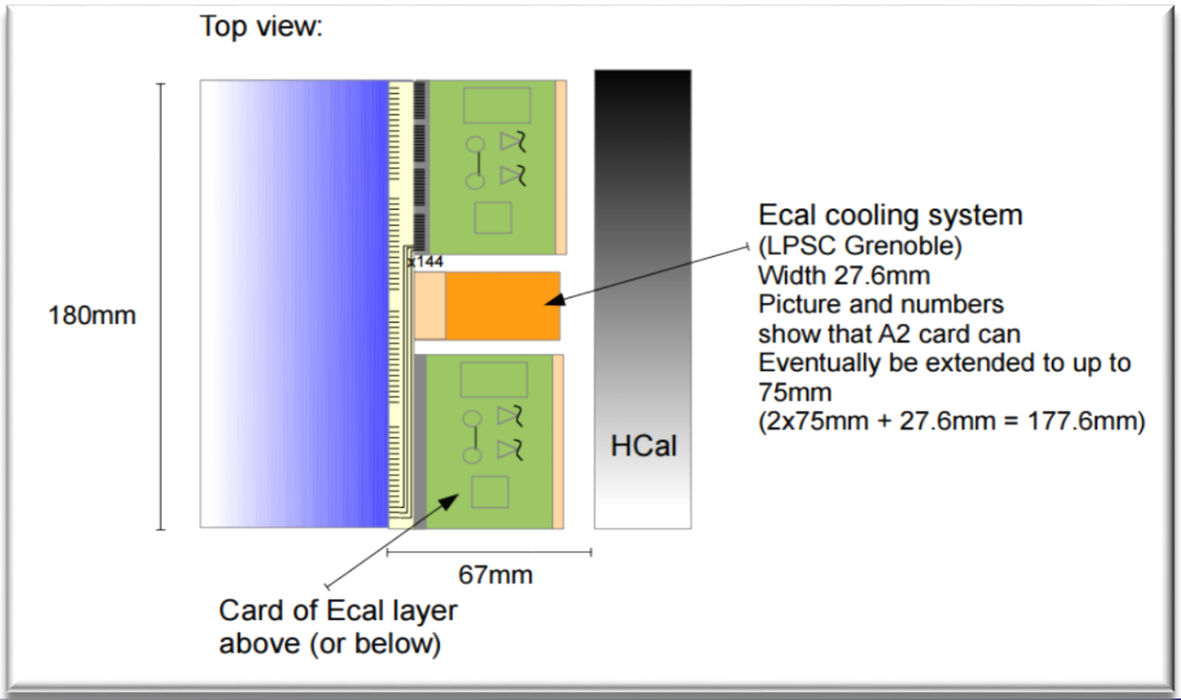
**Space constraints for the Slab Interface Board ( SL-Board):**

- L-shape (even and odd ASUs) Dimensions: see below.
- Maximum Height: **~ 12 mm**

E-CAL Services

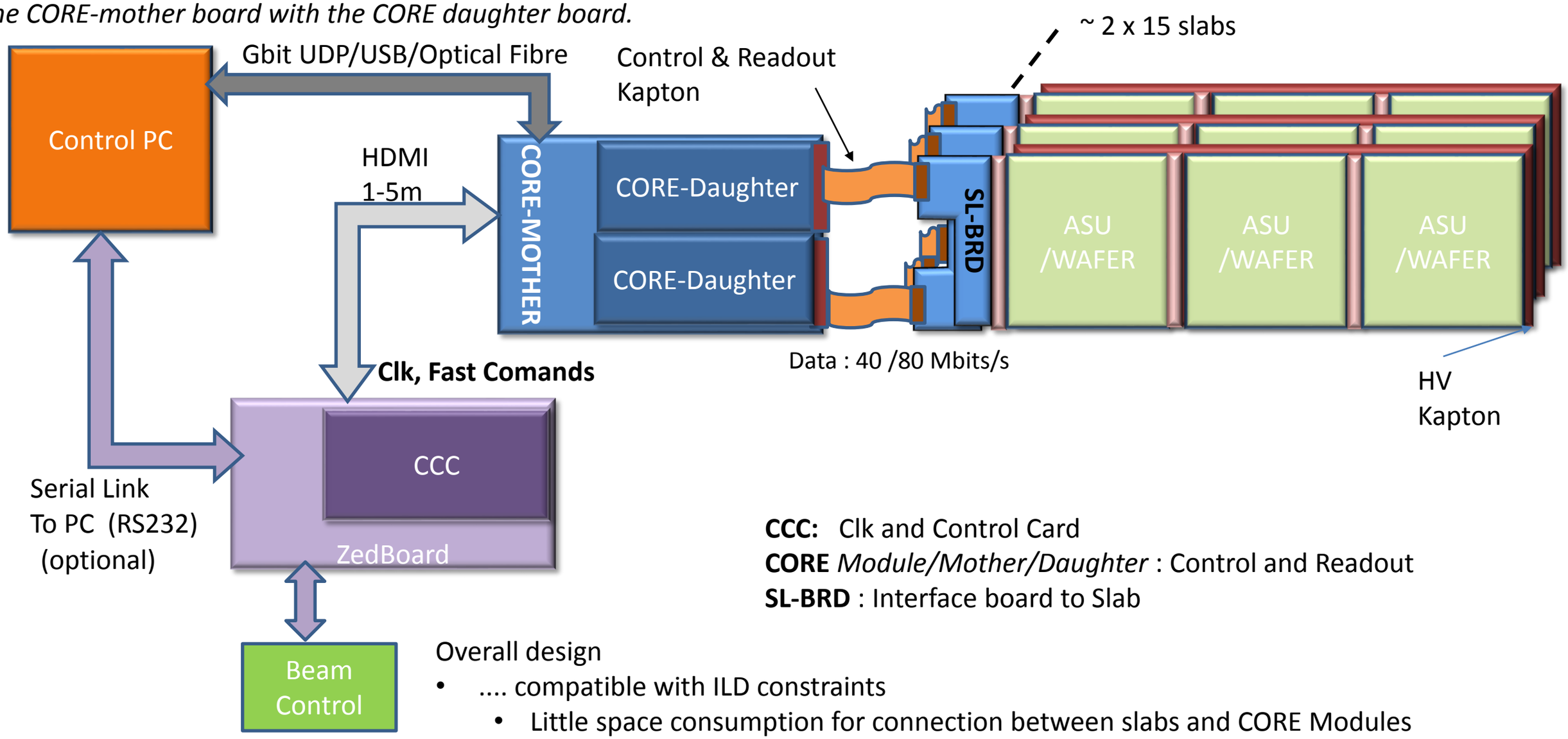




# Global Architecture Scheme

*DIF system for the SiW ECAL is shown with the SL-board, CORE Kapton and the CORE Module consisting of the CORE-mother board with the CORE daughter board.*



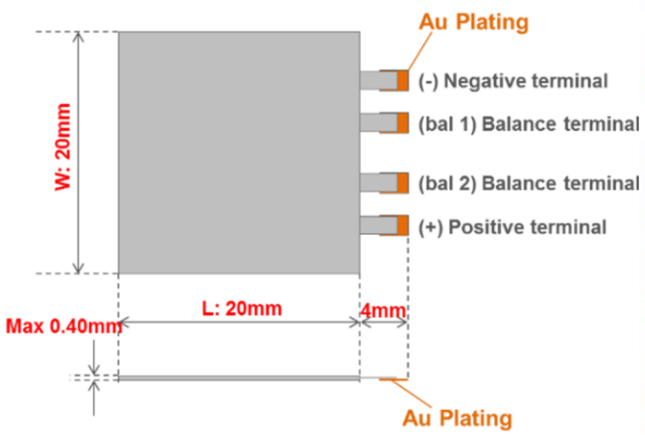

**CCC:** Clk and Control Card
**CORE** *Module/Mother/Daughter* : Control and Readout
**SL-BRD** : Interface board to Slab

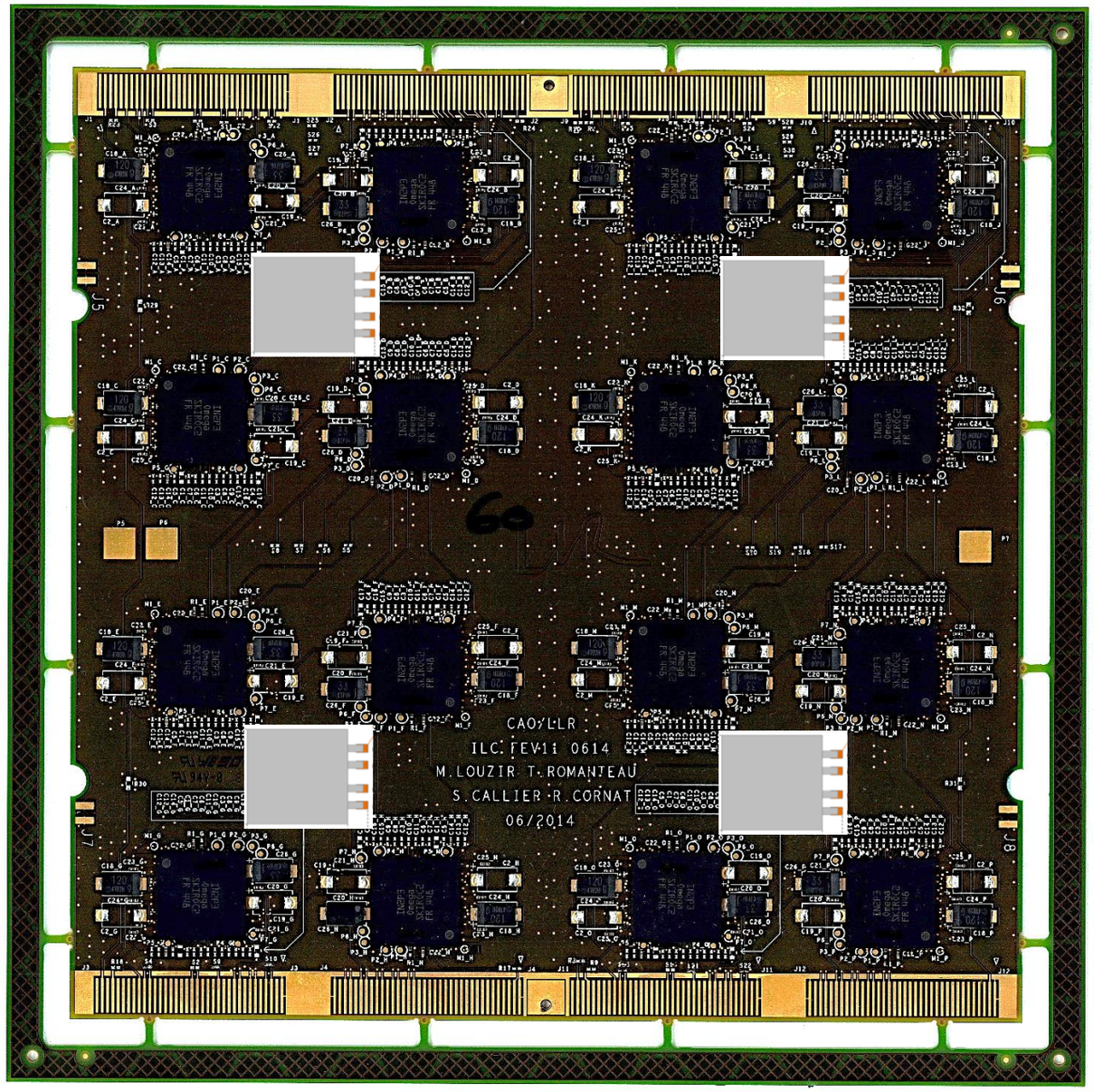
Overall design

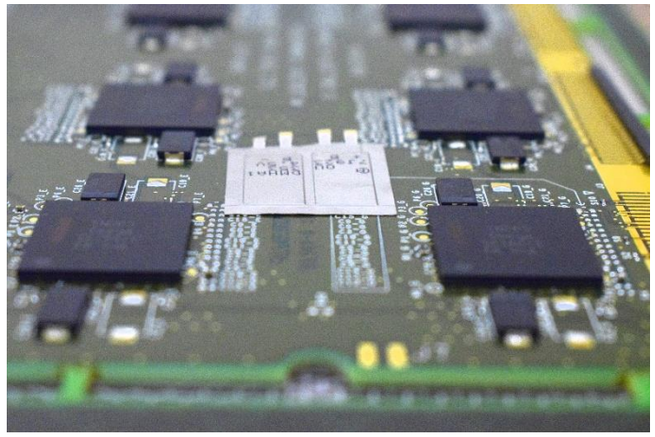
- .... compatible with ILD constraints
  - Little space consumption for connection between slabs and CORE Modules
  - CORE Mother can be placed at the forefront of barrel, Daughter between Ecal and Hcal
- ... assures compatibility with other AIDA2020 developments
  => Paves way for combined beam tests (other calos, trackers etc.)
- SL-Board is delivery for AIDA2020 and P2IO/HIGHTEC

# Ultra-flat Capacitors

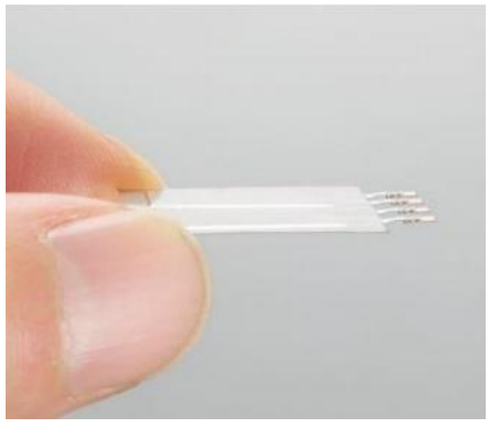

Ultra-Thin Supercapacitor
DMH series
DMHA14R5V353M4ATA0
35 mF / 4.5 V



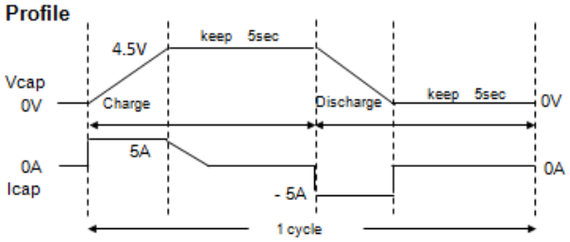



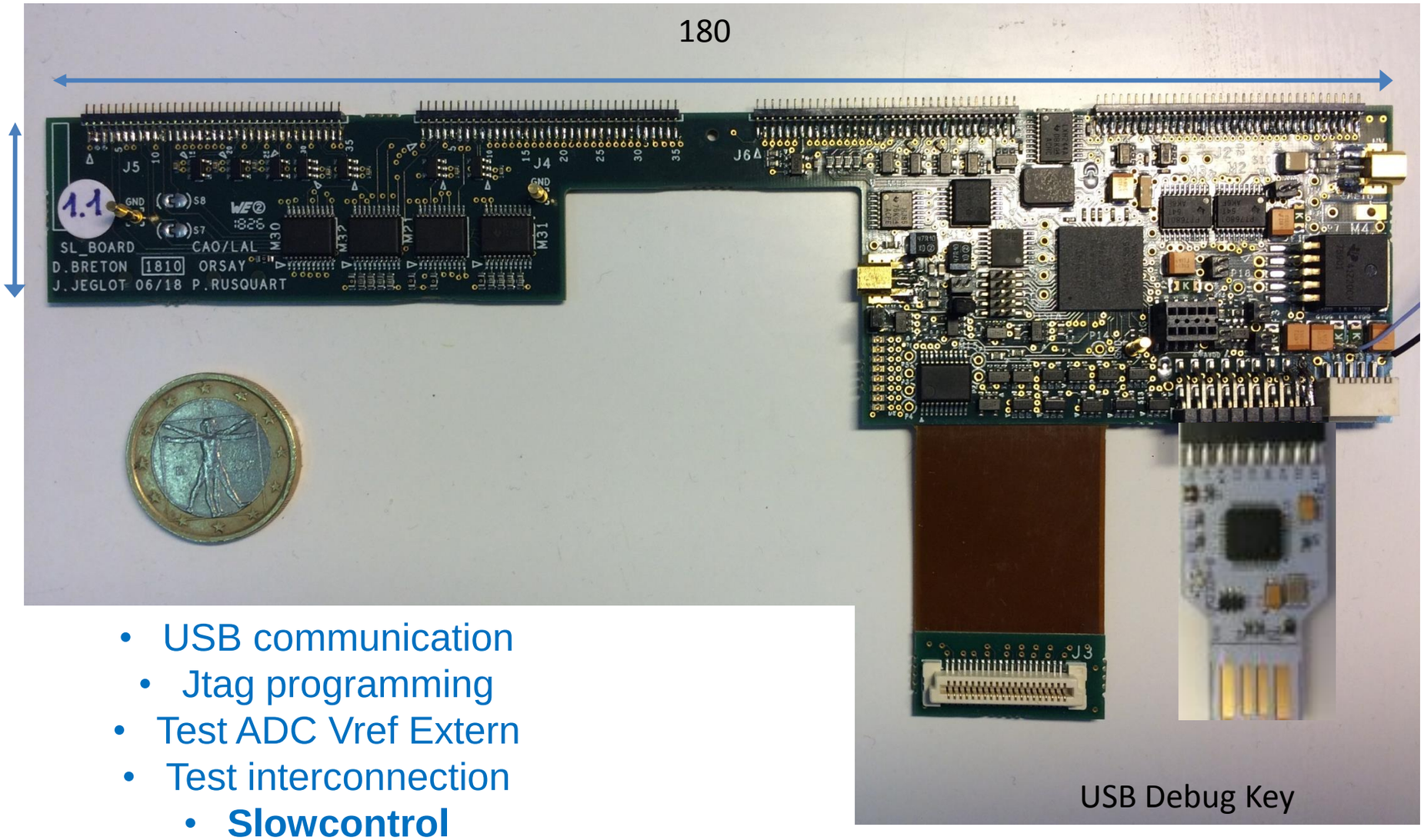
Integrated capacitors permit **the peak current of ~1.5A <u>to be local</u>** during power pulsing => recharge is limited to a total of ~150mA …



Charge/Discharge Cycle Test :
Charge voltage: DC4.5 +0/-0.1V
Temperature : 25 +/-2 ºC
Current:5A
Test cycle : 50,000cycles



# Status of development: SL_board

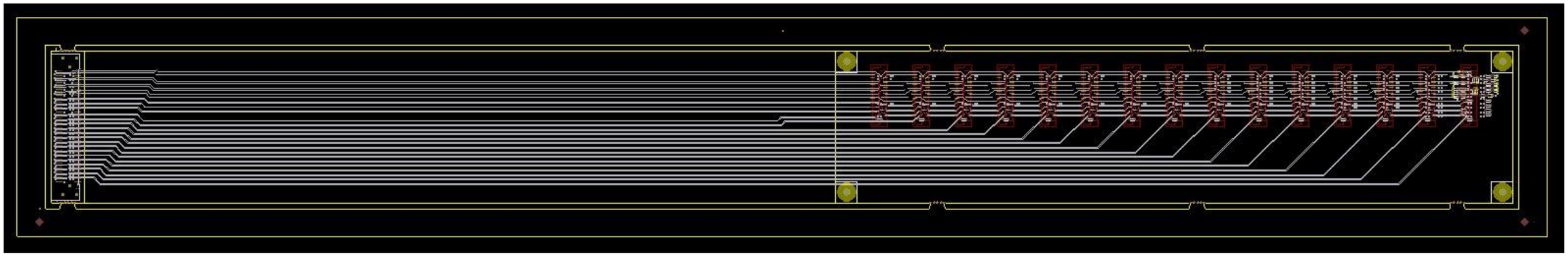


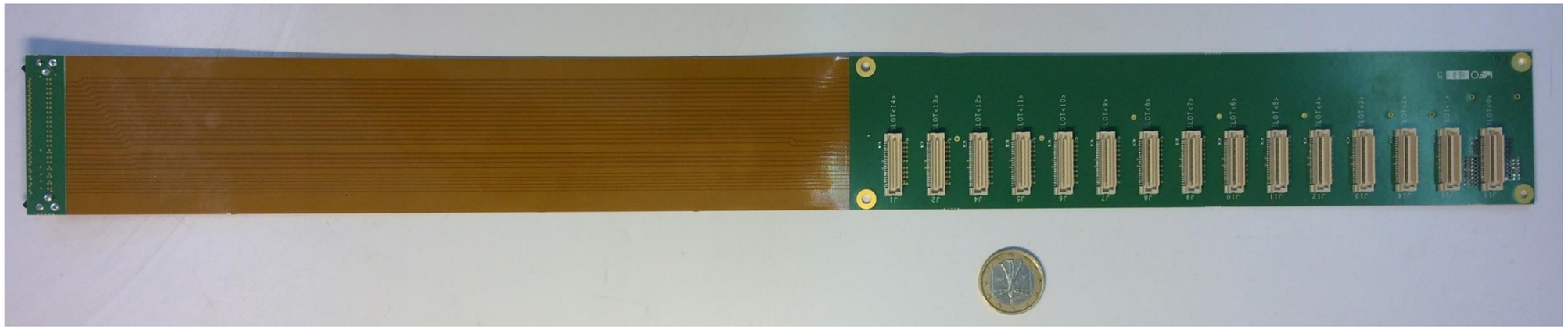

- USB communication
- Jtag programming
- Test ADC Vref Extern
- Test interconnection
- **Slowcontrol**
- **(16 skiroc2a on COB and BGA version)**

TEST OK

# Status of development: CORE_kapton

CORE side — Flexible kapton — Total length ~45cm — Slab side (~22cm, rigid, pitch of 15mm)





**Core Module connector (100 pins):**
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

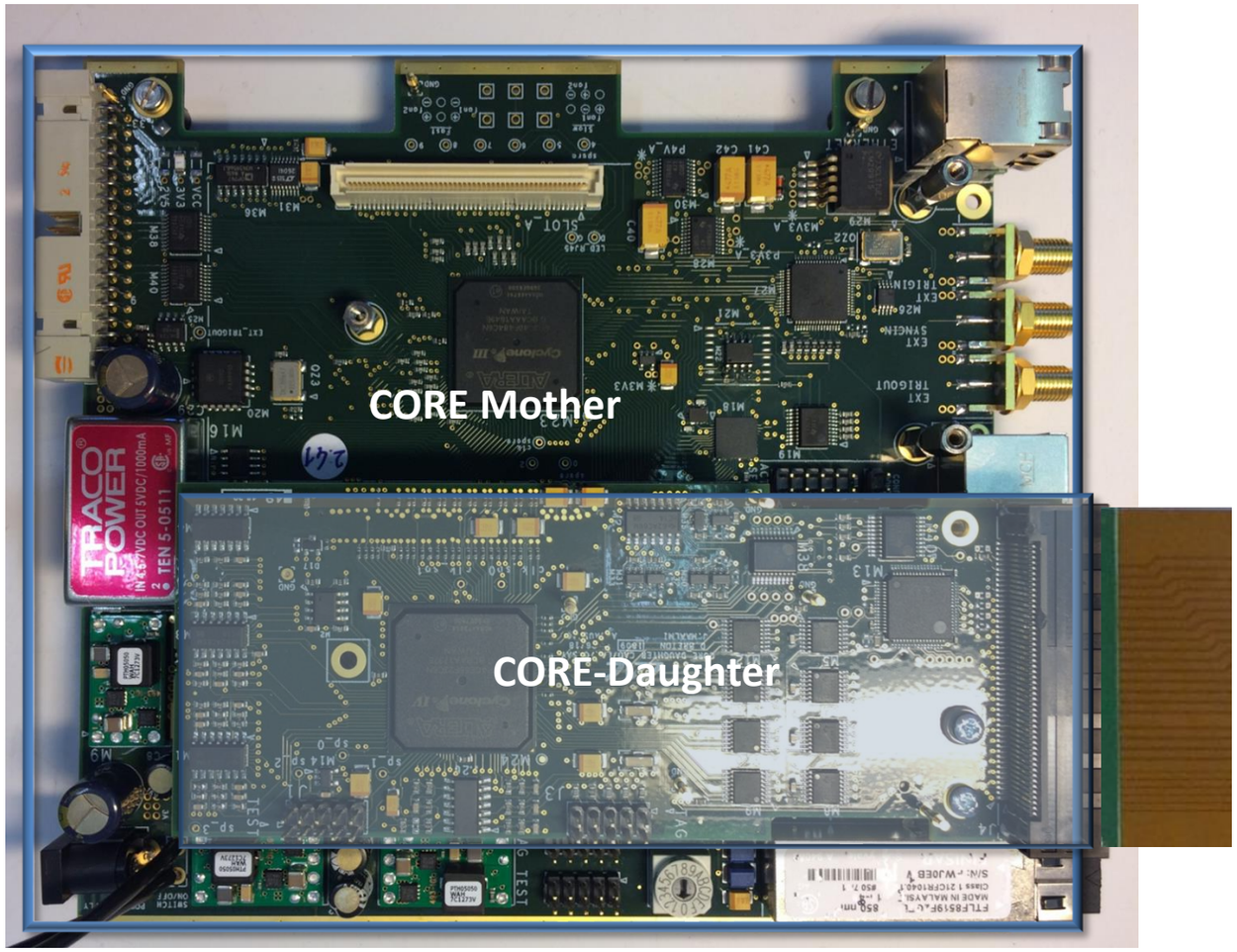
**SL_board connectors (40 pins):**
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

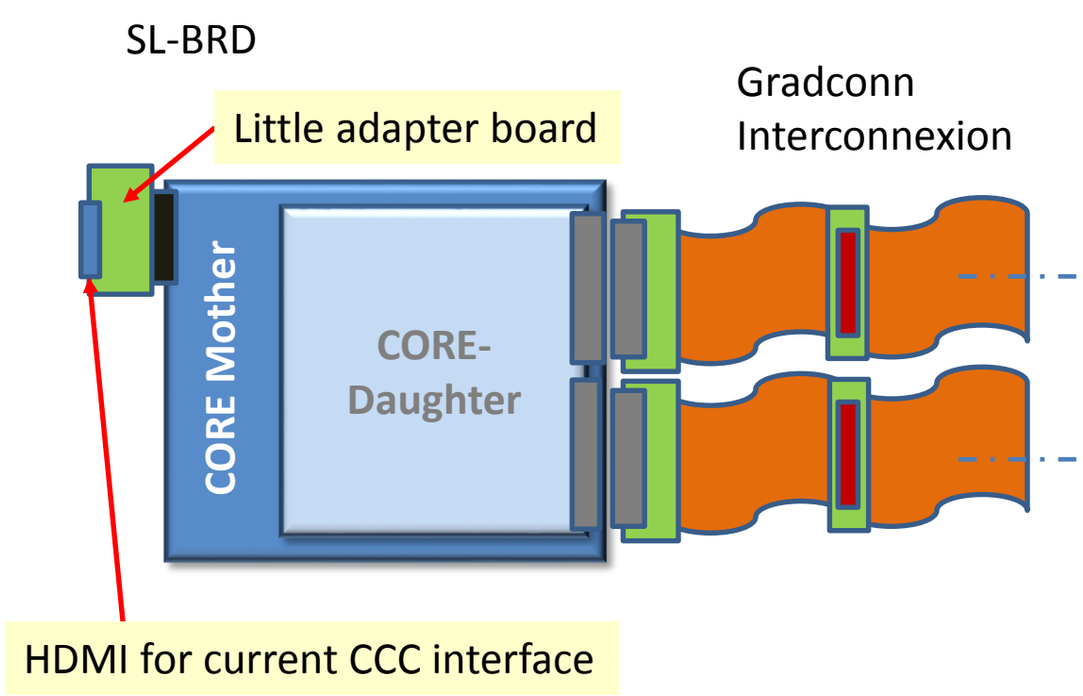
# The Acquisition Module

The Control & Readout Acquisition system will be based on an **existing mother board** that handles:

- Control & Readout through **USB/Ethernet/ Optical fiber**
- Distribution of the clock and fast commands

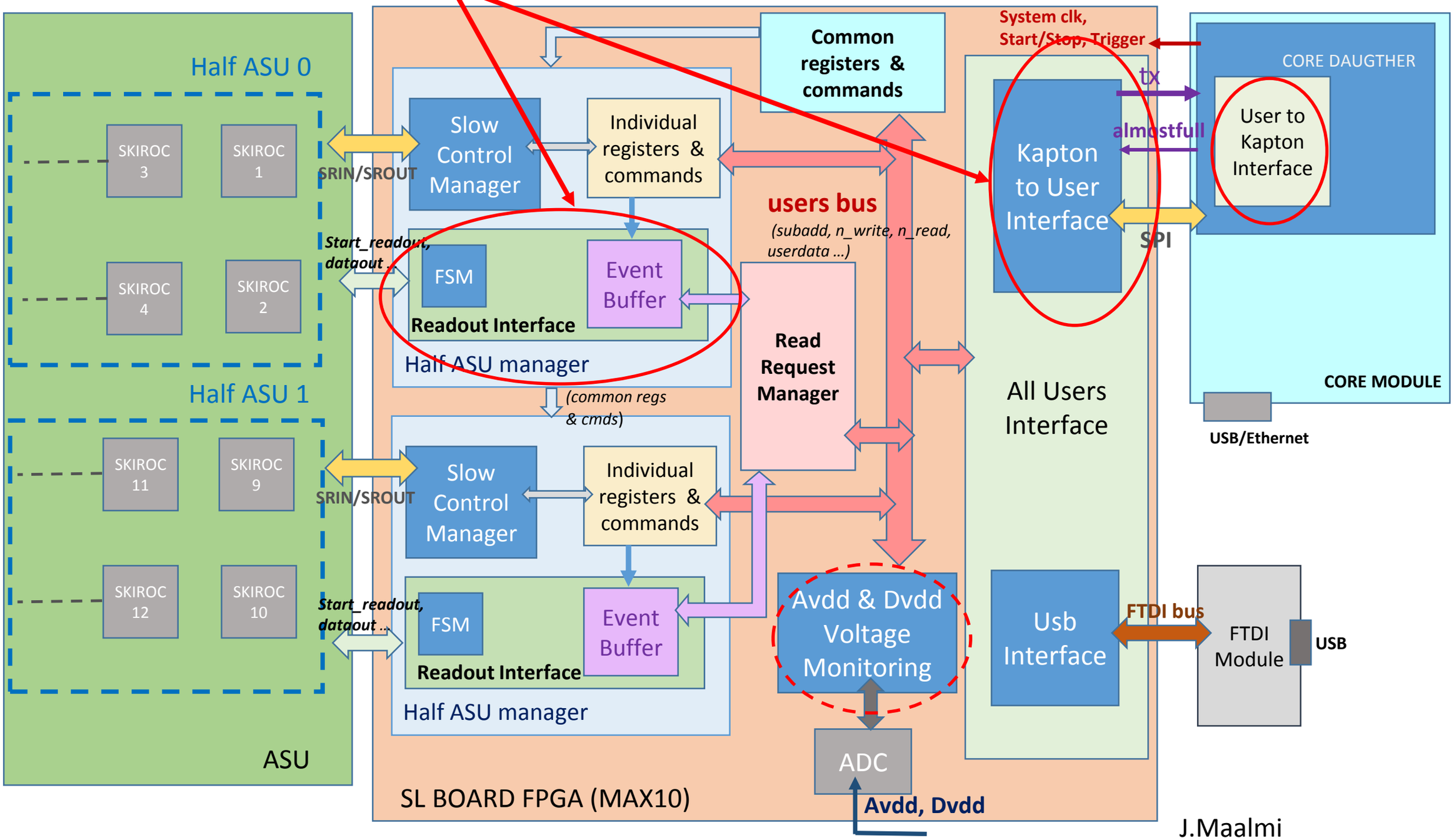
- There are existing low level **C-libraries**. (LAL-ML protocol)
- This LAL development is already used for other experiments.



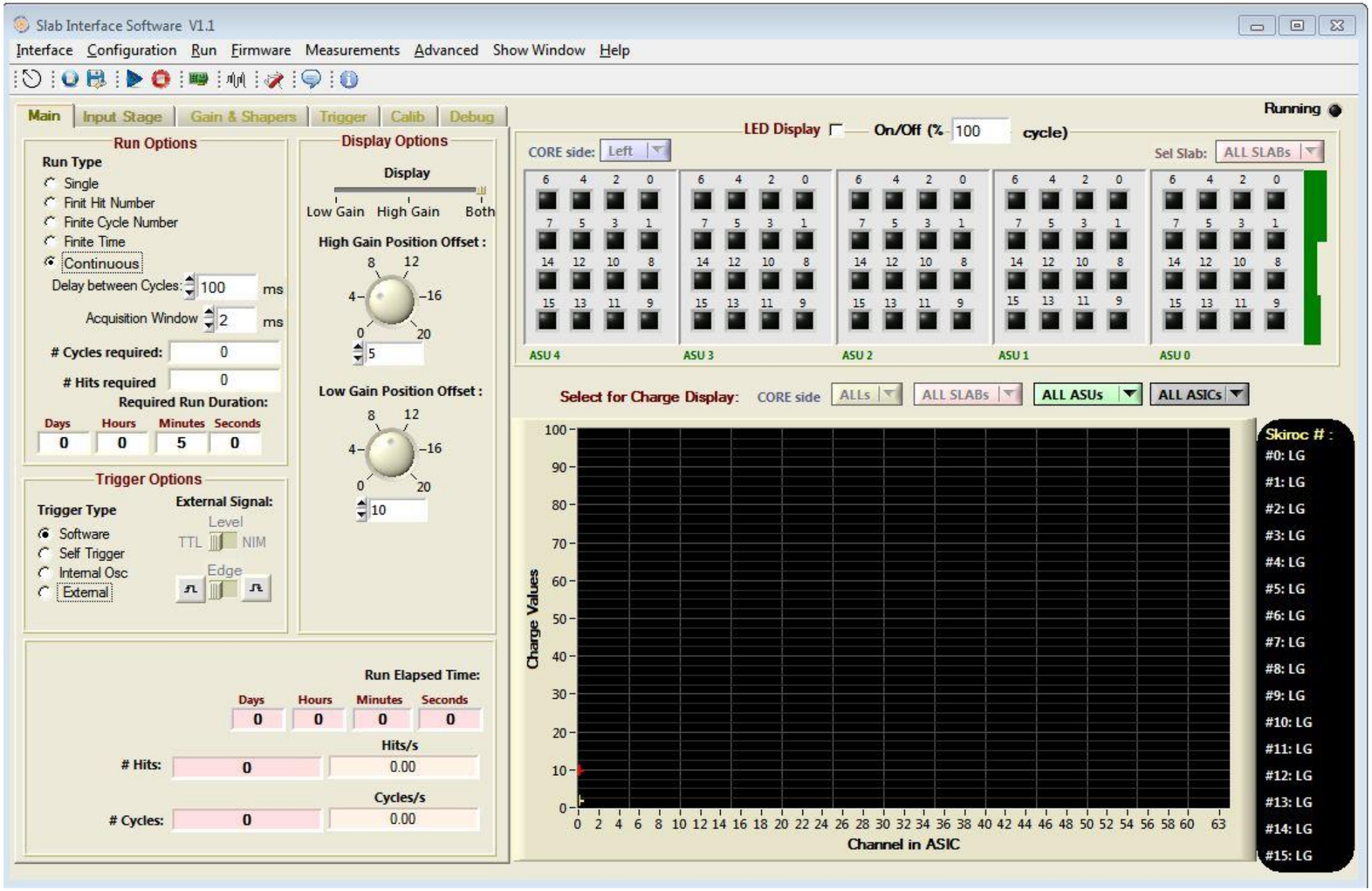
# Firmware Development Status: SL Board FW Schematics

- Remaining Firmware Blocks to develop : **Data Readout Interface** and **Katpton Interface**




J.Maalmi

# Software Development Status: Main Panel for Acquisition:

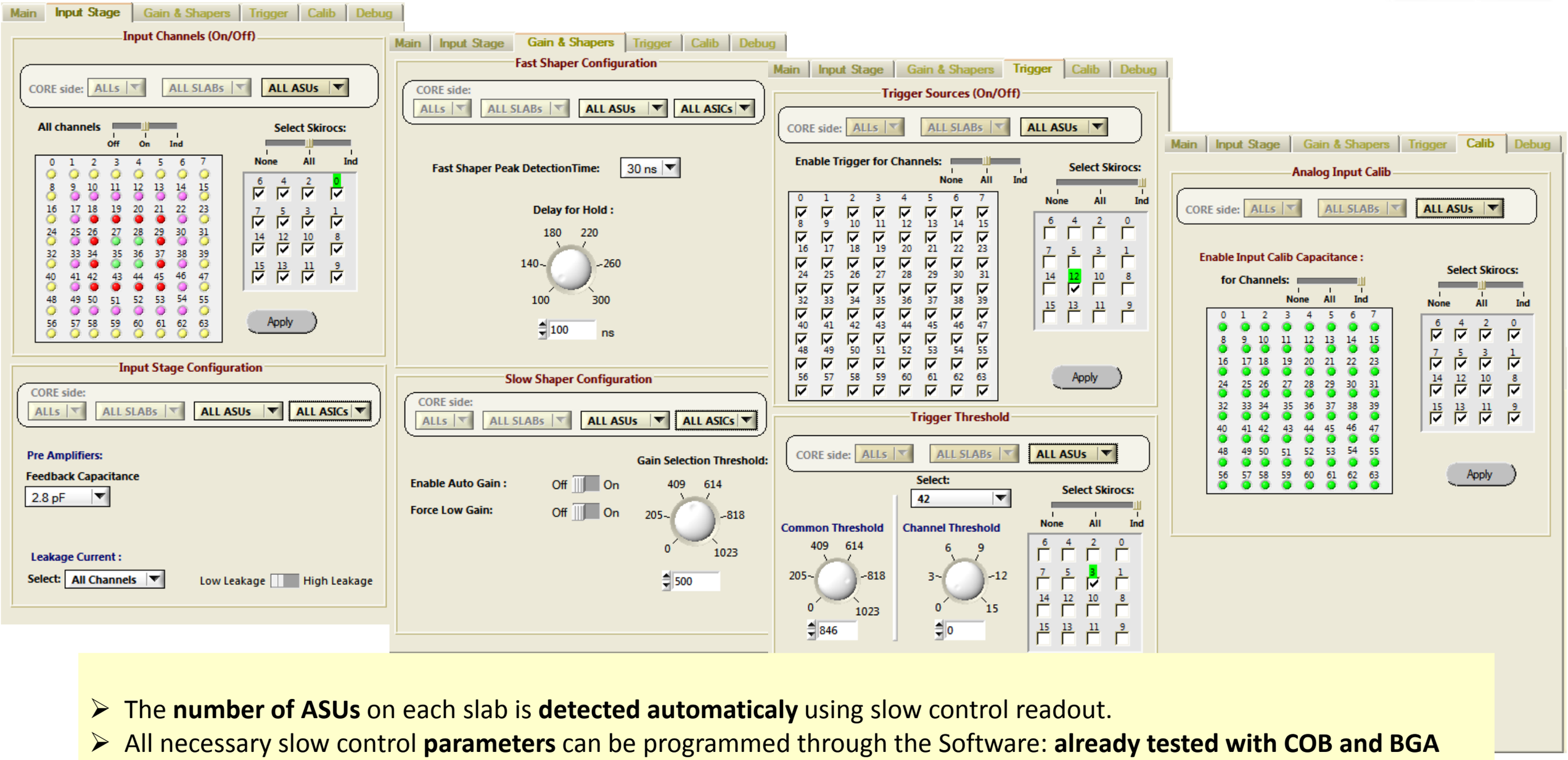



- The Software can handle the communication through FTDI connector **or** through **CORE Module**.
- It handles the **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**
- The C-functions that handles the communication (readout and configuration) can be used as a a library with any other program that handles C-langage.

**Ongoing work for readout …**

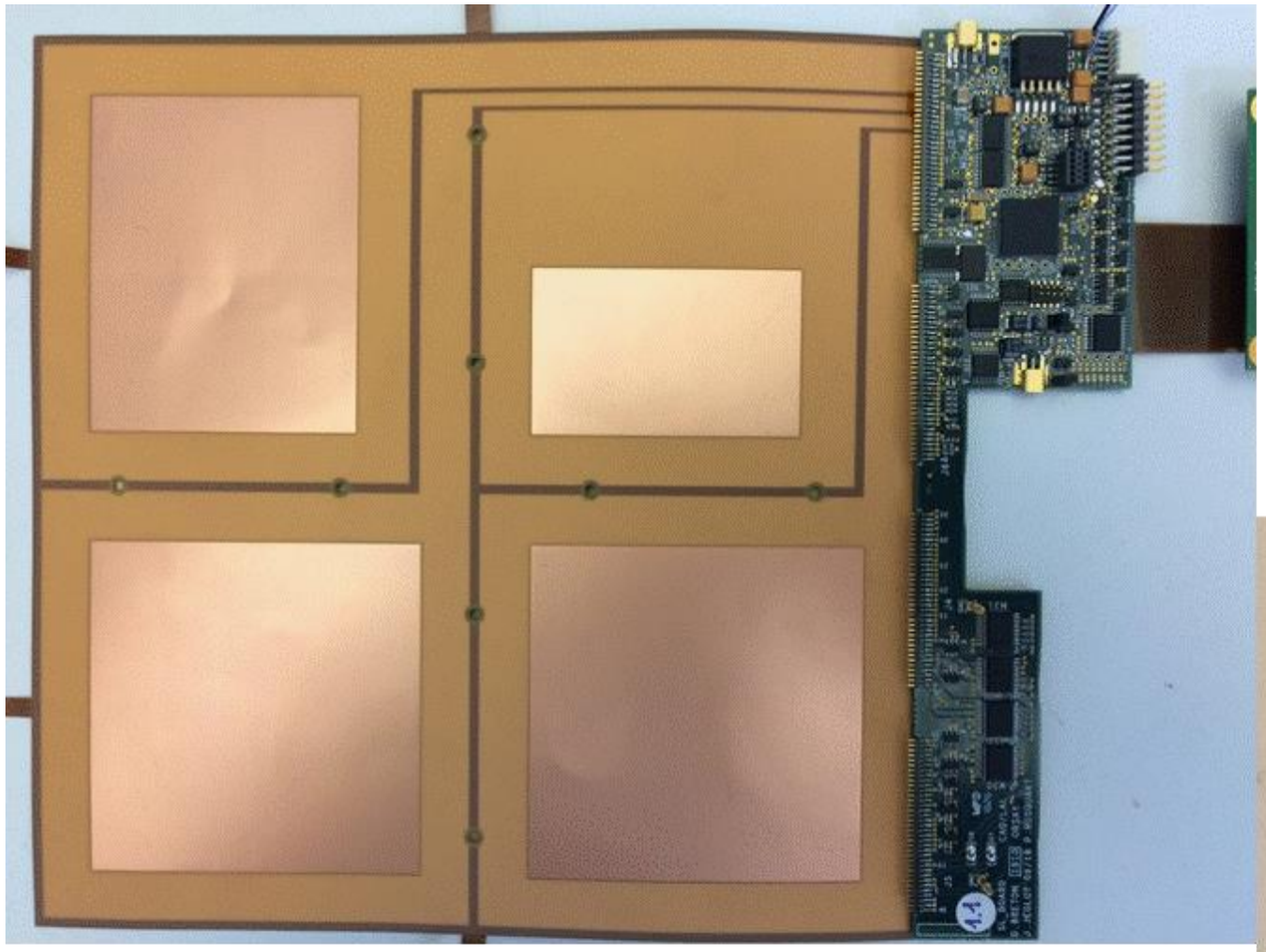
J.Maalmi

# Software Development Status: Panels for Slow Control Configuration

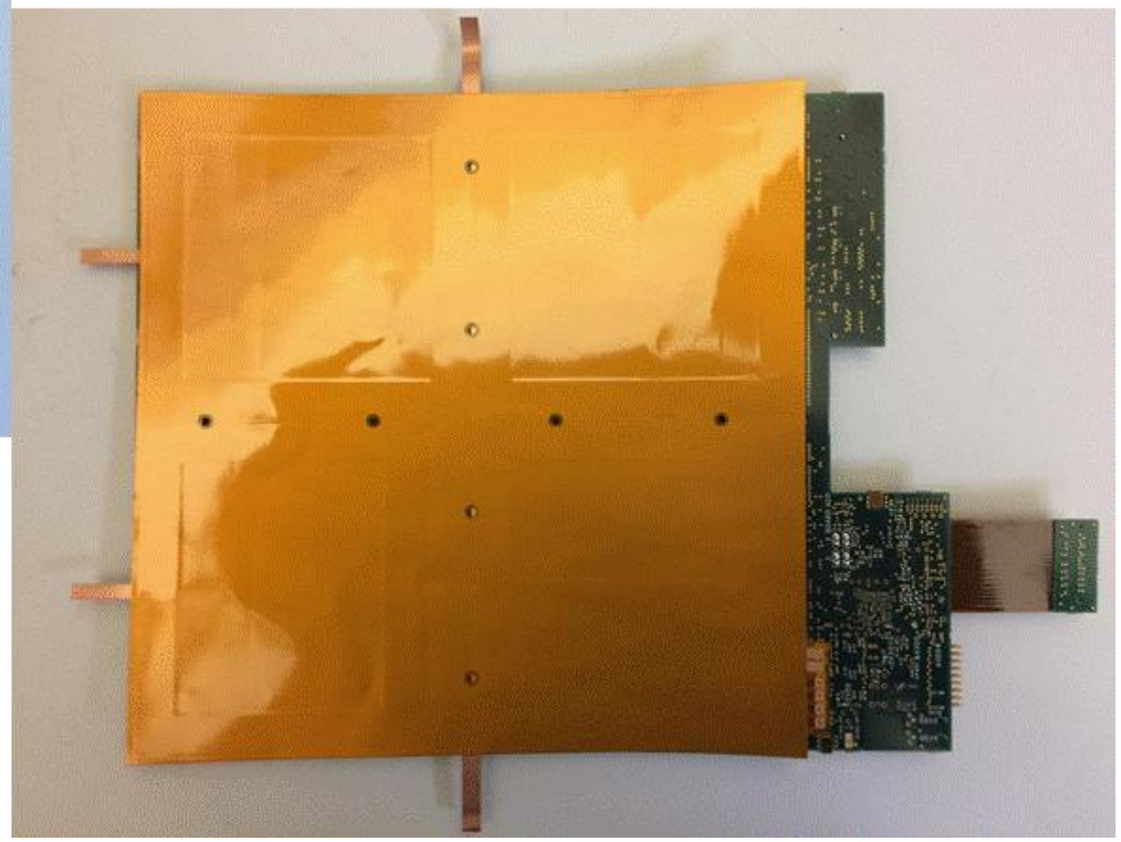



- The **number of ASUs** on each slab is **detected automaticaly** using slow control readout.
- All necessary slow control **parameters** can be programmed through the Software: **already tested with COB and BGA versions of the FEV!**
- Slow control configuration is checked by writing twice the same values to the SKIROC shift register and reading back the pushed value on the SROUT signal.

# Status of development: High Voltage kapton

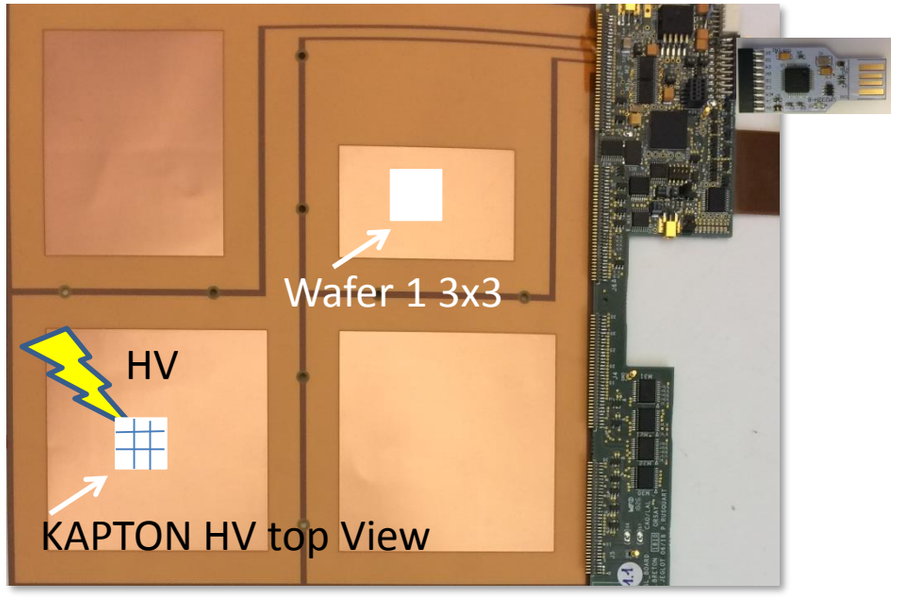


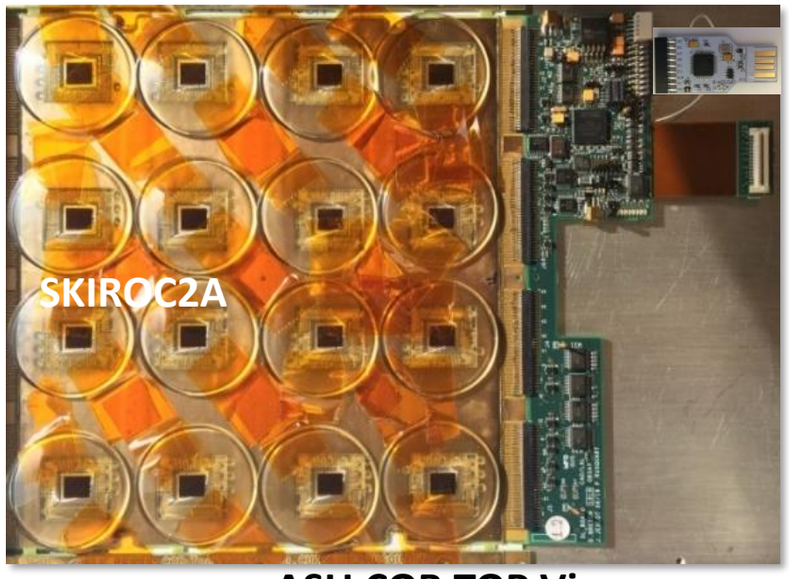
HV Kapton (for 4 wafers power supplies) top view



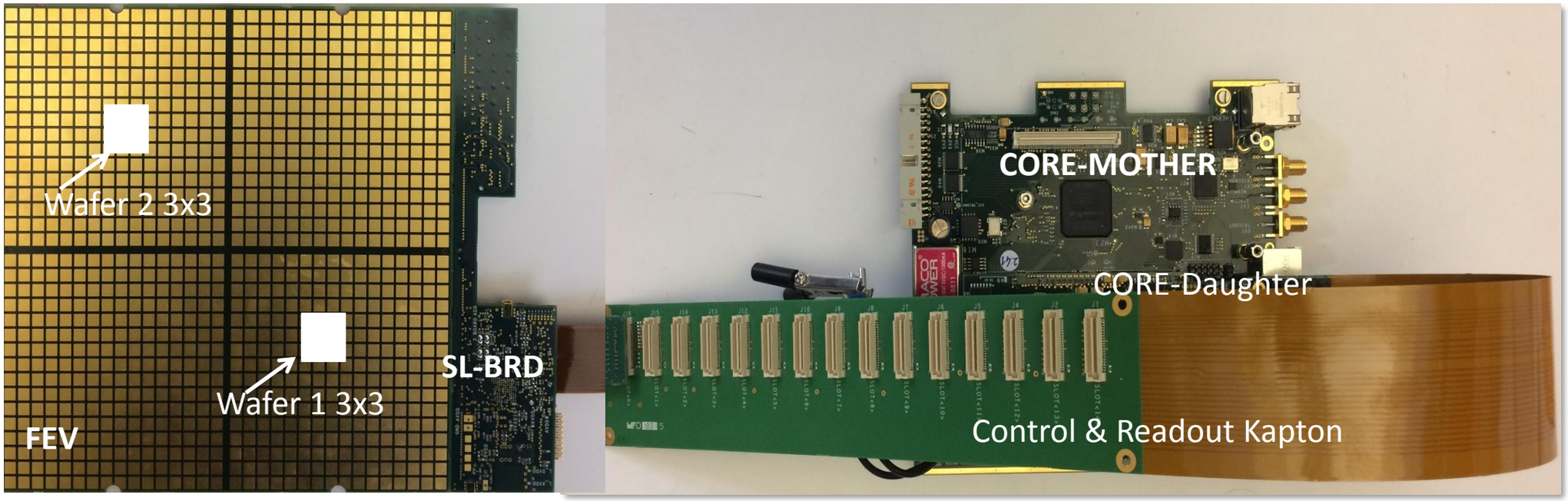
HV Kapton (for 4 wafers power supplies) Bottom view

# Status of development:
# SIW ECAL SYSTEM




**ASU COB TOP View**



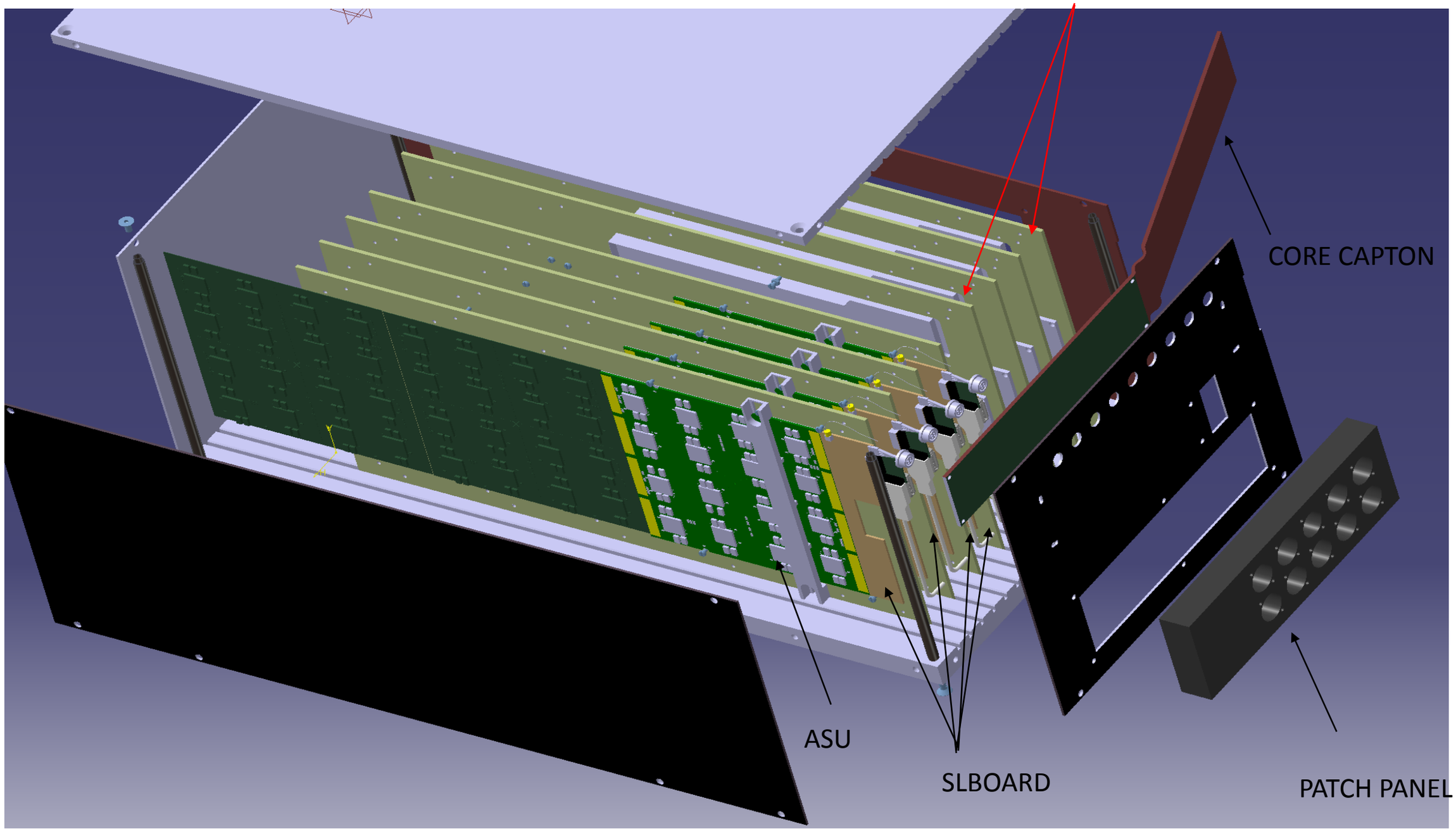

**FEV COB BOTOM View**

Usb communication ok
ASU – Slboard first slow control test ok
Full Firmware & Software in progress

# Status of development: TESTBEAM SETUP

4 SLBOARD WITH ASU COB AND ASU BGA

FREE SPACE TO INCLUDING *Kyushu* SETUP (fev13 Jp +smbV5)

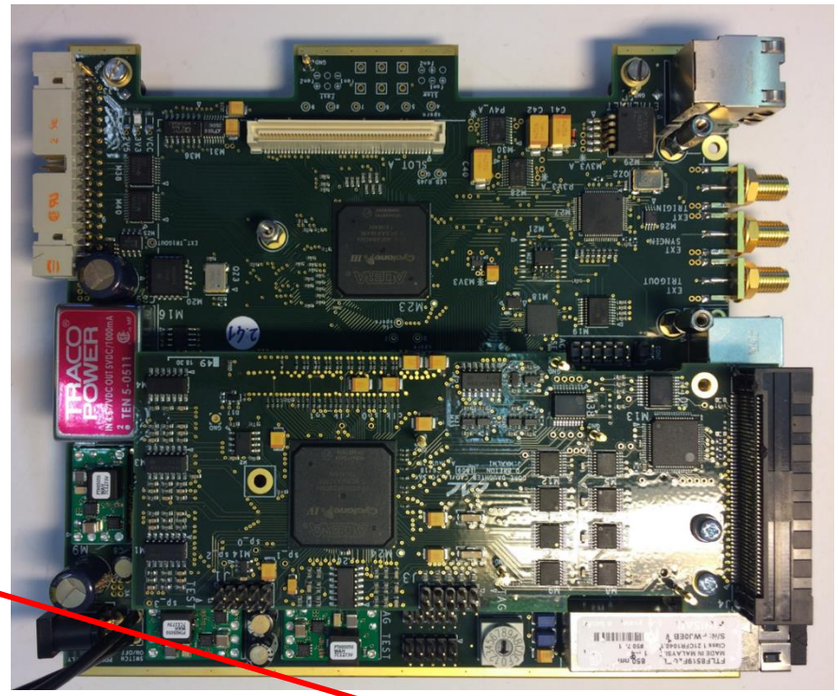


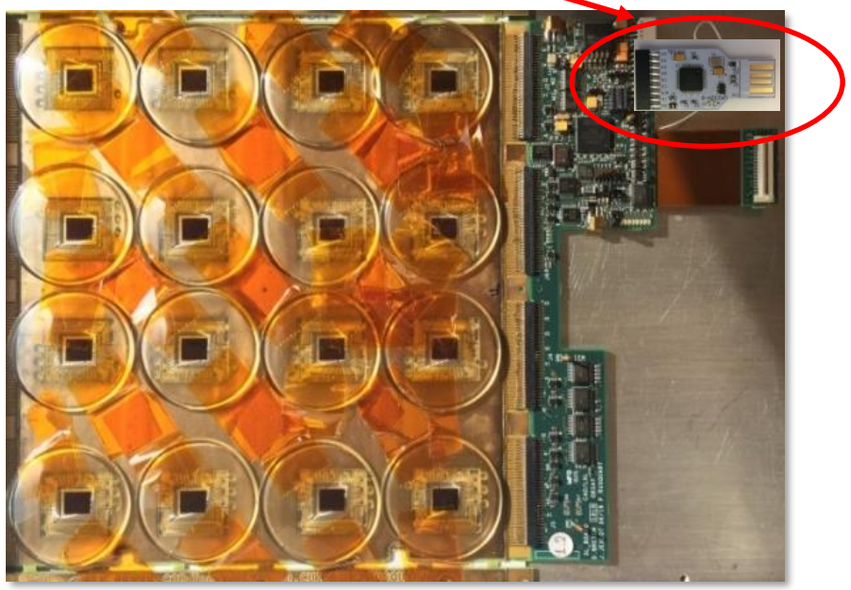
# Preparation for Test Beam in DESY

- We are currently preparing a test beam in DESY (June 2019), there are two options for the **readout**:
  - Readout through **CORE module** (via **USB/UDP**), but still a lot of work in order to develop the communication through the Kapton.
  - Readout of each SL-Board through **FTDI module** directly via **USB.**

- **CORE module,** will be used anyway for **synchronizing** the SL-Boards.

- **Cycles** can be handled :
  - with an **External signal** connected to the External Trigger Input of the CORE Module,
  - Or generated **internally** in the firmware of the CORE Module: the **Delay** between Cycles and the **Acquisition Window** will be programmable by Software.





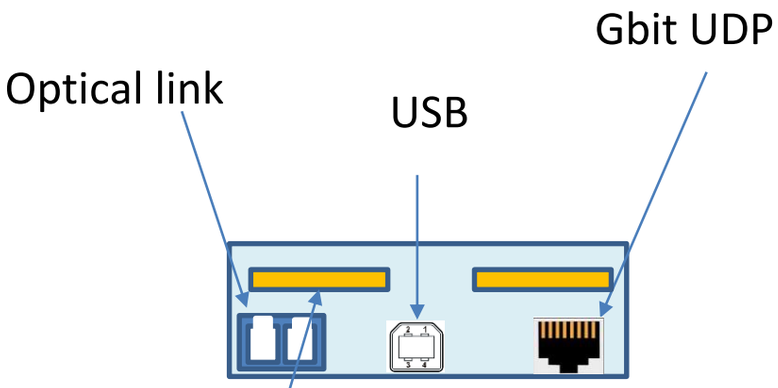
# Conclusion

- The test of the new Digital Interface of the SLABs : the **SL-Board**, is in **good progress:**
  - Slow control configuration of all the SKIROCs on an ASU (BGA and COB) is validated.
  - ongoing work for the data **Readout Interface**.
- We are currently preparing a test beam in DESY for June 2019:
  - We are preparing the mechanical structure that handles the detector and all the electronics
  - We are also working on the Firmware and Software in order to handle:
    - the **synchronization** between multiple SL-Boards using the **CORE Module**
    - the **slow control configuration**, **Data Readout** and **Storage** and the **Acquisition parameterization**.
- Next Steps:
  - Test the **power-pulsing mode** using the ultra-flat capacitors on each ASU.
  - Test the High Voltage distribution capton between SLBOARD and ASU.

# SPARES

# Control & Readout Electronics

**The new developments for the control and readout electronics to satisfy D14.4 (space constraints of an LC Detector) :**

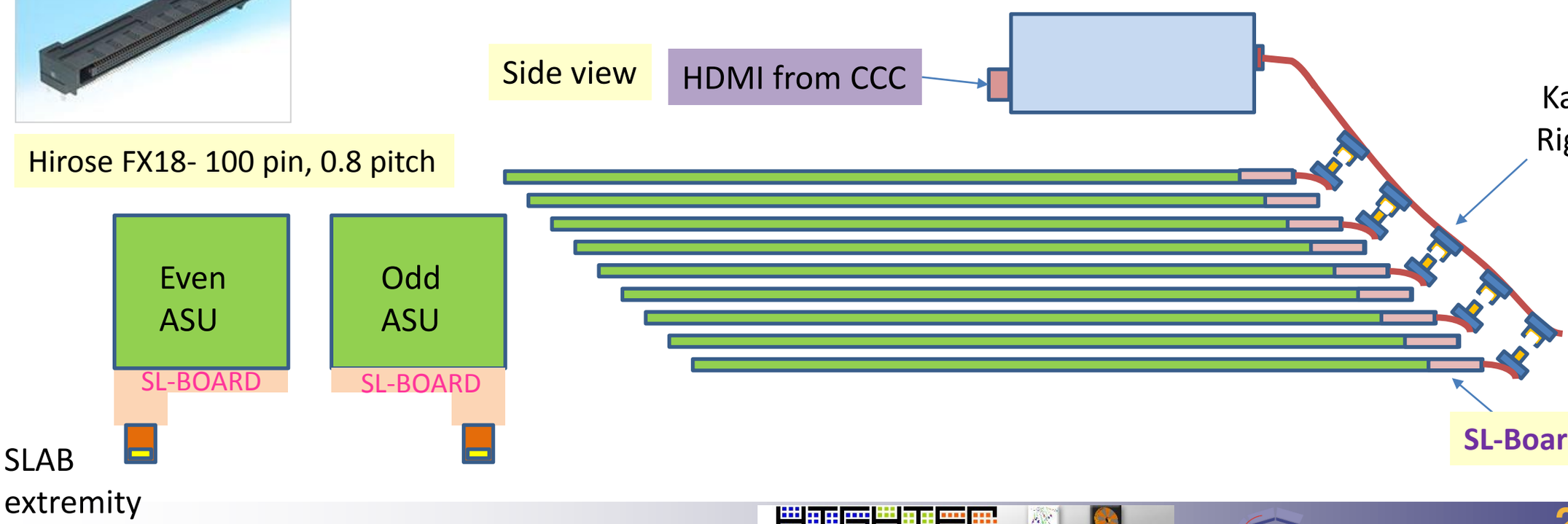


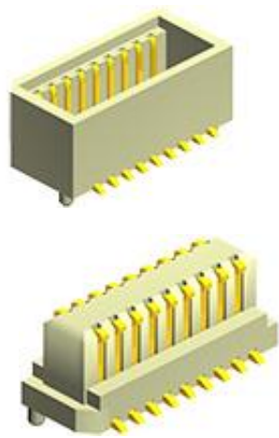

**CORE Module** : Control & Readout Module

Hirose FX18- 100 pin, 0.8 pitch

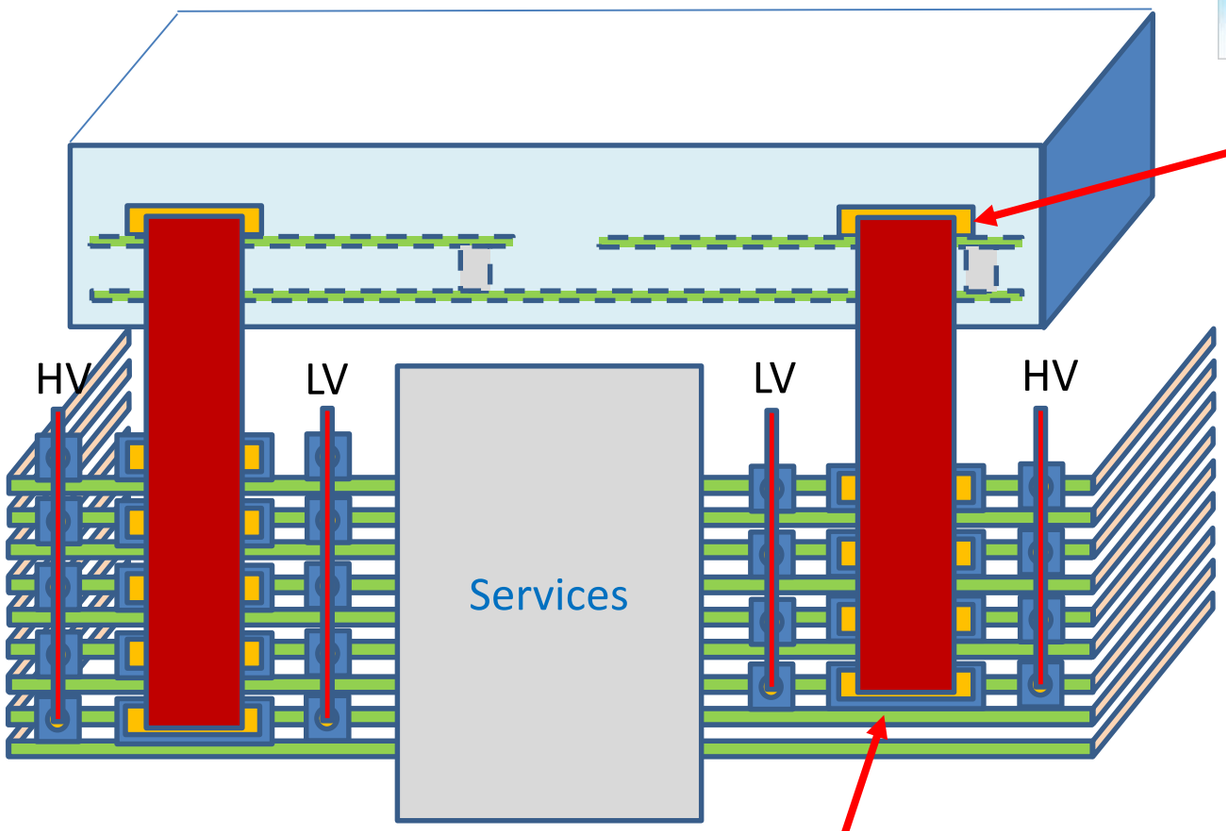
- **SL-Board** :
  Digital interface board situated at the extremity of the Slab, based on a MAX10 FPGA, which handles:
  - Control & readout of the chained ASUs (SKIROC interface)
  - Interface to the CORE acquisition module through a kapton cable (rigid+flexible) in order to have flexibility for the connection inside the detector (45° angle)
  - Local 40MHz oscillator and remote USB interface for standalone control of the Slab (permits independent testing of Slab interface and kapton communications).

- **CORE-Module** : Control & Readout module that handles a column of Slabs, for the prototype phase.



# Control & Readout Signals




**Core Module connector:**
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

**SL-Board Connector**
7 differential pairs for sensitive signals, 2 individual pairs for control and readout, 14 common lines, GND

| | Signals |
|---|---|
| | Clk |
| | Trigger |
| | Start/Stop |
| | Busy |
| | Irq |
| JTAG | TCK |
| JTAG | TMS |
| JTAG | TDI |
| JTAG | TDO |
| SPI | SCK |
| SPI | SDI |
| SPI | SDO |

| Signals |
|---|
| Rx_i |
| Tx_i |
| ADD[0] |
| ADD[1] |
| ADD[2] |
| ADD[3] |
| Spare … |
| GND … |

Full design of ILD compatible electronic services started that includes parts described above

# Power-Pulsing:
# New ultra-flat Capacitors


Proposal: new ultra-flat capacitors on all ASUs for the AVDD decoupling resulting in:

- Peak current reduction: especially through the connectors
- No voltage drop along the slab
- Homogeneous peak power dissipation during power pulsing.

➢ 400 mF capacitor/ 15A (peak Current) at the end of the SLAB to 140 mF / 1.5 A per ASU.

Reminder of power consumption values :

- DVVD (3.3V) 11 mA/chip, total 180 mA/ASU
- AVDD (3.3V) / Chip : 90 mA/chip during ACQ, 20 mA during Conversion, 0.01 mA idle

measured in house and compared with measurements by Stephane Callier (Omega)

- Distributing the capacitors along the slab permits reducing current between ASUs by a factor ~50-100.
- The current peak is local.
- The current delivered for charge reloading of the capacitors will be actively limited at the extremity of the Slab