CALICE AHCAL.

Status of Developments

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CALICE main meeting

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HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

AIDA 2020

DESY

Outline

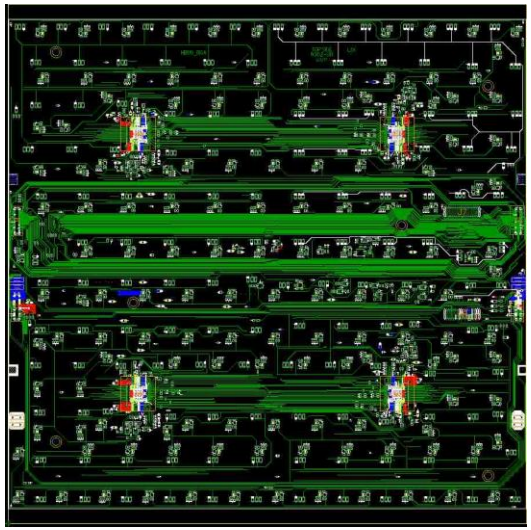
- HBU6 for KLauS ASIC (Uni Heidelberg)
- AHCAL DAQ and Documentation (from Jiri)
- CMS HGCAL Front-End Boards and DAQ

HBU6 for KLauS ASIC

- HBU6 for KLauS ASIC in development (Uni Heidelberg – DESY coorperation)
- Can be operated with AHCAL DAQ
  - New POWER4 board required (supply voltages different)
  - New firmware in DIF required, to be developed.
- KLauS ASICs have been packaged as SPIROC2E (BGA372, Uni HD).
- Status POWER4_HD: 5 boards completed.
- Status HBU6_HD: Layout completed, in first review. To be ordered end April.

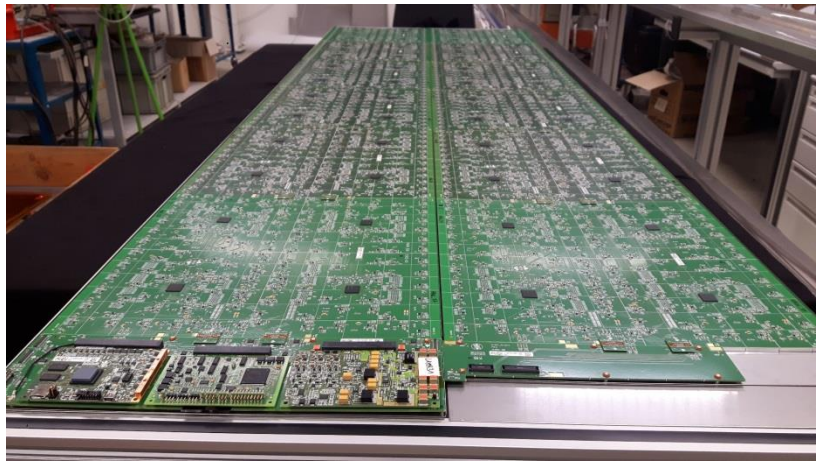
POWER4_HD (left),

HBU6_HD top layer layout (right)



DAQ HW & FW status

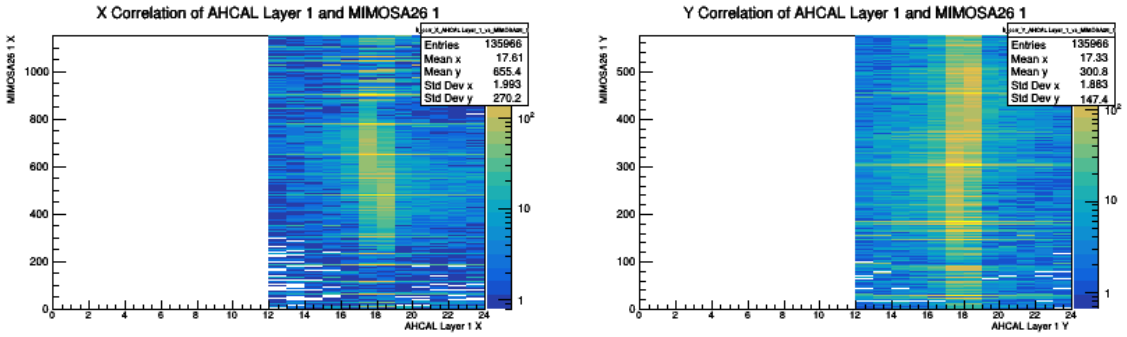
- **Major TCP bandwidth upgrade** on Zynq (**6 → 75** MB/s)
  - Generic AXI4-stream→TCP solution (https://github.com/jkvas/ahcal-axidmatcp). Upgraded Xilinx Vivado version 2014.2 → 2018.2. New Linux kernel DMA driver + userspace TCP server.
  - Implemented & tested: **mini-LDA** (not yet wing-LDA)
- Operating big 2x6 HBUs layer (0.2 x 2 m^2)
  - Risk of burning POWER board → New **DIF2 firmware** necessary
  - enforced power pulsing
  - Acquisition time & duty cycle restrictions (5ms, 10%; configurable)



- Ongoing DIF2 firmware changes:
  - retiming (SPIROC stop condition, ILC mode)
- BIF issue pending: Storage of multiple trigger inputs (in close time proximity)
- All firmwares stored on DESY svn
  - https://svnsrv.desy.de/k5websvn/wsvn/General.ScCalo_DAQ

DAQ SW

- Happily using EUDAQ version 2.1.0: https://github.com/jkvas/eudaq
- Reprocessing of RAW files→slcio in EUDAQ **necessary** for testbeams in 2018
  - to fix the SPIROC2E TDC offsets (different for each BXID stopping parity) and incomplete events
  - Mass-reprocessing preparations ongoing (Lorenz, Jack)
- Combined running with TLU and beam telescope (again):
  - New EUDAQ datacollector implemented (BIF stores independent PMT signal)
  - On-the-fly spatial correlations with telescope via eudaq onlinemonitor
- Documentation on confluence:
  - https://confluence.desy.de/pages/viewpage.action?pageId=102022141

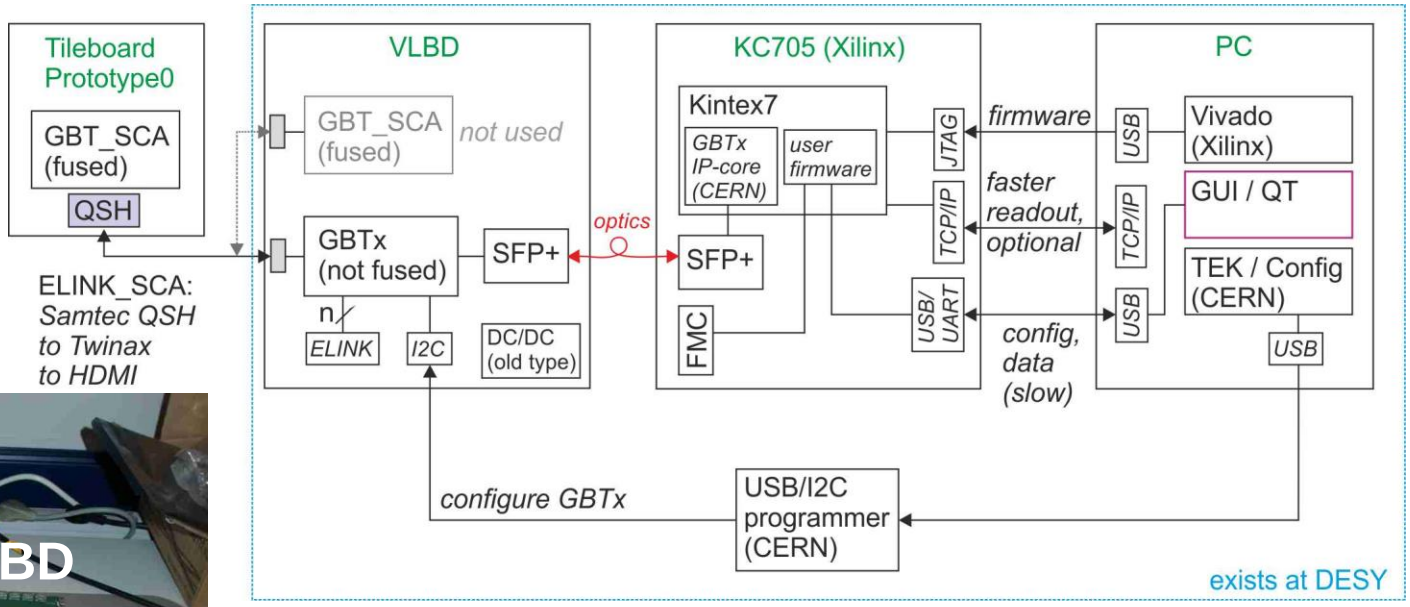


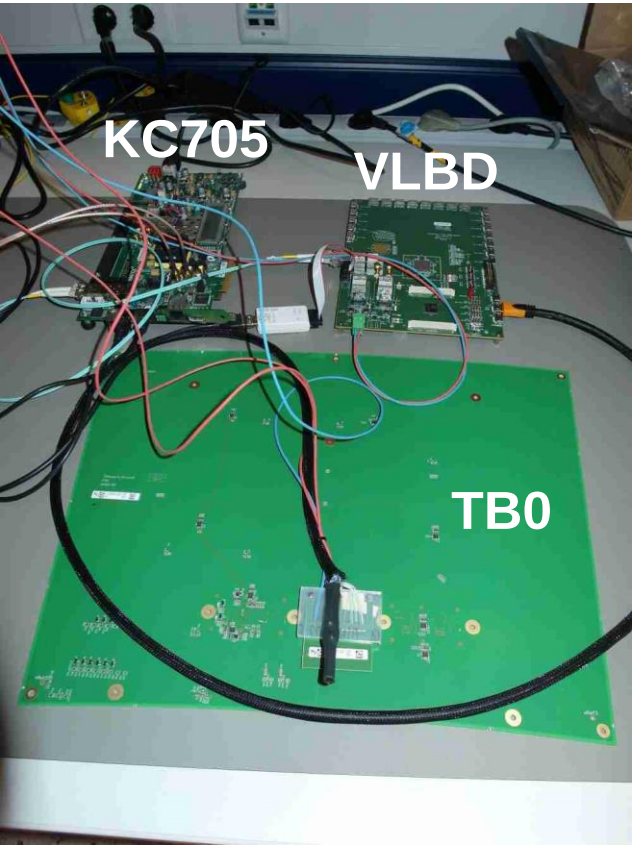
EUDAQ onlinemonitor: shooting between AHCAL tiles. No hot pixel suppression.

A scintillator tileboard detector for CMS HGCAL

- The HBU technology is foreseen for the front-end boards of the Phase II CMS HGCAL detector (outer endcaps). Detector concept is in final evaluation.
- We can profit a lot from CALICE experience
  - MPPC readout and powering.
  - Sensitive analogue electronics, large PCBs.
  - LED system for calibration and monitoring.
  - Tiles and Wrapping.
- But there are also new challenges:
  - High radiation environment, no standard components.
  - DAQ: continuous data-taking.
  - Operation at -30°C.
- New front-end ASIC HGCROC from our OMEGA colleagues with contributions from other institutes is in production.
- First tileboard (TB1) prototype expected July/August 2019

TB0 Prototype and DAQ Setup

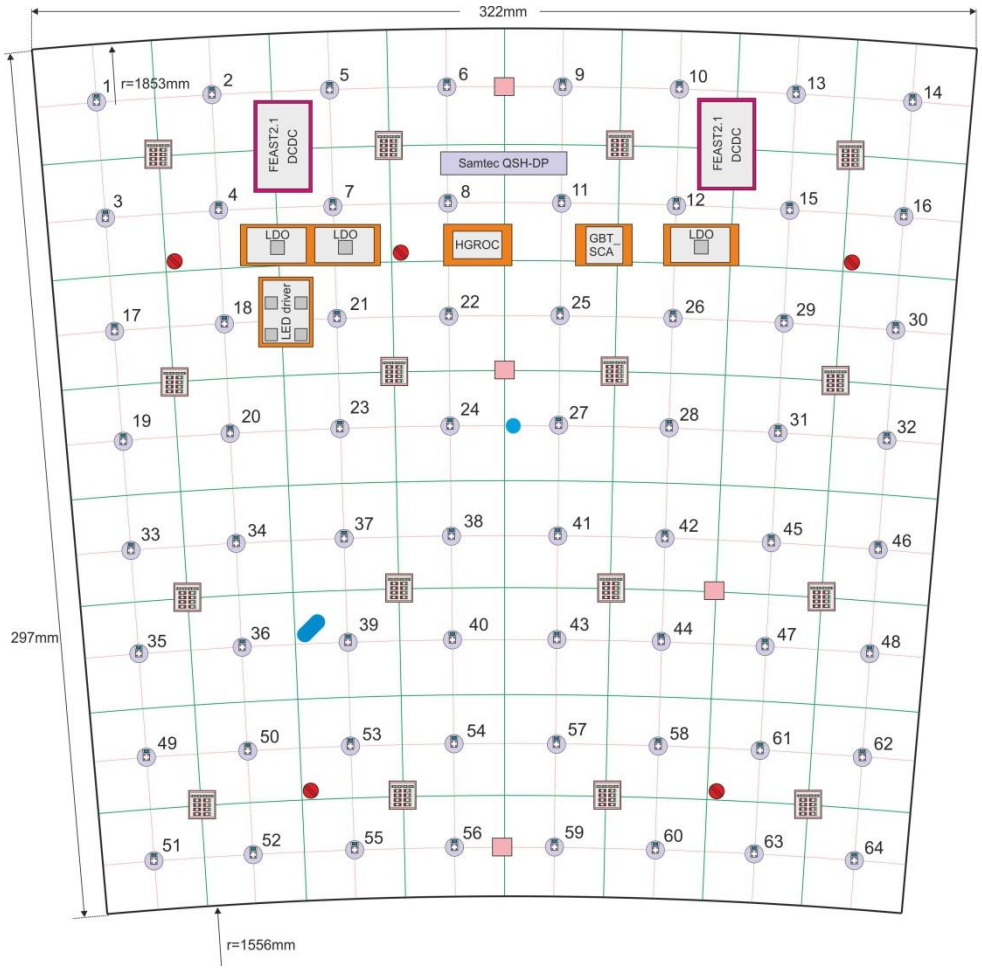


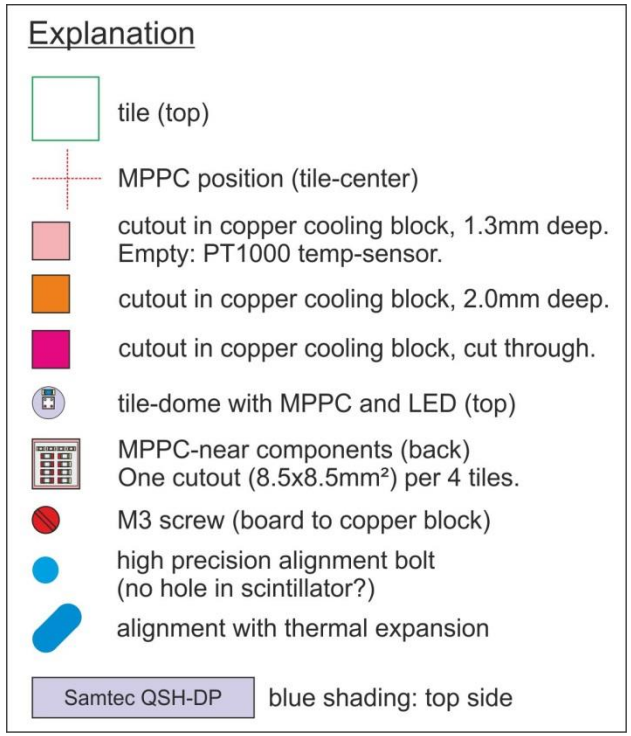


- First setup of complete DAQ chain, mainly derived from existing Atlas setup.
- A first tileboard pre-stage TB0 (mainly GBT_SCA) realized and in operation.

Next step is realistic tileboard: TB1

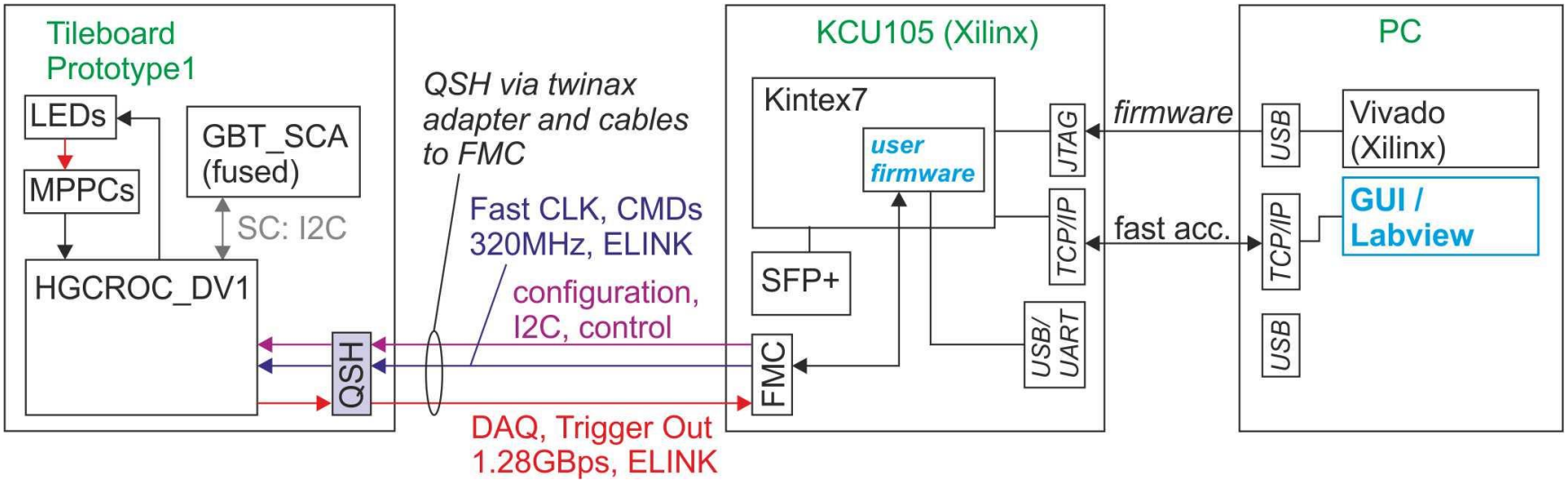
- Already clear picture of TB1: One HGCROC, 64 channels (MPPCs + Tiles), LED calibration system.





As good as possible in scale.
Cutouts can be moved for cooling pipes.
Preliminary!

TB1 prototype DAQ setup



- First step for DAQ: Control and Readout with FPGA prototyping board KCU105.
- Setup and pinout at the interfaces as OMEGA testboard setup for HGCROC_DV1:
  - share DAQ development effort.
  - compare results easily.

Status Hardware and Conclusion

CMS:

- TB0 setup in operation.
- TB1 and both TAs: Schematics completed, have been sent for first evaluation to scintillator group.
- Layout could start now. To be fixed:
  - MPPC footprint
  - Scintillator board (and TB1) geometries.
- Layout is complex and has to start with TB1-outline (geometry). We expect at least 2 months layout development.

AHCAL:

- HBU6 for KLauS chip (Uni Heidelberg) ready for ordering.
- Schematics of DAQ Interface Electronics (DIF, CALIB, POWER, CIB) have been passed to USTC China.