Testbeam Plans 2019

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SiW ECAL Groups in CALICE:

CALICE Collaboration Meeting Utrecht/Netherlands – April 2019

Testbeam 2019

Beam time:

24/6/19 – 7/7/19 at DESY

Objectives:

- Comparison of ASU based on BGA and of ASU based on COB
  Two of each type = 4 ASUs
- Test of new SL-Boards (see Jimmy's talk)
- Validation of FEV13-JP Layers (See Taikan's talk)
- Remark: Long slab studies are going on in lab based on experience on 2018

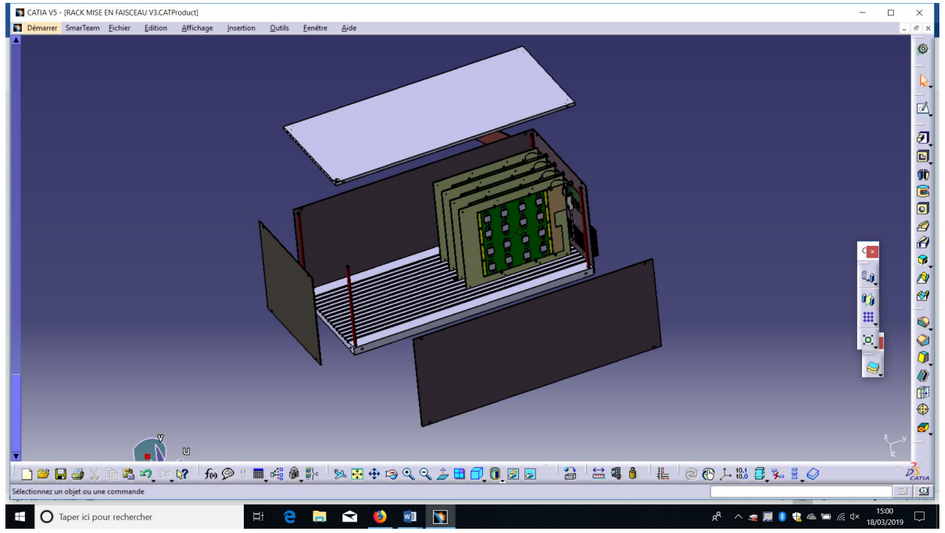
Availability of hardware

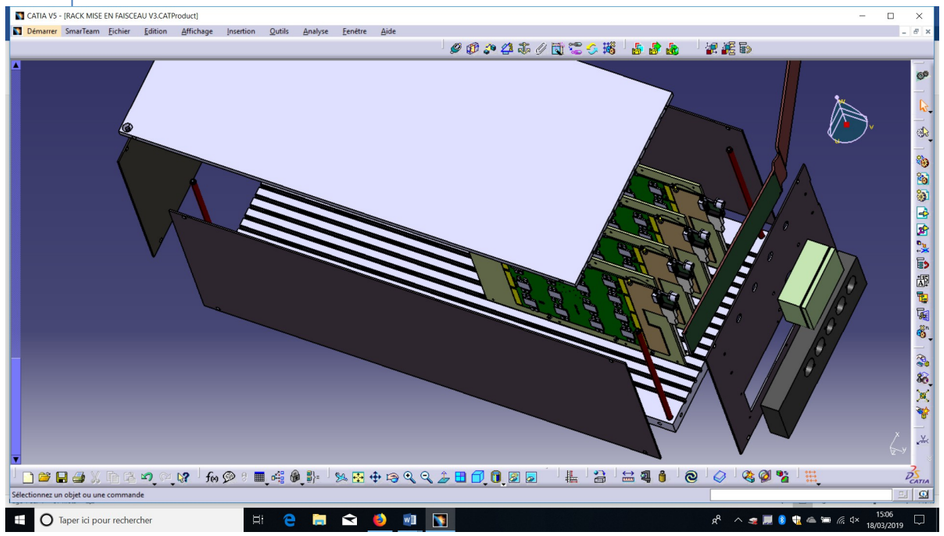
- FEV-BGA
  - 1 FEV11 completely cabled
  - 2 FEV12 will be cabled until middle of April
- FEV_COB
  - 3 FEV COB equipped with ASICs (2 received freshly from CERN Bond Lab)
- 10 SL Boards
- 1 SMBv4 and 1 DIF for check-out of ASUs (“ASU Validation Bench”)
- 5 FEV13-JP

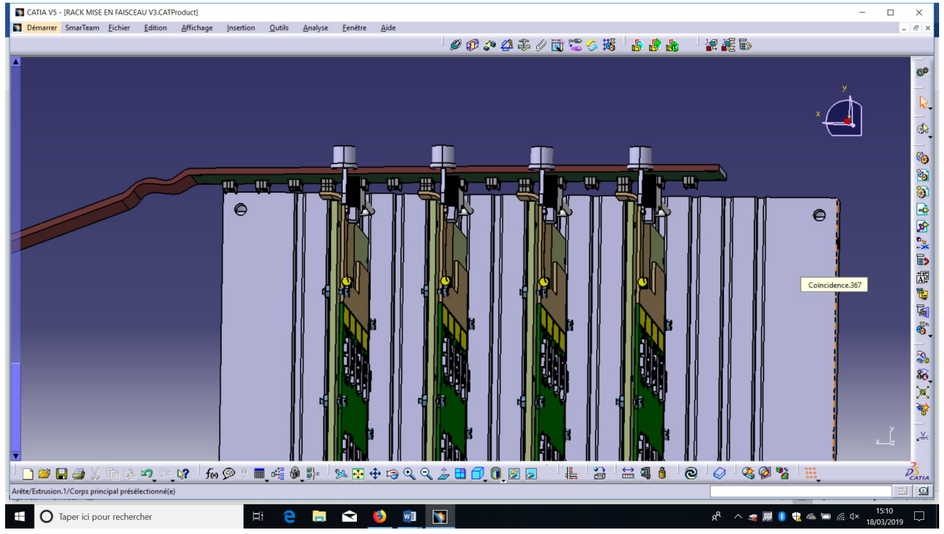
Steps and Milestones

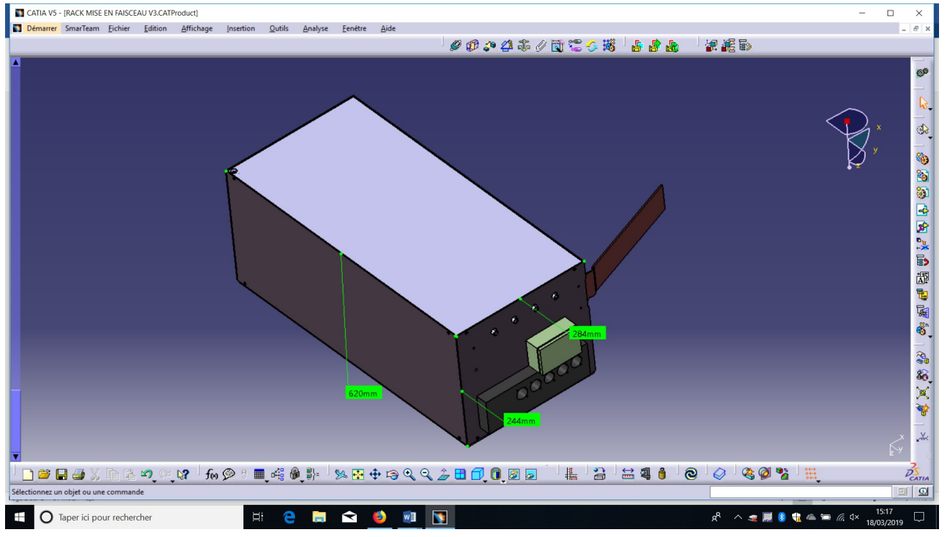
- Design of mechanical structure end of March - **Done (see later)**
- Fabrication of mechanical structure imminent – Time scale ~1 month
  - Mechanical integration of FEVs
- Cabling work 1st batch end of March - **Done**
  - 2nd batch once mechanical structure is available
- Cabling of PCBs middle of April – 75% achieved
- "ASU Validation Bench" ready beginning of April - Ongoing (see later)
- Firmware of SL Boards for SC loading and data readout ready end of May – Ongoing
  - Milestone achieved beginning of by seamless loading of SC to ASUs
- Gluing of wafers during May – in close contact with LPNHE (see later)
- Commissioning of detector in lab – end of May beginning of June

Preparation work – Mechanical Structure



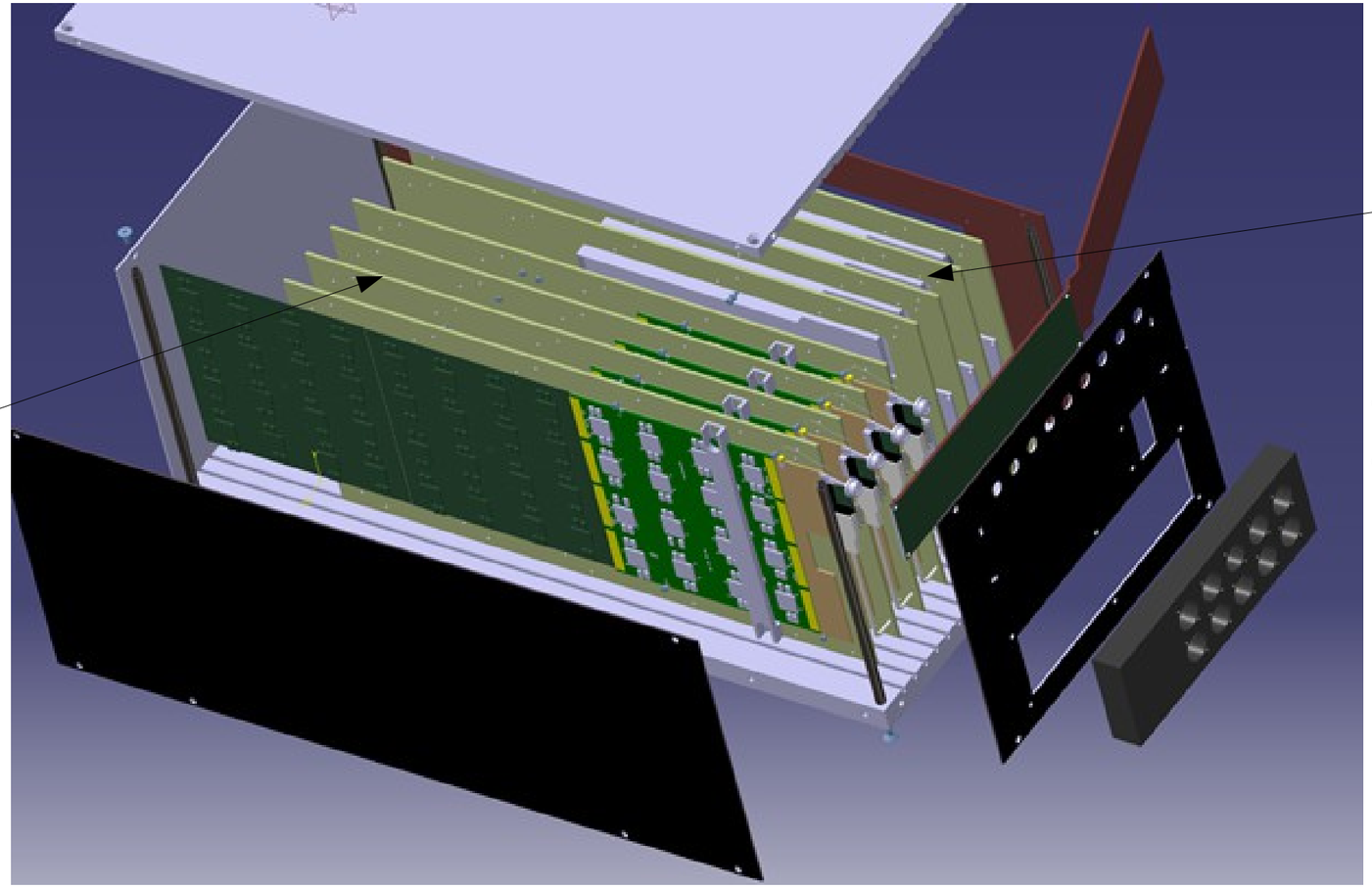






Preparation work – Mechanical Structure Explications

Agreement at preparation meeting 20/3/19 to host FEV13-JP in
=> Adaptation of mechanical structure



FEV13-JP
(require HDMI feed)

Layers
with
SL-Boards

- Plans are ready
- Fabrication starts 15/4/19

Gallas/Thiebault

Status of beam test preparation – ASUs and electronics

- 3/4 PCB are available

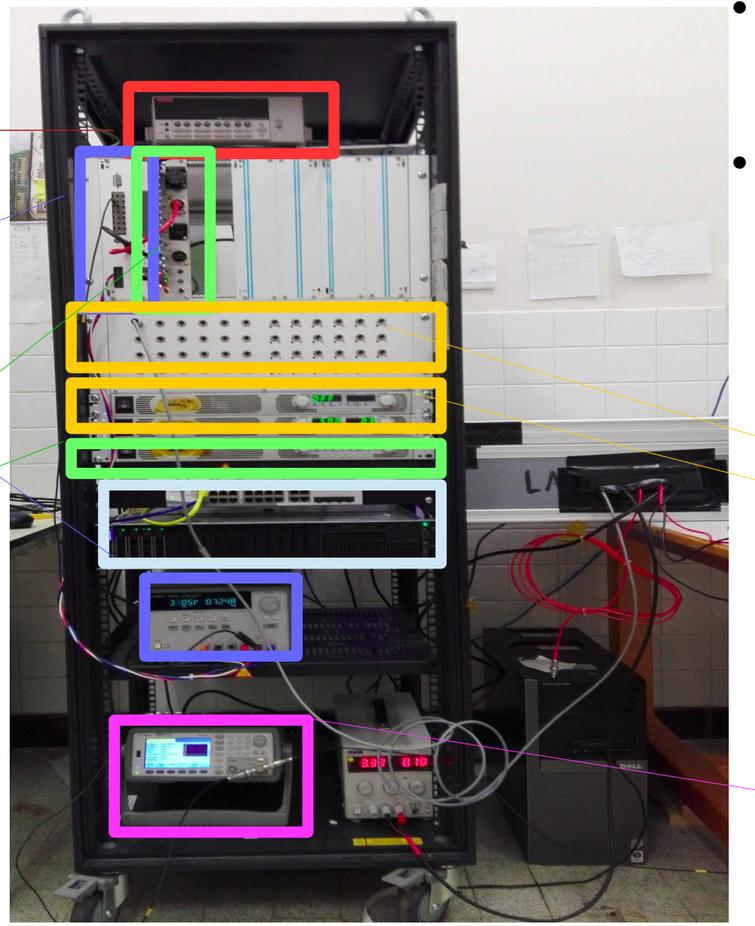
- Check-out with SMBv4 board and existing DIF boards
  - Issues observed during first tests end of March
    - Problems with slow control loading of COB, problems with data r/o of FEV11
    - Headscratching by Remi, Stephane, Jimmy and Adrian didn't lead to a breakthrough
    - Somewhere a devil sits in the system

- Slows down of commissioning and testing before gluing

- Successes with new SL-Board firmware on SC loading for both types of boards gives however confidence that PCBs are technically ok

- The Check-out system is currently the most critical item
  - This is the one that will go to the museum in July

Electronic rack and infrastructure



- New electronic rack set-up at LAL with help of R.Cornat (LPNHE)
  - So far only tested with single slabs.
- It can handle up to:
  - 24 DIF+SMB based slabs.
  - 48 SL-board bases slabs
  - Some combinations: i.e. 12 DIF+SMB + 12 SL-Board based slabs

LV patch panel (LAL Cabling service):

24 for SMB

and 24 for DIFs or SL-boards

“beam” spill generator

To this adds:

- Boxes for HV Distribution and leakage current monitoring
- Cables for “intrastructure” services (LV, HV, signals)

Silicon wafers

- Agreement on TB Preparation Meeting 20/3/19 to start with 1 16x16 wafer/COB and FEV12
- More can be added if results are satisfactory
- Gluing robot at LPNHE is at our disposal
- Need quickly to decide on schedule for wafer gluing (ideally before Easter)

Summary and conclusion

- Test beam preparation in full swing
- COB/FEV12 with SL-Board r/o and FEV13-JP
- Material is available
- Infrastructural components about getting ready
  - Fabrication of mechanical structure about to start
  - Cabling work well in progress (patch panel cabling once mechanical structure is available)
- “ASU Validation bench” (using DIF/SMBv4 system) not operational (critical point at the moment)
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- Need to settle detailed program and shift plans
- Regular beam test preparation meetings (“local” and project-wide)

Backup