KLauS Test & Design

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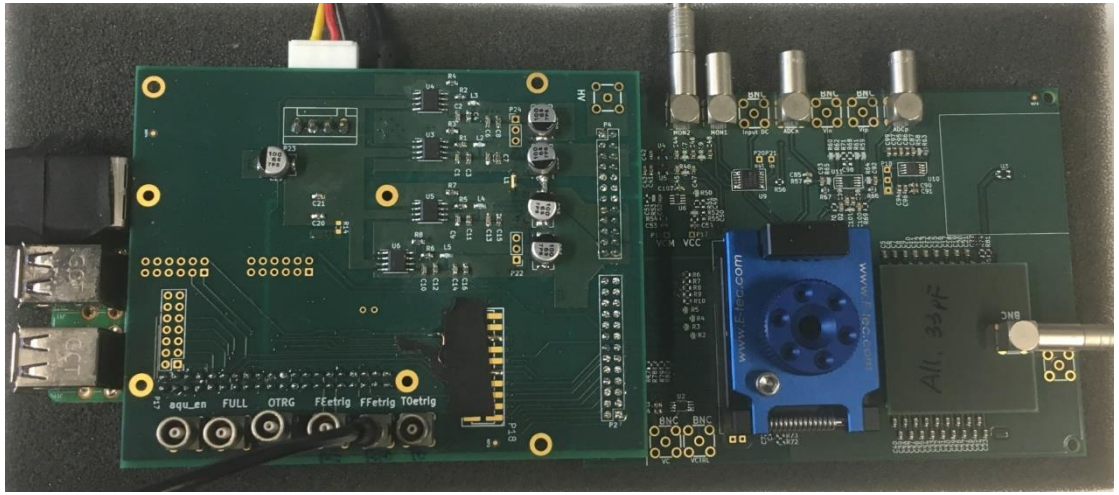
Overview

- **Setup:** raspberry + interface board + testboard + socket

- **Measurement procedure:**
  - **ADC Non-linearity**
  - **Pedestal**
  - **SiPM input bias scan**
  - **Hold delay scan**
  - **Trigger threshold**
  - **Charge integration with auto-trigger**
  - **Others...**

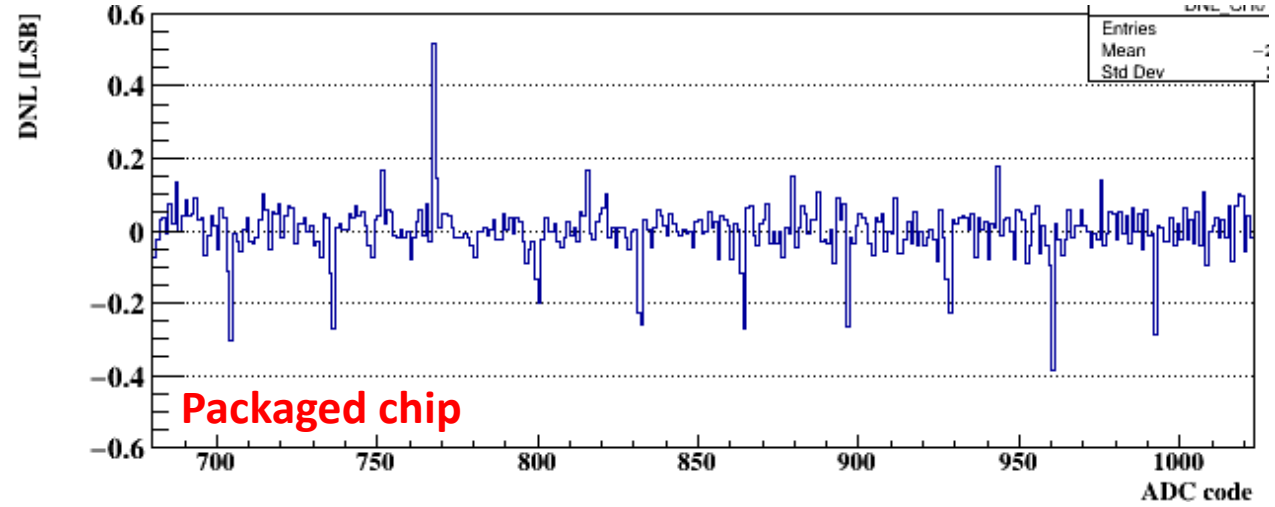


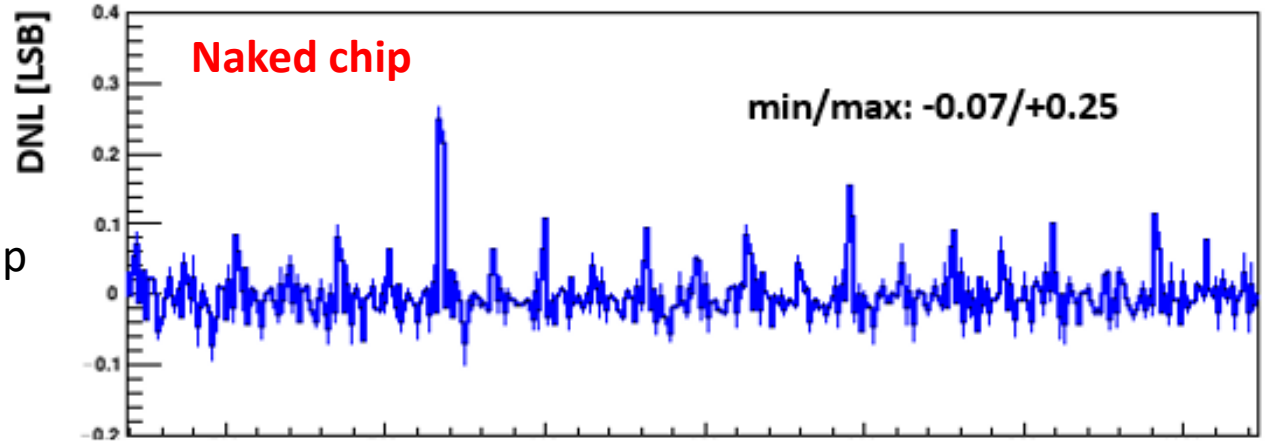
- **3h for the whole test.**

ADC Non-linearity

- **Code density test:**
  - **Ramp signal (0.4-1.7V) to the ADCp**
  - **Archived for calibration usage**

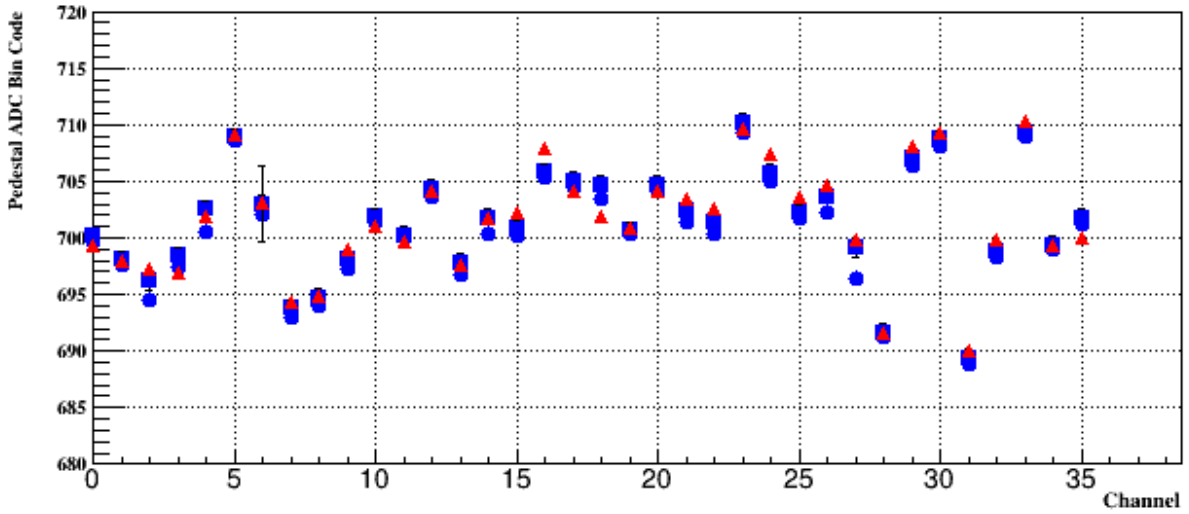
- **Discussion:**
  - **Impossible to do the test on detector, but possible on HBU alone**
  - **INL <1% for all tested channels**
  - **Stable over temperature variation**
  - **Perforance degradation observed**
    - Could be the mechincal stress
    - Observed also after glog-top for naked chip





Pedestal Test

- **Measurement setup:**
  - **ADCp to the front-end output, zero threshold(noise triggerred)**
  - **Archieved for later reference**
- **Discussion:**
  - **Almost the same for different gain branches(and their scales)**
  - **Stable over temperature variations**
  - **BIG variation among channels**



Pedestal Test

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  - **ADCp to the front-end output, zero threshold(noise triggerred)**
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- **Discussion:**
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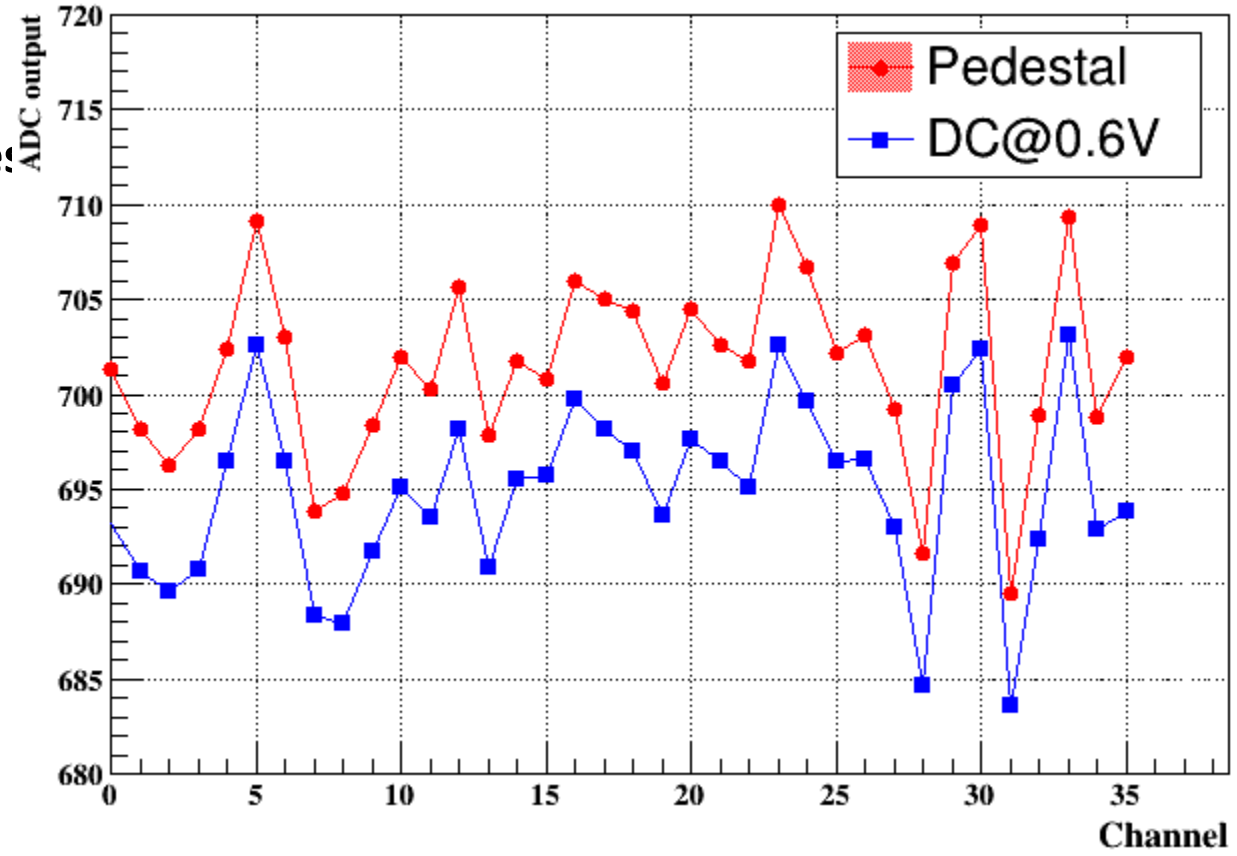
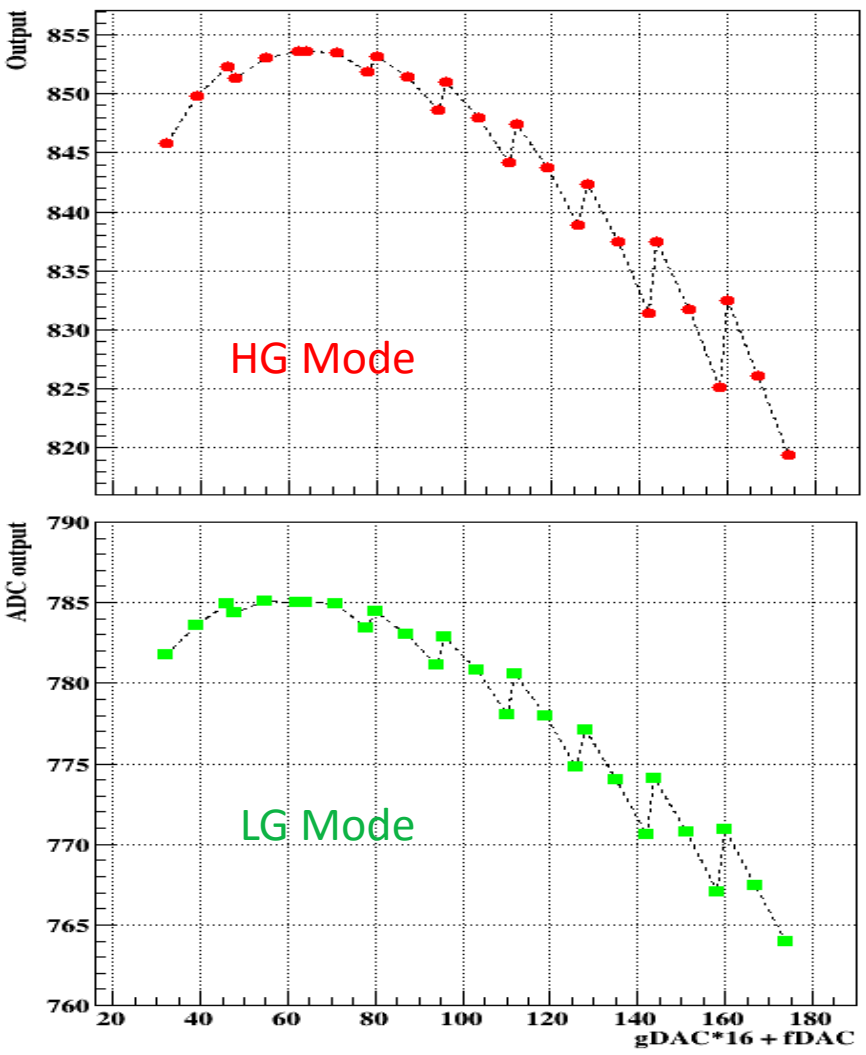
  - **Stable over temperature variations**
  - **BIG variation among channels**
    - Most comes from the ADC comparator
    - Will be re-designed for KLauS6



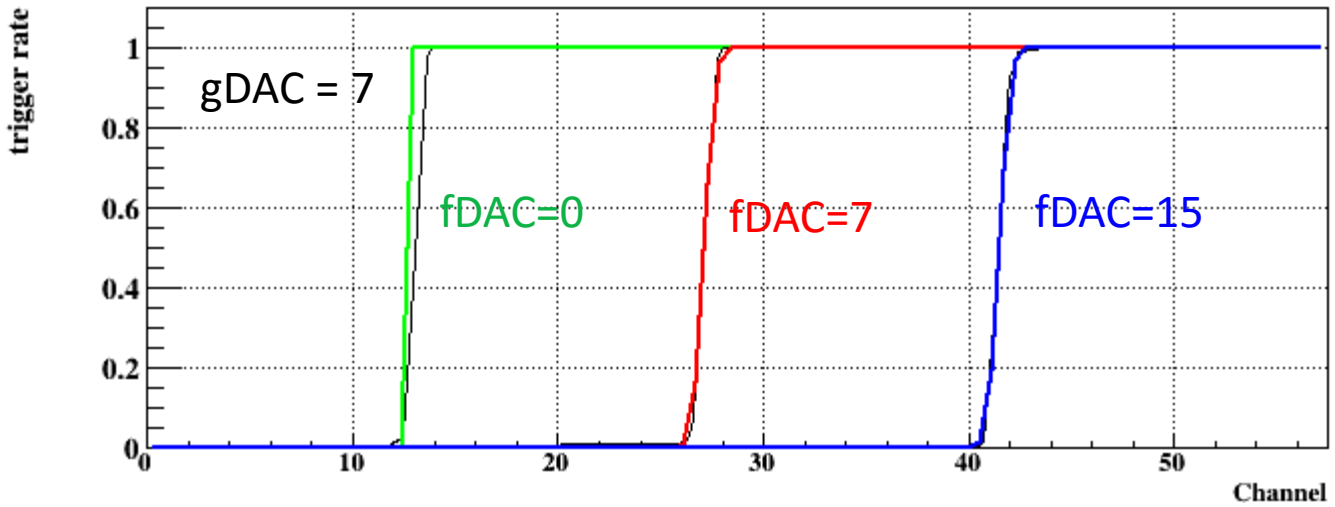
Hold-delay scan

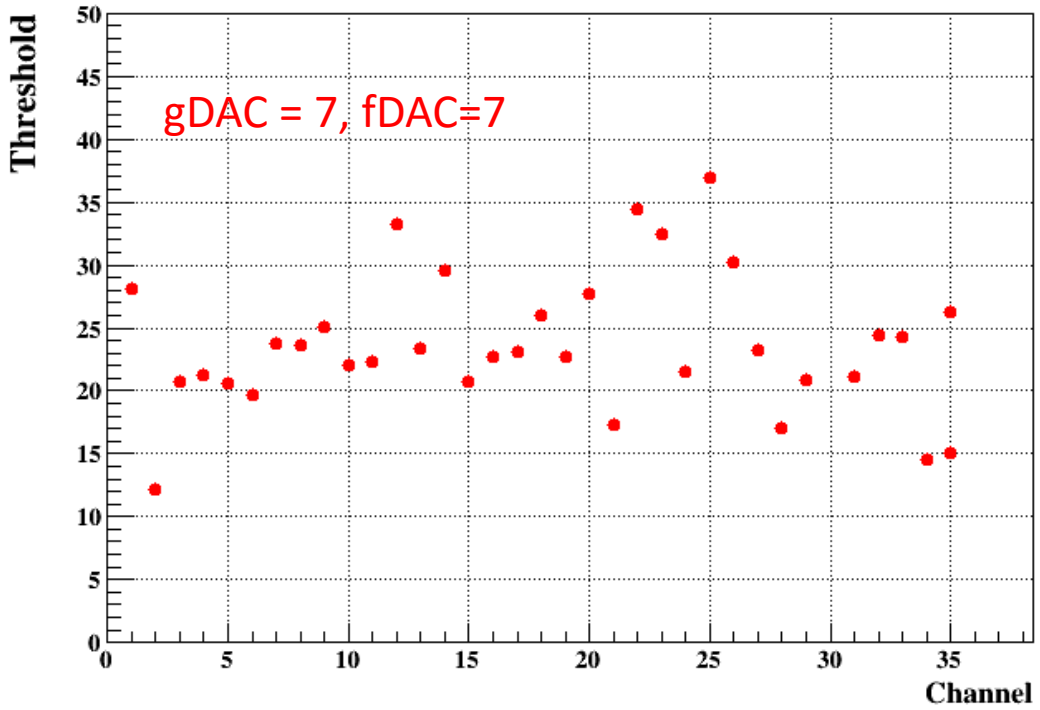
- **Charge injection test:**
  - **Fixed large signal injected**
  - **different DAC setting (gDAC+fDAC)**
- **Discussion:**
  - **Possible to characterize on HBU**
  - **Same „correct“ DAC setting for HG/LG branch**
  - **Variations among the „correct“ setting is not a big issue**



Trigger threshold

- **Charge injection test:**
  - **Charge scan to find the threshold level**
  - **Different DAC setting(gDAC + fDAC)**
- **Discussion:**
  - **Better to characterize it with SiPM**
  - **Large variation, can be tuned by fDAC**

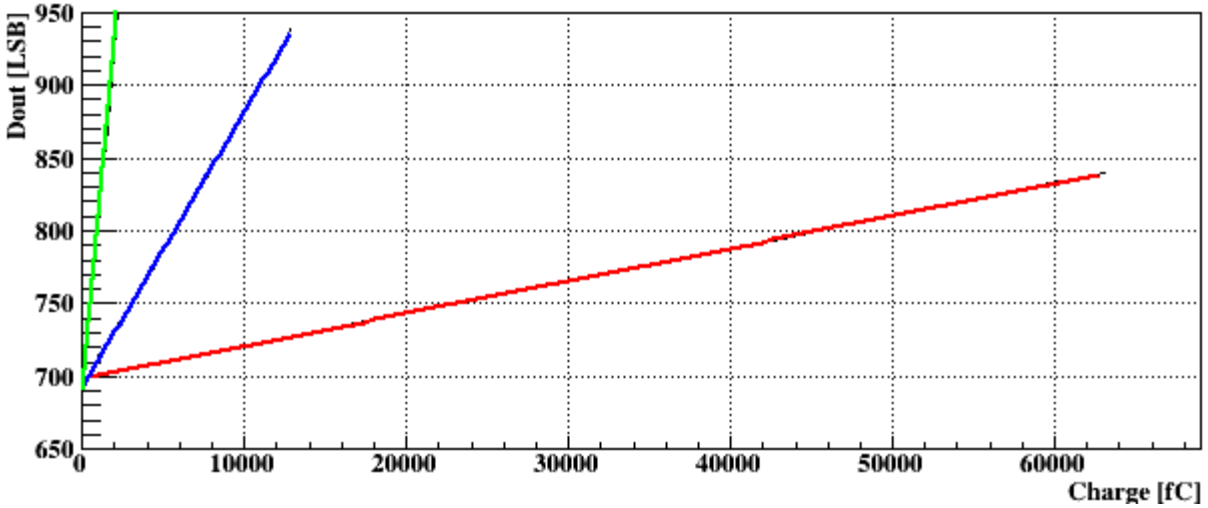


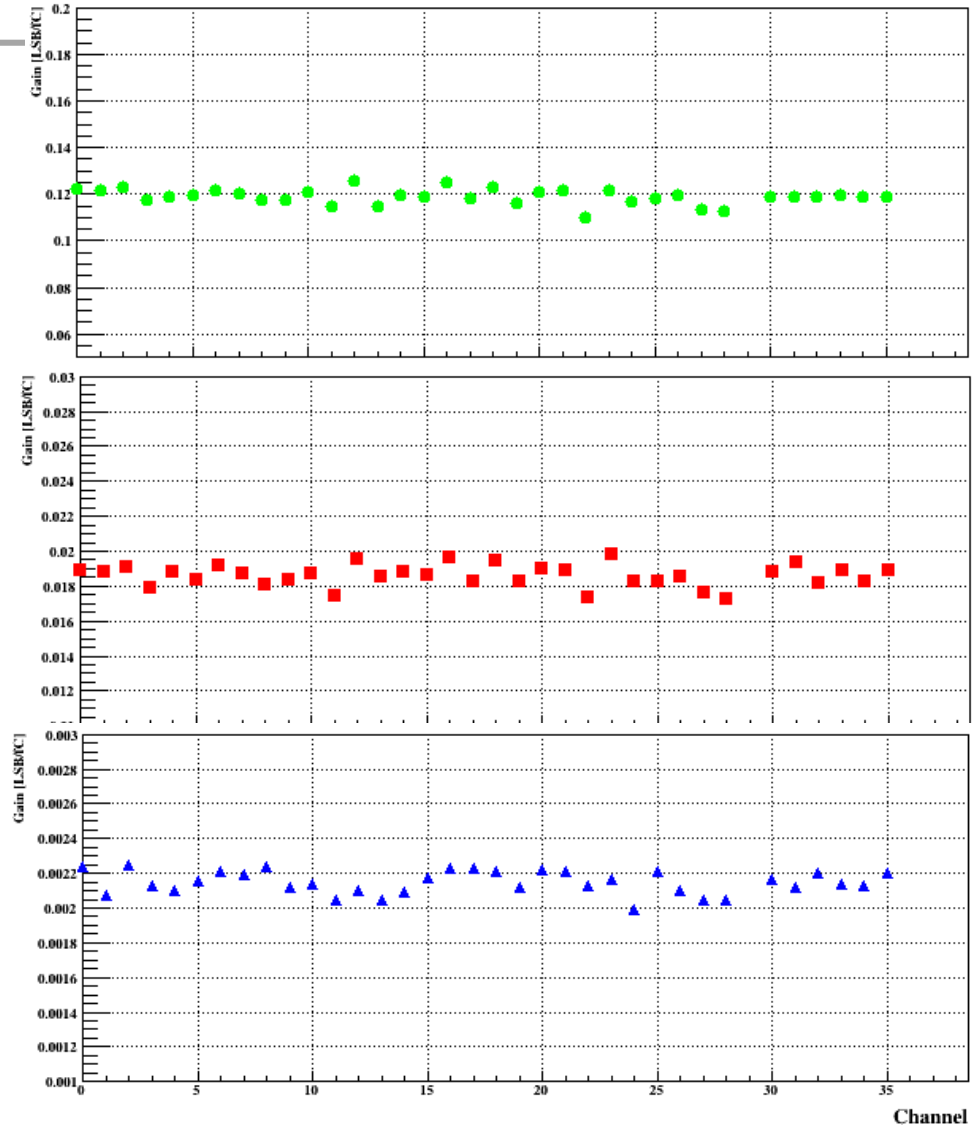


Charge scan

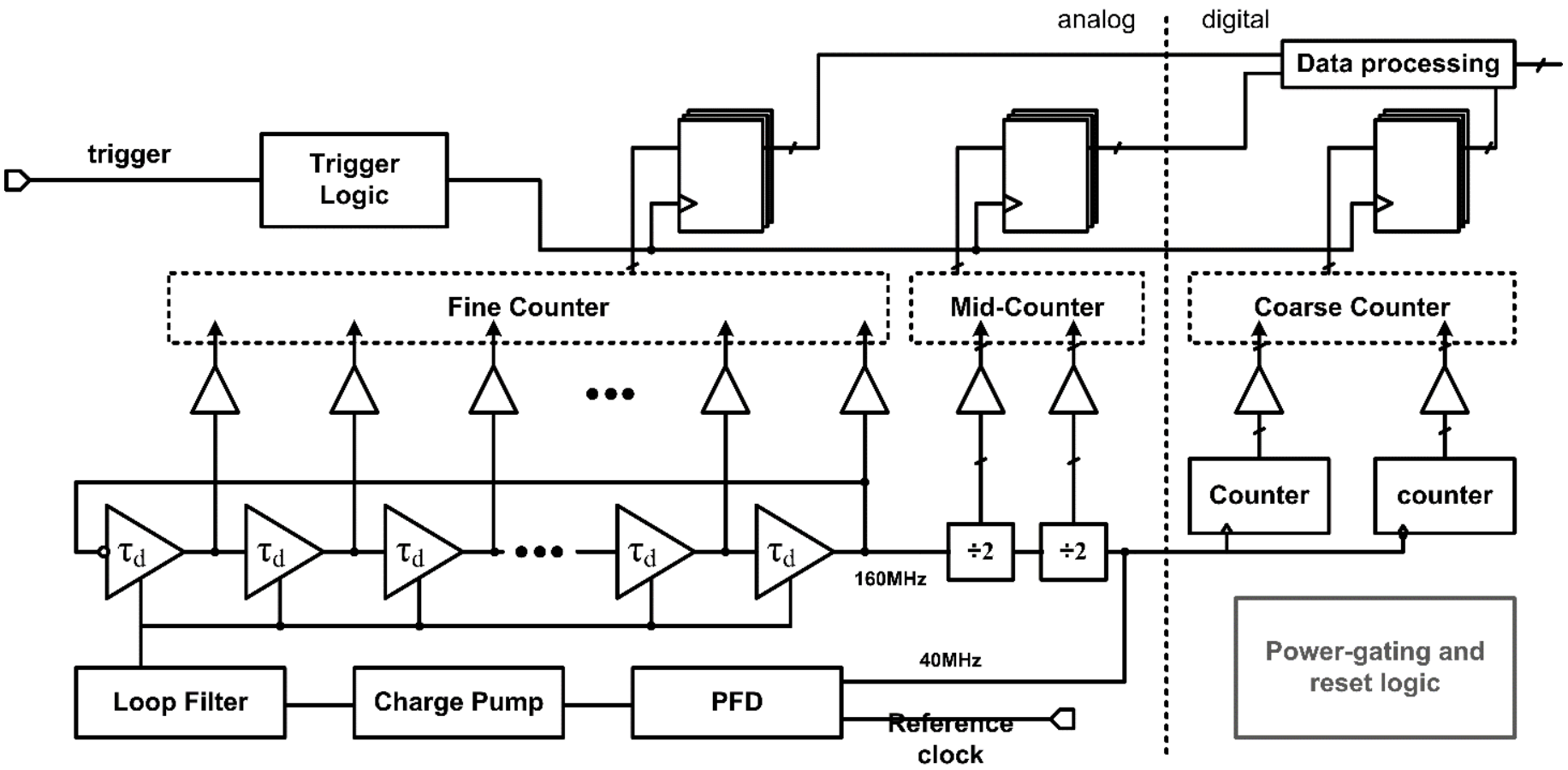
- **Charge injection test:**
  - **Charge scan, 20 points for each channel and gain scale**

- **Discussion:**
  - **Impossible to characterize on HBU**
  - **10% variation among channels**





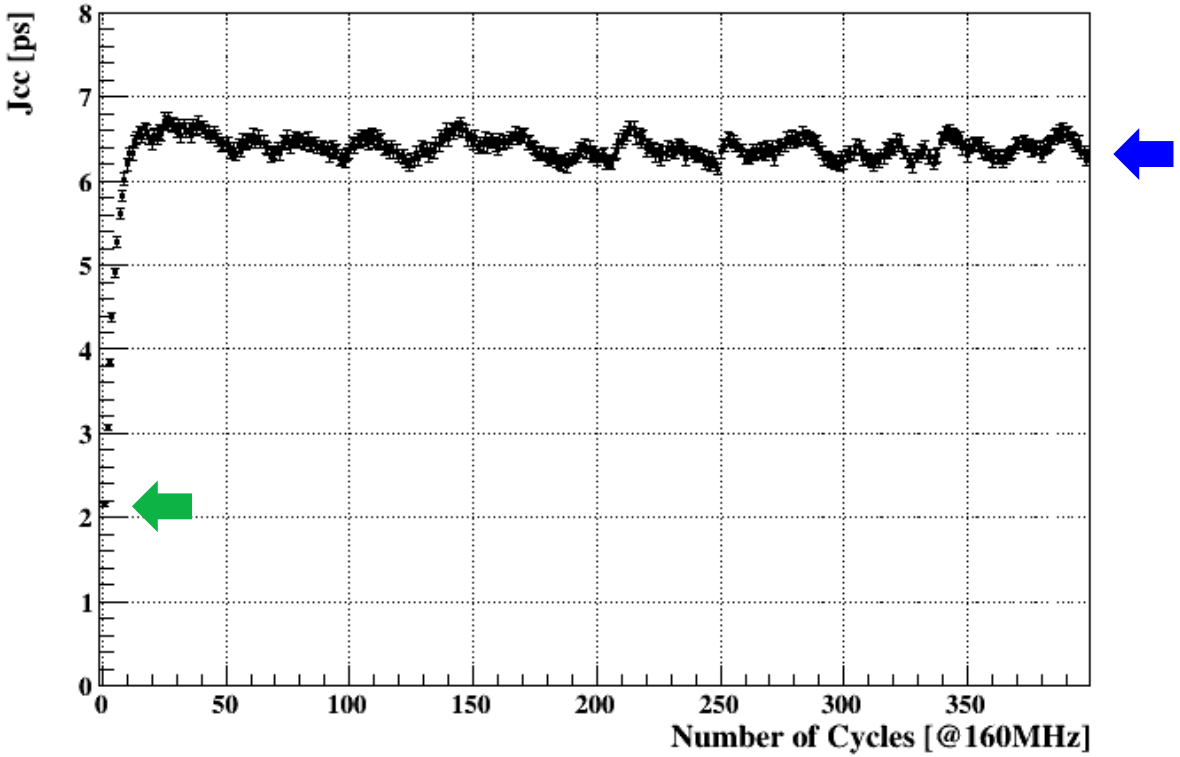
KLauS PLL-based TDC Strucutre

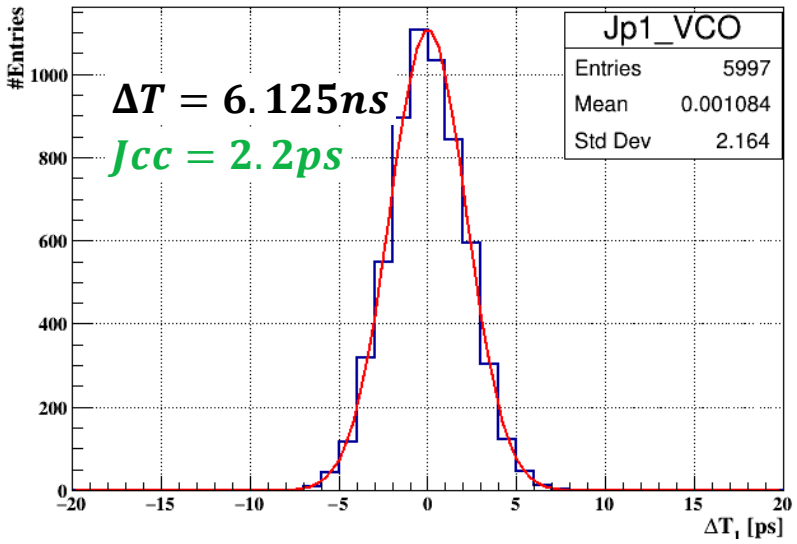


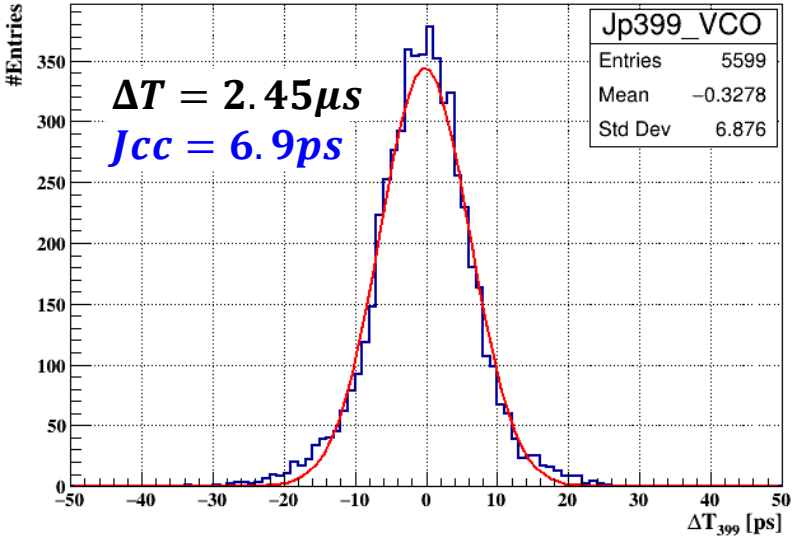
- **Stable**
- **Fast lock < 5us**
- Power consumption:
  - VCO: 2.3mA
  - Buffers: 3.6mA
  - Latches: no DC power
  - Others: 0.6mA
  - Total: 6.5mA
  - 0.35mW/Ch
- **< 2μW/Ch (0.5%PP)**

Simulation results

- **Cycle-to-Cycle Jitter is more interesting to us**
  - **Depends on the loop bandwidth, ideal input clock assumed**
  - **Latch noise also contributes to jitter**
  - **Input reference clock also contributes to jitter**

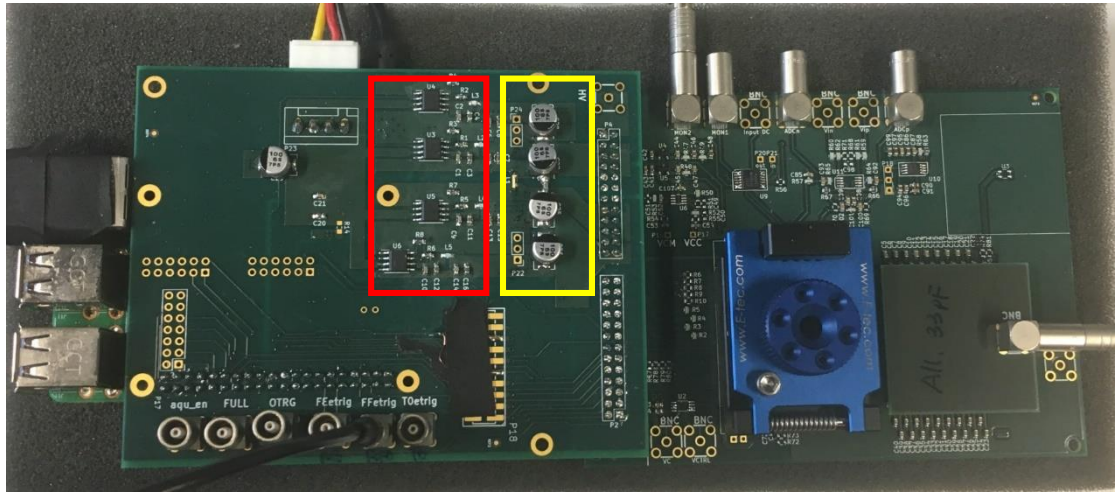






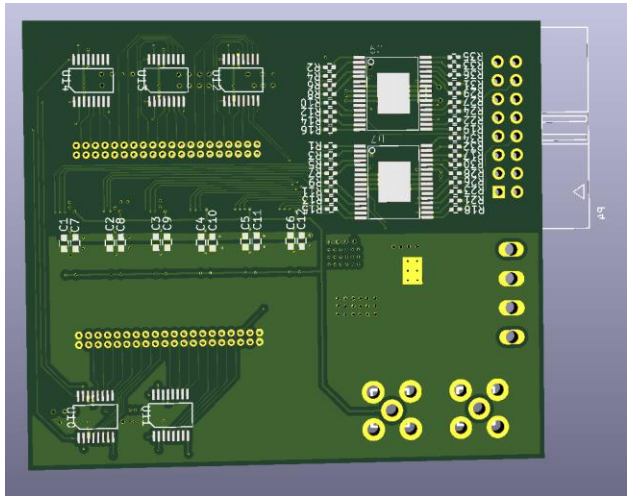
Status report

- **49 chips received, 10 tested**
  - **8 chips working**
  - **1 chip with power problem**
  - **1 chip broken**



- **SiPM input bias scan**

- **Socket issue - Solved**
- **Power issue - Big capacitor needed**



- **The submission for the KlauS6 delayed**
  - **Digital design flow changed**
  - **Changes in front-end according to the uniformity test**

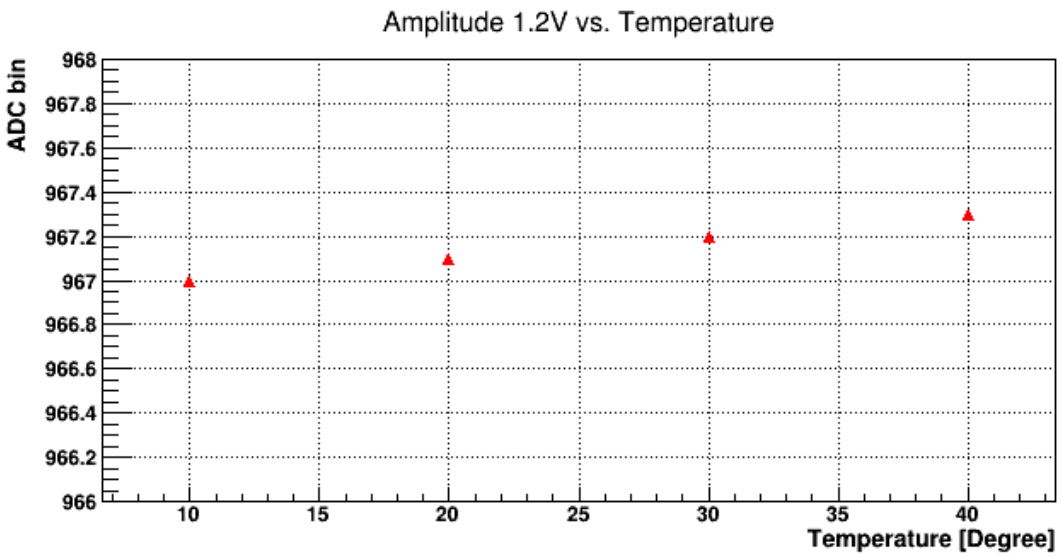
Summary

- **Uniformity test for the BGA packaged chip**

- **The submission for the KlauS6 delayed**
  - **Digital design flow changed**
  - **Changes in front-end according to the uniformity test**

ADC @ different temperature

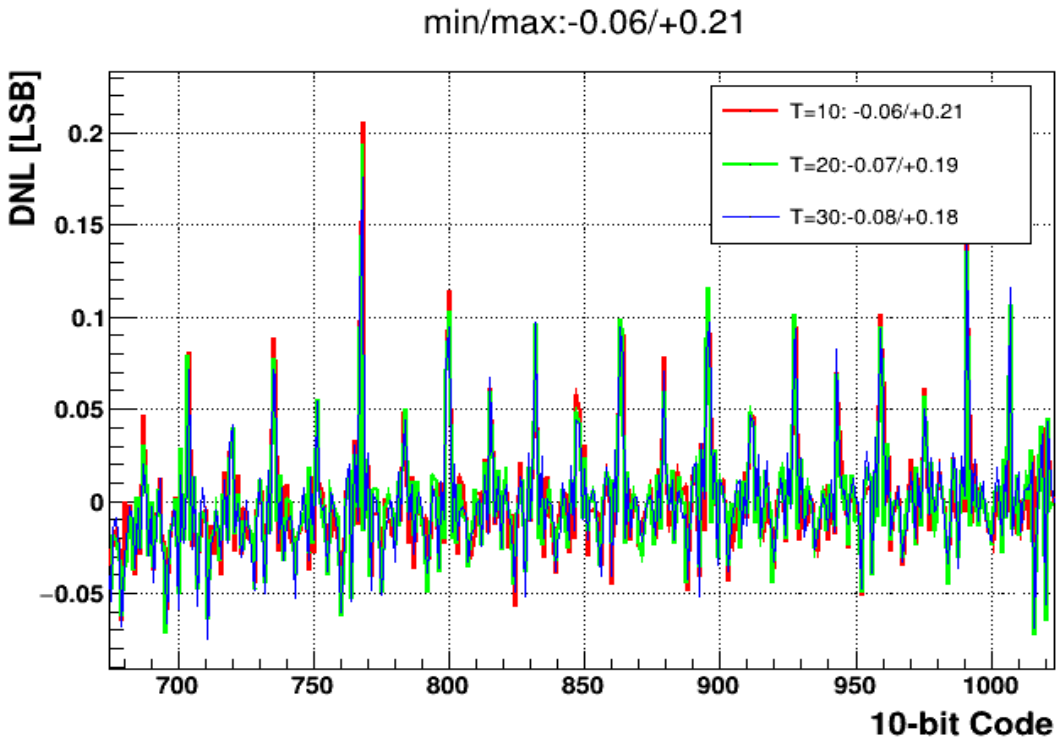
- **AD conversion @ fixed DC input**



No big changes in ADC alone.

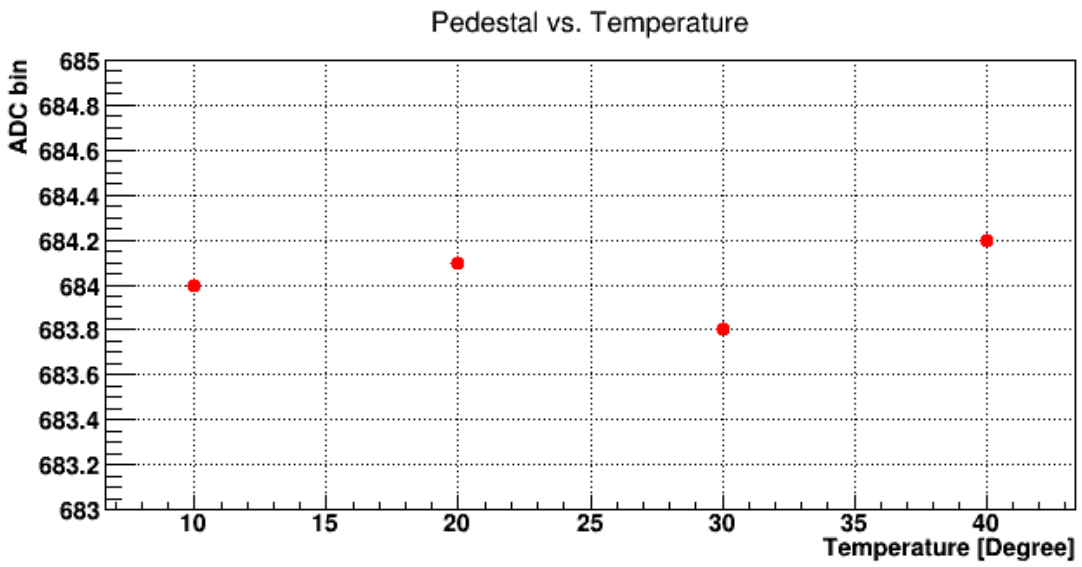
Expected: performance determined by the mismatches between capacitors.

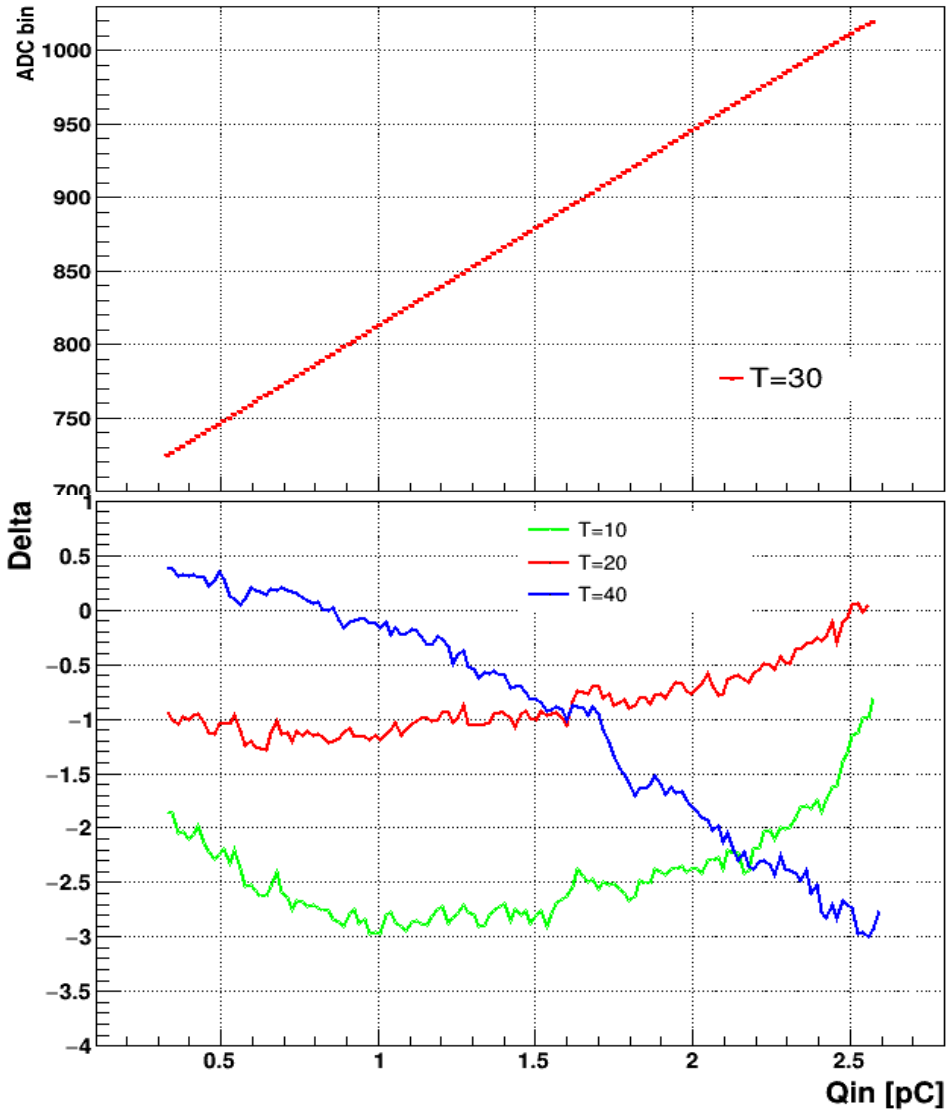
- Differential Non-Linearity (ROI)



Fullchain charge injection @ different temperature

- **Input SiPM bias: doesn't change**
- **Front-end Pedestal: no big change**
- **Charge injection:**
  - **For the working range 20-40°C, delta < 3 bin, within 1% FSR.**





Fullchain @ fixed charge injection

- **Close look at fixed charge injection with pulse reconstruction**
  - **Hold-delay contributes: 0.4ns/°C**
  - **Peak time no changes, but peak height changes around 1bin/°C**