Status of Cooling Studies for CEPC Calorimeters

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CEPC – 100km

CEPC: Higgs Factory @ 240 GeV and Z factory @ 91 GeV

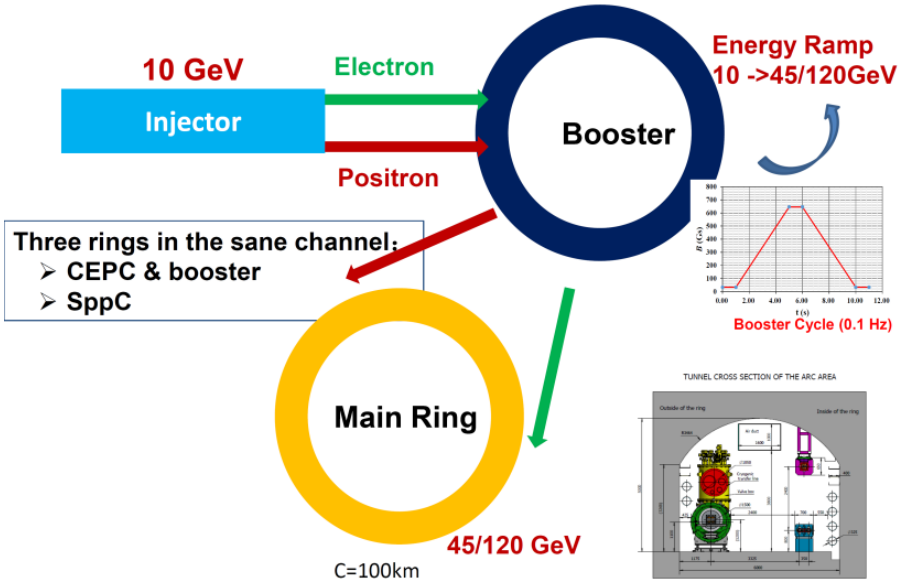
Precision measurement of the Higgs boson and the Z boson

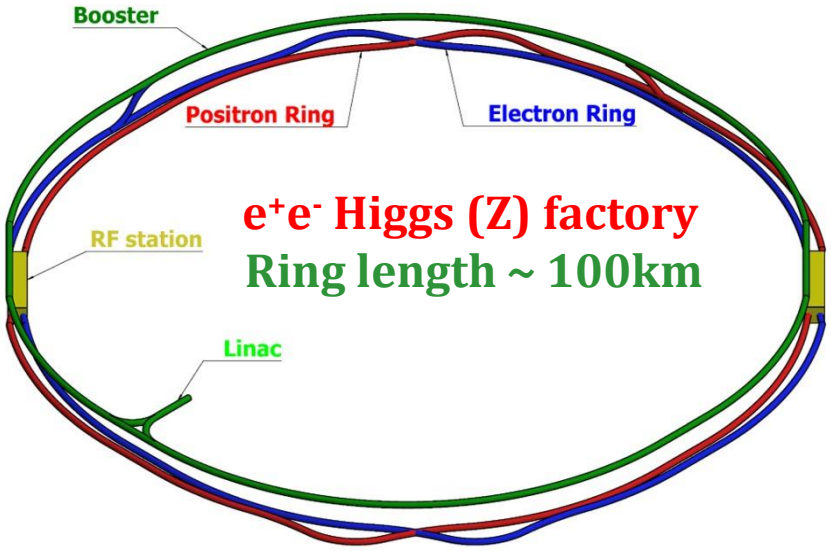
Upgradable to pp collision with $E_{cm} \approx$ 50-100 TeV

Lumi.	Higgs	WW	Z
$\times 10^{34}$	2.93	11.5	16.6

➔ CEPC bunch spacing is 690/210/25ns for H/W/Z runs, respectively

➔ CEPC Operating at continuous mode

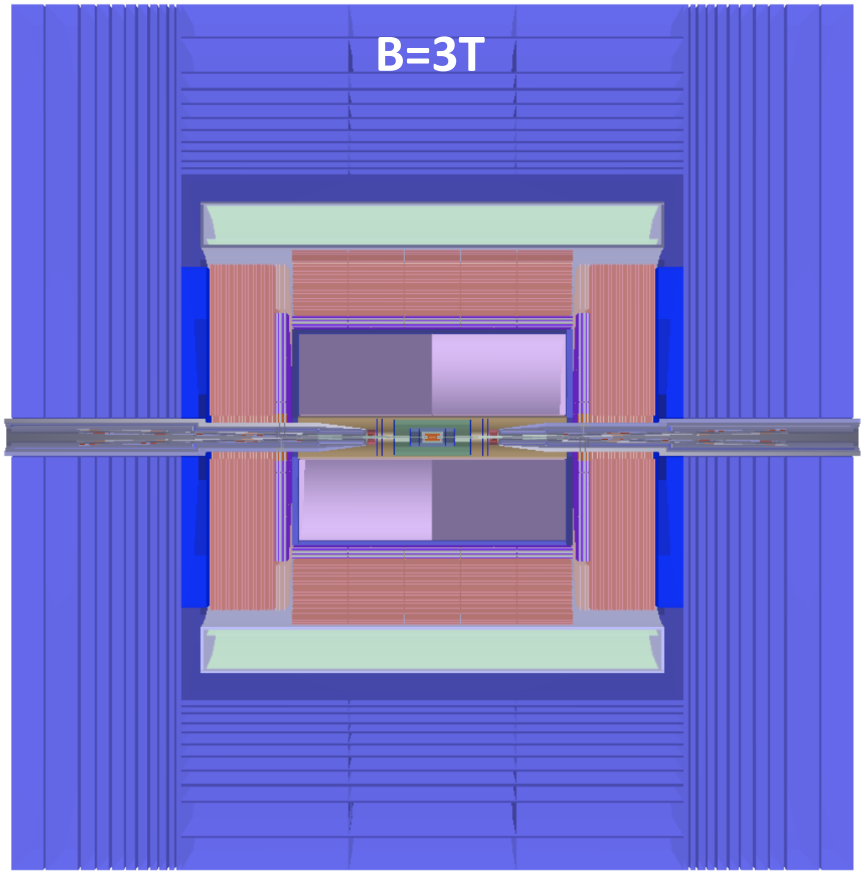




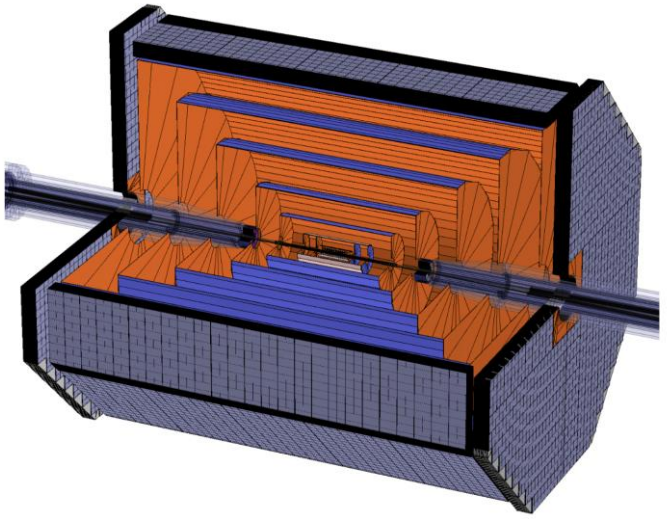
Schematic of CEPC Detectors

Baseline : PFA approach (ILD-like)

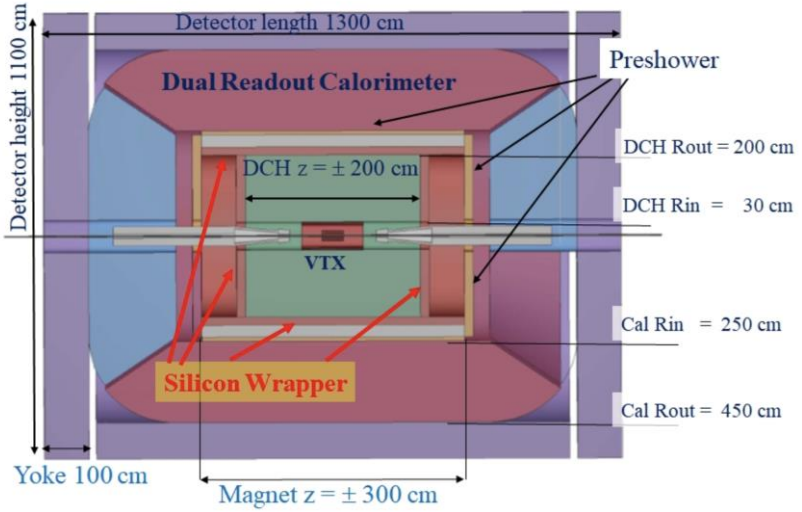
Silicon + TPC + ECAL&HCAL + Muon



Full Silicon Tracker

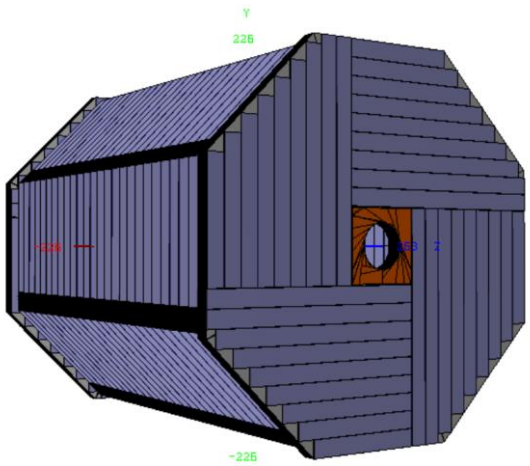


Dual Readout

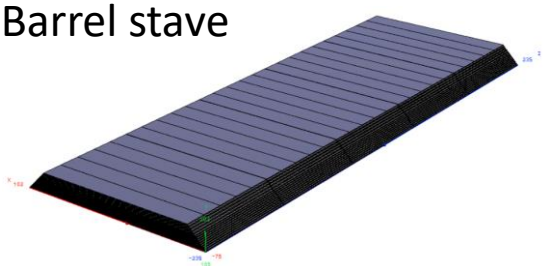


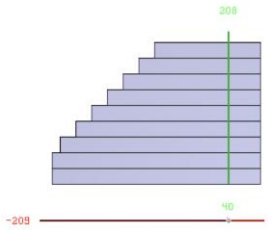
ECAL Layout and Structure

- One cylindrical barrel + two disk-like endcaps
- ~2 m in radius, and ~5.3 m long (Z direction).
- 8 barrel sections: 1 section → 8 staves, 1 stave → 5 modules,
  1 module → 5 columns
- Each endcap → 4 quadrants, 1 quadrant → 9 columns
- Column: slabs integrated into supporting structures
- Best possible hermeticity and minimum crack regions



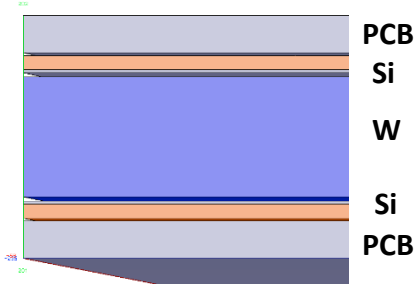
Barrel stave





Endcap quadrant

Slab

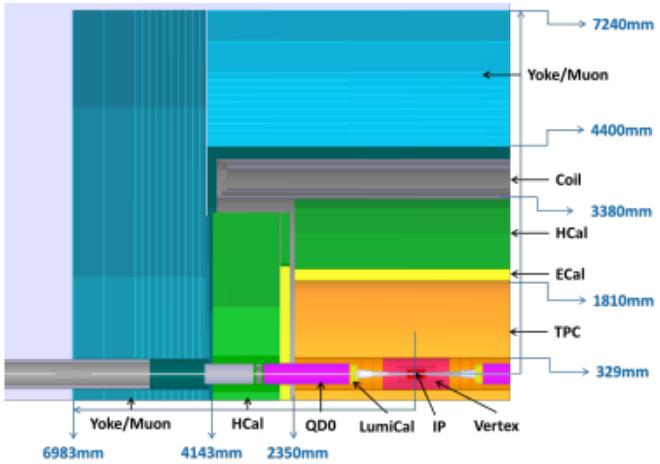


ECAL Channel Count, Power Consumption

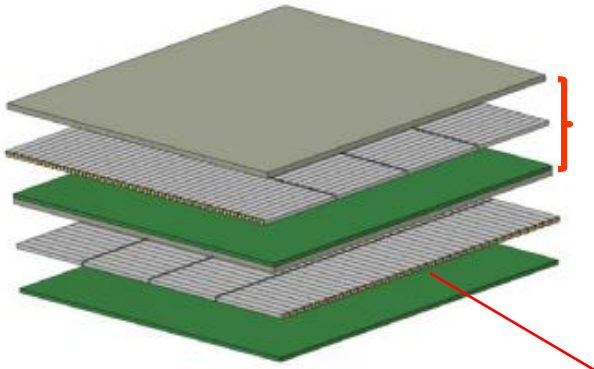
- Numbers of channels
  - **17.3 M for barrel, 7.43 M for endcaps**
- Total power consumption: 146 kW
  - **124 kW (5mW/ch, SKIROC)**
  - **22 kW (9mW/DIF/m^2 × 2400m^2)**
- Active cooling is likely required
- Passive cooling might be possible with a reduced number of channels

  ➔ **larger cell-size (degrade PFA performance?)**

ECAL Model Structure (ScW)



One quarter of CEPC-v1 detector concept



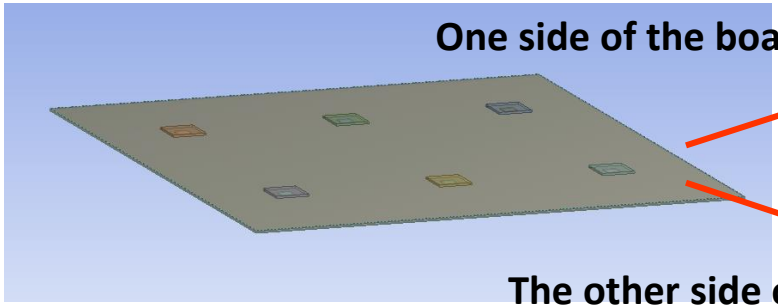
Sandwich Structure

30 layers in total

For each layer:

Tungsten (2.8mm)+
PSD (2mm)+
PCB+ASIC (3.1mm)
SPIROC2B

The First Step

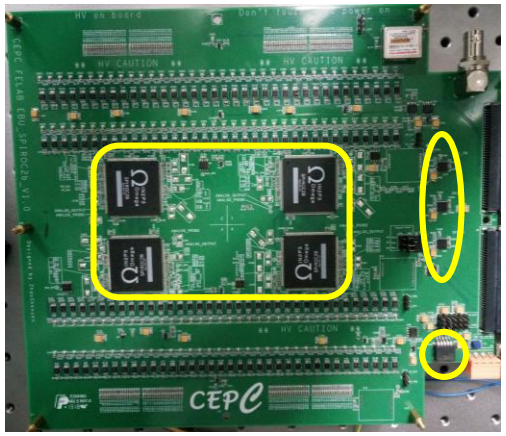


One side of the board: Chips, LDO etc.

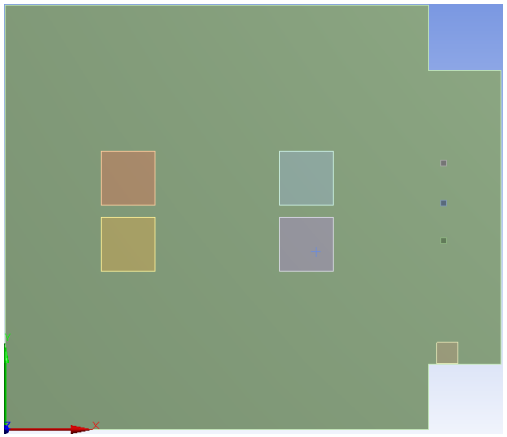
The other side of the board: Temperature-sensitive electronic equipment.

Simulation vs Experimental Setup

USTC+SJTU



Sample Board



Model

Thermal Conductivity:

$$\text{Silicon(Ch ips)}: 148\text{W}\cdot m^{-1}\cdot C^{-1}$$

$$\text{FR-4}: 0.294W\cdot m^{-1}\cdot C^{-1}$$

$$\text{Copper}: 401W\cdot m^{-1}\cdot C^{-1}$$

Specific Heat:

$$\text{Silicon(Ch ips)}: 712J\cdot kg^{-1}\cdot C^{-1}$$

$$FR-4: 1150J\cdot kg^{-1}\cdot C^{-1}$$

$$\text{Copper}: 385J\cdot kg^{-1}\cdot C^{-1}$$

Default Analysis settings

Convection: Stagnant Air

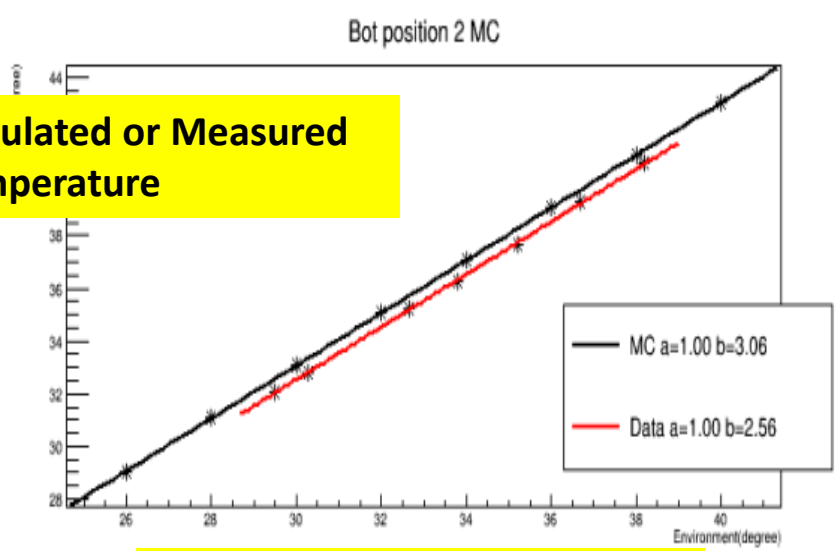
Film coefficient: $5e-06W/mm^2\cdot{}^{\circ}C$

5~25 for Natural flowing air

- ✓ Environment temperature changes from 26 to 40 by 2 degrees
- ✓ Define chip side as top side and scintillator side as bottom side.
- ✓ Put 9 sensors on each side and 2 sensors for the environment temperature.

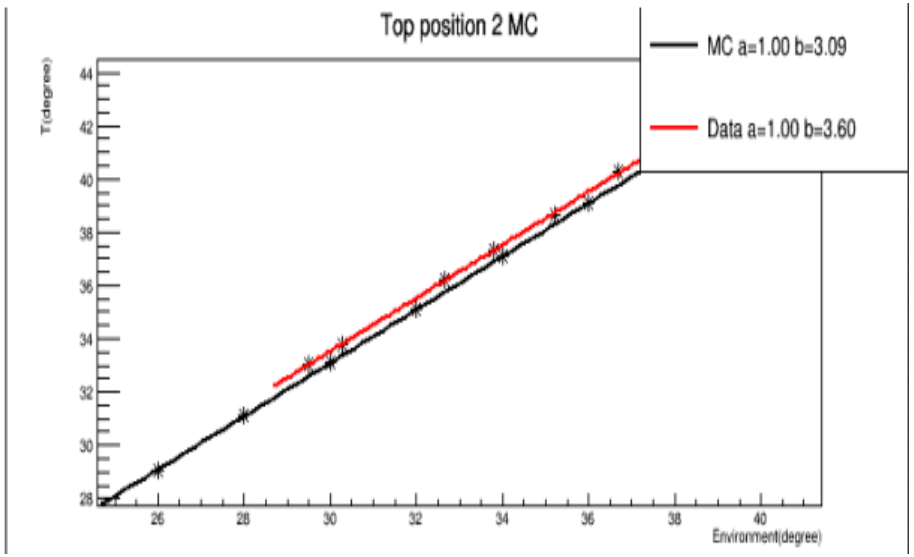
Simulation vs Measured: 4-chip PCB

USTC+SJTU

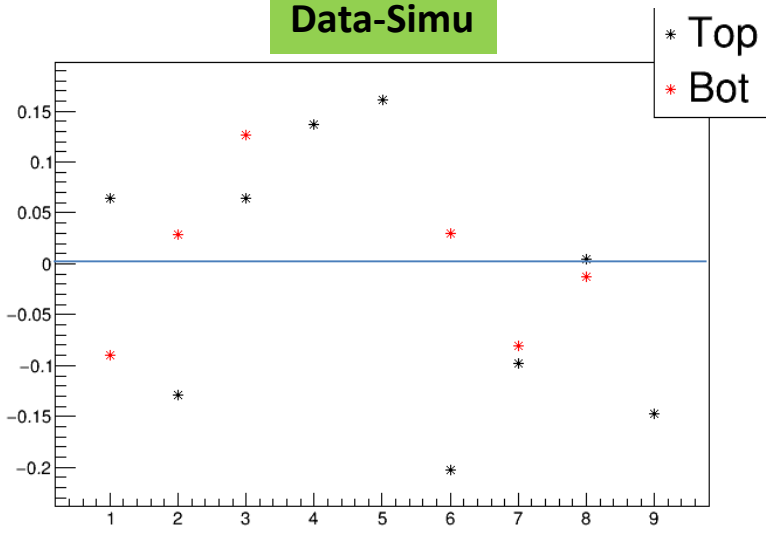


Simulated or Measured Temperature

Temperature of environment



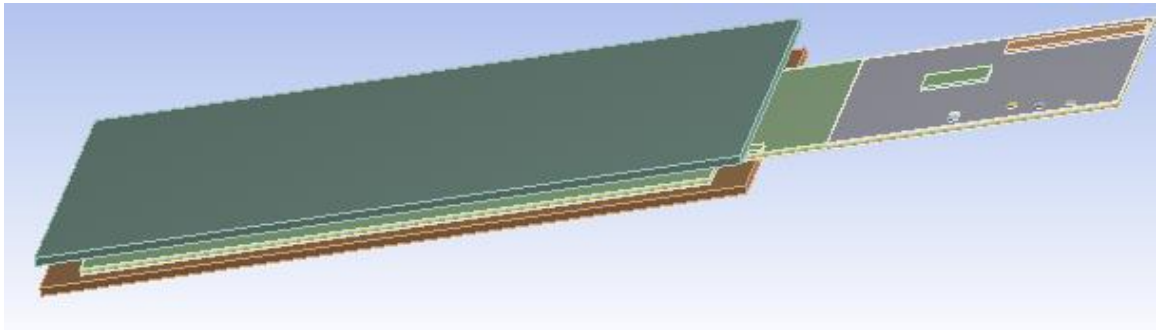
Data-Simu



- Measured results has a good agreement with simulation results
- Take advantage of the good linearity to do the temperature reconstruction
- Small difference between simulation and measured temperatures

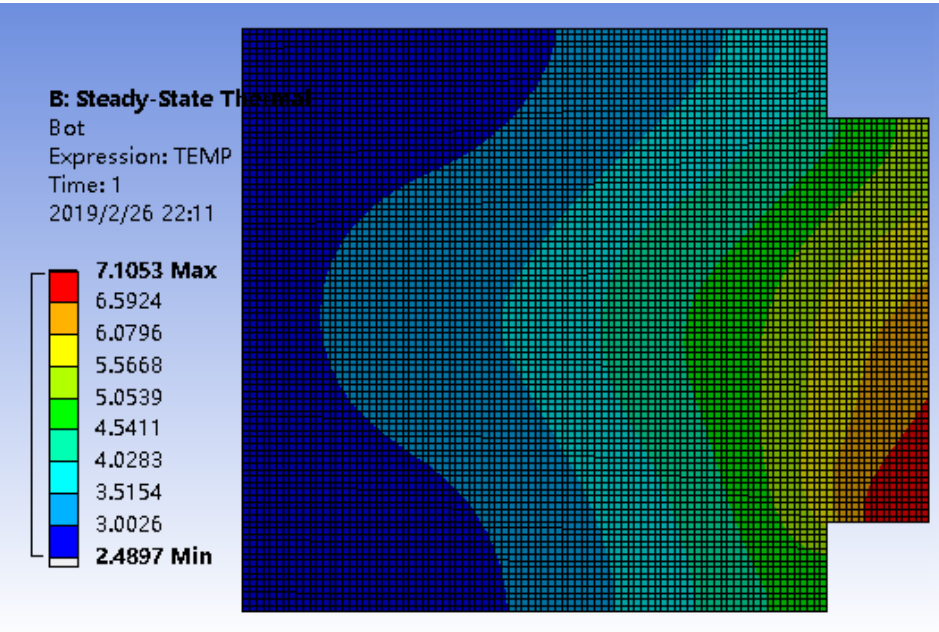
Simulation of Double W + PCB

USTC+SJTU



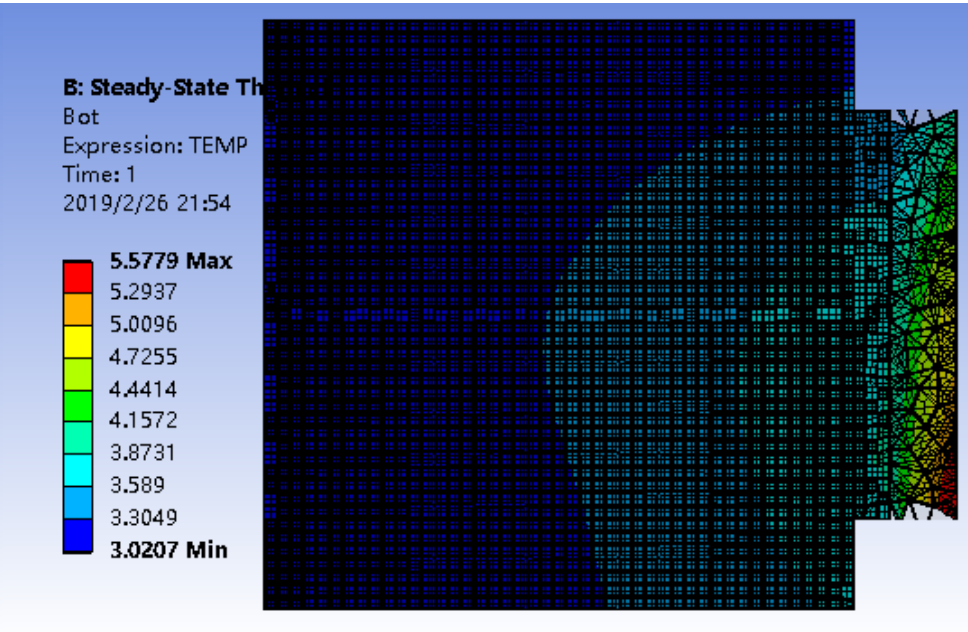
Two tungsten plates (2.8mm) are put on the top and the bottom side

Standalone



Temperature: 2.5-7.1 ℃

Double Tungsten



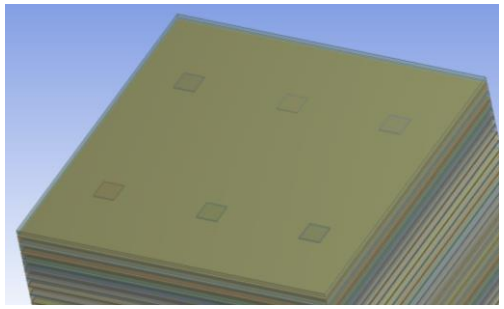
Temperature: 3.0-5.6 ℃

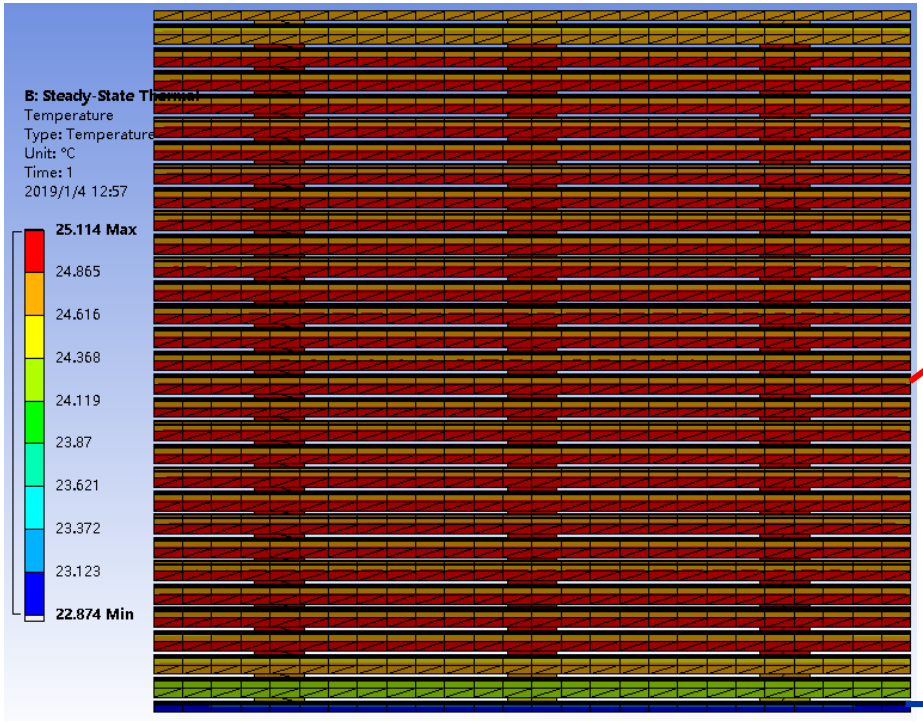
Ambient Temperature: 0 ℃

30-Layer with 6-chip PCB

USTC+SJTU

- Simulation of a 30-Layer model with ScW
- Only 6-chip on each layer's PCB (Polystyrene)
- Due to the influence of adjacent layers, middle layers have higher temperature.

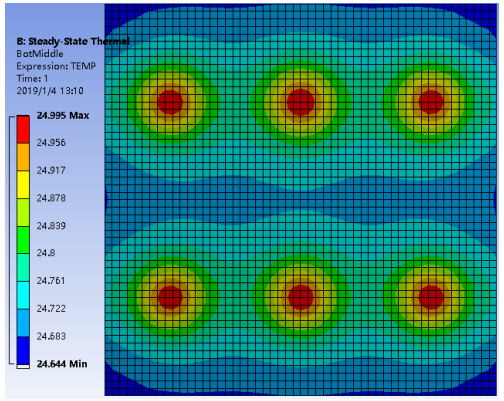




24.99 ℃

Layer15

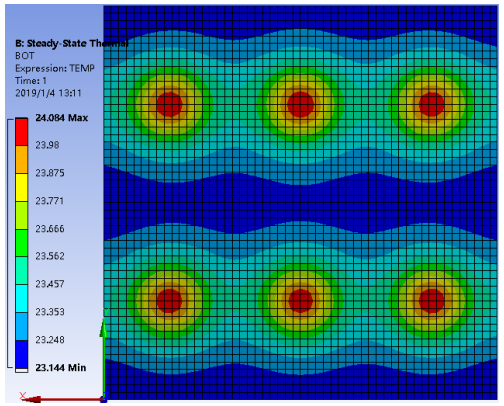
24.64 ℃



24.08 ℃

Layer1

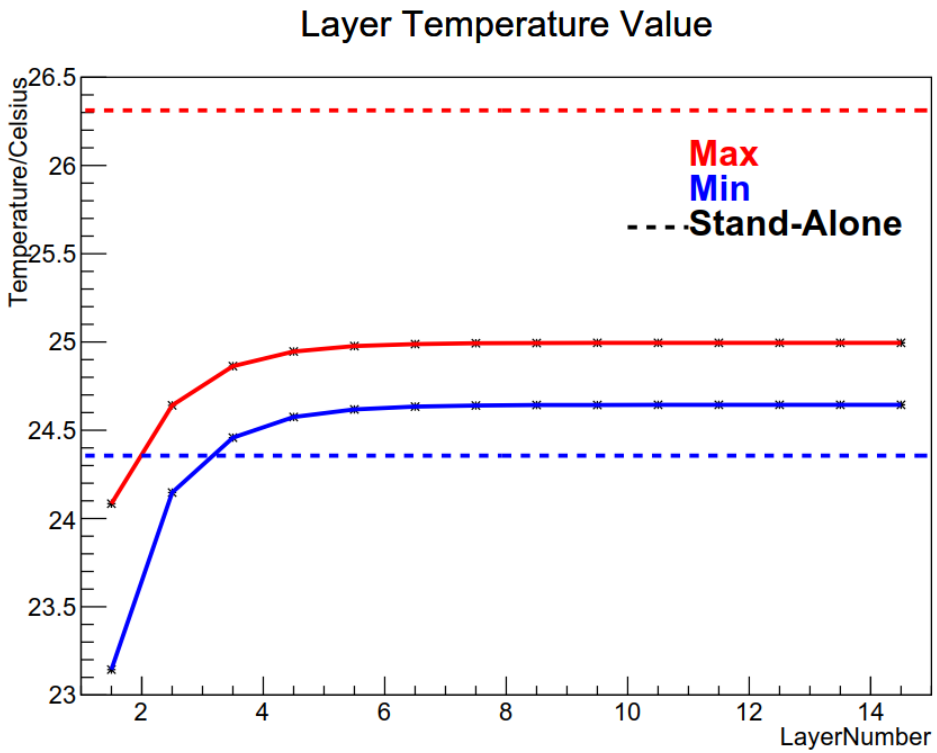
23.14 ℃

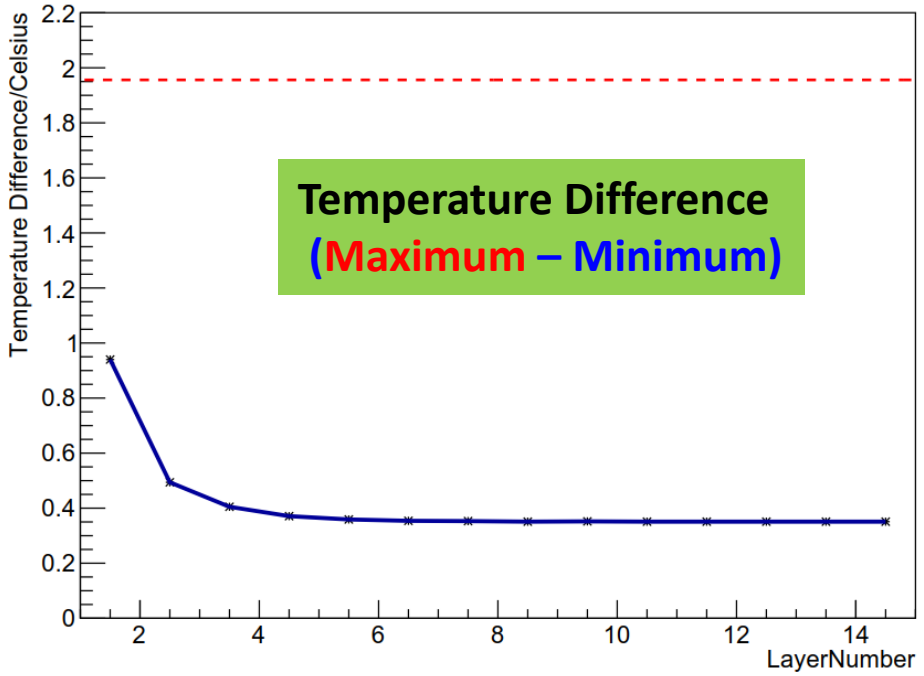


Ambient Temperature:22℃

Temperature vs Layer

USTC+SJTU



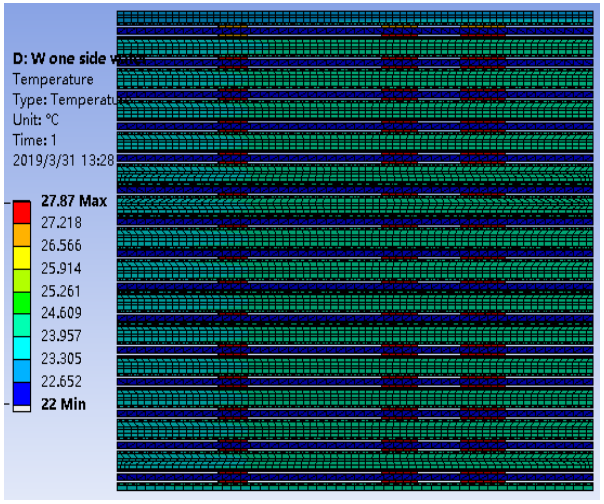


- Due to the influence of adjacent layers, middle layers have higher temperature than layers in the front or end. Temp in the middle part keeps stable.
- With absorbers, the model has a better thermal conductivity, it results in a temperature difference value which is lower than that in a stand-alone PCB.

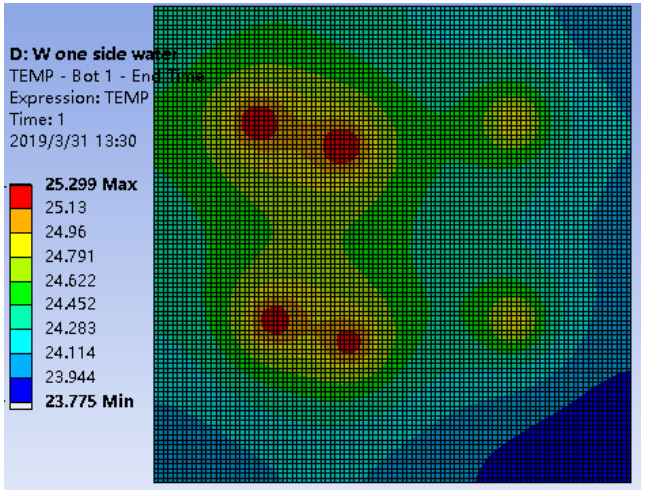
30-Layer With Water Cooling

USTC+SJTU

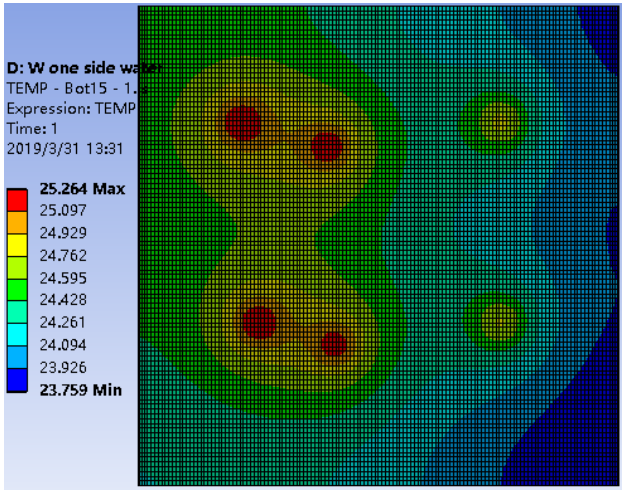
- Test a model with one side of PCB in touch with water
- SIMPLIFIED case in touch with OPEN domain.
- Film coefficient between model and water is 1200 W/(m^2 ^{0}C)
- The domain has a constant temperature value so the flow velocity is not taken into account.



Water Temperature: 22℃



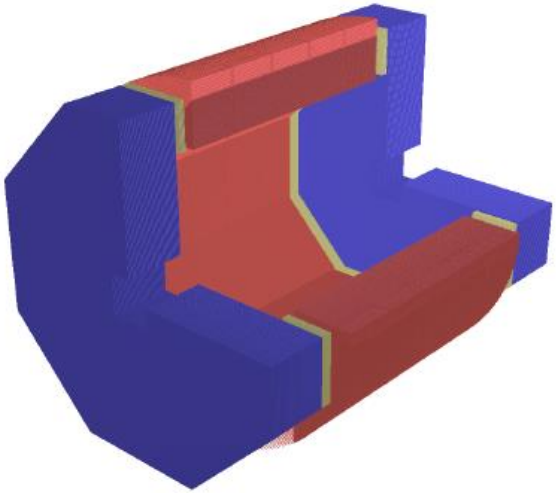
Layer 1

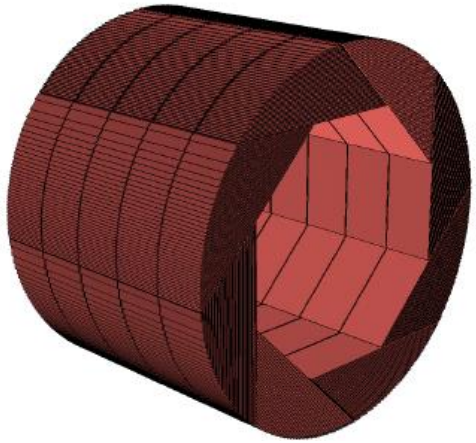


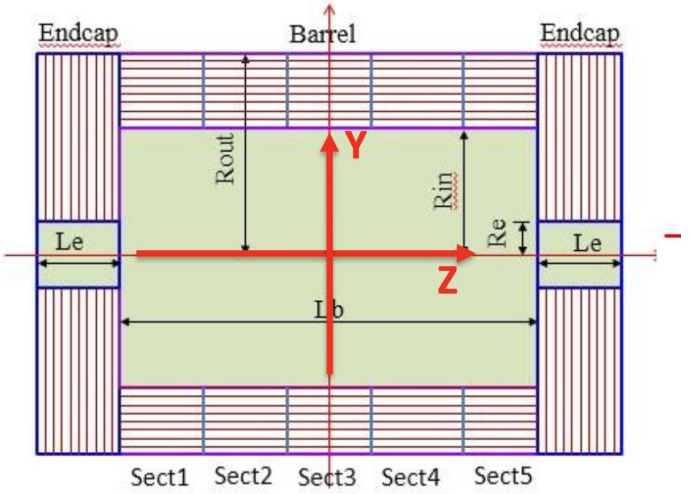
Layer 15

HCAL: Geometry and Layout

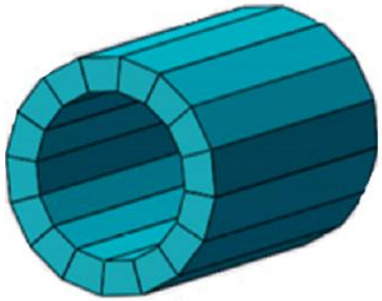
SDHCAL

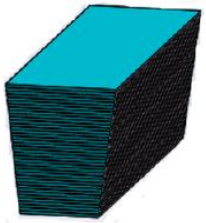


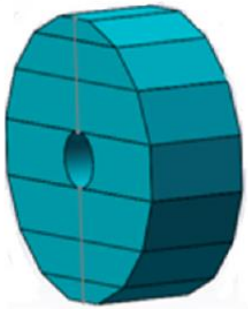




AHCAL







- Inner radius in X-Y plane R_{in} = 2300mm
- Outer radius R_{out} = 3340mm
- Inner & outer of HCAL endcap in Z-axis are 2670mm and 3710mm

HCAL Channel Counts, Power Consumption

- HCAL Barrel, R_{in} = 2.3m, R_{out} = 3.34m, length = 2.67*2=5.34m, N_{layer}=40

  Area of HCAL barrel = $2*PI*[(R_{in}+R_{out})/2]*L*N_{layer}$ = 3782 m^2

- HCAL Endcap (2), R_{in} = 0.35m, R_{out} = 3.34m, N_{layer}=40

  Area of HCAL endcap = $2*PI*(R_{out}*R_{out} - R_{in}*R_{in})*N_{layer}$ = 2772 m^2

Cell Size \ channels	HCAL Barrel	HCAL Endcap	Channels (N_{ch})	Power AHCAL	Power SDHCAL
1cm x 1cm	**37.82M**	**27.72M**	**65.5M**		**101 kW**
2cm x 2cm	9.455M	6.93M	16.4M		52 kW
3cm x 3cm	**4.2M**	**3.08M**	**7.3M**	**110 kW**	**43 kW**
4cm x 4cm	2.36M	1.73M	4.1M	88 kW	
5cm x 5cm	1.51M	1.11M	2.6M	77 kW	

Power Consumption (rough estimation):

AHCAL: 7mW/ch * N_{ch3} + 9W/DIF/m^2 * 6554 (59kW)

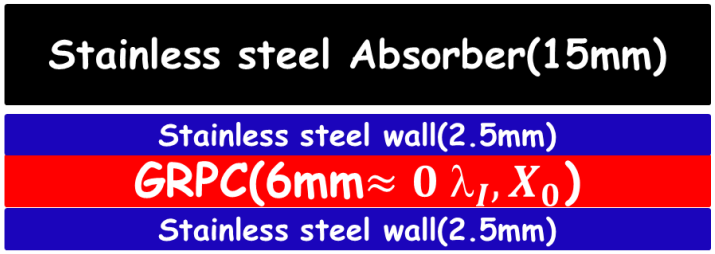
SDHCAL: 1mW/ch * N_{ch1} + 5.4W/DIF/m^2 * 6554 (35.4kW)

Active cooling is likely needed.

Electronics channels / m²

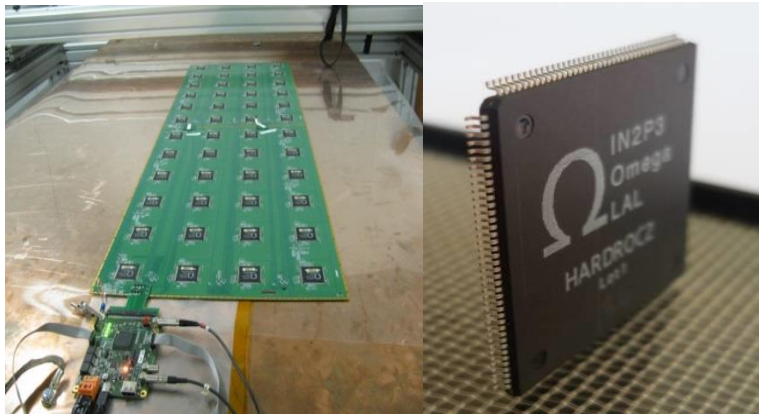
IPNL

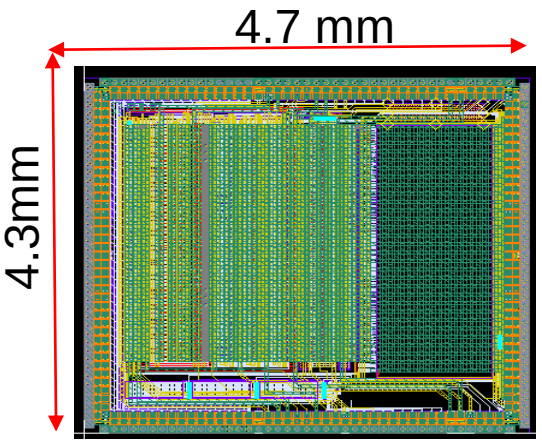
$(0.12\lambda_I, 1.14X_0)$

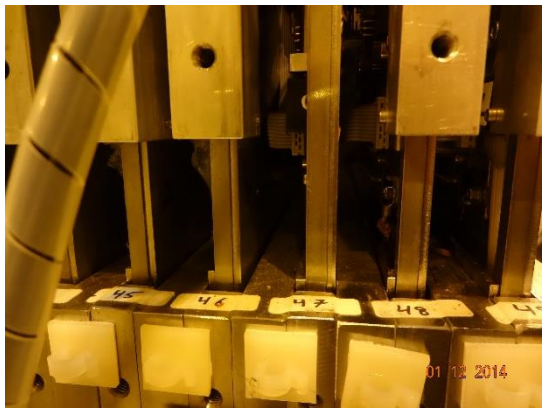


- SDHCAL for CEPC has 40 layers
- Each layer: 3 mm RPC
  + 1.2 ~ 1.4 mm PCB
  + 1.6 mm ASIC (Hardroc)
- 20mm steel absorber (2.5+2.5+15mm)

- 6 PCB to cover 1m² RPC
- Each PCB size: 31 cm * 50cm ~ 1536 channels
- ASIC chip (Hardroc) has 64 channels, 4.3mm*4.7mm, cover (5cm*6cm)
- Each PCB with 1536-channel needs 24 ASIC chips (4*6)
- Power: 1mW/ch * 64 ch = 964 mW/Chip
- Power: 1mW/ch * 6*24*64 ch = 1mW/ch*9216ch/m² = 9.2W/m²







PCB with ASICs

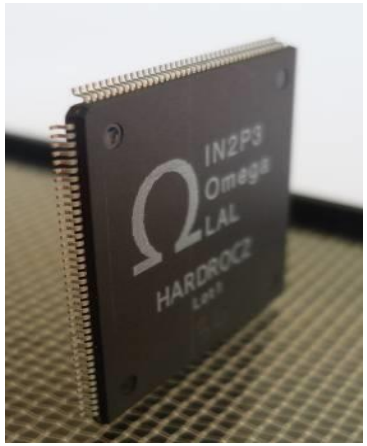
IPNL

- ➔ Each PCB size: 31 cm * 50cm
- ➔ 24 ASIC * 64 ch = 1536 ch
- ➔ 6 PCB to cover 1m^2 RPC
- ➔ Each PCB has 24 ASICs and 1536-ch

Model Geometry: PCB

IPNL+SJTU

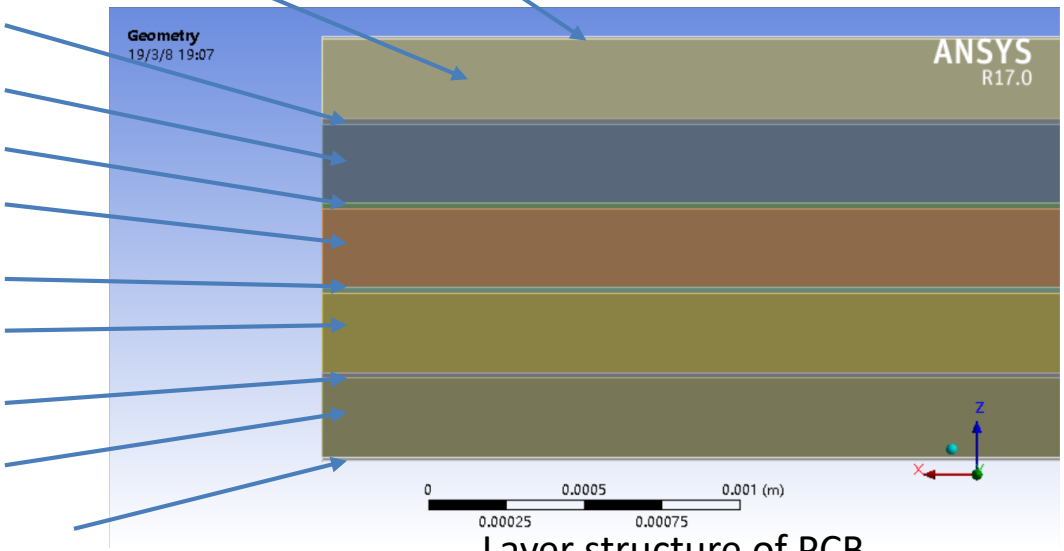
11-layer PCB, thickness 1.36mm:
5 layers FR-4, 6 layers copper



HARDROC2 ASIC:
- cover **2.8cm×2.8cm**
- chip **4.7mm×4.3mm**
- power: **64mW/chip**

From top to bottom are:

1 0.333oz copper(11.667microns)
2 10mil FR-4(250microns)
3 0.5oz copper
4 10mil FR-4
5 0.5oz copper
6 10mil FR-4
7 0.5oz copper
8 10mil FR-4
9 0.5oz copper
10 10mil FR-4
11 0.333oz copper



Layer structure of PCB

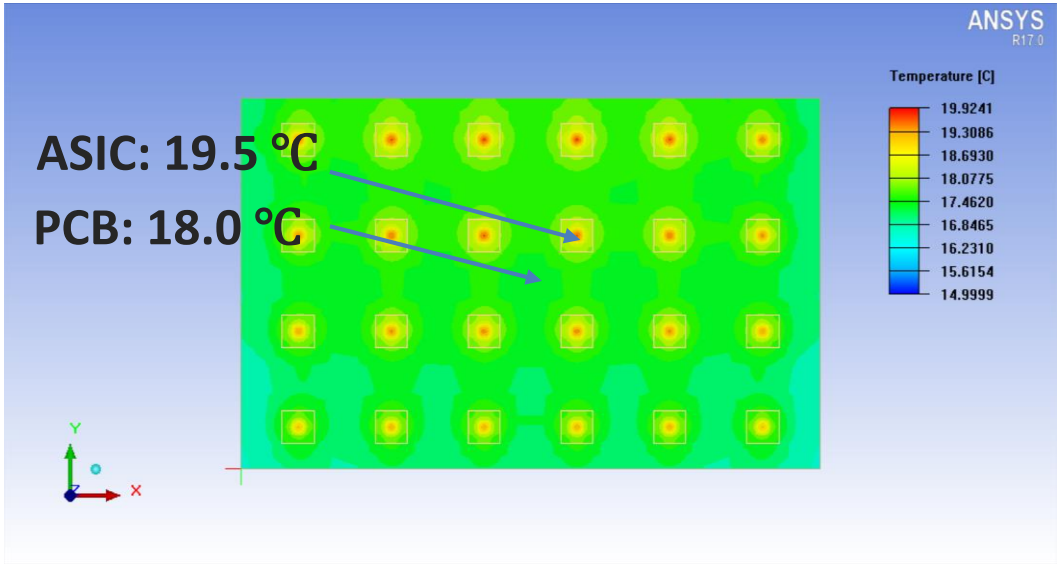
Simulation vs Measurements

IPNL+SJTU

Temperature Simulation:

- PCB+ASIC: 18 – 19.5 ℃
- ΔT: 1.5℃

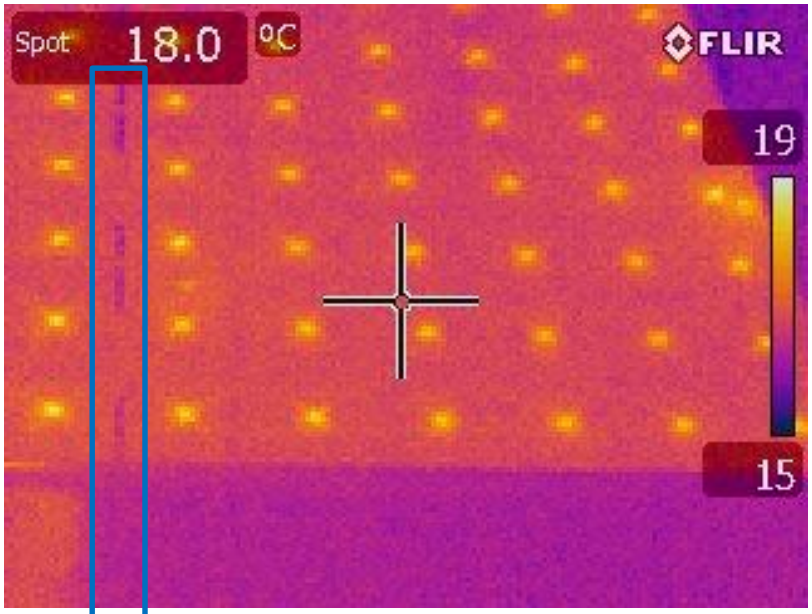
Simulation at SJTU



Temperature Measurements:

- PCB+ASIC: 18 – 19 ℃
- ΔT: 1.0 ℃

Measured at IPNL

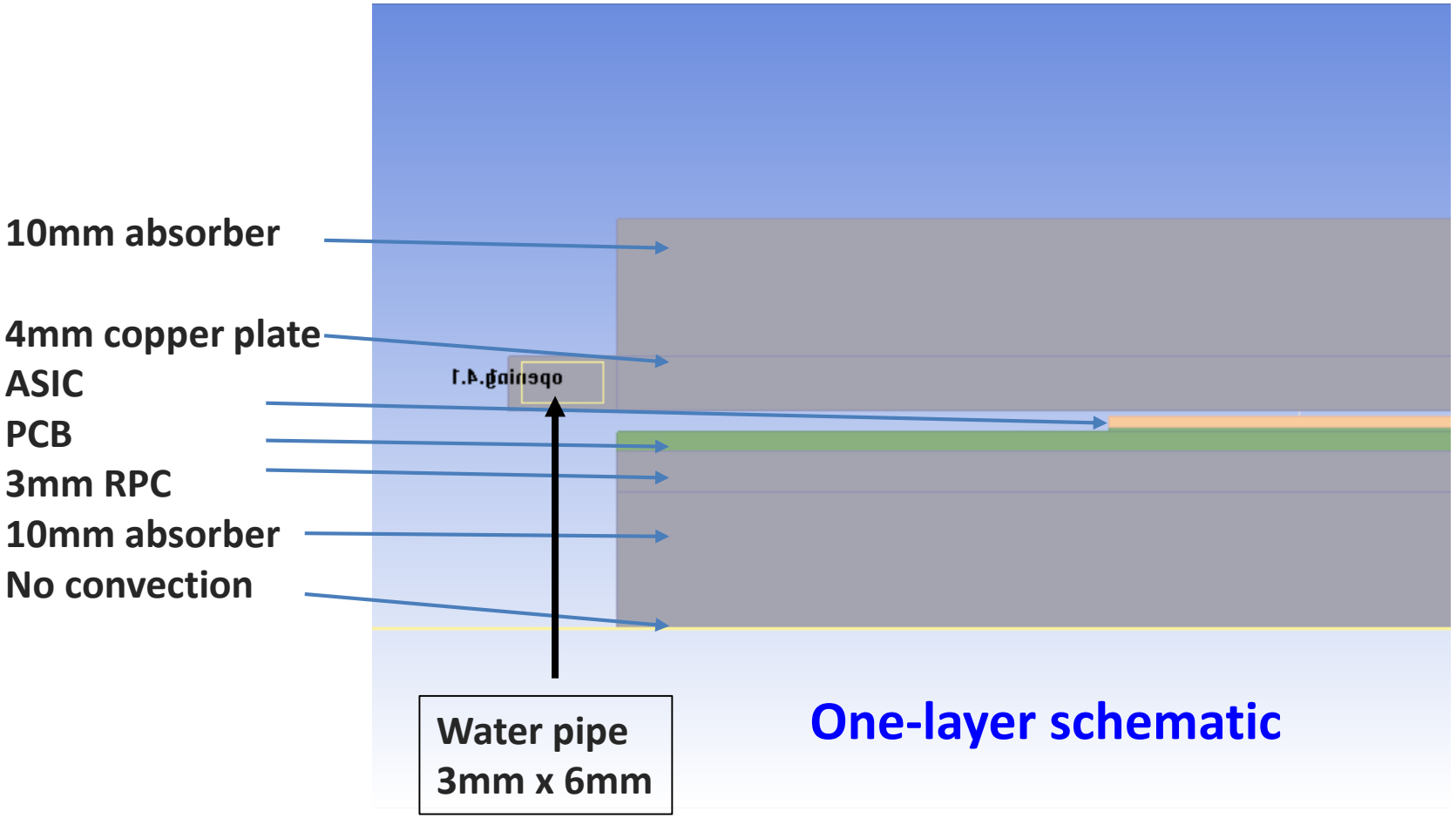


Initial temperature: 15℃,
convection parameter: 3W/(K*m²)
Simulation with Icepak

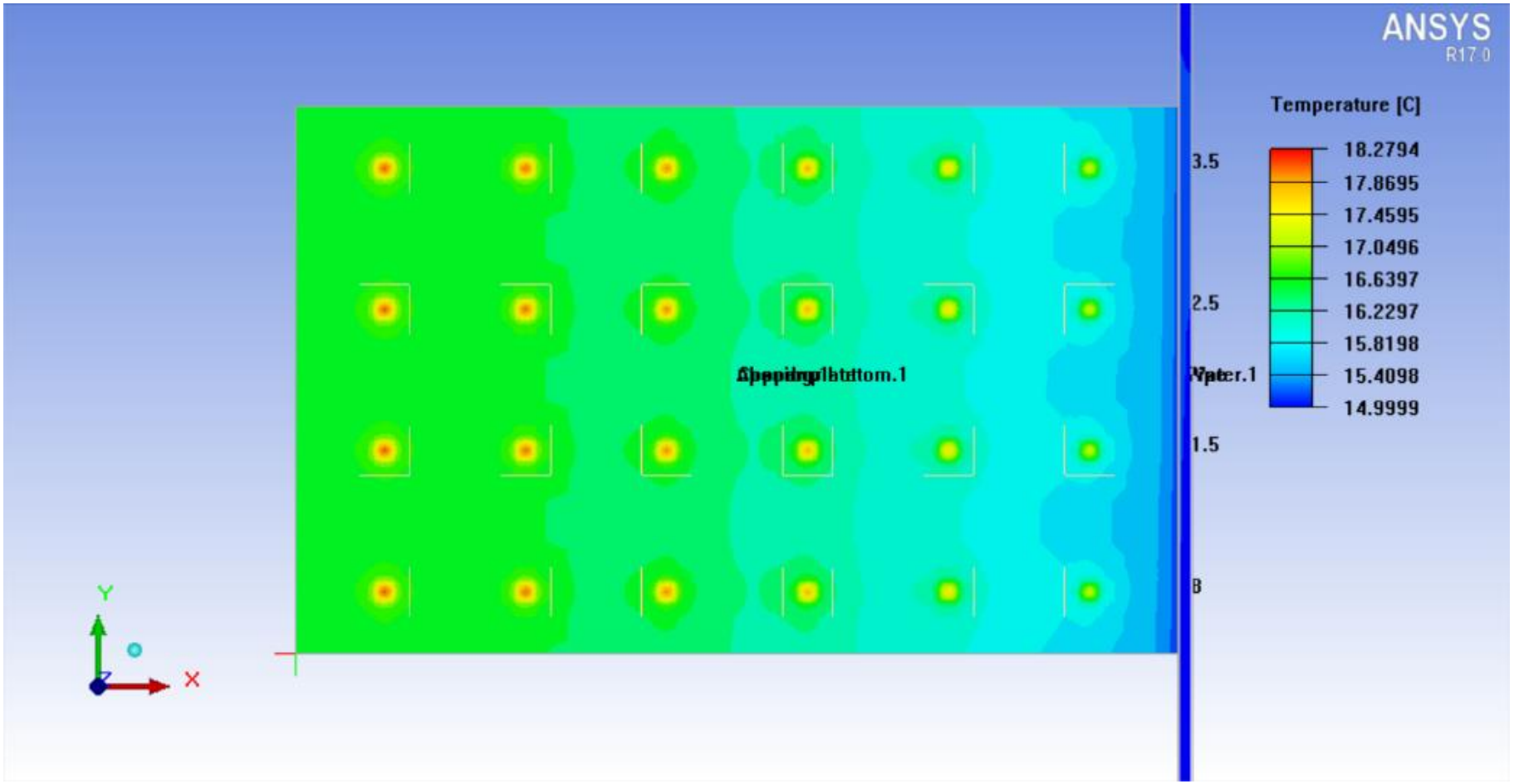
Low temperature at the gap region between two PCBs

Geometry with Water Cooling: 1-Layer

- One layer structure with stainless steel on both sides
- Water pipe connect to one side of copper plate

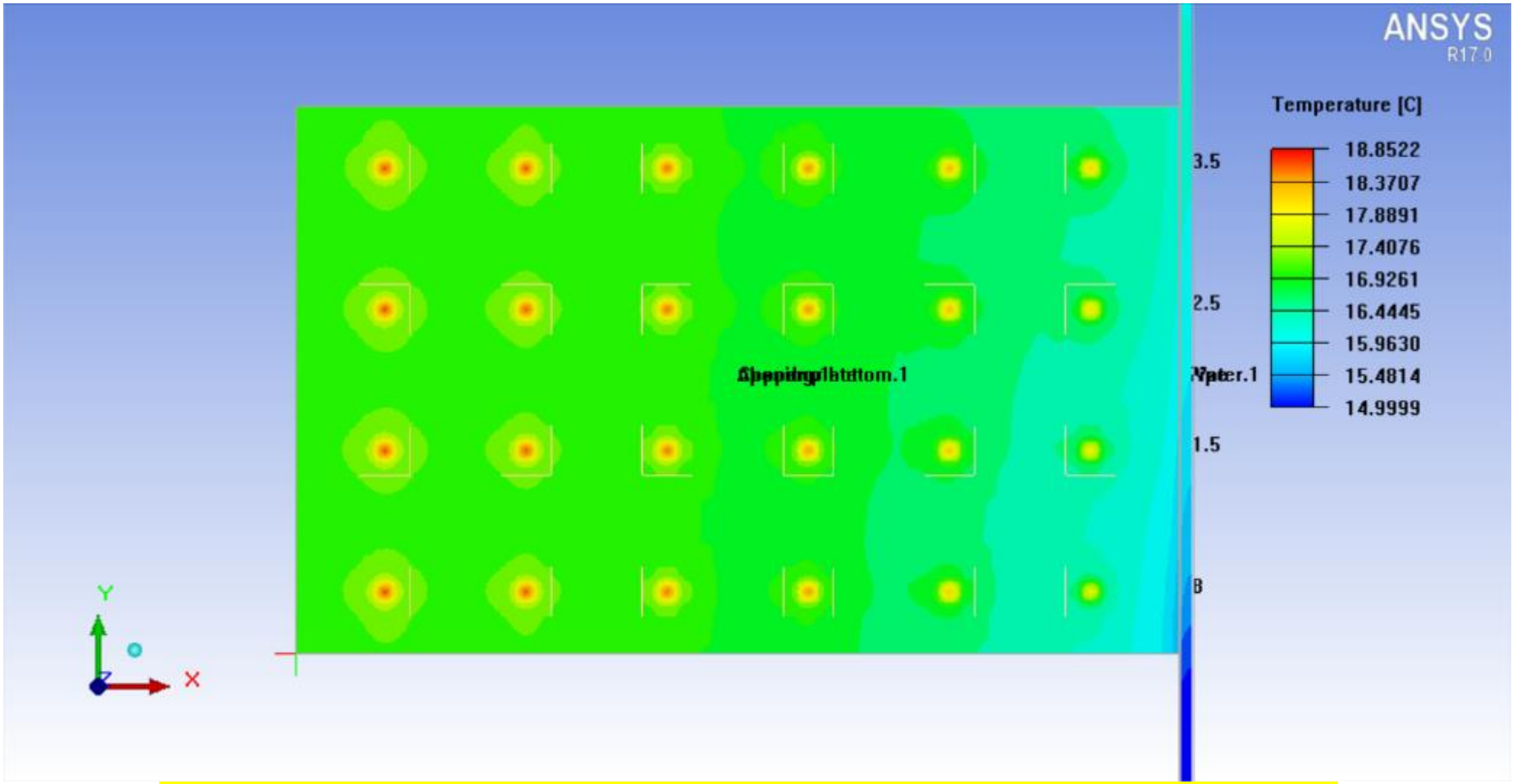


Results with Water Cooling: 1-Layer



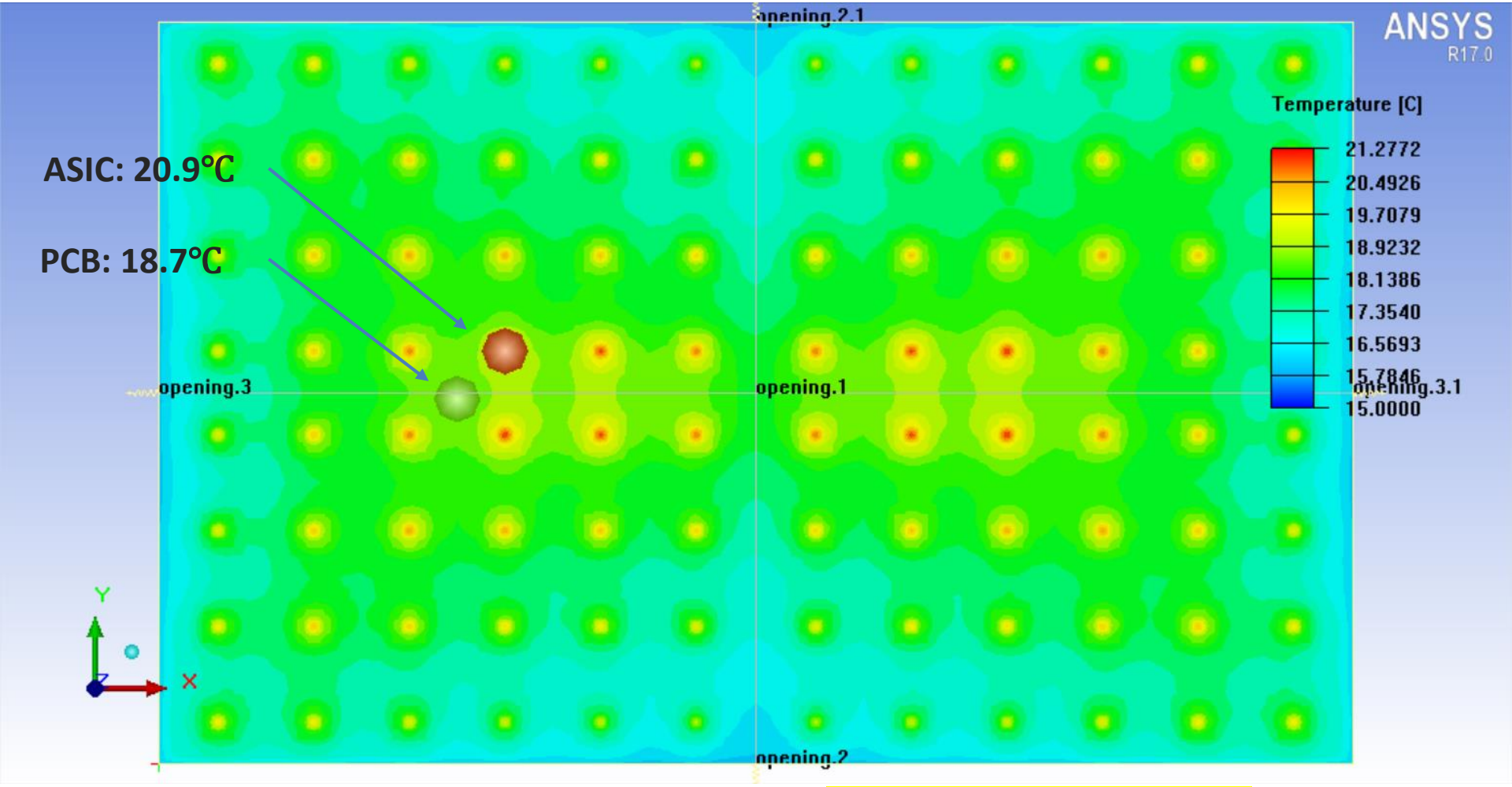
Initial temperature: 15 ℃, water flow rate: 0.1m/s
Maximum temperature: 18.3 ℃

Results with Water Cooling: 1-Layer



Initial temperature: 15 ℃, water flow rate: 0.01m/s
Maximum temperature: 18.9 ℃

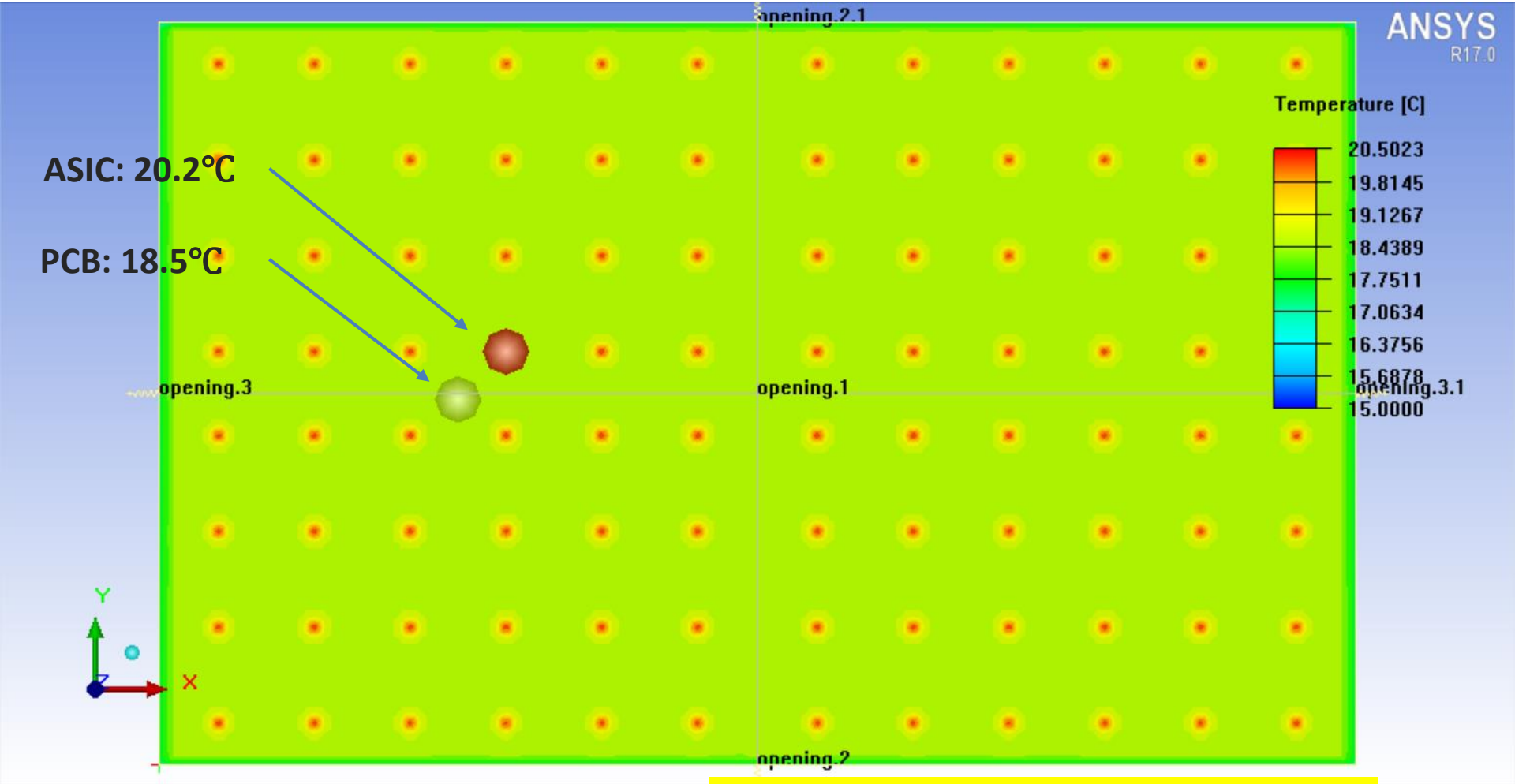
Results with 4 PCBs (Adiabatic)



Result in Icepak, 4PCBs
PCB bottom condition: adiabatic

1 PCB → 4 PCBs
ASIC: 19.5→20.9 ℃
PCB: 18.0 → 18.7 ℃

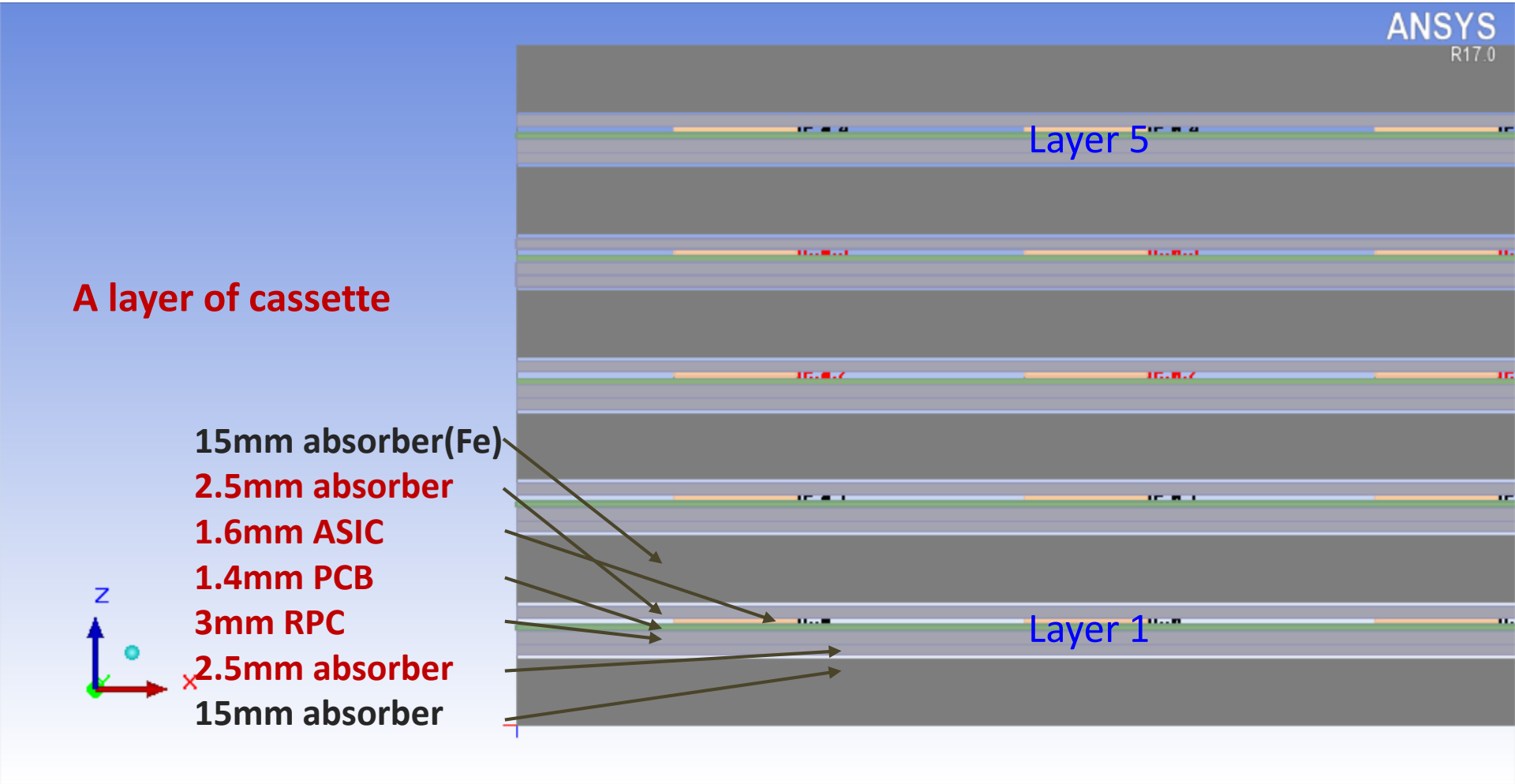
Results with 4 PCBs (Wood)



Result in Icepak, 4PCBs
PCB bottom condition:
attached by wood table

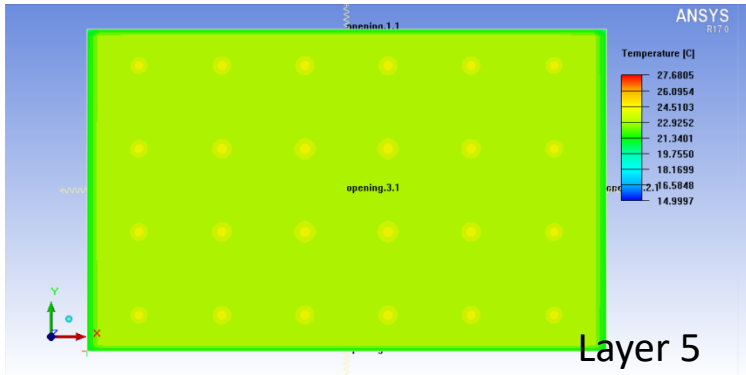
1 PCB → 4 PCBs(Adiabatic) → Wood
ASIC: 19.5 → 20.9 → 20.2 ℃
PCB: 18.0 → 18.7 → 18.5 ℃

Geometry with 5-Layer

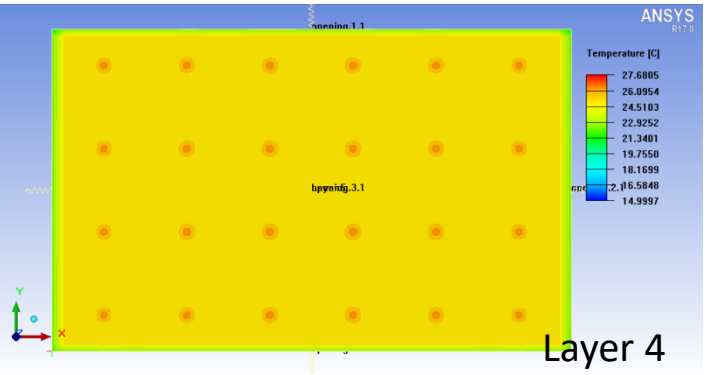


A 5-layer model without cooling, gravity along -z

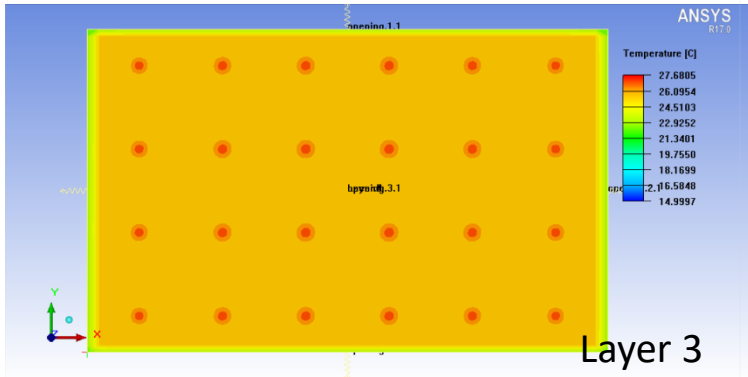
Simulation Results: 5-Layer



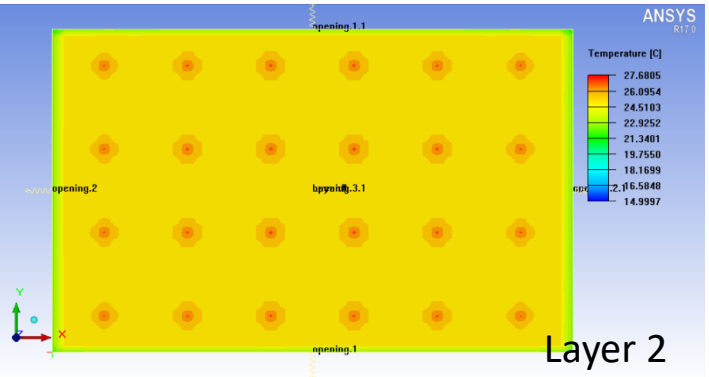
Layer 5



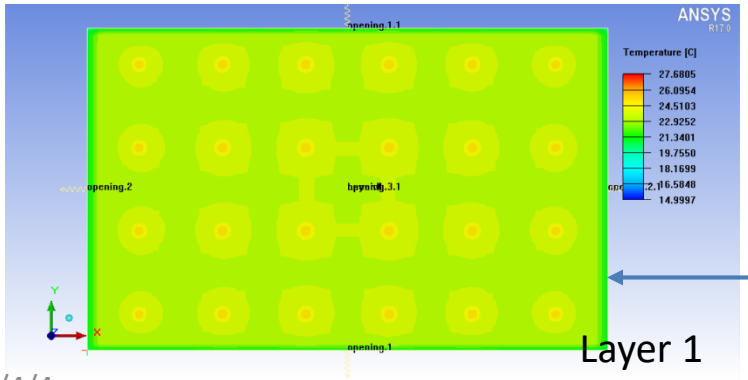
Layer 4



Layer 3



Layer 2

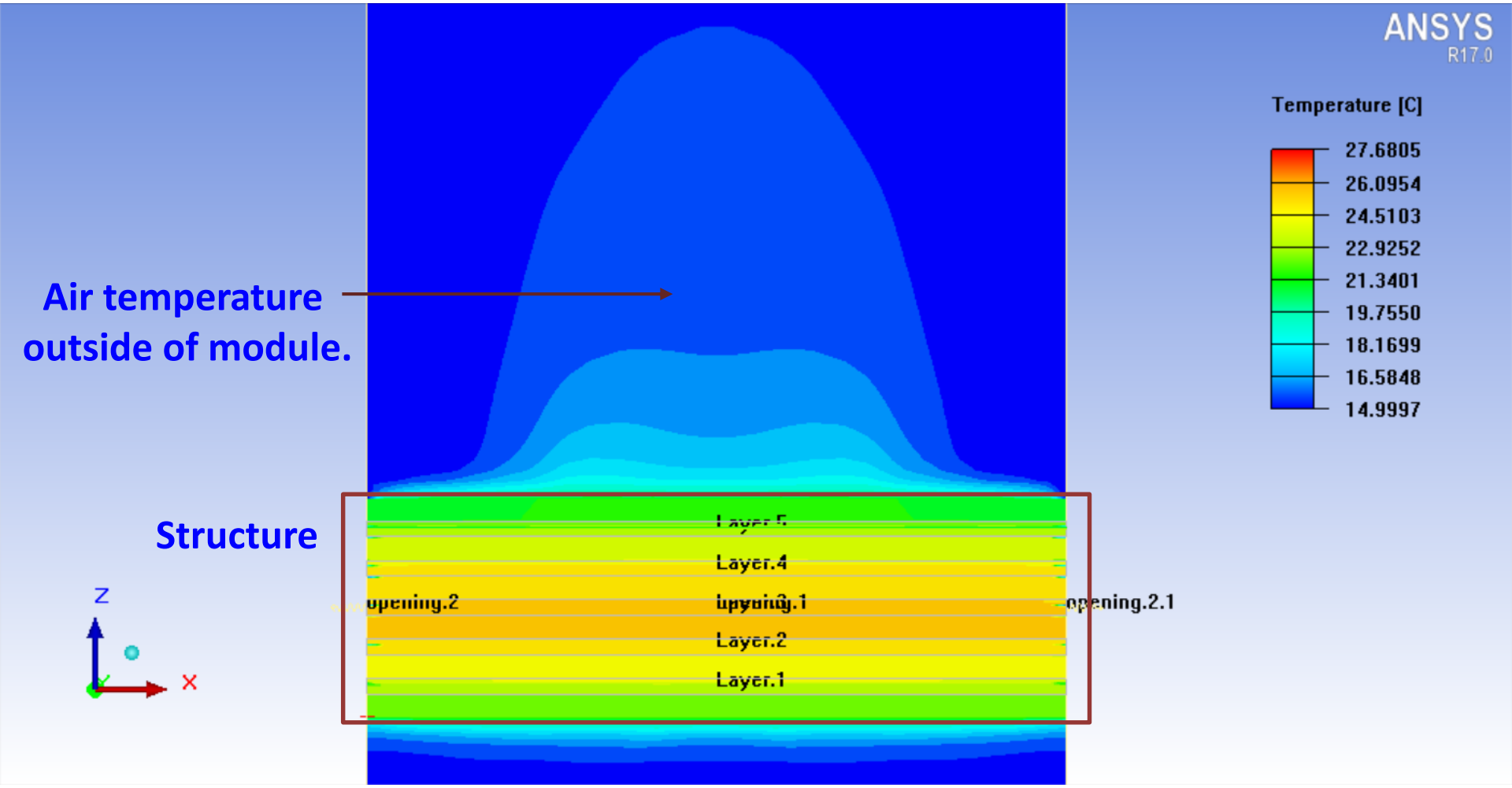


Layer 1

Result in Icepak, 5-layer structure

Low temperature due to an opening

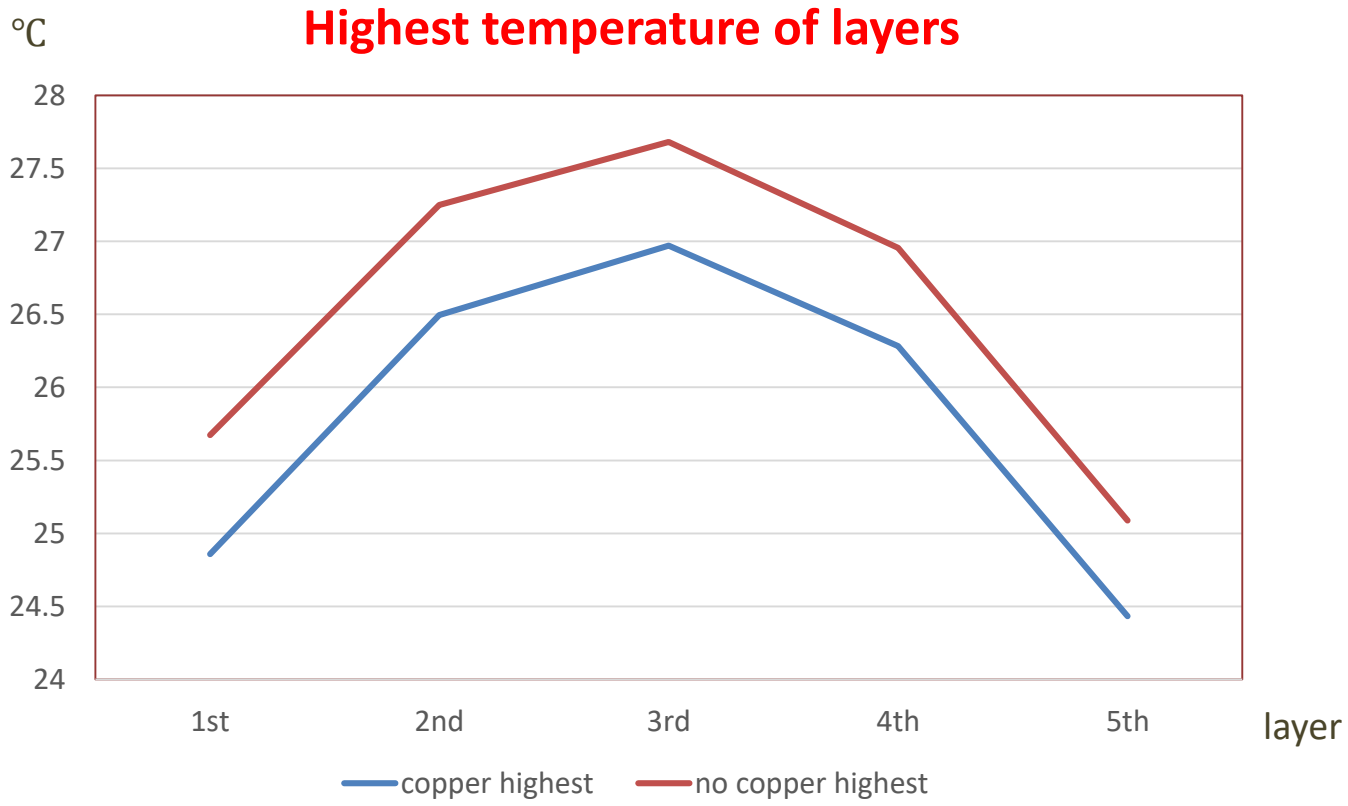
Simulation Results: 5-Layer



Result in Icepak, 5-layer structure, cross section with air

Results with copper plates

- The 2.5mm stainless steel absorber is replaced by **1.5mm stainless steel + 1mm copper plates**
- Comparison of maximum Temp with/without copper plates



Results with or without Copper Plates

Layer	Highest T (℃)	Lowest T (℃)	Standard deviation (℃)	Mean (℃)
Results with Copper Plates (1mm)				
1	24.8593	20.0959	0.472	22.9
2	26.4953	21.3039	0.481	24.7
3	26.9714	21.7191	0.470	25.3
4	26.2836	21.3638	0.429	24.7
5	24.4337	20.2269	0.358	23.0
Results without Copper Plates (0mm)				
1	25.6728	20.5871	0.494	23.7
2	27.2482	21.7730	0.505	25.4
3	27.6805	22.1545	0.494	26.0
4	26.9548	21.7669	0.454	25.3
5	25.0883	20.5913	0.384	23.6

Results with Power Pulsing: 1% duty cycle

- 64mW/chip ➔ 0.64mW/chip
- Temperature can be well controlled in power pulsing mode

Layer	Highest T (℃)	Lowest T (℃)	Standard deviation (℃)
1	15.1900	15.1112	0.00724
2	15.2025	15.1208	0.00746
3	15.2047	15.1231	0.00740
4	15.1966	15.1185	0.00702
5	15.1784	15.1067	0.00635

Summary and Future Plans

- Active cooling is needed for CEPC calorimeters operating at continuous mode
- Simulation results are comparable to measured temperature on PCB and Chips.
- Temperature goes higher with multi-layer structure
- Copper plates help to extract heat from the structure
- Water cooling helps to extract addition heat

Future Plans:

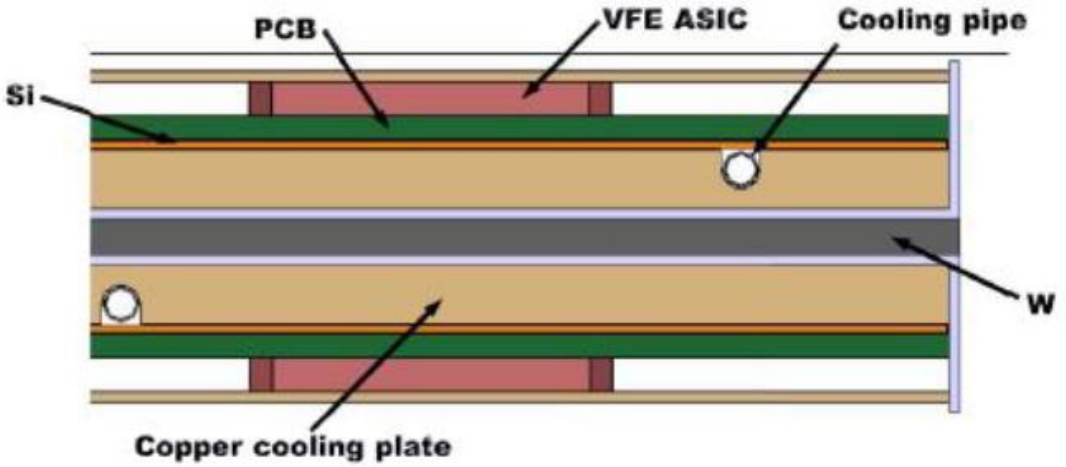
- Design cooling system for both ECAL and HCAL
- To build multi-layer cooling module with copper plate and tubes, use water or evaporative CO_2 as cooling agent

Active Cooling

- CEPC is designed to operate at continuous mode with beam crossing rate: 2.8×10^5 Hz. Power pulsing will not work at CEPC.
- Compare to ILD, the power consumption of VFE readout electronics at CEPC is about two orders of magnitude higher, hence it requires an active cooling
  - Evaporative CO_2 cooling in thin pipes embedded in Copper exchange plate.
  - For CMS-HGCAL design: heat extraction of 33 mW/cm^2, allows operation with 6×6 mm^2 pixels with a safety margin of 2
- To be modelled for Mokka simulation

➔ **Transverse view of the slab with one absorber and two active layers.**

➔ **The silicon sensors are glued to PCB with VFE chips, cooled by the copper plates with CO_2 cooling pipes.**



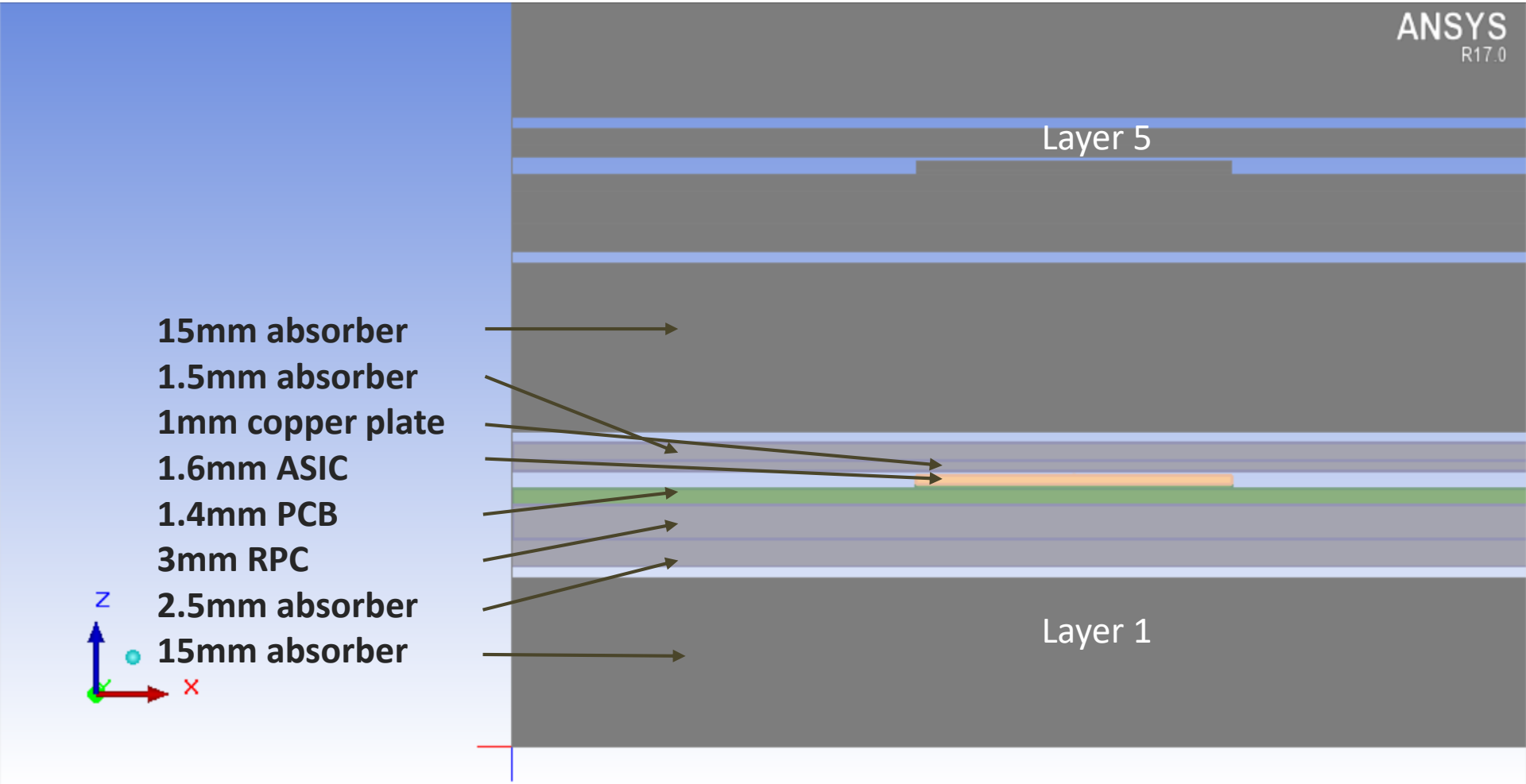
Simulation setup

- Turbulent mode
- Radiation: all solids
- Air flow: triggered by gravity
- Convection: natural convection
- Heat source: 64mW per chip /0.64mW in pulsing mode

Thermal conductivity:

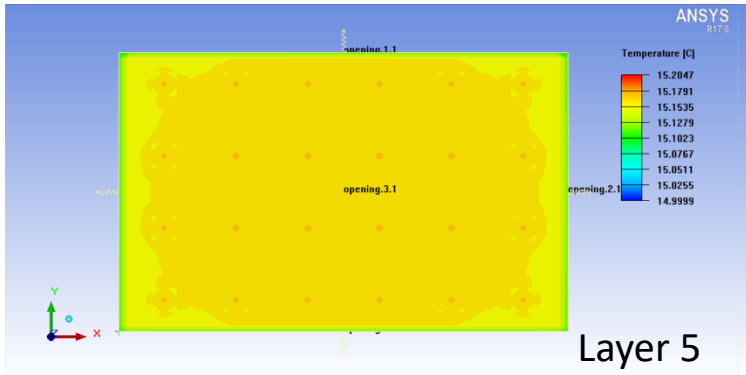
- absorber: stainless steel 14.4W/(m*K)
- RPC: glass 1.5W/(m*K)
- PCB: FR-4 0.35W/(m*K) copper 387.6W/(m*K)
- ASIC: silicon 180W/(m*K)

Geometry with Copper Plates

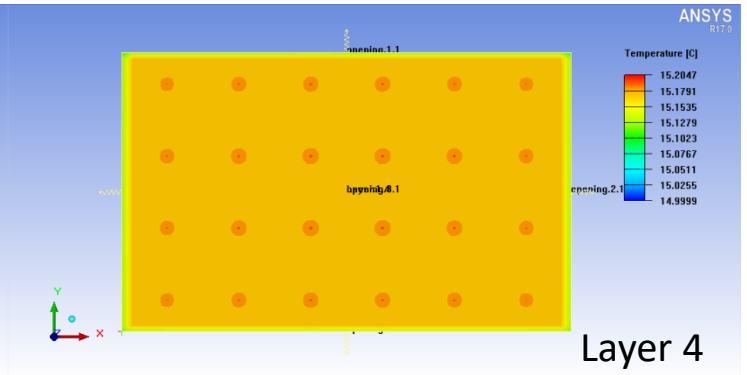


A 5-layer model with copper plate,
gravity along -z

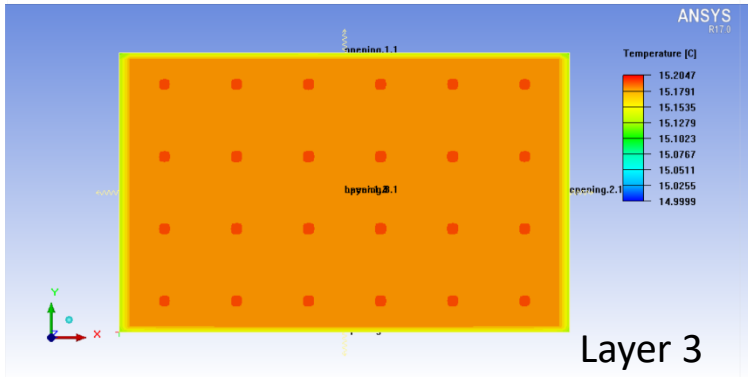
Results with pulsing power



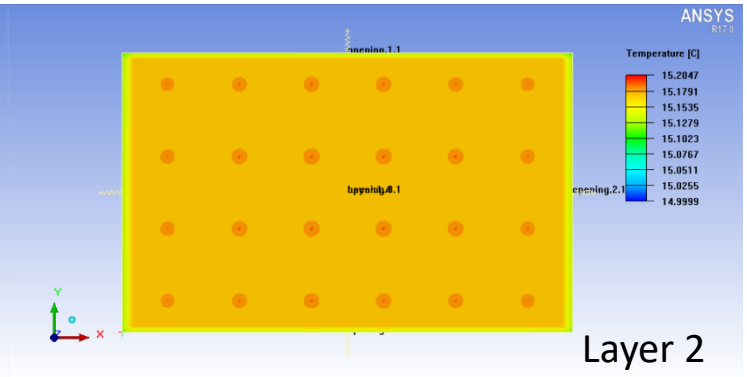
Layer 5



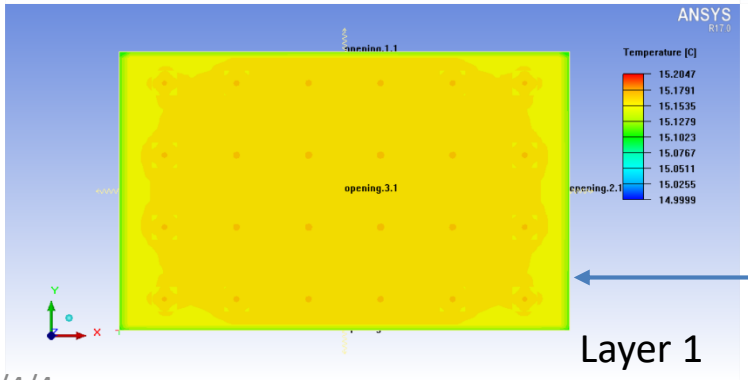
Layer 4



Layer 3



Layer 2



Layer 1

Result in Icepak, 5-layer structure

Low temperature due to an opening

Comparison with photos: DAQ

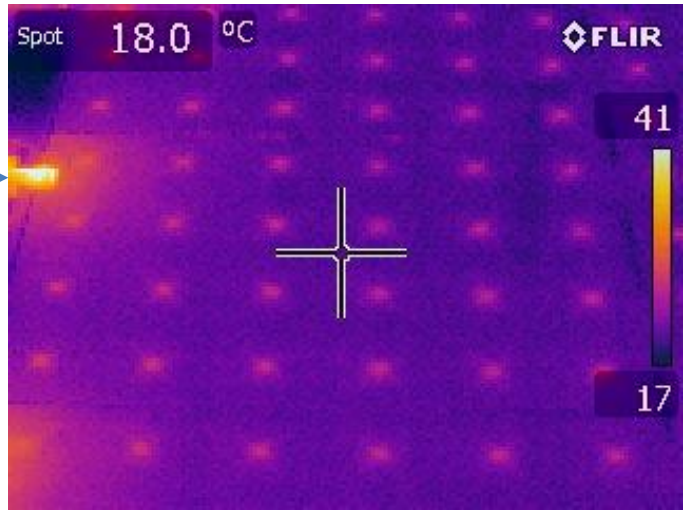
Icepak vs steady-state thermal

- **higher resolution on chips**

Icepak(wood condition) vs photo

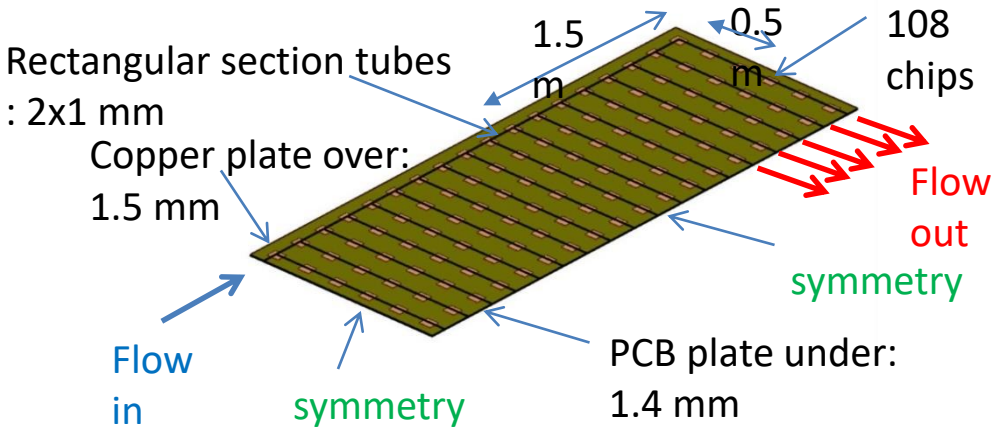
- **similar temperature difference between ambient and electronics**
- **both uniformed distribution on PCB**
- **a greater heat source in photo**

DAQ

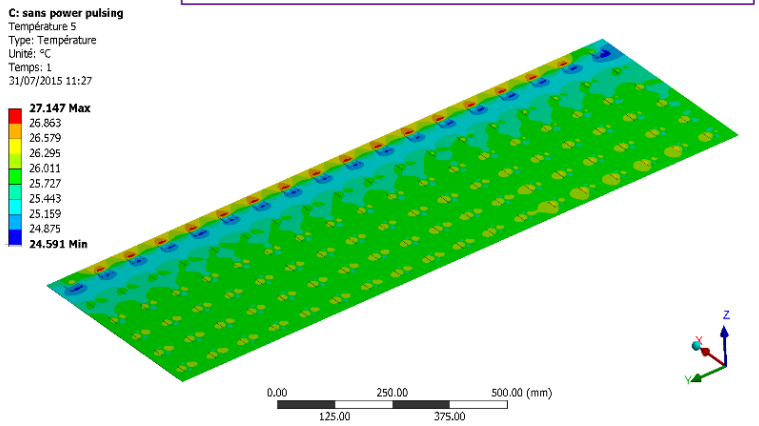


Active Cooling

Cooling may become necessary if it is operating at continuous mode (CEPC)



27.147 (max) – 24.591 (min) =2.556 °C



- A water-based cooling system inside copper tubes in contact with the ASICs to absorb excess heat.
- Temperature distribution in an active layer of the SDHCAL.

- **To simulate temperature distribution in an active layer**
- **To simulate temperature distribution for 1m*1m*1m (40 layers) SDHCAL**
- **optimize tube size and geometry**
- **optimize water flow rate and cooling capacity**

Water cooling : h = 1000 W/m²/k
Thermal load : 90 mW/chip

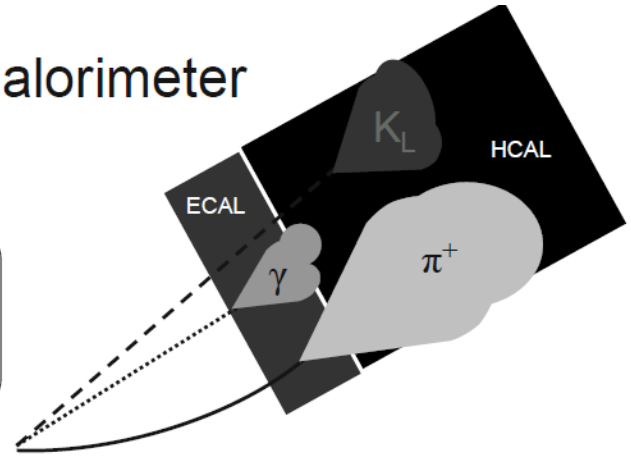
Particle Flow Algorithm

Particle Flow Algorithms and Imaging Calorimeter

The idea…

Charged particles } measured with the { **Tracker**

Neutral particles } measured with the { **Calorimeter**



Particles in jets	Fraction of energy	Measured with	Resolution [σ^2]
Charged	65 %	Tracker	Negligible
Photons	25 %	ECAL with 15%/√E	$0.07^2\ E_{jet}$
Neutral Hadrons	10 %	ECAL + HCAL with 50%/√E	$0.16^2\ E_{jet}$
Confusion			$\leq 0.24^2\ E_{jet}$

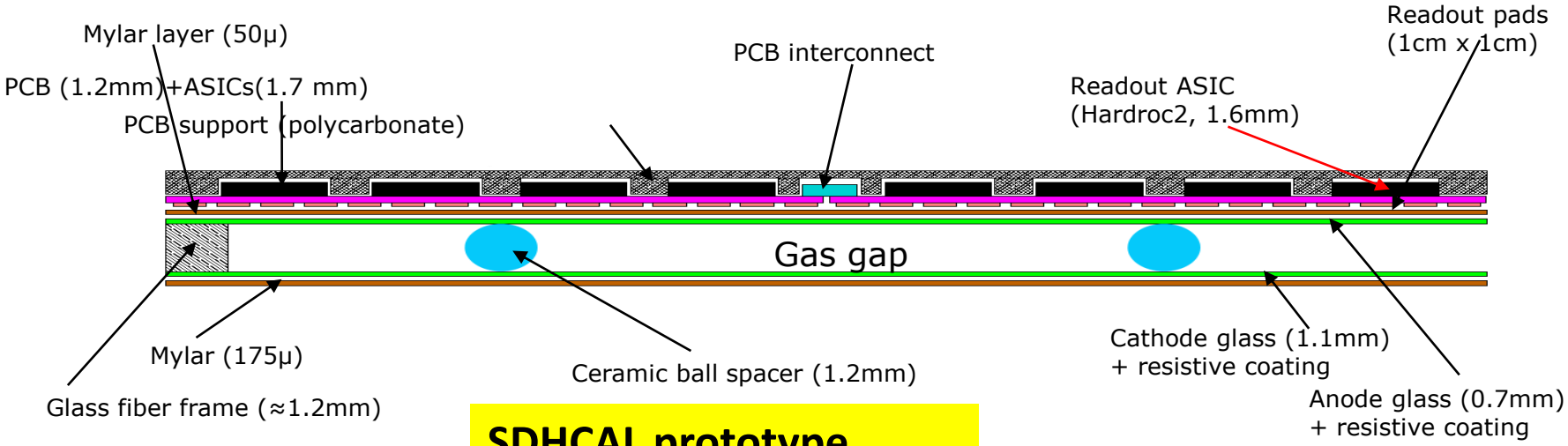
} 18%/√E

Required for 30%/√E

Requirements for detector system

→ Need excellent tracker and high B – field
→ Large R_I of calorimeter
→ Calorimeter inside coil
→ Calorimeter as dense as possible (short X_0, λ_I) } **thin active medium**
→ Calorimeter with **extremely fine segmentation**

SDHCAL based on RPC



Large GRPC R&D

- ✓ Negligible dead zone
- ✓ Large size: 1 x 1 m²

$(0.12\lambda_I, 1.14X_0)$

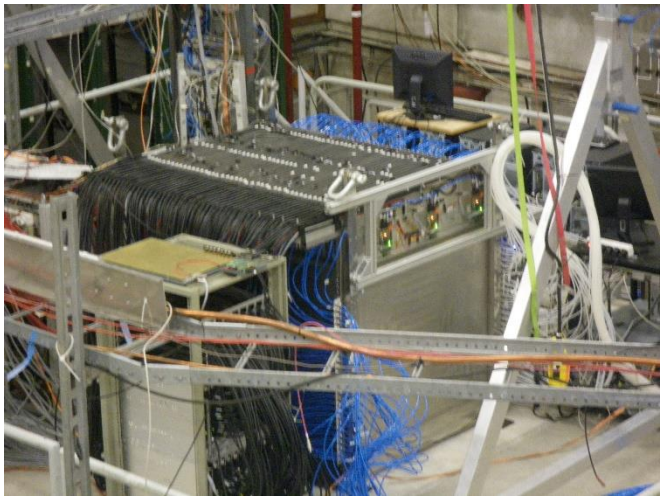
Stainless steel Absorber(15mm)

Stainless steel wall(2.5mm)

GRPC(6mm≈ $0\,\lambda_I, X_0$)

Stainless steel wall(2.5mm)

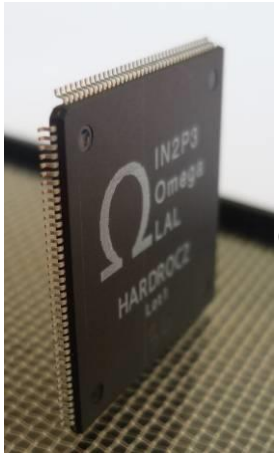
SDHCAL prototype
Size: 1m x 1m x 1.4m
No. of layers: 48
Cell size: 1cm x 1cm
No. of channels: 440K
Power: 1.4mW/ch

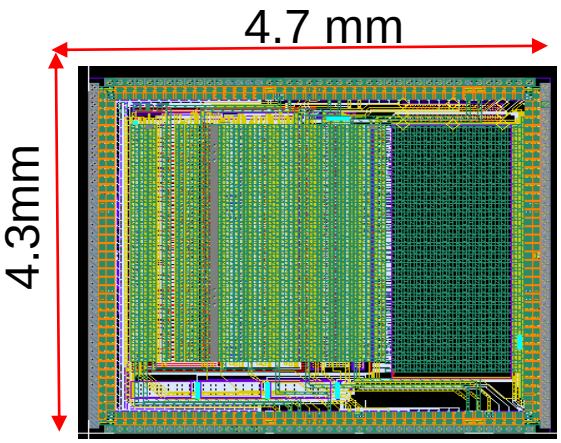


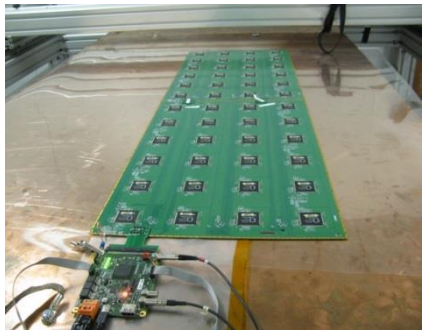
ASIC HARDROC (64 ch)
3-threshold: 110fC, 5pC, 15pC

Electronics Readout

ASICs : HARDROC2
64 channels
Trigger less mode
Memory depth : 127 events
3 thresholds
Range: 10 fC-15 pC
Gain correction → uniformity



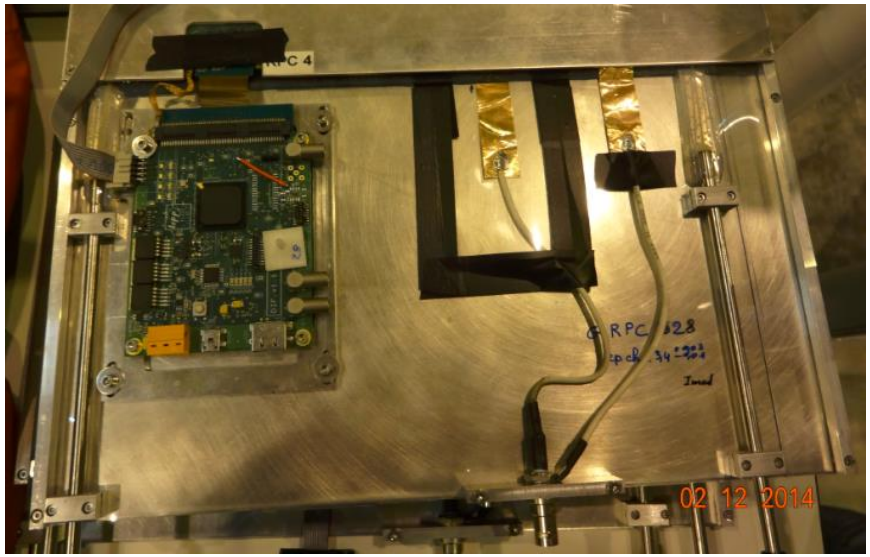




Printed Circuit Boards (PCB) were designed to reduce the cross-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two so the 24X2 ASICs are daisy-chained. $1\times1m^2$ has 6 PCBs and 9216 pads.

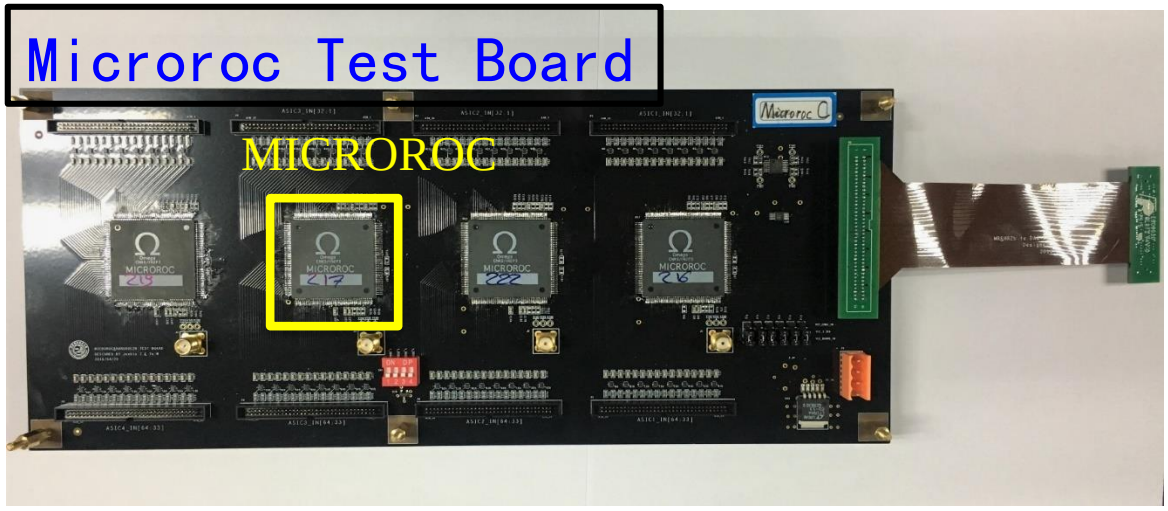
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



Readout ASIC

Readout ASIC	Channels	Dynamic Range	Threshold	Consumption
GASTONE	64	200fC	Single	2.4mW/ch
VFAT2	128	18.5fC	Single	1.5mW/ch
DIRAC	64	200fC for MPGD	Multiple	1mW/ch, 10μW/ch
DCAL	64	20fC~200fC	Single	——
HARDROC2	64	10fC~10pC	Multiple	1.42mW/ch,10μW/ch
MICROROC	64	1fC~500fC	Multiple	335μW/ch, 10μW/ch

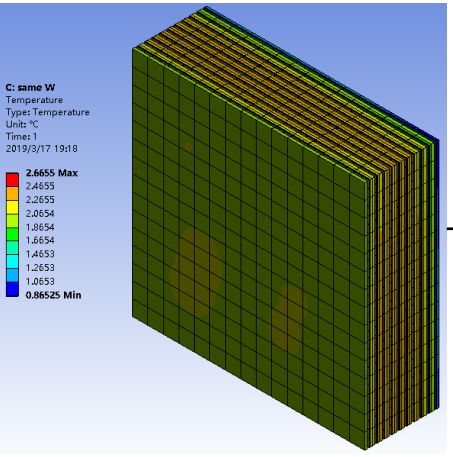
Considered the multi-thresholds readout, dynamic range and power consumption, MICROROC is an appropriate readout ASIC



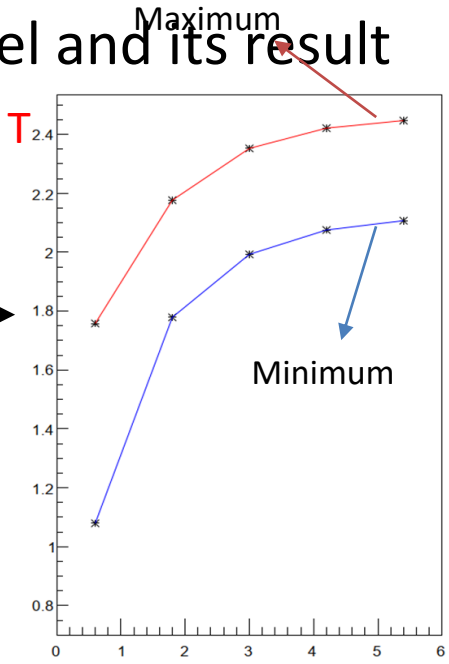
MICROROC Parameters

- Thickness: 1.4mm
- 64 Channels
- 3 threshold per channel
- 128 hit storage depth
- Minimum distinguishable charge:2fC

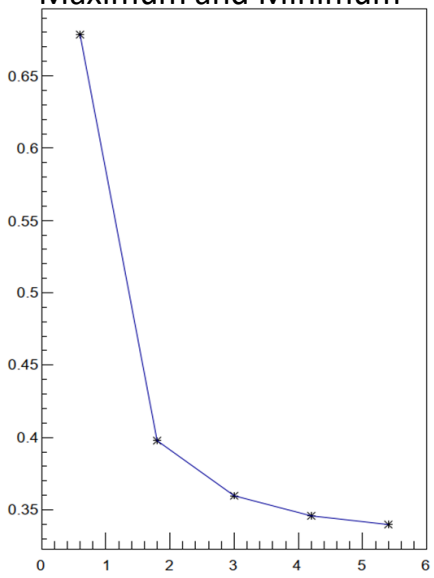
10-Layer model and its result

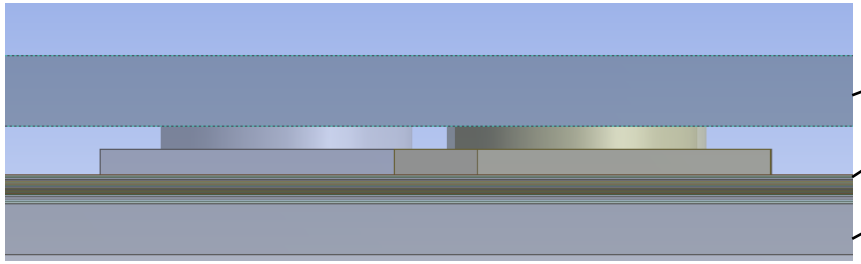


Data Analysis on layer effect



Difference value between Maximum and Minimum

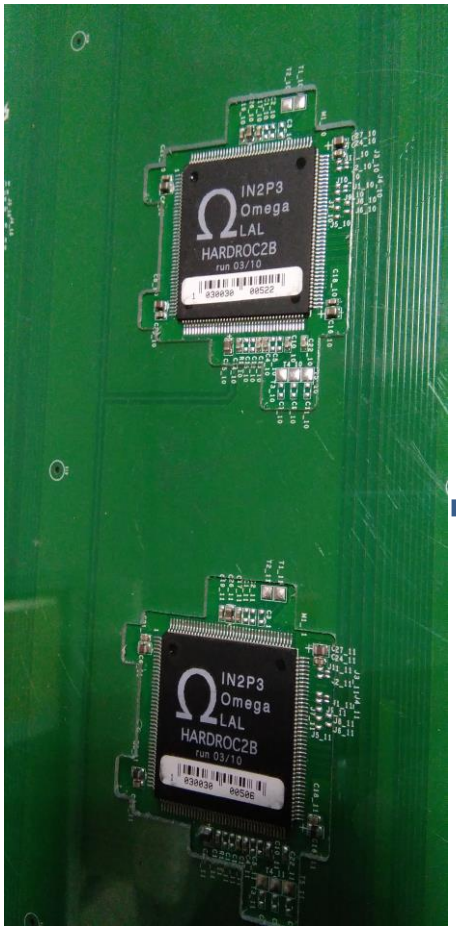




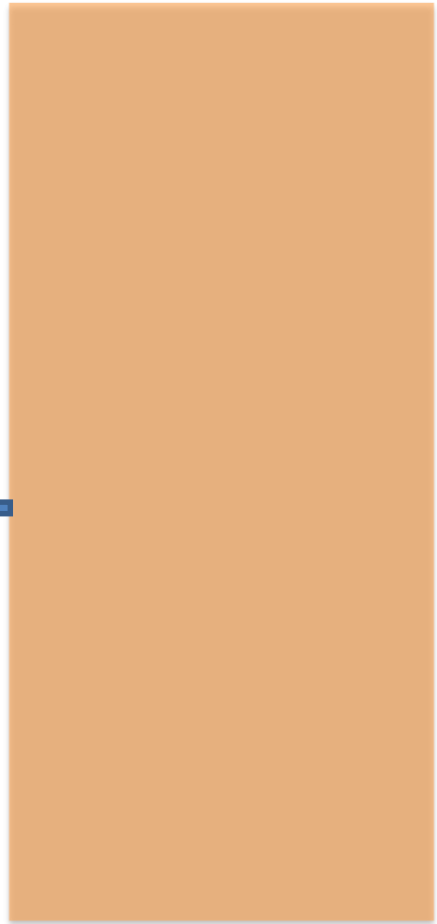
- W-Copper alloy
- Electronic board
- PSD

Each layer

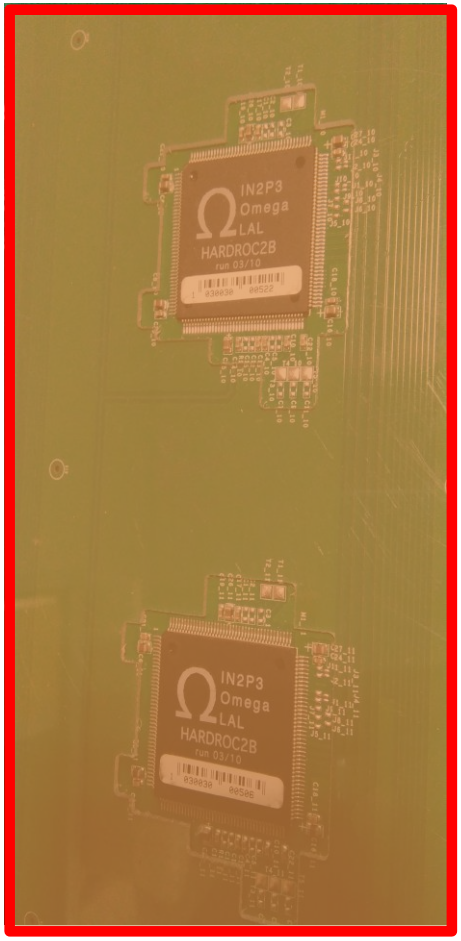
Active Cooling on RPC+PCB



RPC+PCB+ASIC
H ~ 6mm

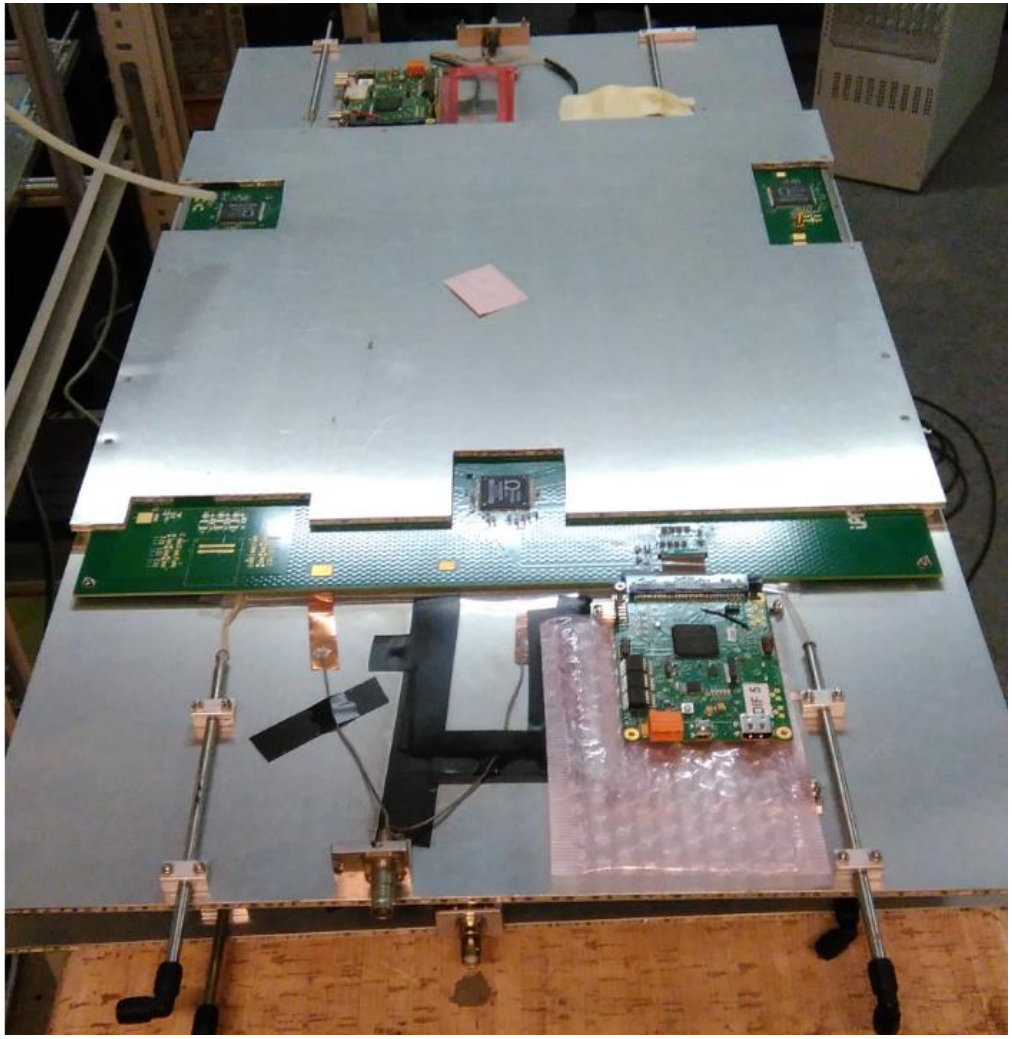


Copper/Al sheet
on top H ~ 1mm



Watering cooling
along sides

PCB with ASICs



➔ **ASIC chip (Hardroc) has 64 ch, 4.3mm*4.7mm, cover (5cm*6cm)**

➔ **Thick of stainless steel box is 2.5mm in each side, gap is 7mm (RPC+PCB+ASIC=6mm)**

Choice of Material

Material	Thermal Conductivity [W / (m K)]	Price ($/lb)
Stainless Steel	16	1
Aluminum	205	1
Cooper	401	2.8
Silver	429	230
Water	0.606	-
Air	0.0262	-

Cooper or Aluminum has good thermal conductivity and reasonable price !