CLIC Workshop 2019
CERN
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FONT

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- FONT IP system and cavity BPM signal processing
  - Recent beam stabilisation results
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- FONT upstream position and angle system
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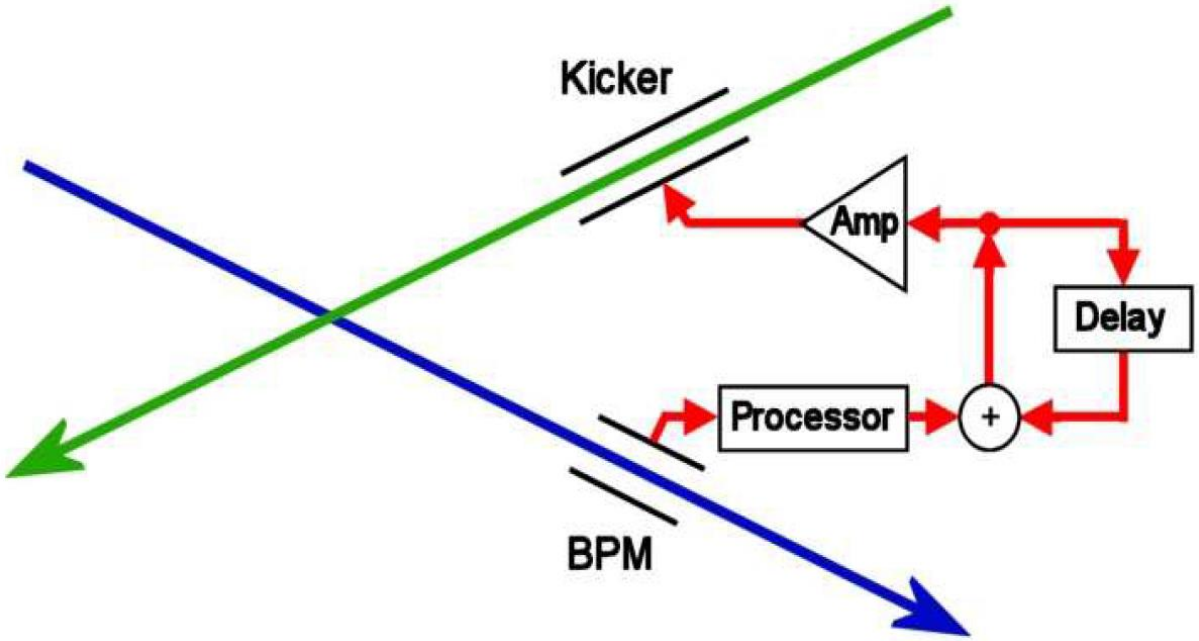
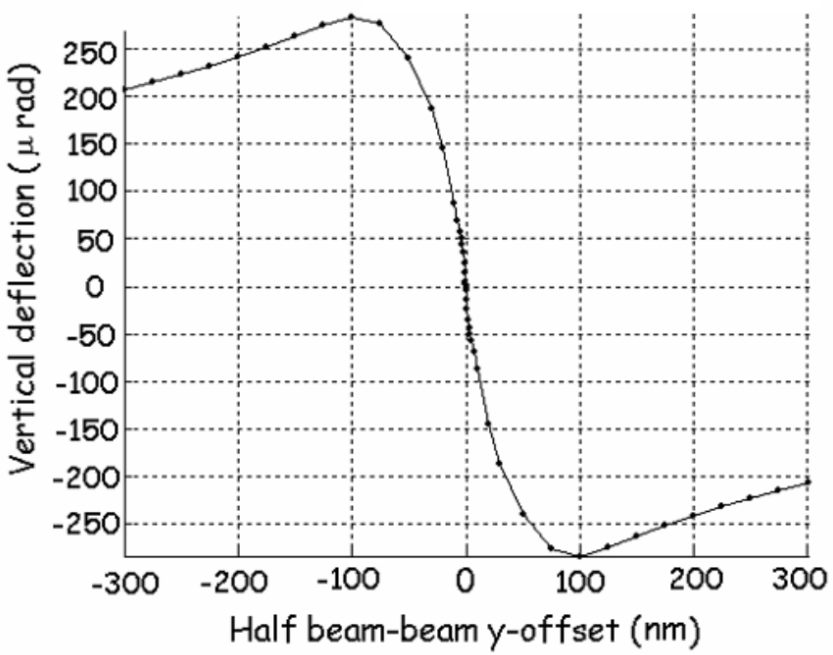
- Prototype stripline BPM processor for CLIC

Interaction Point feedback

- Offset of bunches at IP inferred from position of first bunch measured at downstream BPM
- Second bunch kicked upstream of IP in other beamline to compensate for this misalignment
- Delay loop preserves correction for subsequent bunches



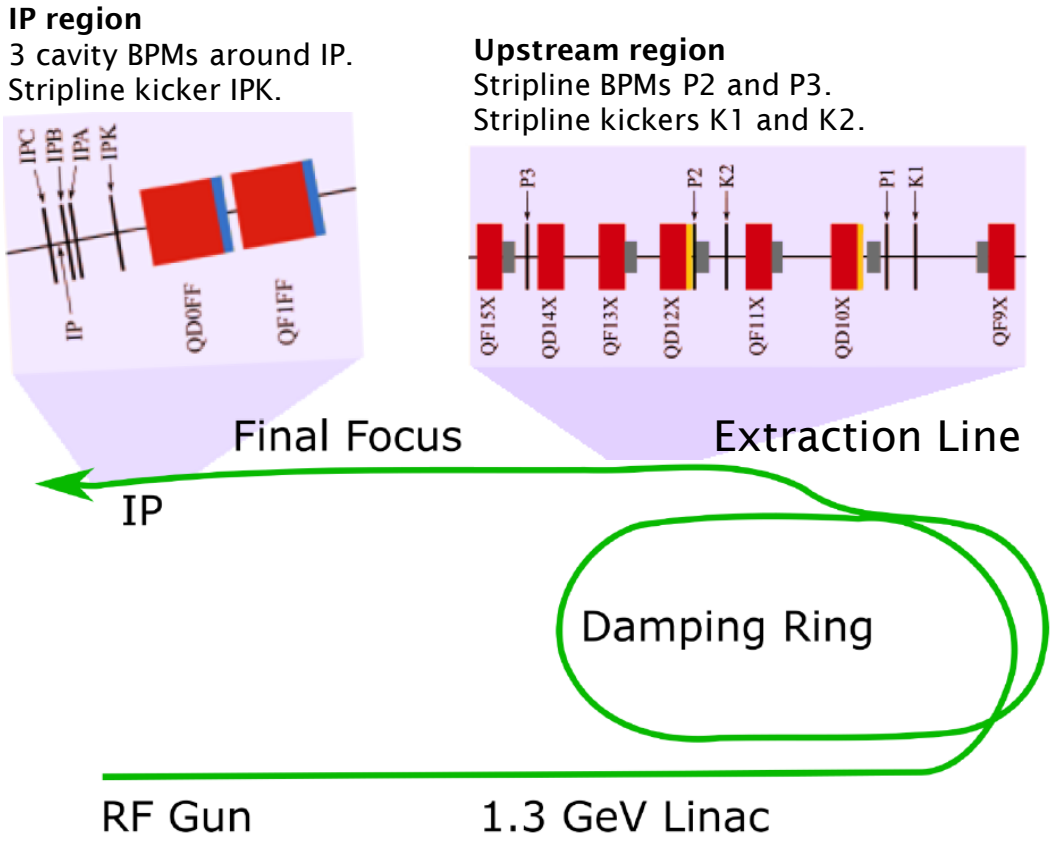
Beam-beam deflection curve



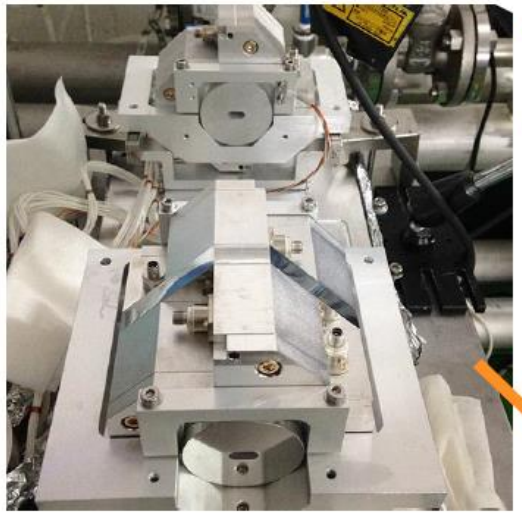
Beam stabilisation at ATF2

- ATF2 = test accelerator at KEK in Japan with 1.3 GeV electron beam
- ATF2 collaboration has two goals for beam:
  - 37 nm beam size
  - nm level beam stability

- FONT5A digital board processes BPM waveforms to determine correction, generates kicker drive signal
- Ultra-fast amplifier used with stripline kicker to apply beam deflection
- Uses bunch trains of two bunches with bunch spacing of ~280 ns

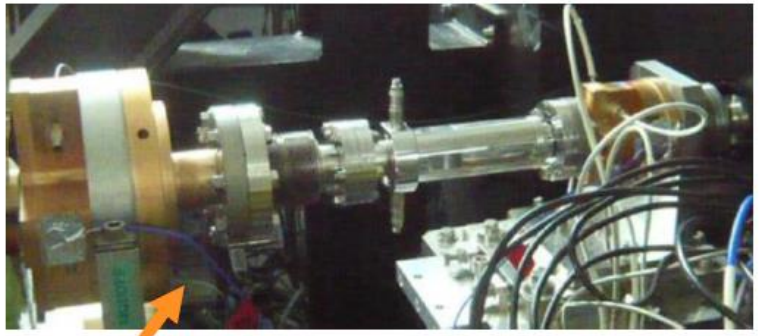


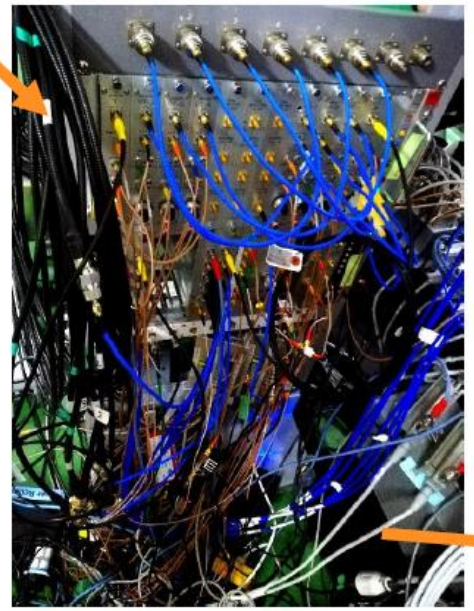
FONT IP feedback system



- Cavity Beam Position Monitors - IPA, IPB and IPC.
- We are now able to attenuate the three BPMs individually, allowing us to use all three BPMs while working in nominal optics.

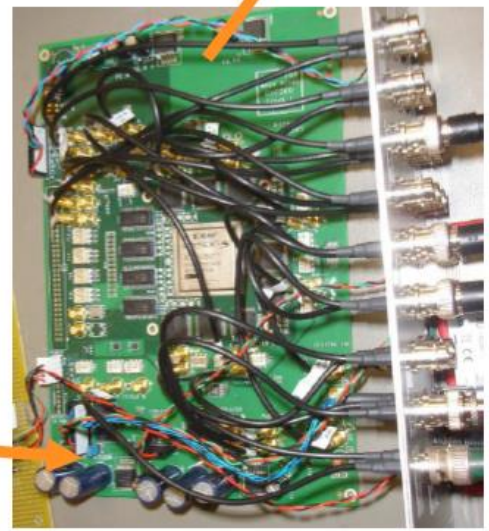
- Strip-line kicker and specialised amplifier used to provide correction.





- Two-stage processing electronics: down-mix and process cavity signals.

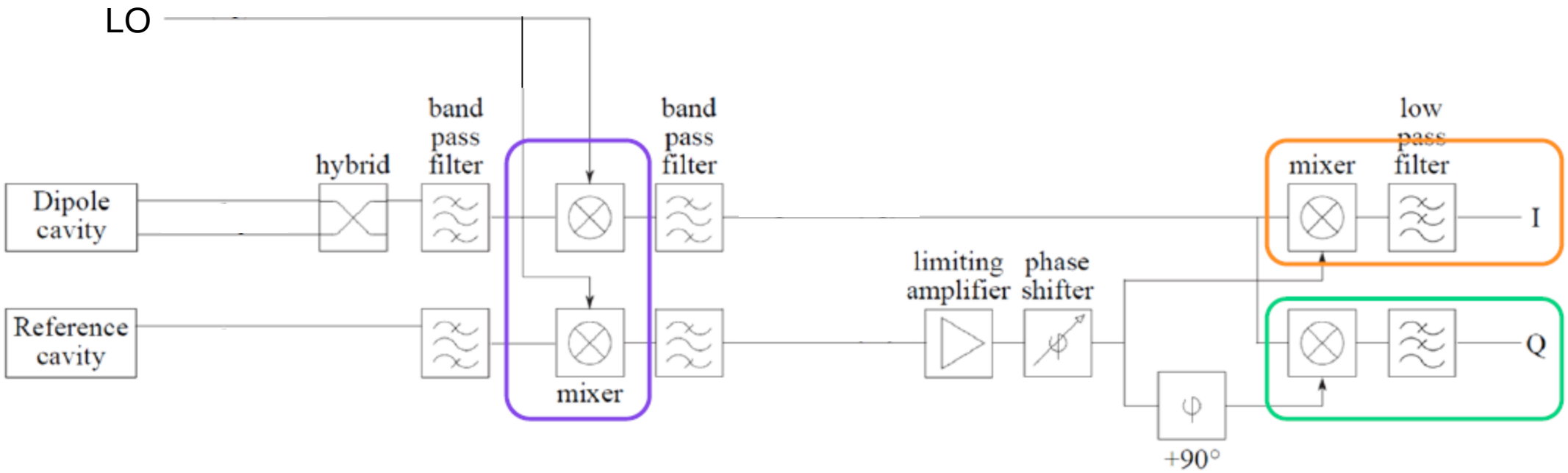
- The signals output from the processing electronics are sampled by the ADCs and used to calculate a bunch position.



- FONT 5A digital board.
- ADC inputs, DAC outputs.
- Contains a Field Programmable Gate Array (FPGA).

Slide by R. Ramjiawan

Cavity BPM signal processing



First stage (converter): dipole signals (position and charge dependent) and reference signal (charge dependent) down-mixed using a frequency-multiplied version of the DR LO

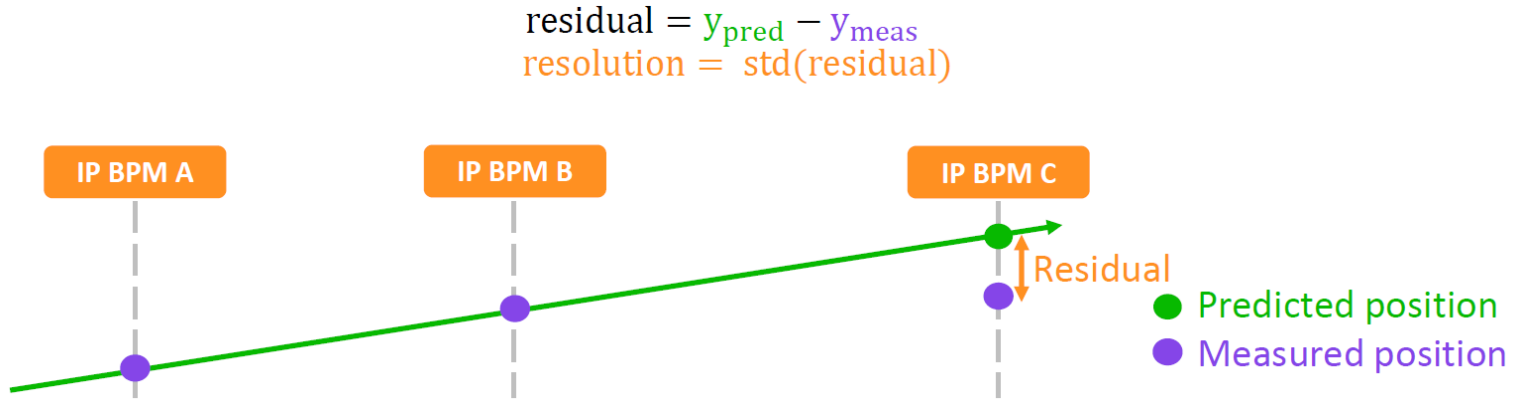
Second stage (detector): dipole signal down-mixed by the reference signal to form the I and by the reference signal with a 90° phase shift to form the Q

Bunch position given by $y = \frac{1}{k}\left(\frac{I}{q}\cos\theta + \frac{Q}{q}\sin\theta\right)$ where θ, k are calibration parameters

Slide by R. Ramjiawan

Highest resolution achieved

- Recent focus has been on improving the **usable resolution** of the system that applies to real-time position measurements used for feedback.
- Higher resolution can be achieved in off-line analysis by fitting bunch position as a function of additional parameters.



Resolution	IPA (nm)	IPB (nm)	IPC (nm)	Justification
Geometric	20.6 ± 1.0	20.6 ± 1.0	20.6 ± 1.0	-
Fit to position (fit for k)	20.4 ± 1.0	20.5 ± 0.8	20.3 ± 0.8	Fit out error in k
Fit to position and charge	19.9 ± 0.9	19.9 ± 0.8	19.7 ± 0.9	Fit out error in k and position-charge correlation
Fit for k and theta (fit to I and Q)	20.3 ± 1.0	20.3 ± 0.8	20.2 ± 0.9	Fit out error in k and theta.
Fit for k and theta and to charge	19.6 ± 0.9	19.6 ± 0.8	19.6 ± 0.8	Fit out error in k and theta, and position-charge correlation.
Fit for k, theta, charge and self Q’	19.5 ± 0.9	19.6 ± 0.8	19.2 ± 0.8	Fit out all of the above and residual position information in Q’ / Q’ coupling in through phase jitter.

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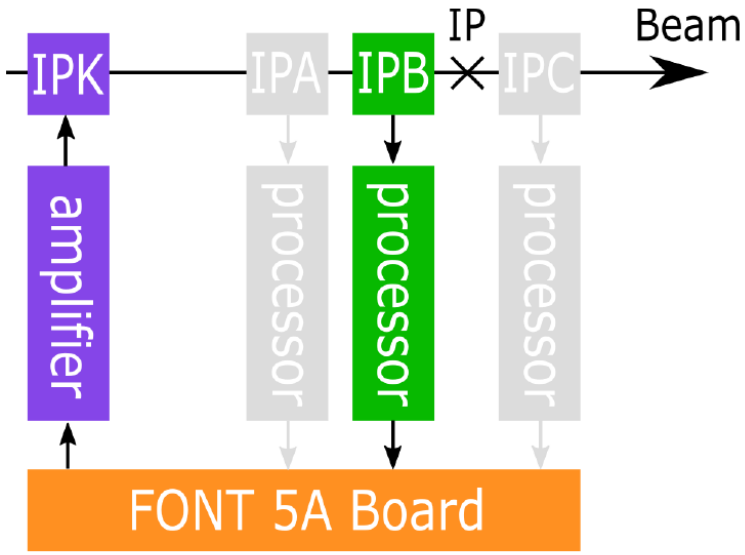
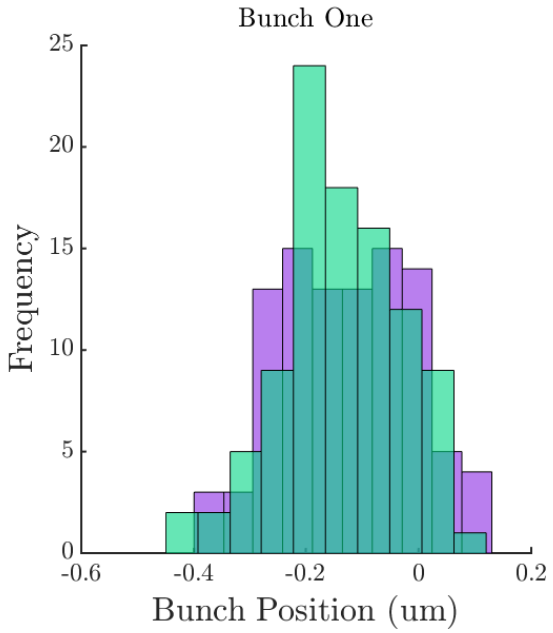
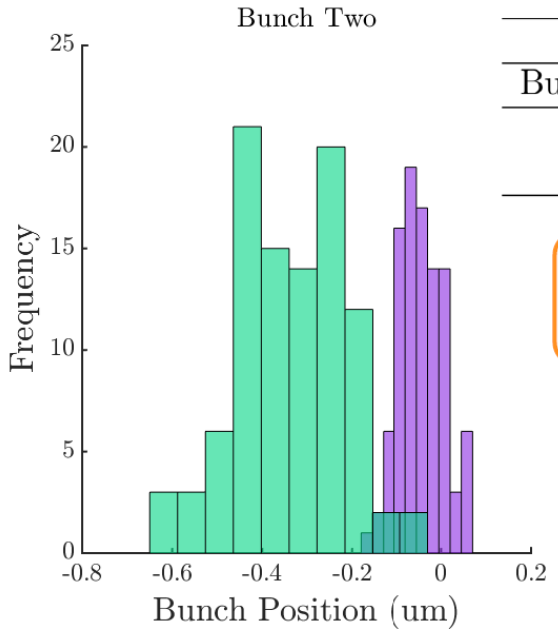
IP feedback: 1-BPM mode



- Position measurements at one BPM used to stabilise beam locally
- Limit to feedback performance = $\sqrt{2} \times \sigma_{res}$
- Previous best stabilisation in single-sample 1-BPM mode = **74 nm**

Latest results using waveform integration





	Position jitter (nm)	
Bunch	Feedback off	Feedback on
1	109 ± 11	118 ± 8
2	119 ± 12	50 ± 4

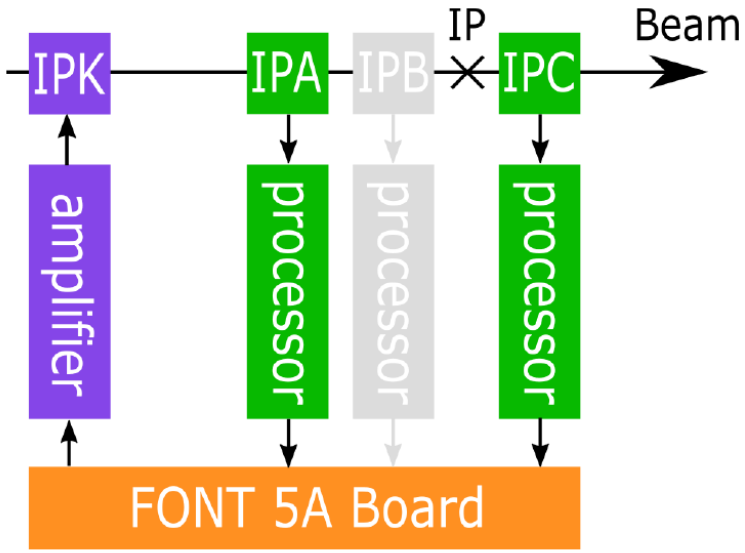
Feedback stabilising to:
50 ± 4 nm.

Feedback off correlation: **84%**
Feedback on correlation: **−26%**

- 10 samples integrated.
- Stabilisation below 55 nm was repeatable.

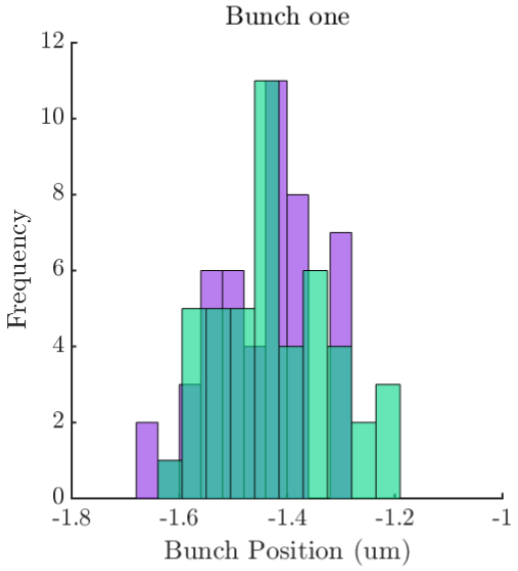
Slide by R. Ramjiawan

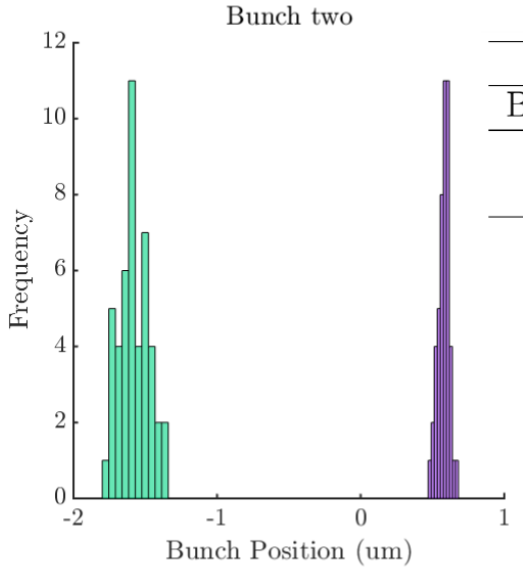
IP feedback: 2-BPM mode



- Beam position measurements at two BPMs (IPA and IPC) used to stabilise beam at intermediate location (IPB)
- Limit to feedback performance = $1.25 \times \sigma_{res}$
- Previous best stabilisation in single-sample 2-BPM mode = **68 nm**

Latest results using waveform integration





	Position jitter (nm)	
Bunch	Feedback off	Feedback on
1	106 ± 16	106 ± 16
2	96 ± 10	41 ± 4

Feedback stabilising to:
41 ± 4 nm.

Feedback off correlation:
91.6%

Feedback on correlation:
41.3%

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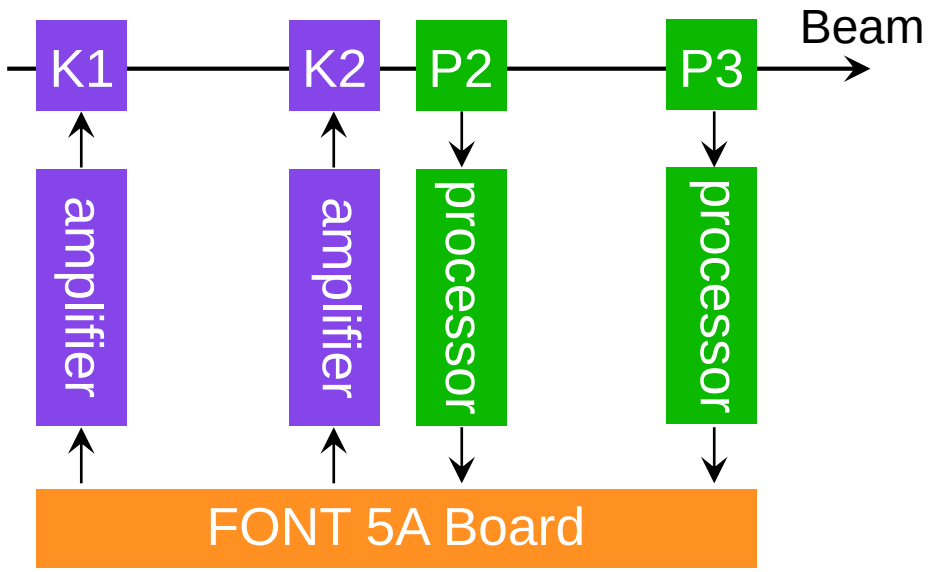
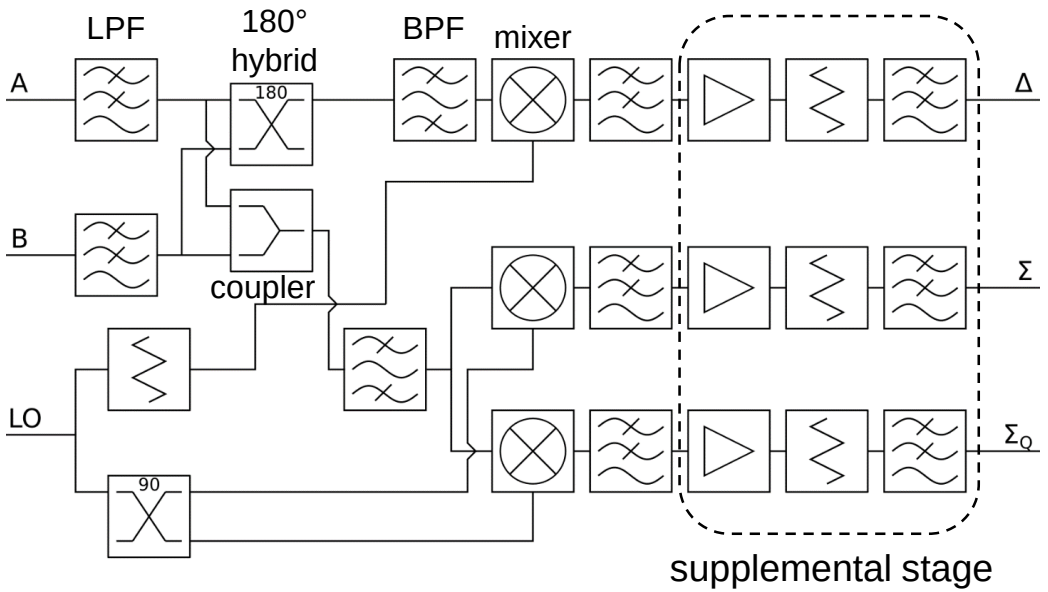
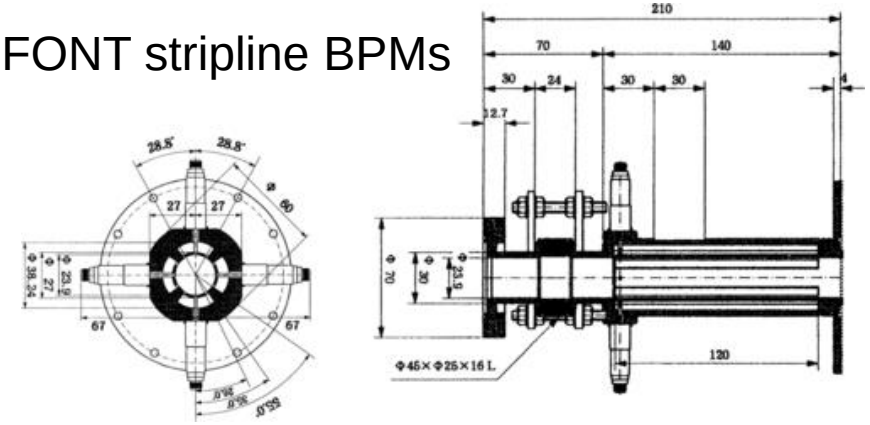
Upstream system: 2-BPM, 2-kicker

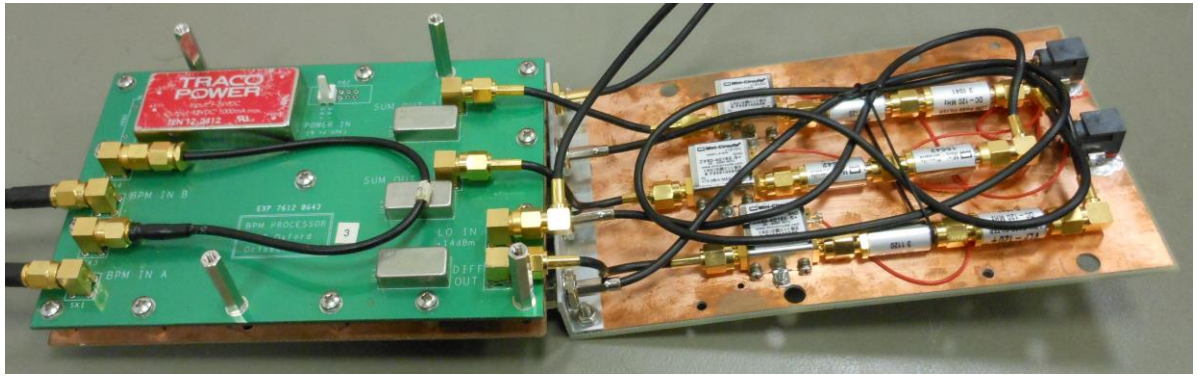




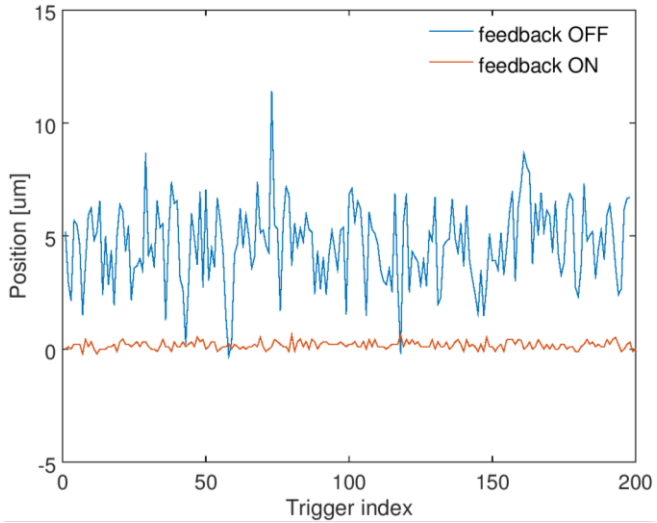
FONT stripline BPMs

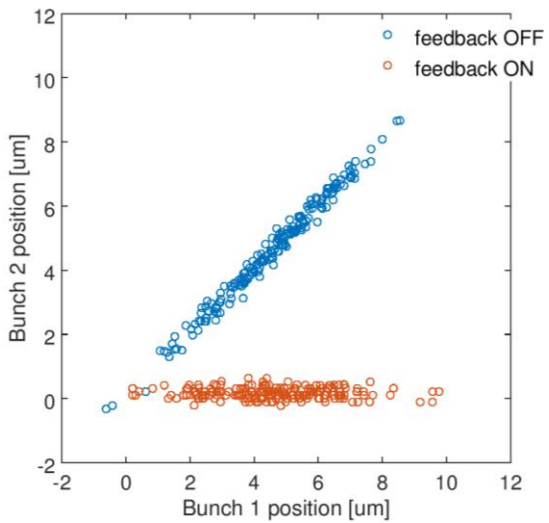


FONT stripline BPM processors



Upstream feedback results



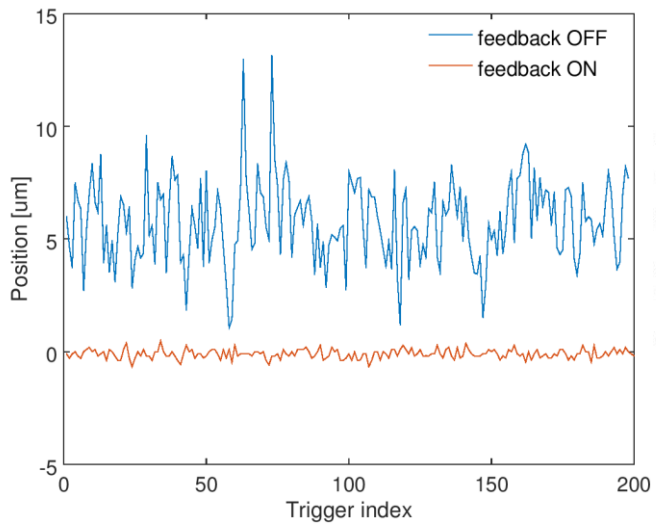


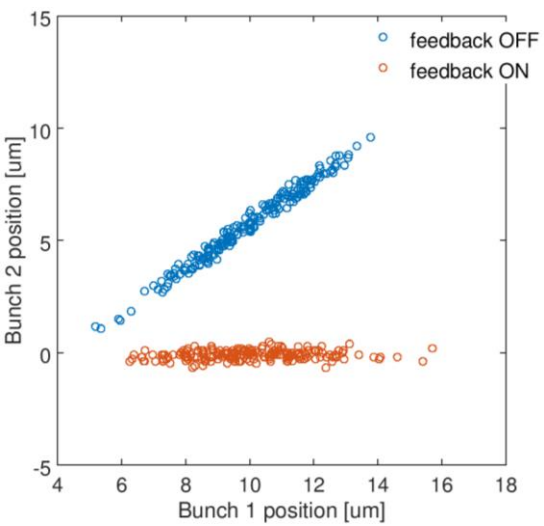
Position jitter of bunch 2
1.78 μm (feedback off)
0.17 μm (feedback on)

Bunch-bunch correlation
0.994 (feedback off)
-0.035 (feedback on)

P2

Reduction factor
= 10.5





Position jitter of bunch 2
1.85 μm (feedback off)
0.20 μm (feedback on)

Bunch-bunch correlation
0.992 (feedback off)
0.163 (feedback on)

P3

Reduction factor
= 9.1

Diode processor

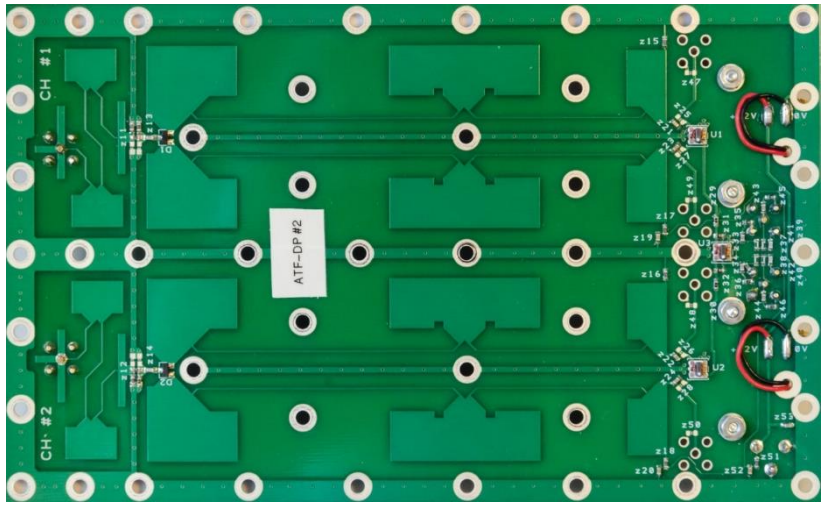
Motivation

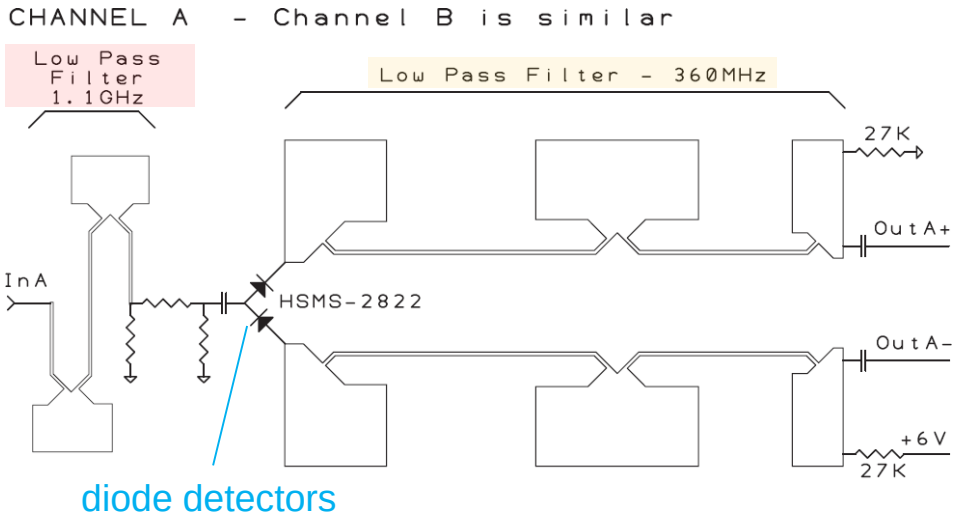
- The Compact Linear Collider (CLIC) will require a beam position feedback system at the interaction point (IP)
- This will require a beam position monitor (BPM) with the following characteristics:
  - Low latency, simple, reliable, rad-hard, tolerant of high magnetic field (no ferrites!)
- These requirements are met by a stripline BPM used with the simplest possible processor: a diode detector on each strip

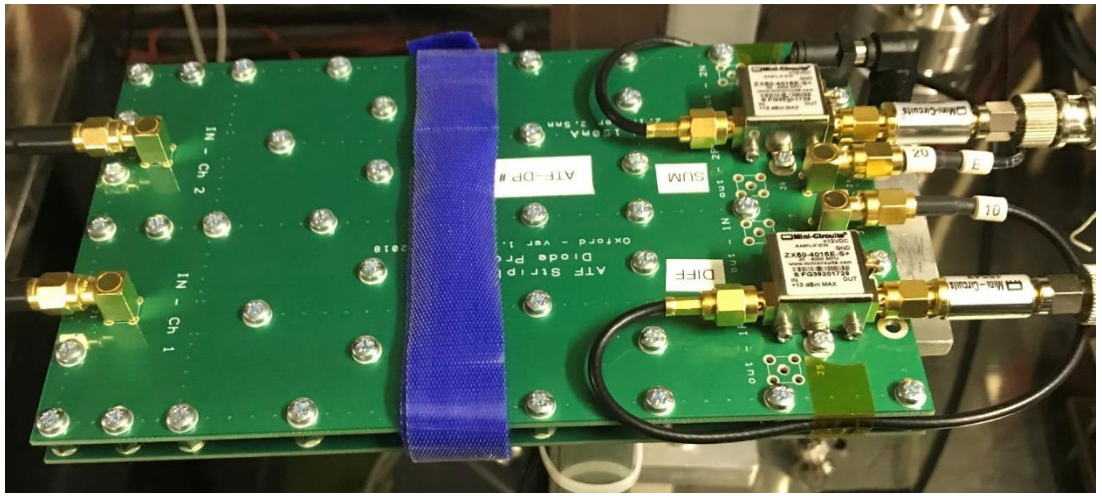
Design

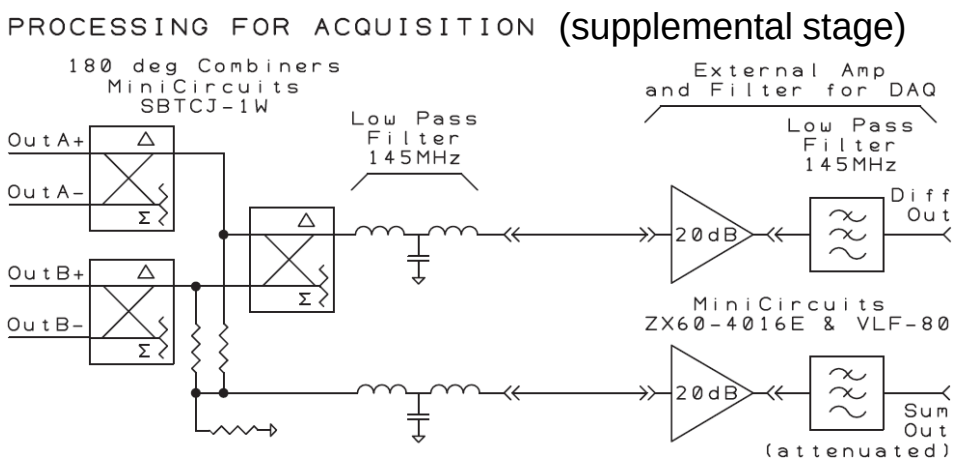
- A prototype was constructed for testing at the KEK Accelerator Test Facility (ATF)
- Processor designed to scale up in frequency
- At CLIC processor outputs would be input to differential amplifiers
  - FONT5 digitizer at ATF unable to handle pulses this narrow due to 357 MHz ADCs, so supplement diode processor with an additional stage to condition signals

Diode processor schematic

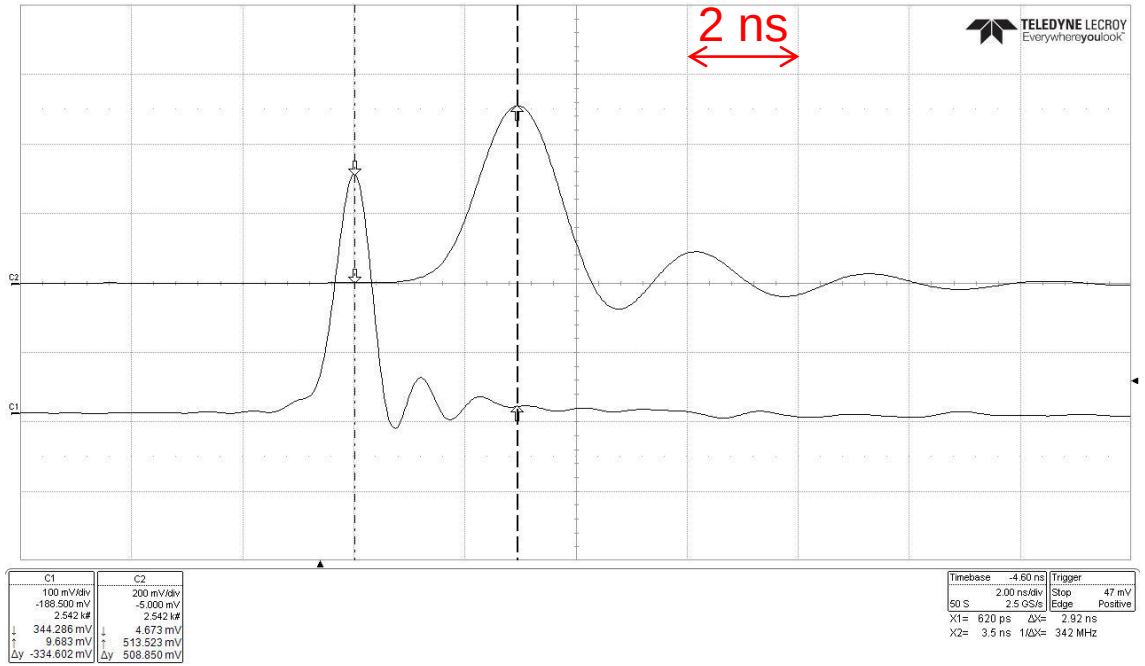


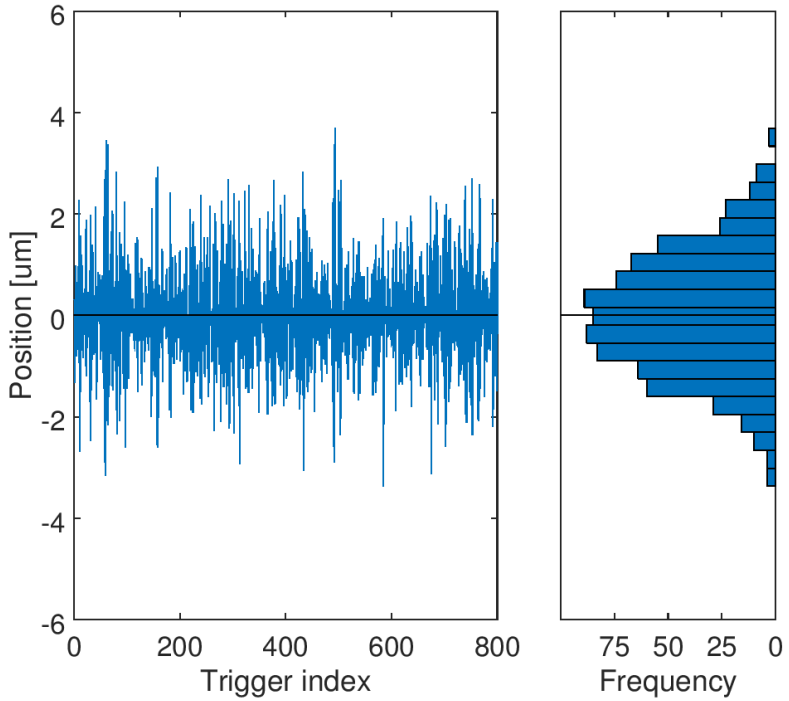






Diode processor performance





Latency measured in lab:
Diode processor only: **2.9 ns**
+ supplemental stage: **10.4 ns**

2.9 ns would scale to ~1.0 ns for CLIC-optimized design

- Diode processor with supplemental stage instrumented on P1; conventional processors (resolution = 200 nm) on P2 and P3
- Diode resolution estimate ~325 nm

Summary

- Best **IPBPM resolution** ever measured: **~20 nm**
- Best **IP feedback** performance:
  - 1-BPM mode
    - Smallest jitter of corrected bunch (**single-sample**) = **74 nm**
    - Reduced to **50 nm** by **integrating** 10 samples
  - 2-BPM mode
    - Smallest jitter of corrected bunch (**single-sample**) = **68 nm**
    - Reduced to **41 nm** by **integrating** 5 samples
- Best **upstream feedback** performance: P2, P3 jitter of **~200 nm**
- Diode processor achieves **~ns latency** and **<1 μm resolution**