FireDAQ for FLAME – architecture and hardware considerations

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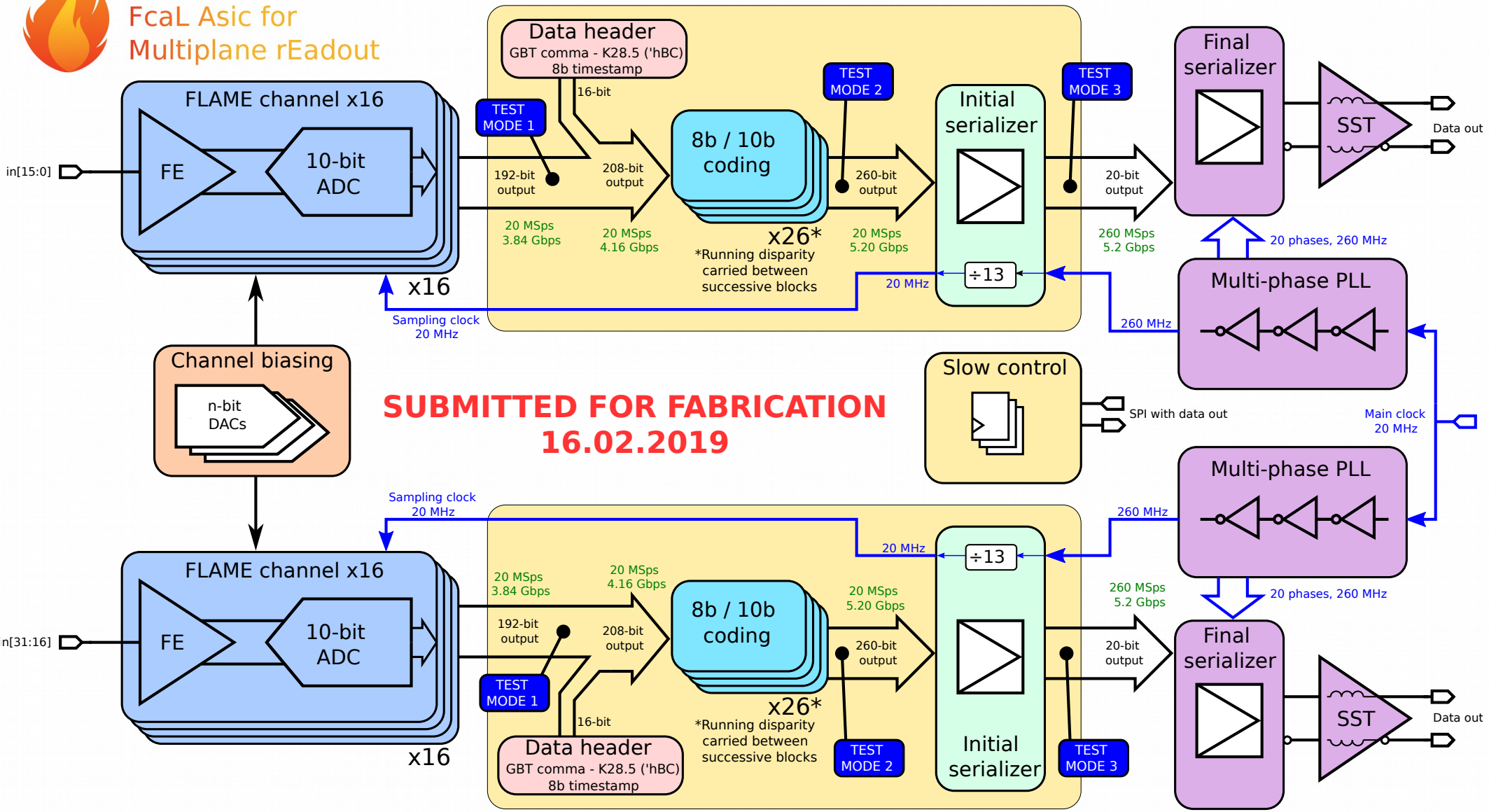
Outline

- New readout scheme
  - New Trenz Electronic module with Zynq UltraScale+
- FPGA firmware details
- System bandwidth (maximal event rate)
- Work to be done (and by whom...)

FLAME ASIC architecture

FLAME
FcaL Asic for Multiplane rEadout

•Two 16-channel, fully functional blocks → two “ASICs” in one padring to save the PCB area and maximize the instrumented sensor area



Trenz Electronic TE0808 modules

€999.00 (1,188.81 € gross) *

Prices plus VAT plus shipping costs

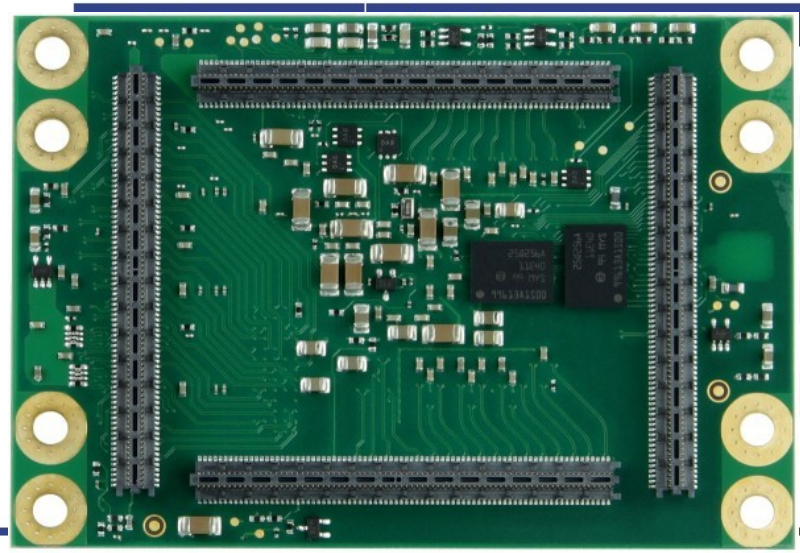
expected to be available on 24-Nov-2018

1 | Add to shopping cart

Remember

Order number: TE0808-04-09EG-1EE

In Stock: 0



Description | Downloads | Resources

Product information "UltraSOM+ MPSoC Module with Zynq UltraScale+ XCZU9EG-1FFVC900E, 4 GB DDR4"

The Trenz Electronic TE0808-04-09EG-1EE is a MPSoC module integrating a Xilinx Zynq UltraScale+ ZU9EG, 4 GByte DDR4 SDRAM with 64-Bit width, 128 MByte Flash memory for configuration and operation, 20 Gigabit transceivers, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking connections.

All parts are at least extended temperature range of 0°C to +85°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options.

All this on a tiny footprint of 5.2 x 7.6 cm at the most competitive price. These high-density integrated modules are smaller than a credit card and available in several variants.

Slightly shorter than the credit card

Trenz TE080X baseboard for developement

UltraITX+ Baseboard for Trenz Electronic TE080X UltraSOM+

This could be very helpful, we are trying to buy one just now

€799.00 (950.81 € gross) *

Prices plus VAT plus shipping costs

expected to be available on 07-Dec-2018

1 | Add to shopping cart

Remember

Order number: TEBF0808-04

In Stock: 0

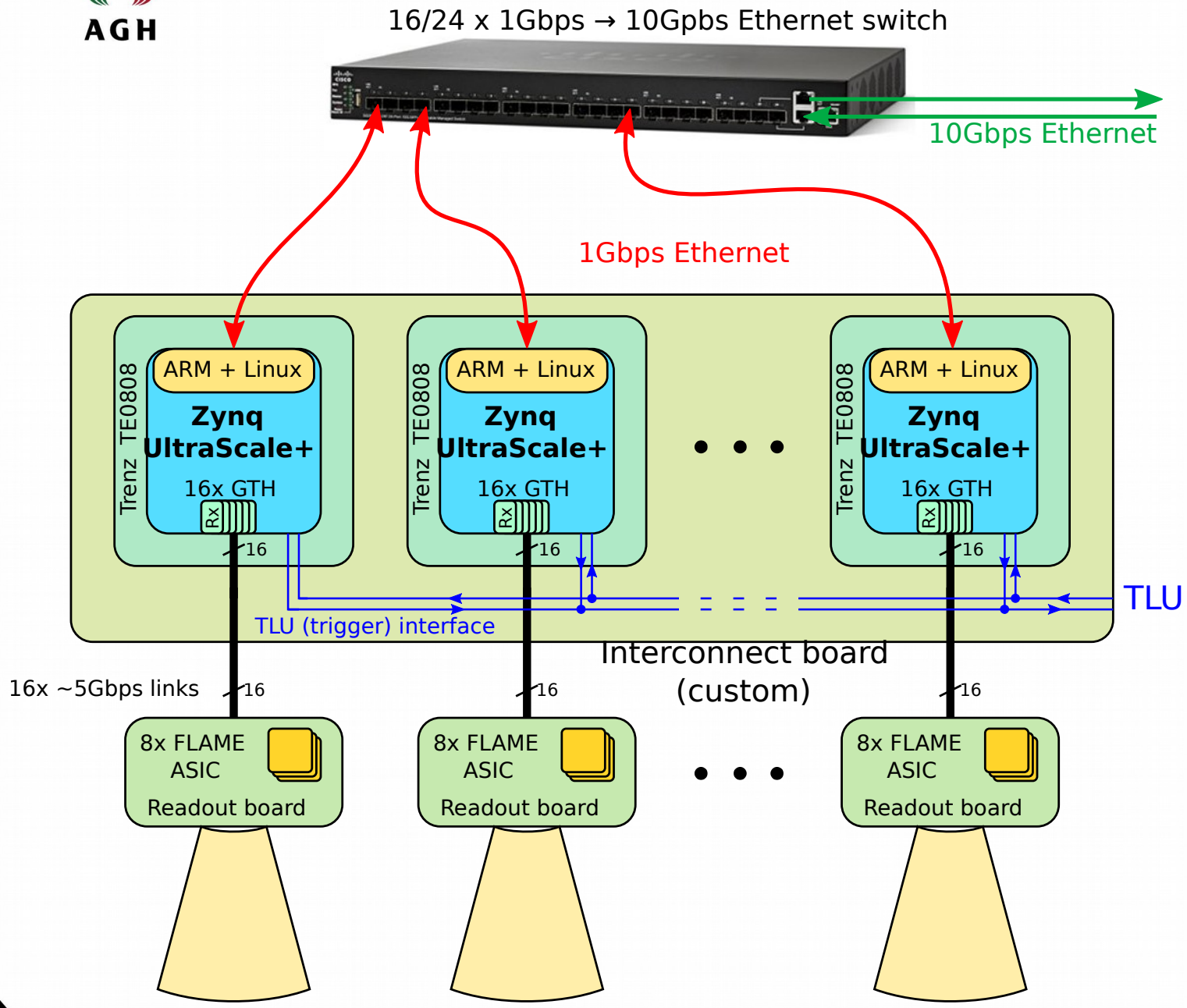
Quantity	Unit price
To 9	€799.00 (950.81 € gross) *
From 10	€719.10 (855.73 € gross) *
From 25	€679.15 (808.19 € gross) *
From 50	€639.20 (760.65 € gross) *
From 100	€599.25 (713.11 € gross) *
From 250	€559.30 (665.57 € gross) *
From 500	€519.35 (618.03 € gross) *
From 1000	€479.40 (570.49 € gross) *

Description | Downloads | Resources

Product information "UltraITX+ Baseboard for Trenz Electronic TE080X UltraSOM+"

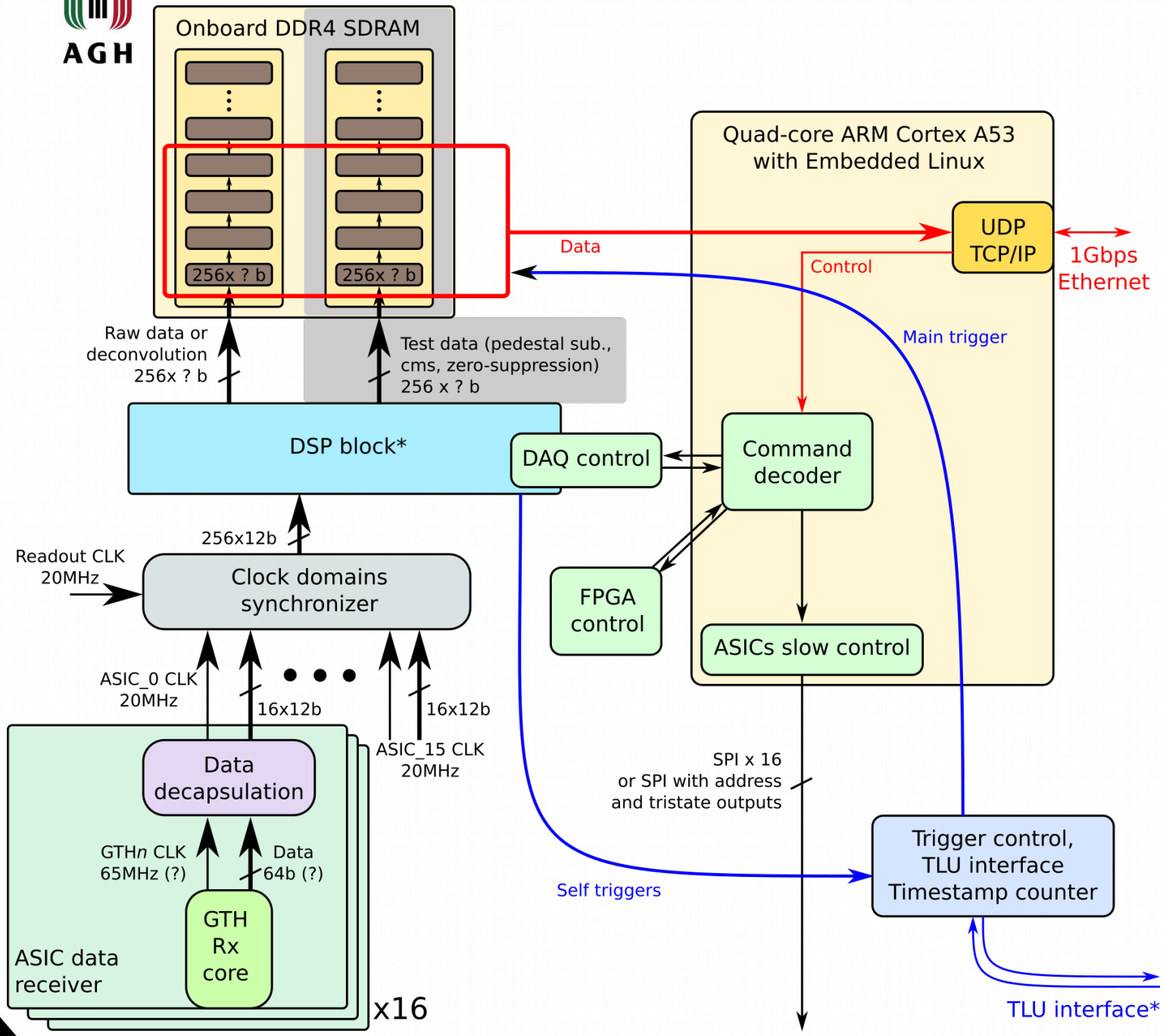
The Trenz Electronic TEBF0808 carrier board is a baseboard for the Xilinx Zynq Ultrascale+ MPSoC modules TE0803, TE0807 und TE0808, which exposes the module's B2B connector pins to accessible connectors and provides a whole range of on-board components to test and evaluate the Zynq Ultrascale+ SoMs and for developing purposes. The carrier board has a Mini-ITX form factor making it capable to be fitted into a PC enclosure. On the PC enclosure's rear and front panel, MGT interfaces and connectors are accessible, for the front panel elements there are also Intel-PC compatible headers available.

Proposed DAQ architecture



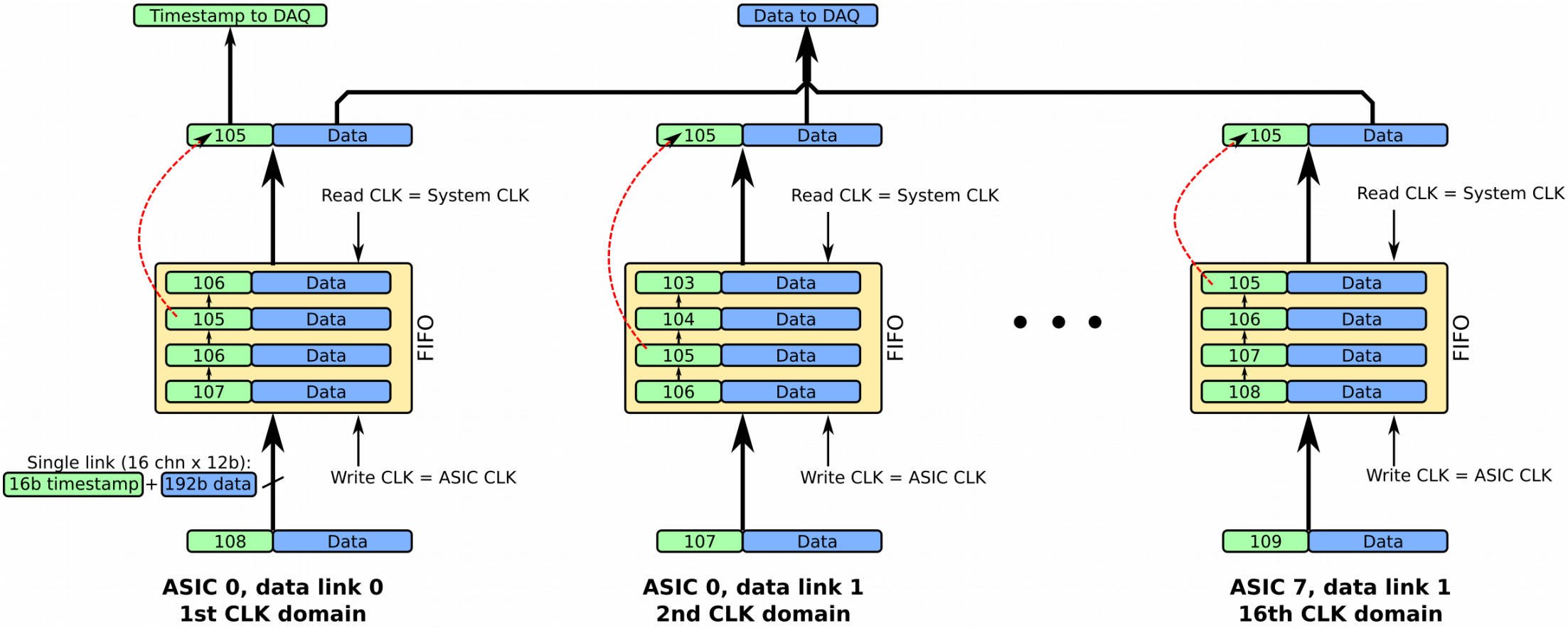
- 8 FLAME ASICs / plane = 256 channels = 16 data links (2 links per ASIC)
- New Trenz Electronic modules with Zynq UltraScale+ FPGAs available from the end of this year.
- 16 GTH transceivers / FPGA = 1 FPGA / plane
- Integrated ARM + embedded linux = 1Gbps Ethernet “for free”
- Simple Ethernet switch used as data concentrator
- One drawback – TLU (trigger) interface and timestamp synchronization not so straightforward...

Proposed DAQ architecture



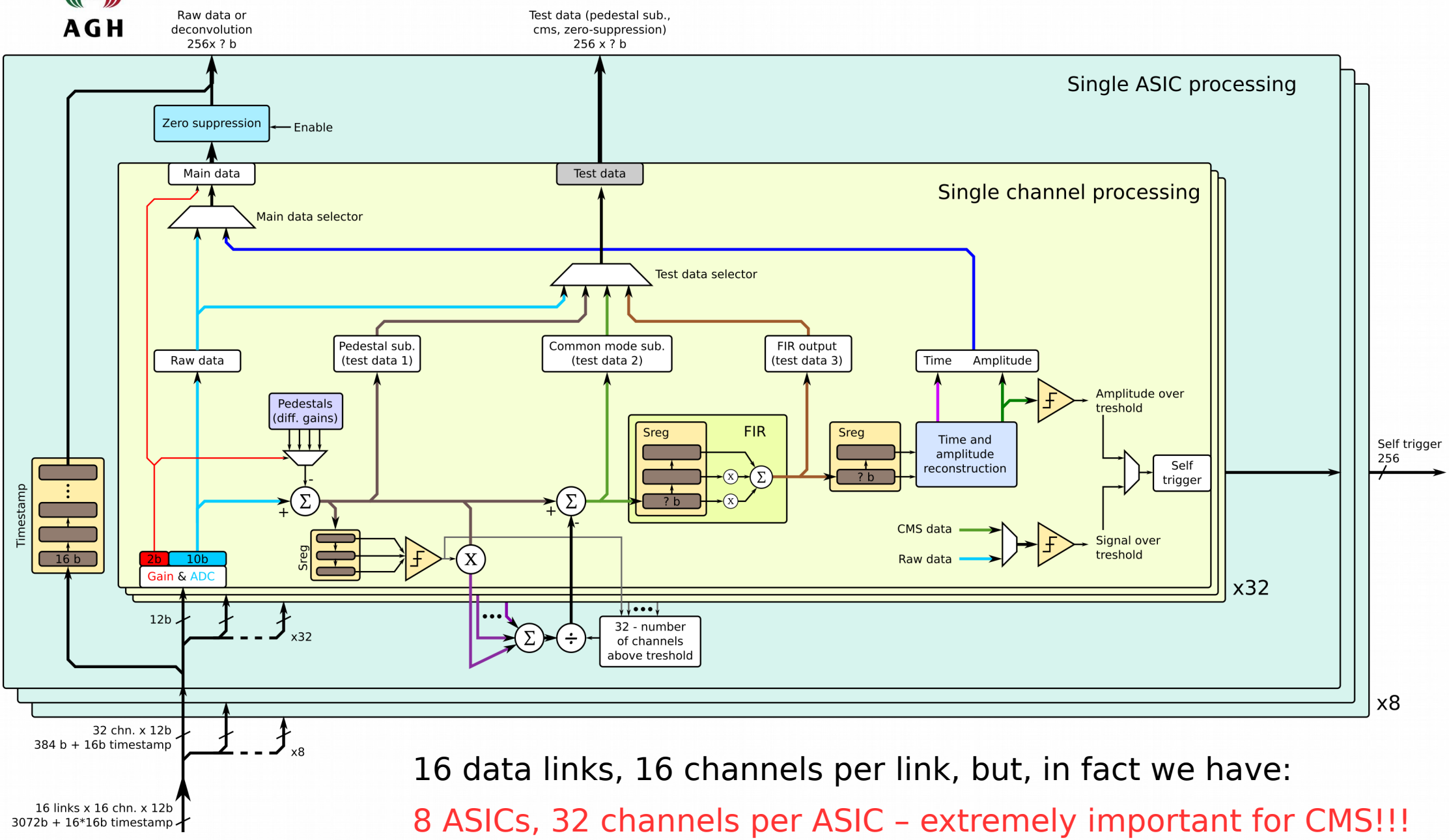
- Data from 8 ASICs (16 links) received by GTH transceivers and decapsulated
- Clock domains (16 receivers = 16 domains) synchronized with main CLK (see next)
- DSP (pedestal, cm subtraction, FIR, deconvolution, ZS)
- Data feed by FPGA logic into onboard RAM
- On trigger data read out by ARM and send out through 1 Gbps ethernet
- DAQ and ASICs slow control – by software on ARM (linux)

Clock domains synchronizer



- Clock domains synchronizer combines samples with the same timestamp and synchronizes clock phases
- If one ASIC / data link is dead, the synchronizer should build incomplete sample and inform DAQ that one data channel is missing and should not be processed, especially in cms procedure

DSP scheme



16 data links, 16 channels per link, but, in fact we have:

8 ASICs, 32 channels per ASIC – extremely important for CMS!!!

Work status and responsibilities

Firmware

- FLAME data receiver (*IFJ Krakow → ???*)
  - Done, but on different FPGA – have to be ported to UltraScale+ Zynq
- Clock domains synchroniser (*JINR Dubna*)
  - Probably done
- DSP (*JINR Dubna*)
  - Not started yet, waiting for software DSP model (*by me*)
- Control, TLU interface, timestamp synchronization, etc. (*???*)
  - Not started yet
- ARM linux, ethernet & software (*???*)
  - Not started yet

Hardware (PCBs)

- FLAME testboard, readout (detector plane) PCB (*AGH Kraków*)
  - Not started yet, waiting for final FLAME padring
- FPGA interconnection board PCB (*AGH Kraków*)
  - Not started yet, waiting for tests on Trenz Electronic module and some decisions...

Summary and questions

- New DAQ scheme proposed based on Zynq UltraScale+ modules
- Some firmware details still have to be fixed
- We should decide how to share the work on firmware

  1) **Who can help – Krakow / Dubna / somebody else?**

- We should buy more TE0808 modules on the beginning of next year

  2) **How many layers are we going to use in testbeam next year and how many in the future?**

  3) **Can anyone buy a few more modules?**