HBU6_HD.

Status

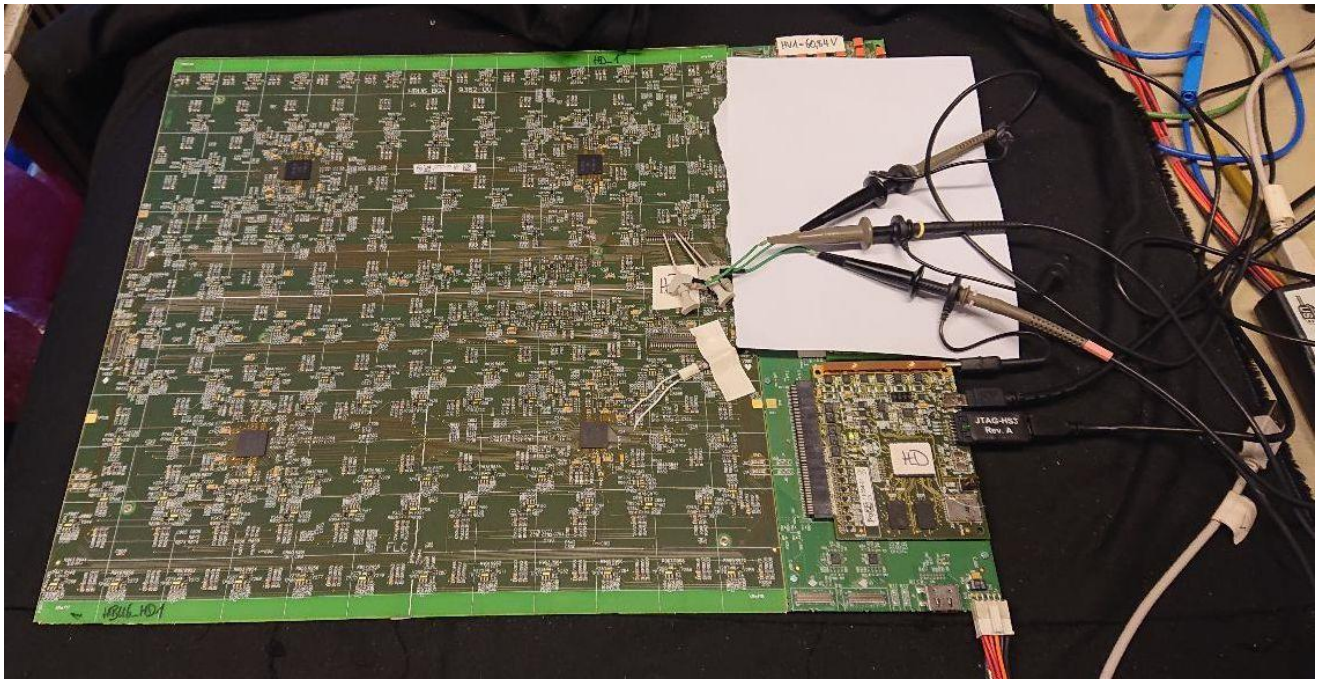
Zhenxiong Yuan, Mathias Reinecke

CALICE main meeting

CERN, October 1st, 2019

Status Commissioning HBU6_HD

- New child in HBU family: HBU6_HD with KLauS ASICs (cooperation Uni Heidelberg, DESY)
- Two HBU6_HDs with KLauS5 ASICs, 4 new POWER4 boards completed.
- First commissioning at DESY Sept. 2019: Zhenxiong, Mathias.



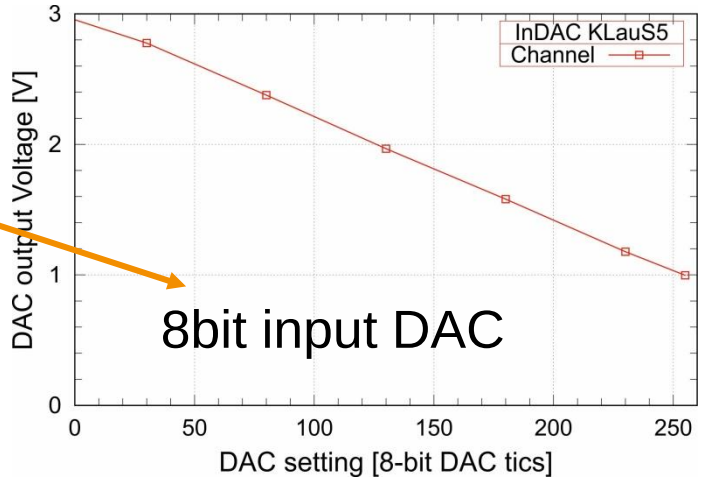
HBU6_HD DAQ – differences to current DAQ

- Finally, HBU6_HD is supposed to run with our CALICE DAQ: Synchronously, in parallel to our current HBU modules.
- Following differences have been identified:
  - Number of slow-control bits.
  - Readout data in same data frame, but with different length and interpretation in DAQ.
  - KLauS is active continiously, no sequence: Data-taking, AD-conversion, readout. No timing control by „start_acquire“, except in power pulsing (precise enough?).
  - Event timing info: No Bunch-X-ID in KLauS, only 16bit TDC => limits for „timeout“

- Requires new DIF firmware and Labview DAQ (at first: USB, single layer).

Status Commissioning HBU6_HD

- All supply and reference voltages (smoke test): **OK**
- Resets, Clocks and their signal quality: **OK**
- Slow control programming: **OK**
- Slow control Labview
  (SC data to and from file): **OK**
- Main DAQ Labview: **OK, preliminary**
- DIF firmware: **OK, preliminary**



- I2C communication: **OK, but slow**. From oscilloscope: 800pF (huge, >6x higher than expected) capacitance on the I2C lines. Reduced I2C speed to 300kbit/s. Now works fine. Not enough time for debugging.
- I2C data readout: **Not OK**: Only one ASIC sends (not understood) data on I2CA. Second ASIC only deliveres „empty frame“ pattern. Reason unknown (all signals to ASICs look fine, DIF delivers complete data frames, KLauS OR36 output shows accepted ext. triggers). => Tests ongoing.

Conclusion and Outlook

- HBU6_HD sends signs of life (slow control, first dummy data frames). Slow-control Labview and preliminary versions for DIF firmware and main Labview available. No big show-stopper so far.
- Problem of I2C readout is currently not understood. Needs Debugging.

- Next steps after debugging:
- Characterization on single board level (lab + testbeam).
- Integration into CALICE DAQ with multi-layer setup, including central clock distribution (CCC) and parallel configuration, readout (LDA) is final step. Probably, changes in LDA firmware required.