CALICE/ILD SiW-ECAL
an adaptative design

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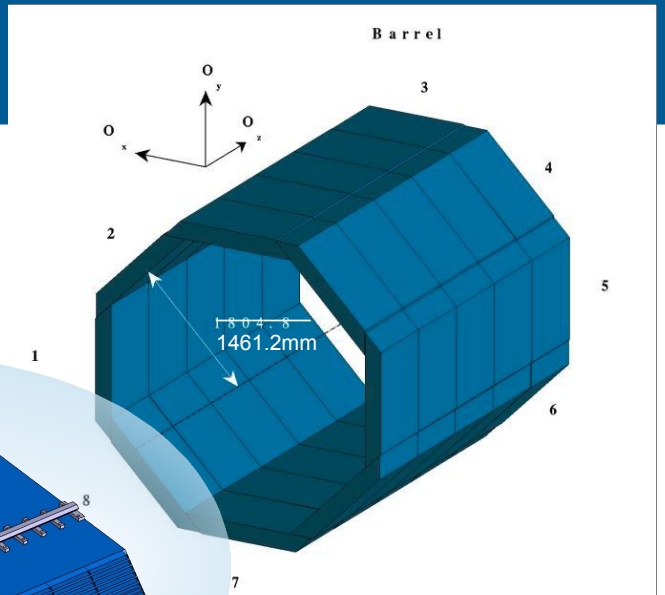
TNA support + WP14

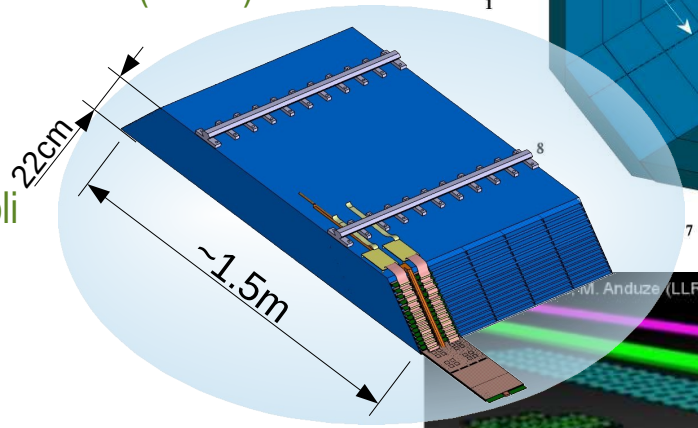
SiW-ECAL geometry

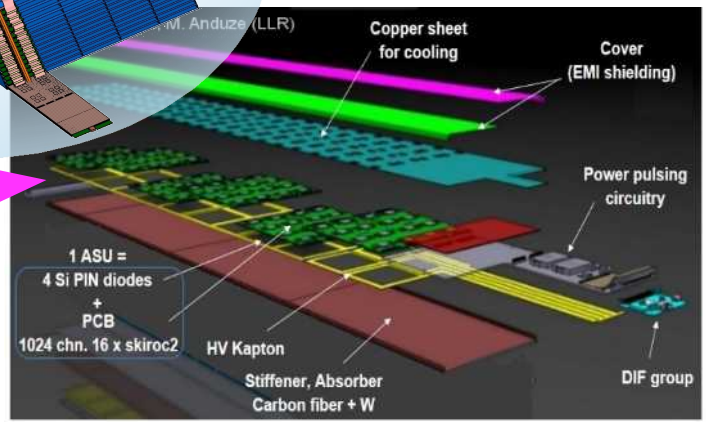
Approximated dimensions for the small model

- for exact dimensions : see ECal Technical Design Document by Henri Videau (LLR), Marc Anduze (LLR) and Denis Grondin (LPSC) available on https://llrbox.in2p3.fr/owncloud/index.php/s/eeVeAlyv8o27VRF
  - Small ILD with 26 layers ⟶ §5 of TDD.
- Modular construction : modules of 5 towers of 13 alveoli
  - slabs double sided with embedded RO electronics ⊃
  - Slab dimensions : 186mm × (1472mm – 1081mm)

    (for R=1462mm, th=223.2mm)
  - 8+ – 5+ square ASU of 186mm.
    - ASUs = 4 SI diodes from 6'' wafers,
      1024 chan of 5.5×5.5 mm²,
      16 SK2 chip of 64 chan.







+ vert. mirror

SiW-ECAL Building blocks: SLAB's & ASU's

R&D for "mass production" and QA

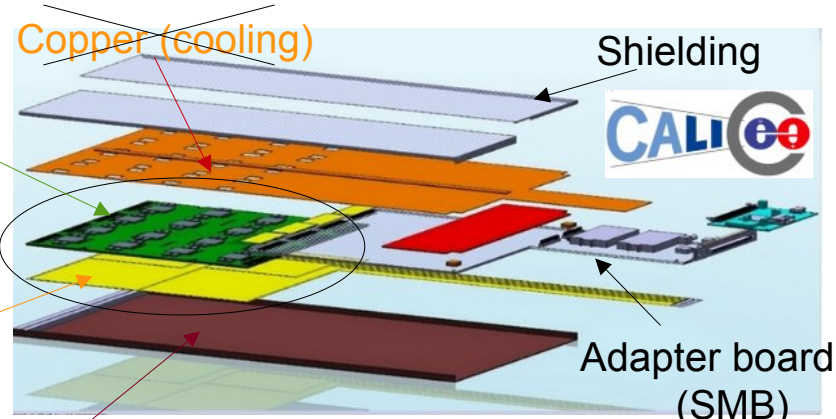
- Quality tests & preparation of large production
- Modularity ⟶ ASU & SLABs
- Choice of square wafers
  - (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 (1.5) m, $|Z_{Endcaps}|$=2,4 m)

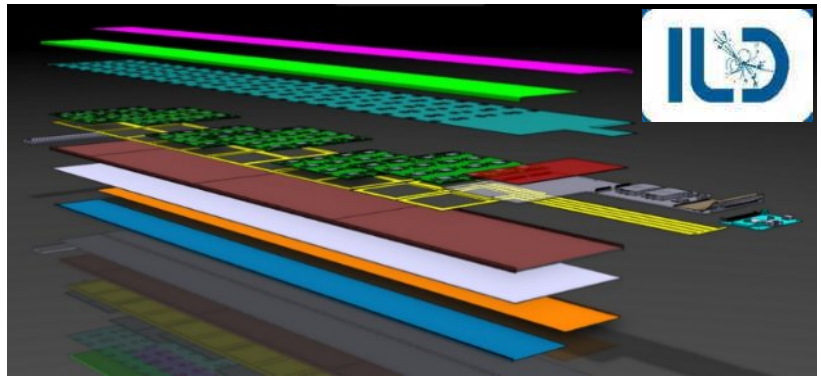
- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types) – 16 (2 types)
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m²)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - ≠ lengths and endings

Tests of producibility

Tests of feasability



U layout of a **short slab**



U layout of a **long slab**

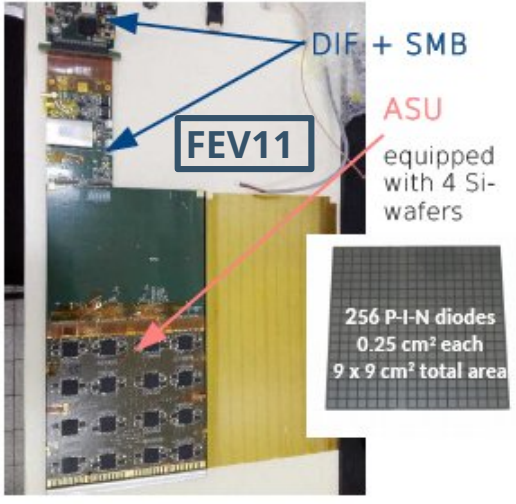
ASU: 12+ years of R&D

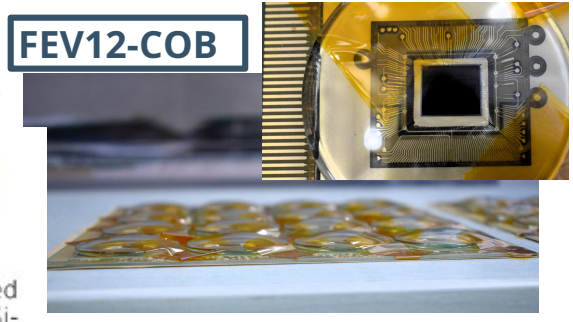
Most complex element: electro-mechanical integration

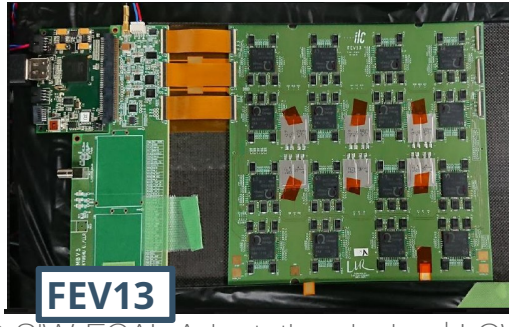
- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints

3 versions working

- with S/N_{Trig} ≥ ~12 (for 320µm)







Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	Slab:FEV11	10 units, 320µm	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	10 SLAB: 5 FEV11 320µm 5 FEV13 650*µm Compact stack	SK2 & SK2a (⊃timing)	Improved S/N (1/64 masked ch.) Timing...
1st COB	2019	FEV12-COB	1 wafer, 500µm	S/N ~ 22

1st “electric long slab” for ILC/ILD

Scale to support electronics

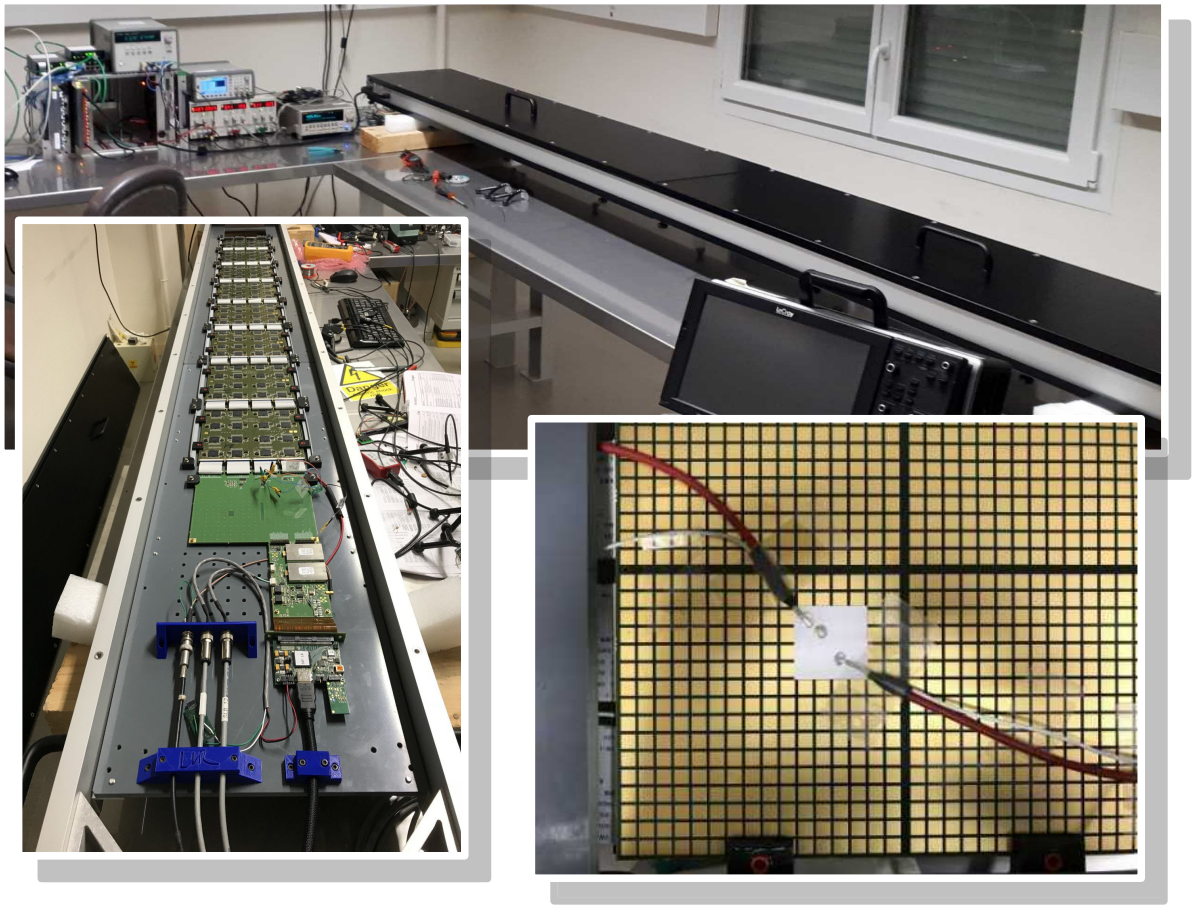
- Support of interface boards + 12 ASUs (DBD)
- 2+6+4 ASUs = ~3.2 m Max length for Endcaps
- Total access to upper and lower parts
  - 320µm Baby wafers (20×20 mm², 4×4 pixels)

Mechanical characteristics

- Movable: table and to beam test
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm for 3m
- No electrical contacts scale / cards

Shielding vs Light and CEM



Electronics adjustments

Path length induced reflexions on clock line

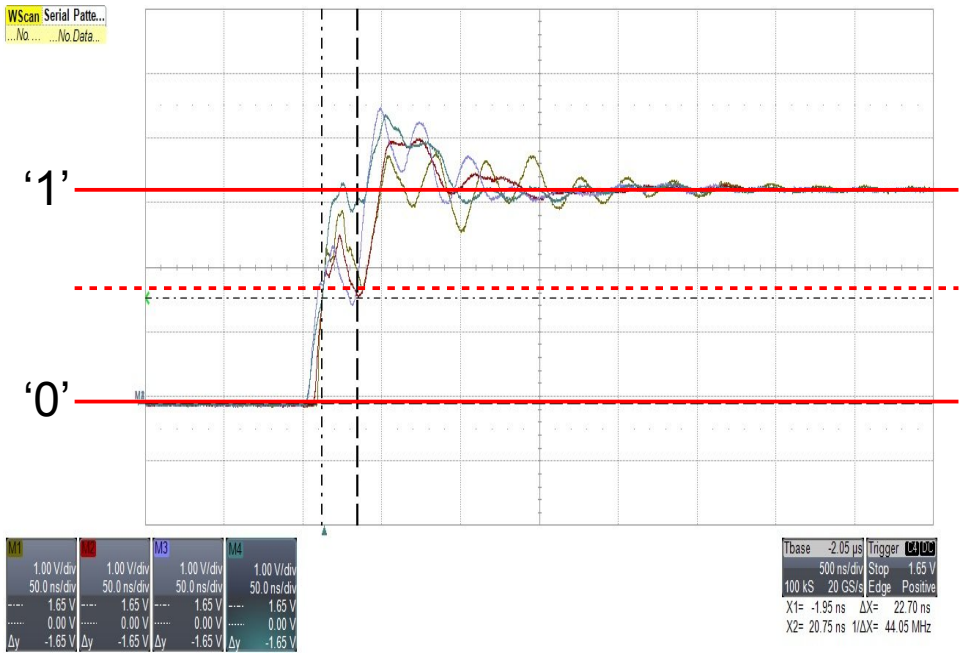
- Fluctuation over logical level
- Extra clock tick ⟶ bad ASIC configuration
- RC filter adaptation (Sigrity simulation)

Impedance adaptation required depending on length

- **Limited to 8 FEV11** + baby-wafers

Noise in the signal

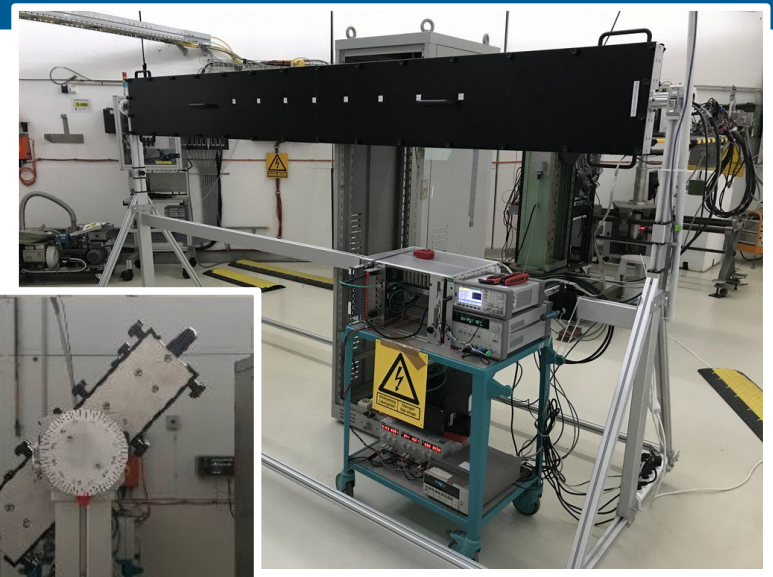
- High frequency perturbation in the HV line
- Solved by RC filters on the HV line
  - Possible back-propagation of ASICs noisy channel through HV ?

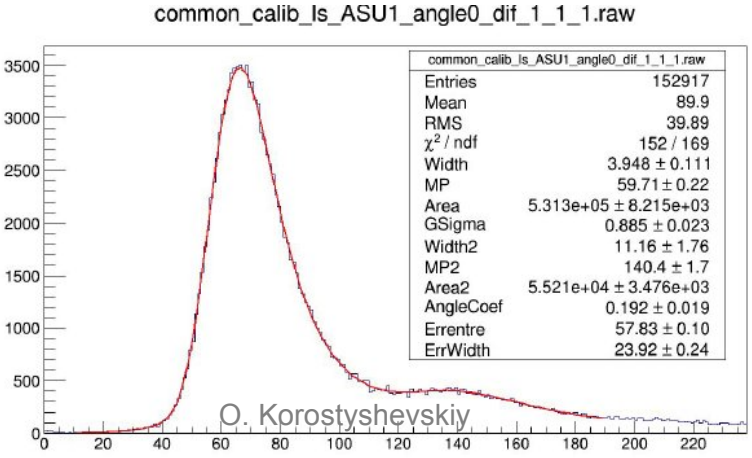


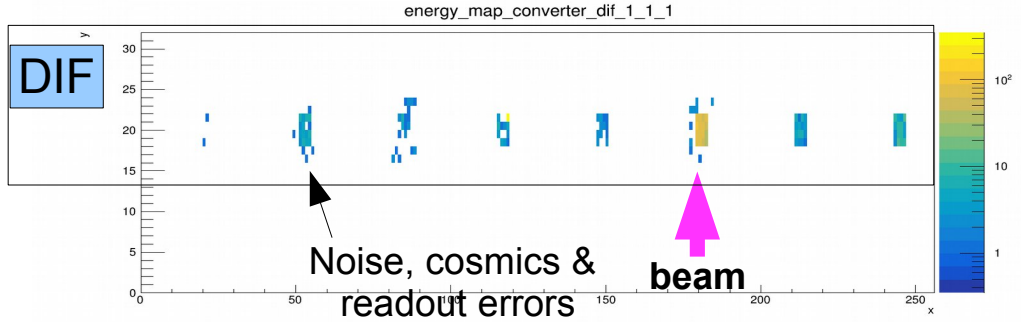
DESY-2018 beam test

2 weeks beg of July: full test of all prototypes:

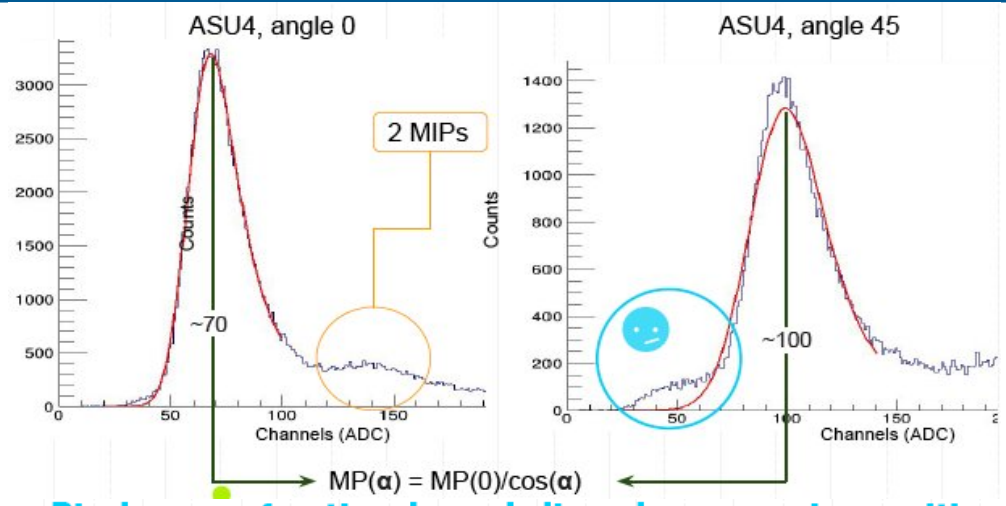
- Electric long slab: **8 FEV11** + baby-wafers
- Very clean response to “mip” (punch through e-)
- 1/2h beam on each ASU @ 0, 45, 60°

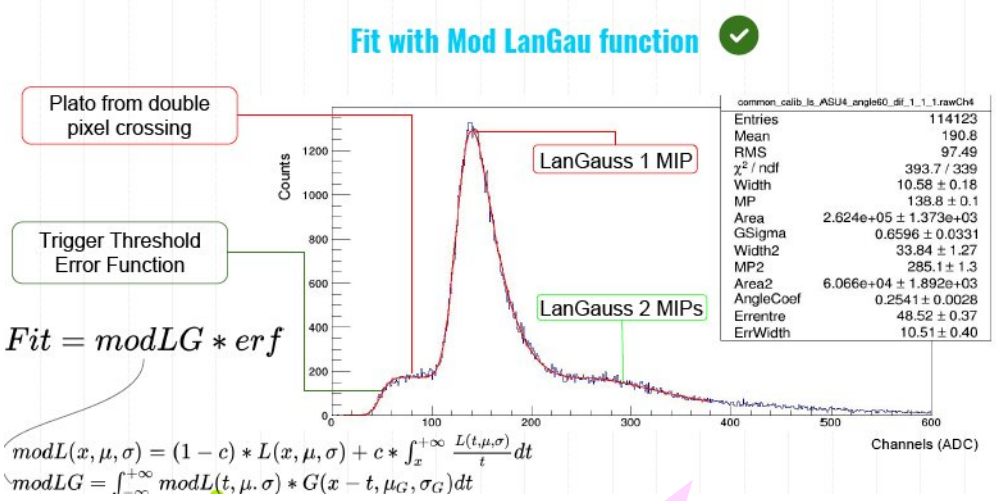


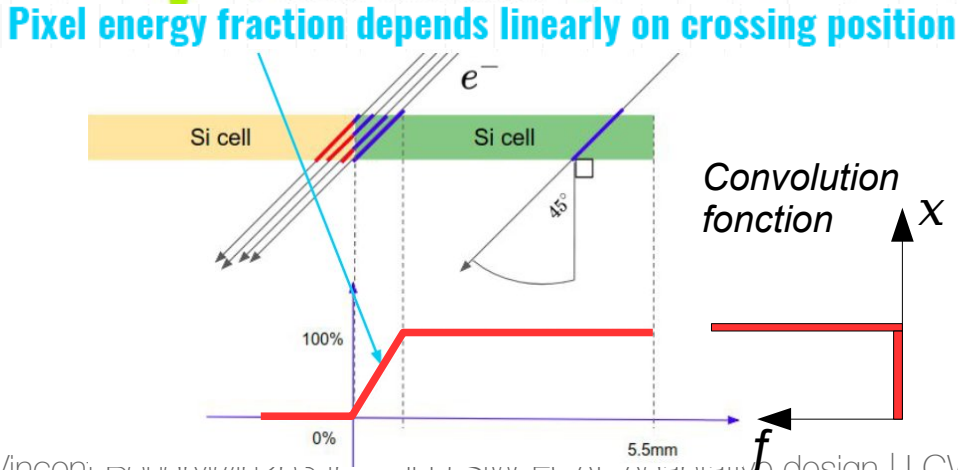


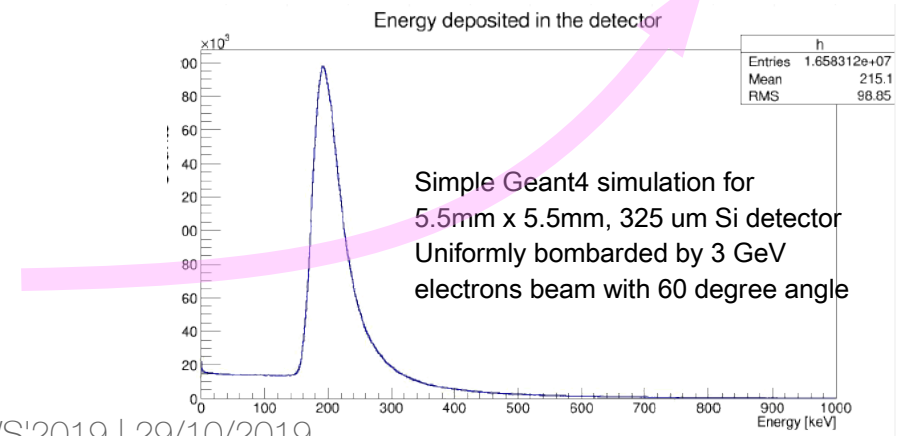


Mip analysis





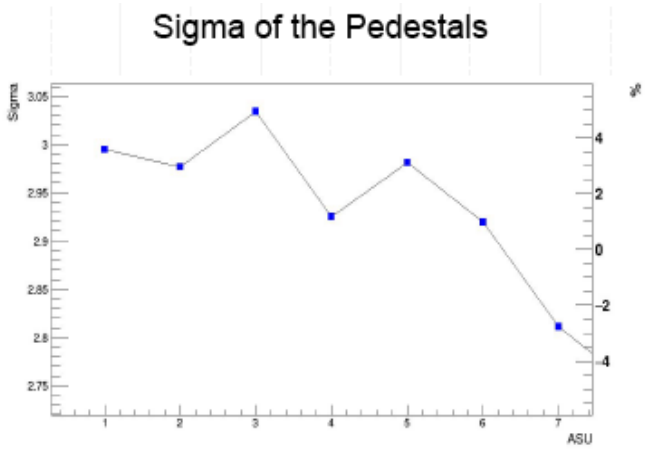


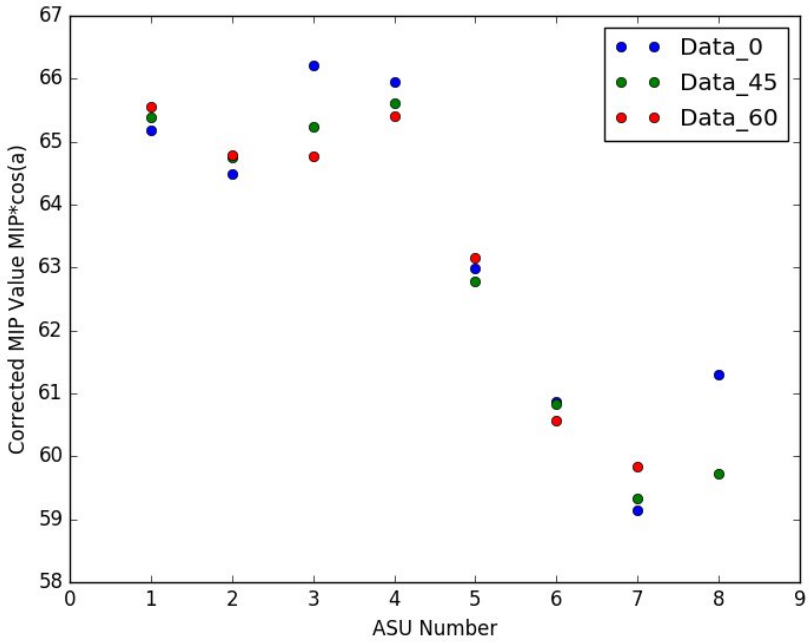


MIP response vs position

mip MPV *cos(θ) vs ASU#

- OK for 4 1st ASU's
- Small drop ~of signal ~2%/ASU for ≥ ASU#5
- Also hints similar drop on σ_{ped}





⇒ Voltage & Gain drop ?

Power pulsed mode with ballast et end of slab
(or just random build-up effect from chip variability ?)

MIP fluctuation

2 systematic effects has been identified

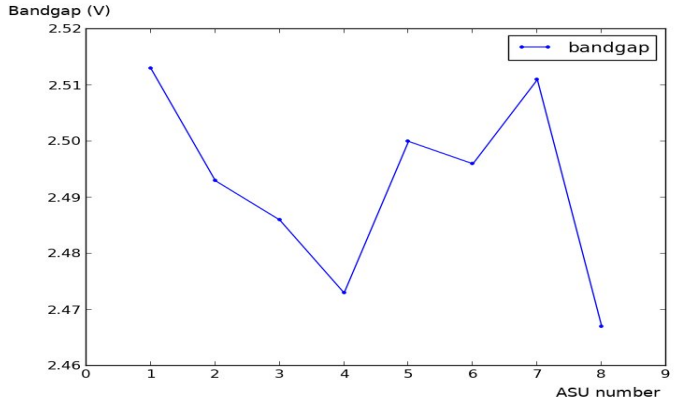
- Bandgap discrepency (over 128 ASICs).
  - σ=19.2 mV peak to peak=200mV
- Voltage linear decrease over slab length

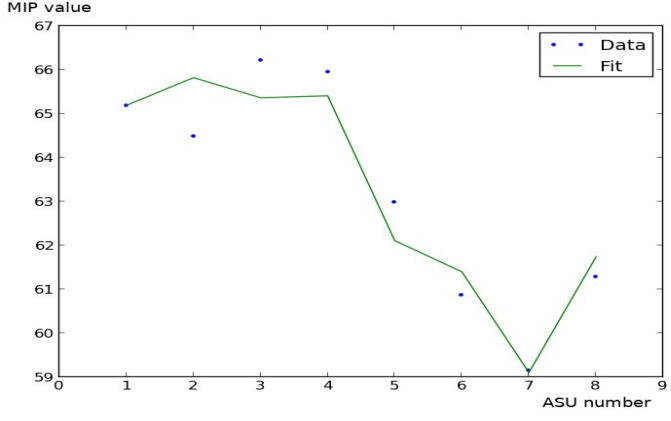
Curve shape can be fitted by weighted sum of these two effects

$$MIP(\mathrm{ASU}) = a * \mathrm{ASU} + b - c * \mathrm{bandgap}(\mathrm{ASU})$$

Solutions

- Reduce bandgap in ASIC design (already reduced in Skiroc2a version)
- Compensate bandgap by software
- Select ASICs to mitigate fluctuation
- Use fixed length power supply to avoid discrepancy





Requirements for an improved design

Better handling of signal:

- FEV13 much improved design
- FEV12-COB: ≠ problems on ASICs
- Improved ASIC: SK2a

HV distribution per ASU

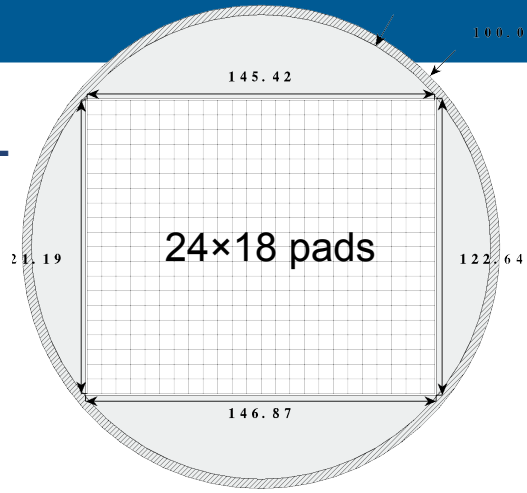
- avoid noise back-propagation ?

LV per ASU ?

- or better regulation near / on ASIC ?
  - dissipation ?
- Flat Capacitors on board
  (but discontinued by Murata)

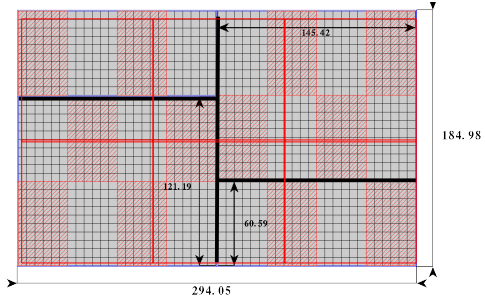
Longer ASUs ? ~ new ILD SiW-ECAL

- e.g. 16 ⟶ 24 ASICs
- reduced # of ASU & connections:
  - 8 ⟶ 6 ASU's in barrel
  - 12 ⟶ 8 ASU's in endcaps



Use Larger wafers ?

- Geometry compatible with 6'' and 8'' matrices
- ⚠ incompatible partitions:
  - 2×16 = 32 cells ≠ 27 = 1.5×18 cells
  - 3×16 = 48 cells ≠ 44 = 2×24 cells



Going to ∅ 200mm × 725µm Wafers…

From CMS HGCAL development & Hamamatsu contacts: future is 200mm (8'') ingots, 725 µm thickness

- ≥ June 2020 ?
- Mechanical constraints → ~187 mm alveoli, ~12 cm wafers

Improved performances due to thicker wafers:

- EM resolution: $\sigma(E)/E \propto 1/5\sqrt{(1+th/100\mu m)}$
- Noise ~ C ~ width²/th
  - depl. Voltage @ cst conductᵧ ~ th² → leakage current stable ?
- Signal ~ th ↗,

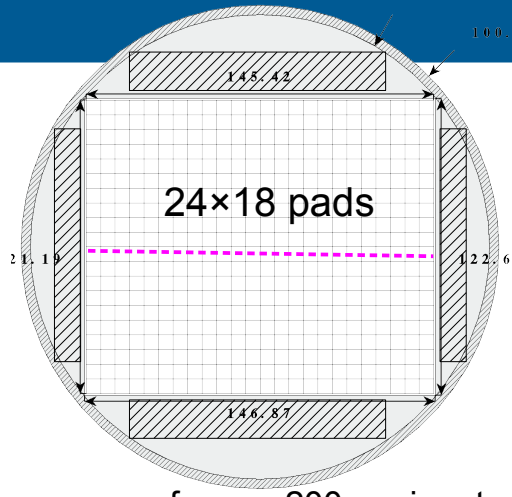
  S/N ~ th² × 2 for 725µm vs 500 µm (5 from 320µm)

  → Larger cells ? → Less electronics → Less heat, less €€, …

  → less gain ? → less heat OR less noise → faster readout, less heat

  → lower auto-trig thr, (1/3 mip @ 4σ) → 100% efficiency for mips

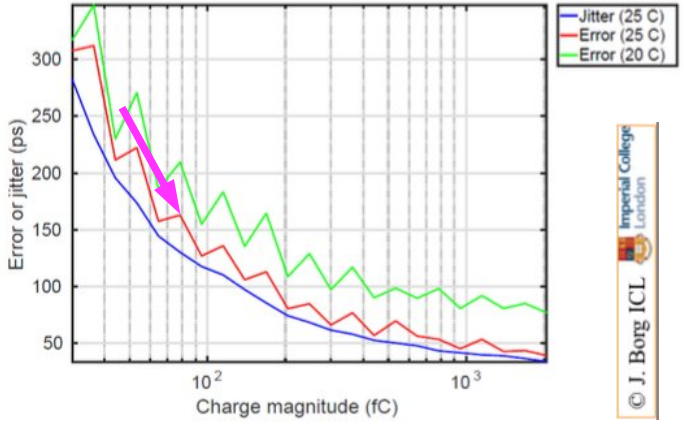
  also Improved timing perf (esp. for mips)



+ ½ wafers

wafers on 200mm ingot ; 63 % use of surface
with side matrix for det. margins : 87 % ?

Time Jitter



© J. Borg ICL

Implication of HL schemes

Higher $\mathscr{L} \Rightarrow$

- Occupation / bunch train ↗
  - More memory for events
    - But large margins

Higher repetition rates × longer bunch

- Power = $f_{rep} \times \sum P_{ASIC_part} \times \tau_{spill_part}$
  - $\tau_{spill} = \tau_{Ramp\text{-}up} + \tau_{Train} + \tau_{Conv}$
    $= \mathcal{O}(\mu s) + \{ \ldots \} + \mathcal{O}(100's\ \mu s)$
    - $\tau_{Train} = \Delta T_{bunches} \times N_{bunches}$
    - $\tau_{Conv} \propto$ (occupancy + Noise ≥ thr.)

Critical also for Power budget

⇒ Full ZERO suppr. needed

HL-ILC:

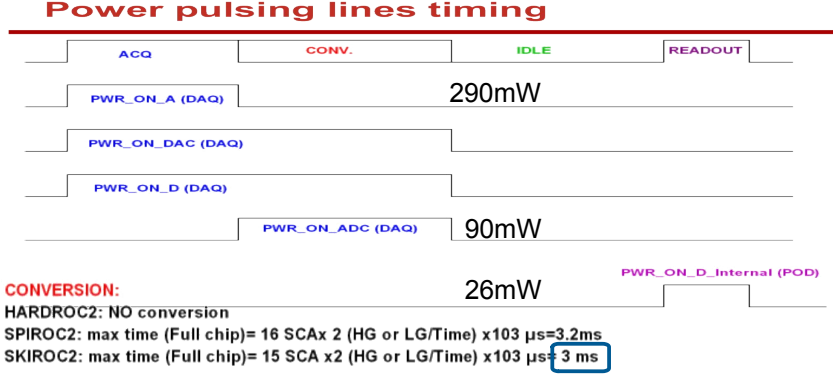
- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : τ_{Train} : 1 → 2 ms
- f_{rep} ×2 (3): 5 → 15 Hz

Dominated by ACQ time:
P(~25µW/ch) × 6

HL-CLIC:

- $\mathscr{L}$ × 2
- $N_{bunches}$ → : τ_{Train} : 176 ns
- f_{rep} ×2 : 50 → 100 Hz

Dominated by Set-up &
Conversion time: P (~82µW/ch) ×2

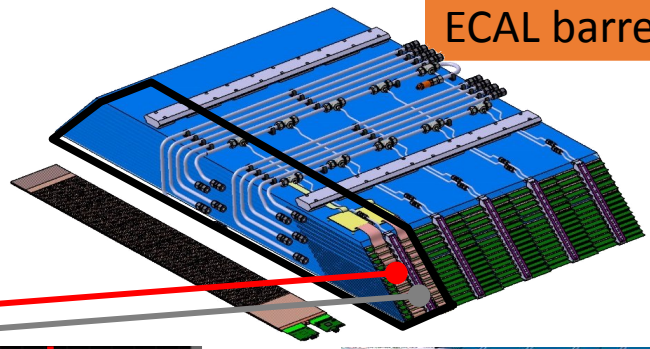


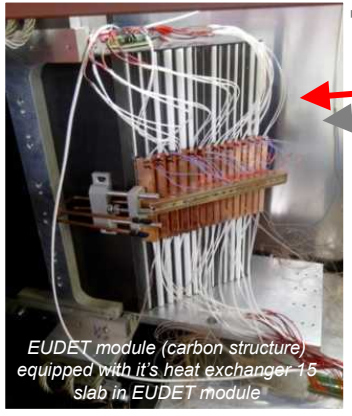
SK2 chips

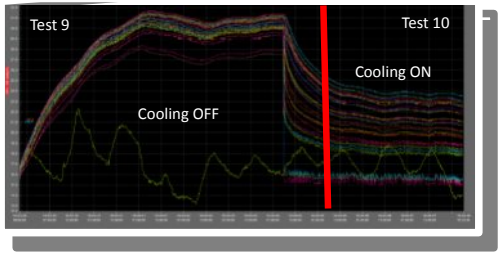
64 ch full conversion

Passive cooling

ECAL barrel



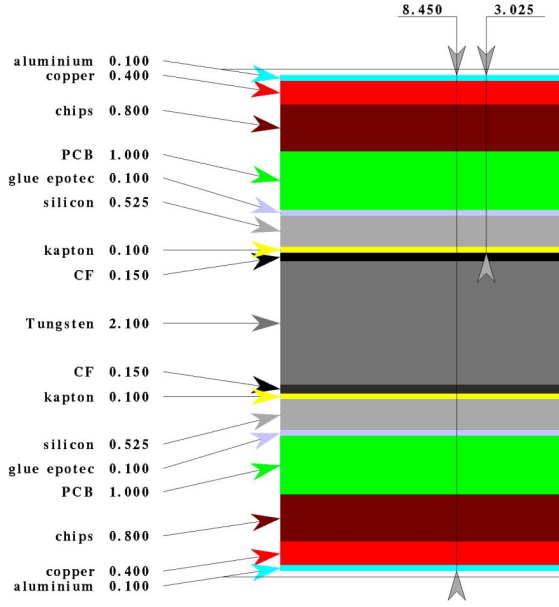


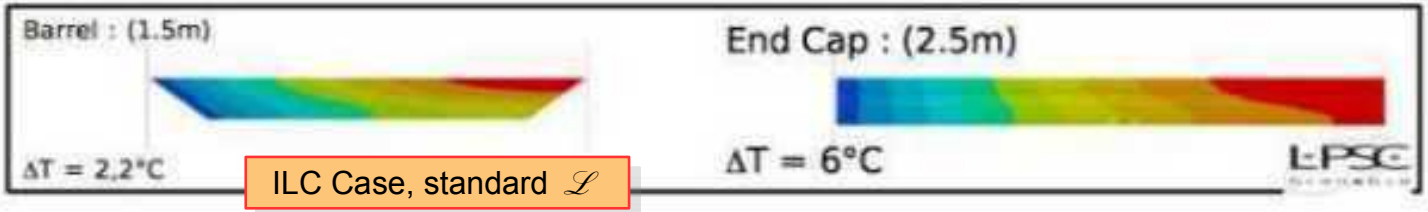


ECAL end cap

First tests results in line with simulations

3.0mm Det
+ 2.1mm W



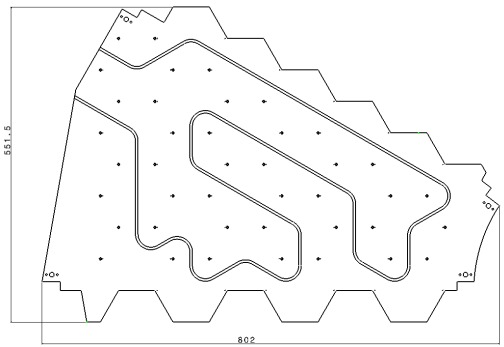


ILC Case, standard $\mathscr{L}$

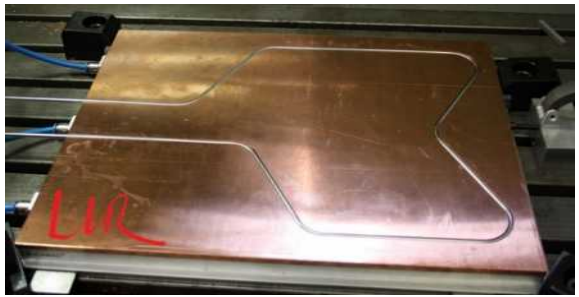
AIDA report 08/18
http://cds.cern.ch/record/2624680

Active cooling → 'Continuous colliders'

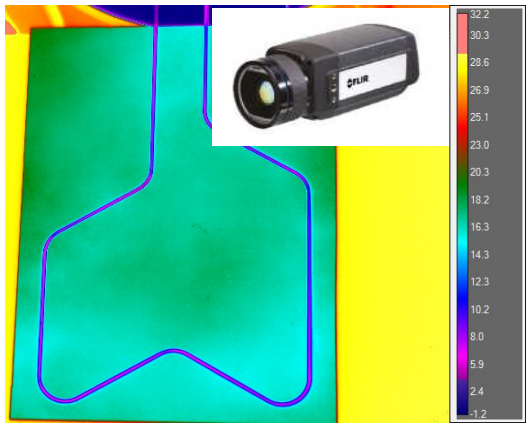
R&D using CMS studies (Courtesy of Th. Pierre-Emile from CMS-LLR group)

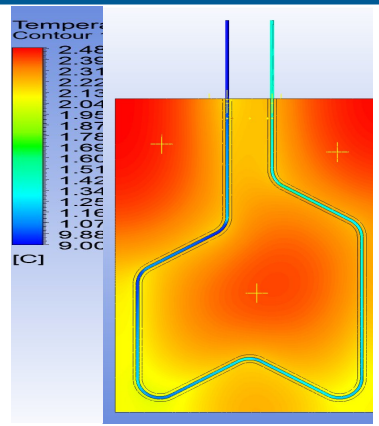


Copper plate prototype dimensions information



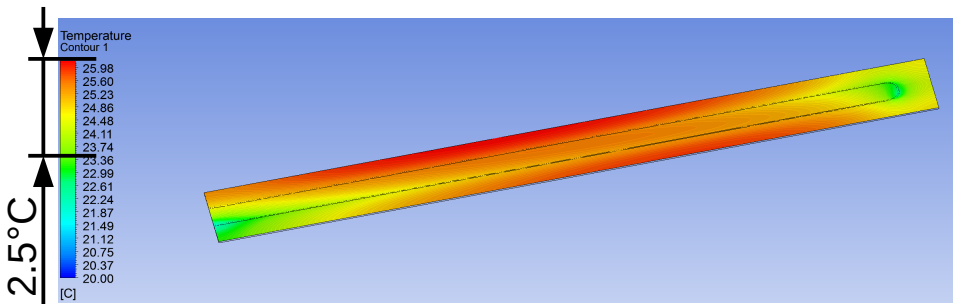
Pipe insertion on a cooling prototype for FEA correlation



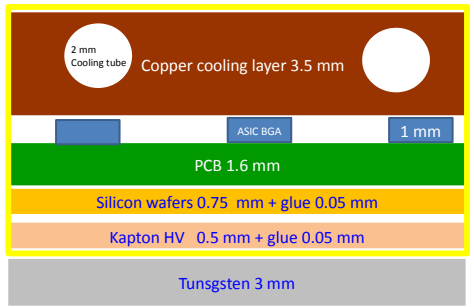


Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling



Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe



+3mm of Copper/Layer

= 2× cont. operation of a SLAB

Conclusions & prospectives

ILD Long Slab prototype

- **1st readout over long chain**: design R&D, power distribution, grounding; connexions between ASU's
  - ⇒ adjustment on HV, & LV distribution, clock distribution was required:

  ⇒ Decrease of response vs distance to PS (~10% in 8th ASU) ≡ 50% distribution, 50% ASIC variability
  - improved LV distribution or regulation
  - Need to complete test of ASIC prior to mounting for pairing

to be implemented in next versions of FEV's, BGA and COB

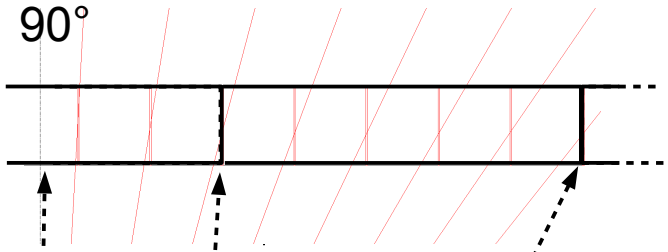
- 725µm thickness with 200mm (8") wafers ; 5.08 ⟶ 6mm cell size
  - Gain on almost all aspects
- Control for all elements prior to mounting: Wafers, ASICs, FEV, Connectors ⇒ DB of params

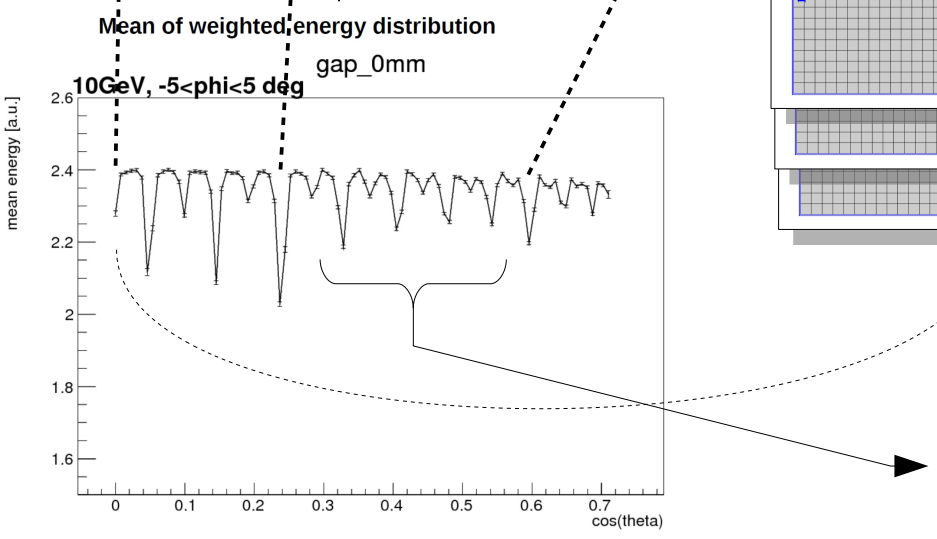
High-$\mathscr{L}$ schemes: Power $\propto \mathscr{L}$ (semi-trivially)

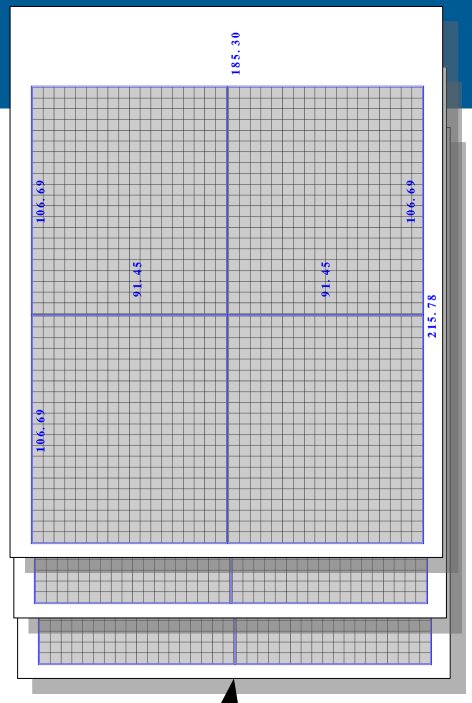
- Full 0-suppr chips and adaptative noise mitigation needed

Back-up

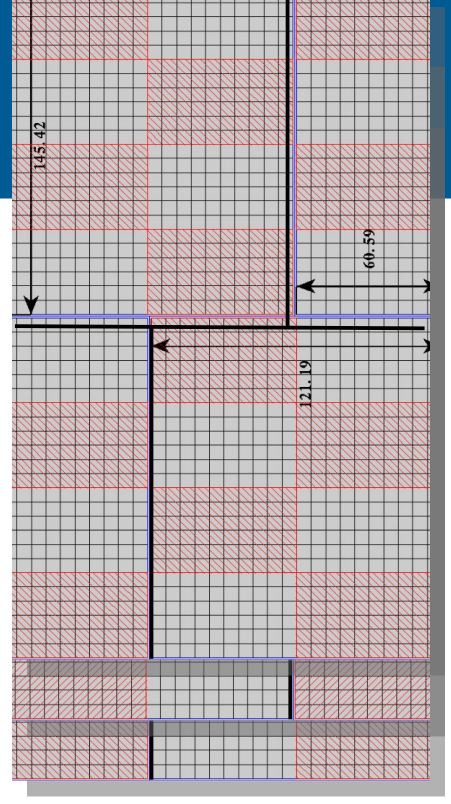
Reduced gaps



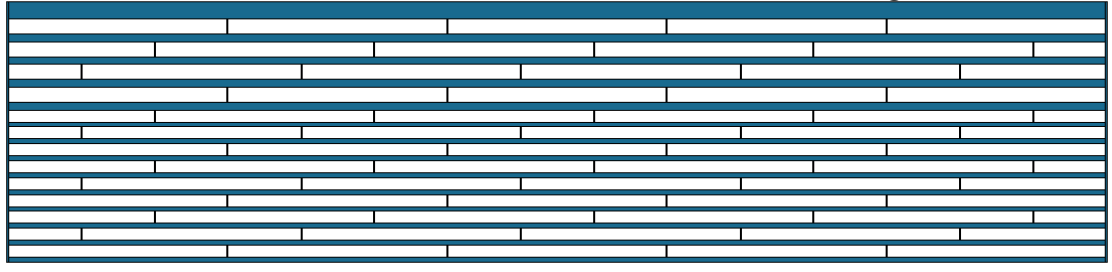




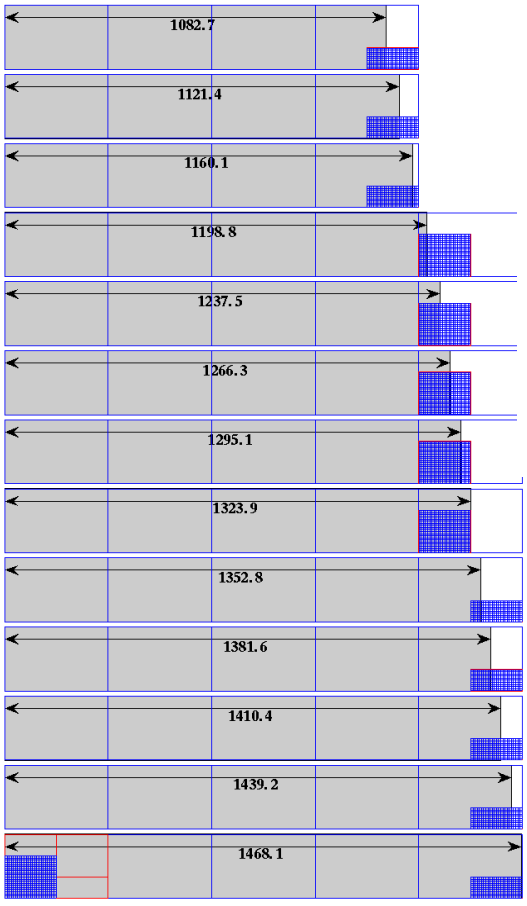
Reduced alignment of inter-wafer gap



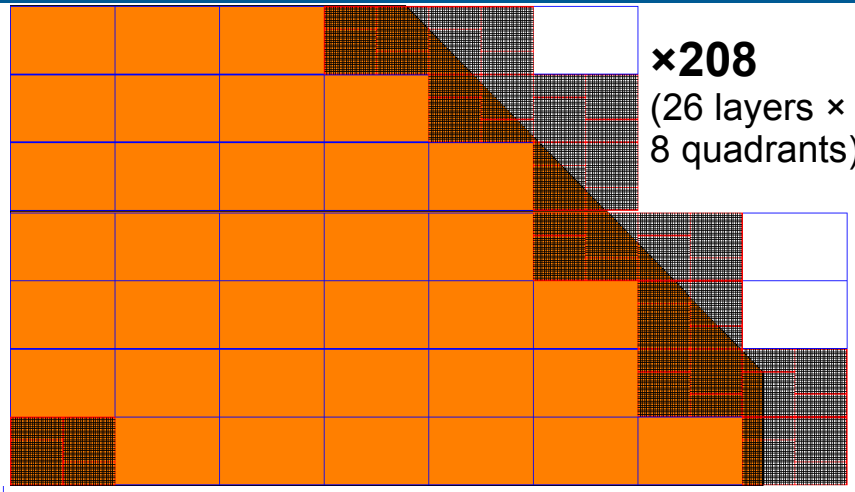
Possible *additional* reduction of inter-slab alignments



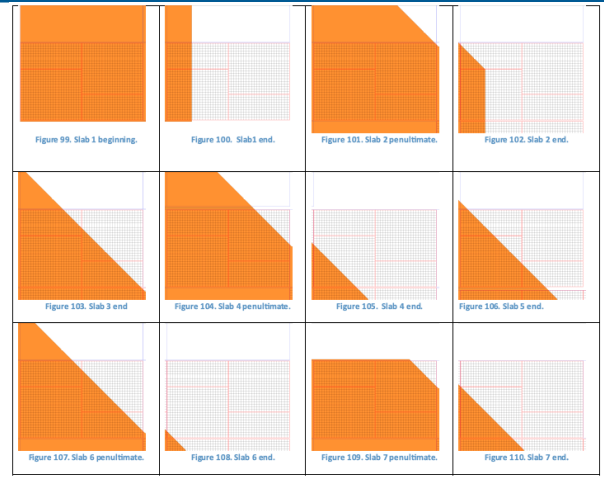
Tiling with 200mm (8’’) wafers



×400
(2 sides × 5 columns ×40 modules)

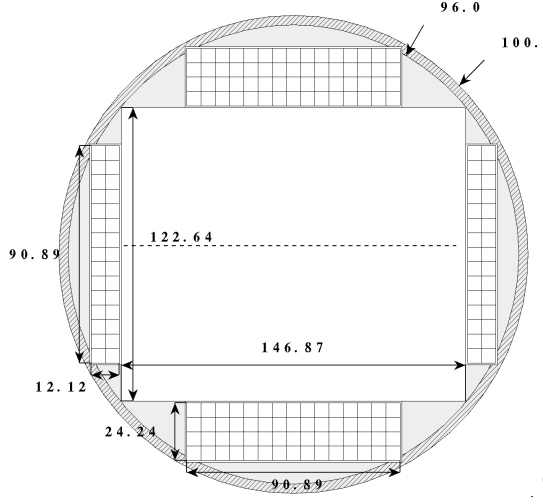


×208
(26 layers × 8 quadrants)



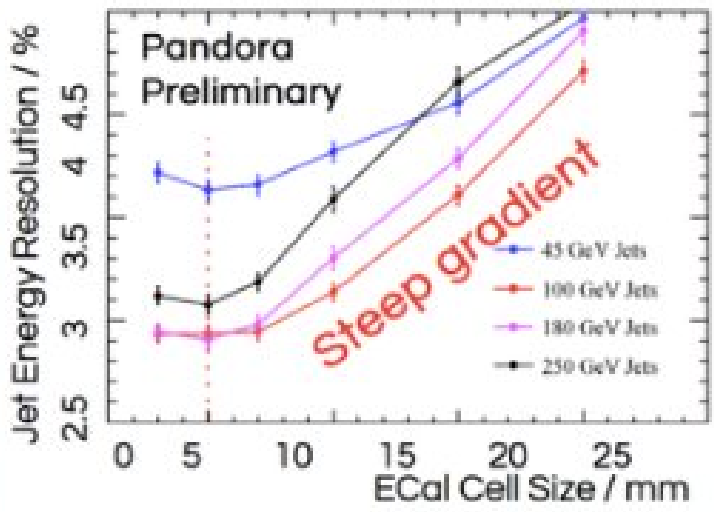
Matching of large and small rectangles, triangles and diamonds to be detailed for optimal use

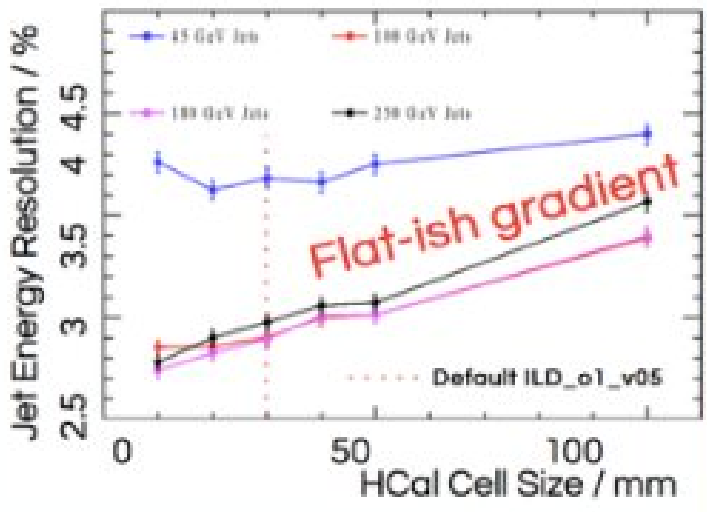
add’l small rectangles:
87 % use of surface
(83 % for an hexagonal shape)



Optimal cell-size (DBD)

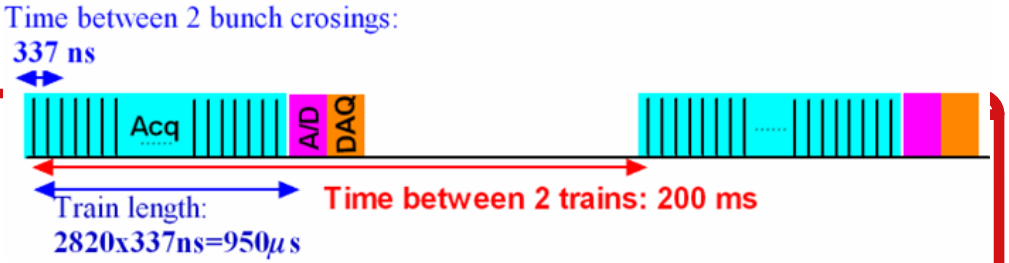
* Detector optimisation studies (Cambridge/DESY):



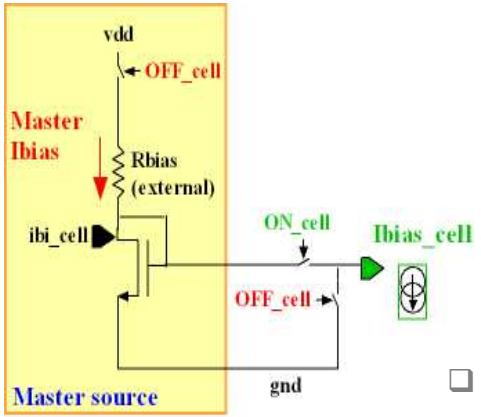


*See optimisation studies slides for reconstruction details.

POWER PULSING in SK2



- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**
- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch

Power estimations

	mW
P_ACQ	290
P_CONV	90
P_RO	26

	TAU_PO/ms	E_PO/µJ	**Tau_SPILL/ms**	E_ACQ/µJ	τau_CONV/ms	E_CONV/µJ	E_SPILL/µJ	f_rep/Hz	P_TOT/µW	P_TOT/µW/ch	Ratio HL/Lumi
ILC	0.005	1.450	1.000	290.000	0.10	9	300.45	5	1502.25	23.47	
HL-ILC	0.005	1.450	2.000	580.000	0.20	18	599.45	15	8991.75	140.5	5.99
CLIC	0.005	1.450	0.176	51.040	0.02	1.58	54.07	50	2703.7	42.25	
HL-CLIC	0.005	1.450	0.176	51.040	0.02	1.58	54.07	100	5407.4	84.49	2