SiW Ecal Compact Digital Electronics:
implementation & performance in test beam

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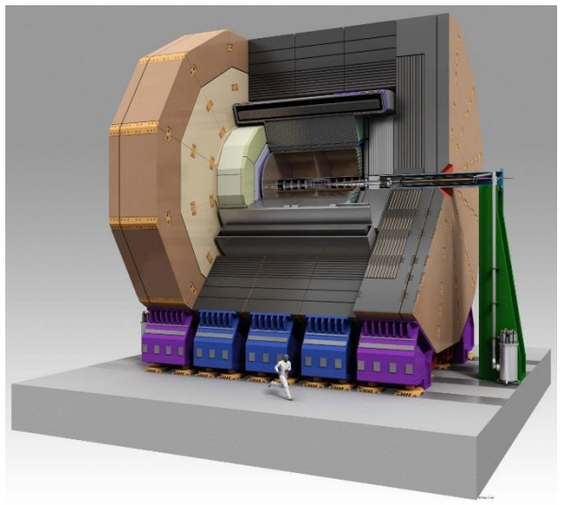
On behalf of the groups working on the CALICE SiW ECAL

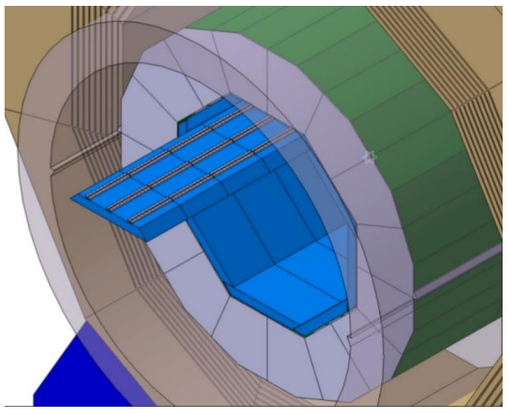
Introduction

- Description/ status of the new SiW Ecal compact digital electronics
  - SL-Board + Kapton interface
  - CORE module : Control and Readout



- Implementation in last test beam : June 24th – July 7th 2019
  - Physics results will be presented in next talk
- Poster presented at Twepp 2019 :

  « New compact readout electronics for SiW Ecal »
- Future plans



Reminder:
Constraints on Readout Electronics

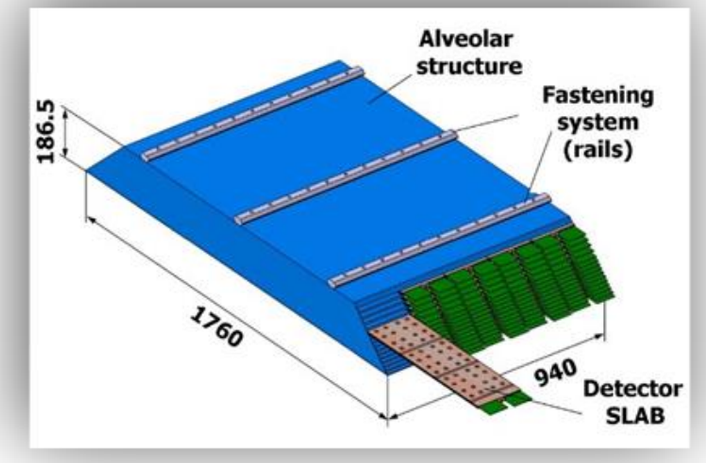
Spatial constraints for the Active Sensor Units (ASUs)

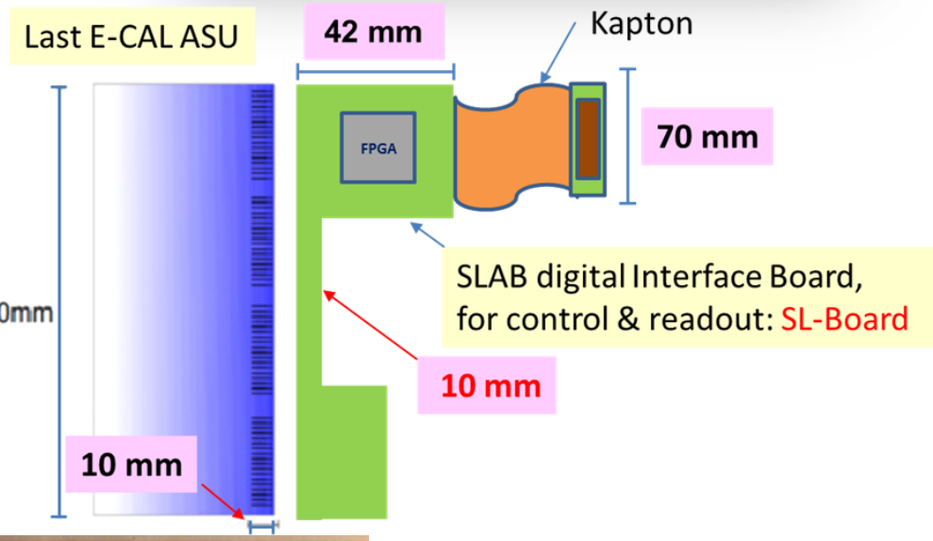
- Very limited space **between layers (depending on the total number of layers)**.

➢ Two protoype versions have been realized with different SKIROC packaging and thickness:

✓ BGA option : PCB + components*(1,2 mm)* + connectors = **~ 3,2 mm**

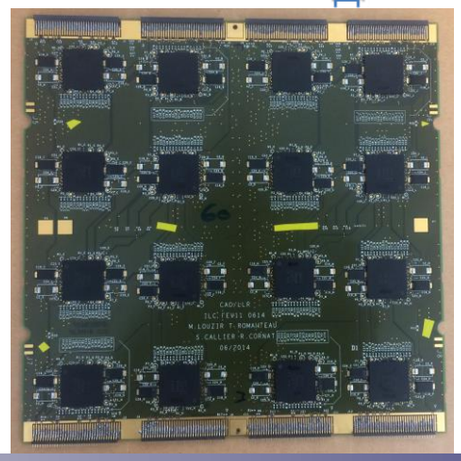
✓ COB (Chip On Board) option : PCB and ASICs **= 1,2 mm** + connectors = **~2,3 mm**



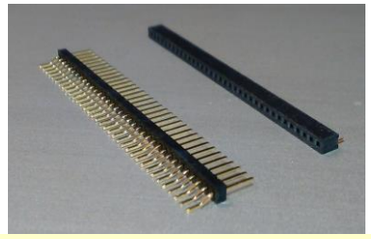


Constraints for the Slab Interface Board (SL-Board)

- The SL-board will be installed between ECAL and HCAL, separated by only 67 mm
- L-shape because of the cooling system
- Maximum Height : **6 to 12 mm depending on the location**
- Control & Readout electronics at the extremity of the Slab
- Signal integrity over a Slab : up to 15 interconnected ASUs
- Very low power consumption (~ 150 mA/ Slab) : needs to run in **power pulsing mode**

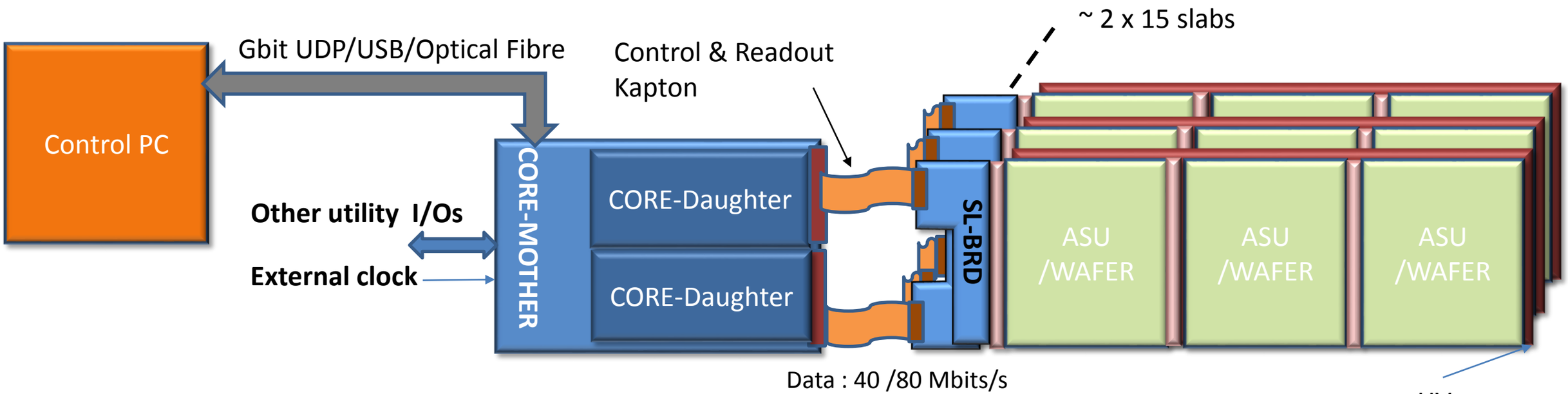


ASU: FEV 11, with Skiroc BGA option, and the gradconn connectors



Gradconn connectors (1,5 mm high)

Global Architecture Scheme



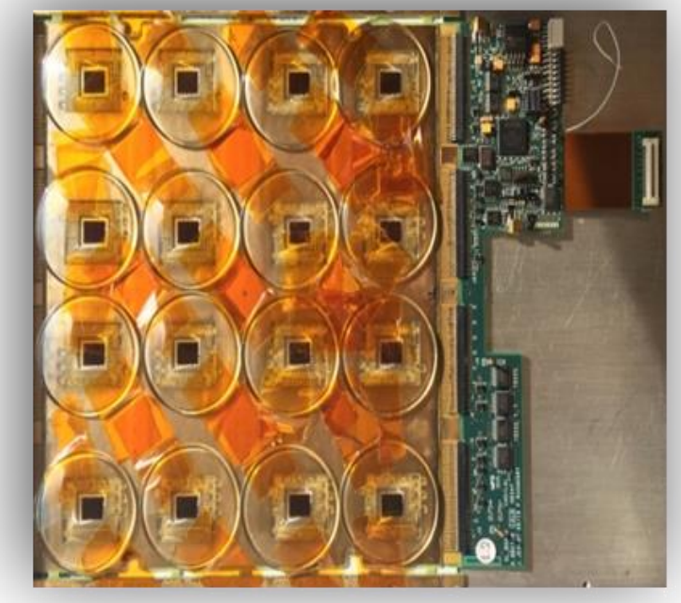
CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab

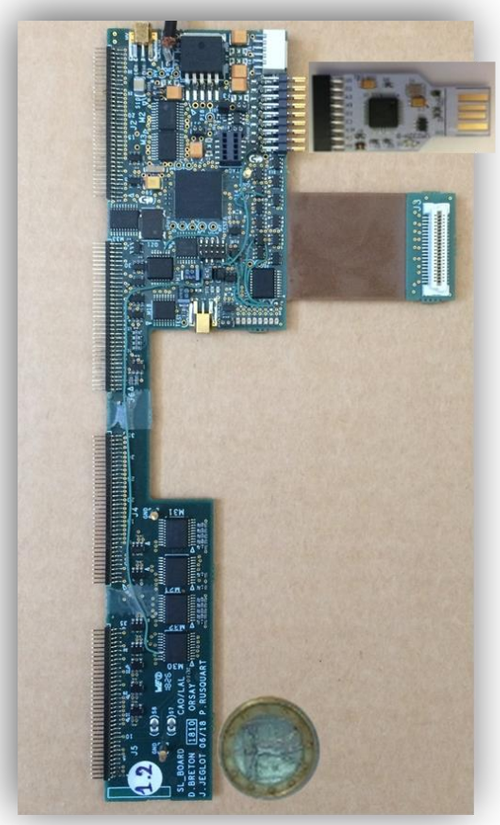
External clock and Utility I/Os : possibility to be synchronised with other systems!

The SL-Board

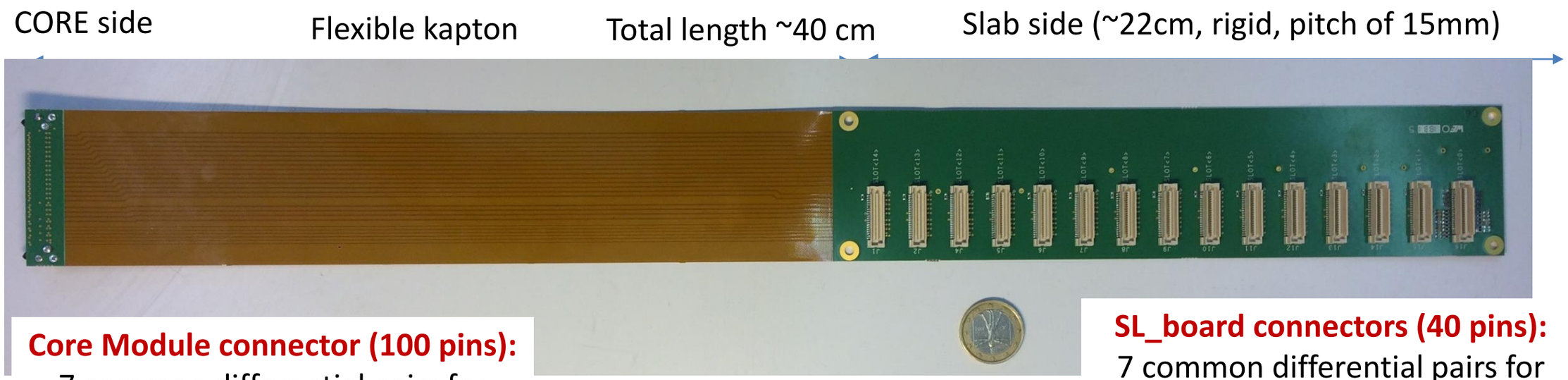
The **SL-Board** is the sole interface for the **~10,000 channels of a slab :**

- It delivers the **regulated power supplies,** including **High Voltage**, **controls** the SKIROC ASICs, and **perfoms the full data readout**.
- It is connected to the CORE-Kapton via an internal **kapton layer** and a 40-pin connector.
- It is based on a **MAX10 from ALTERA**, which is a mix of CPLD and FPGA.
- It includes an ADC which will be used to monitor the pulsed power supply.
- Very size **limited:** 18 cm in width, 10 to 42 mm in length.
- Its **own power** consumption is **< 1W**
- It can also be an **autonomous system** with direct computer access for testing and characterization purposes (using the **FTDI USB module**).





The SL Board Core-Link (Core-kapton)

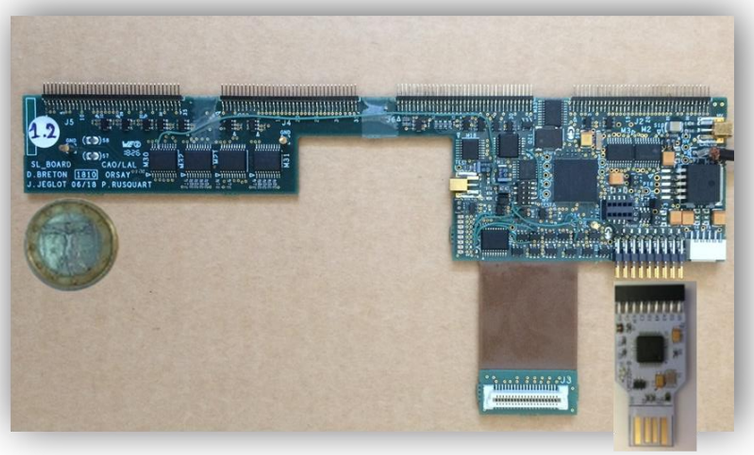


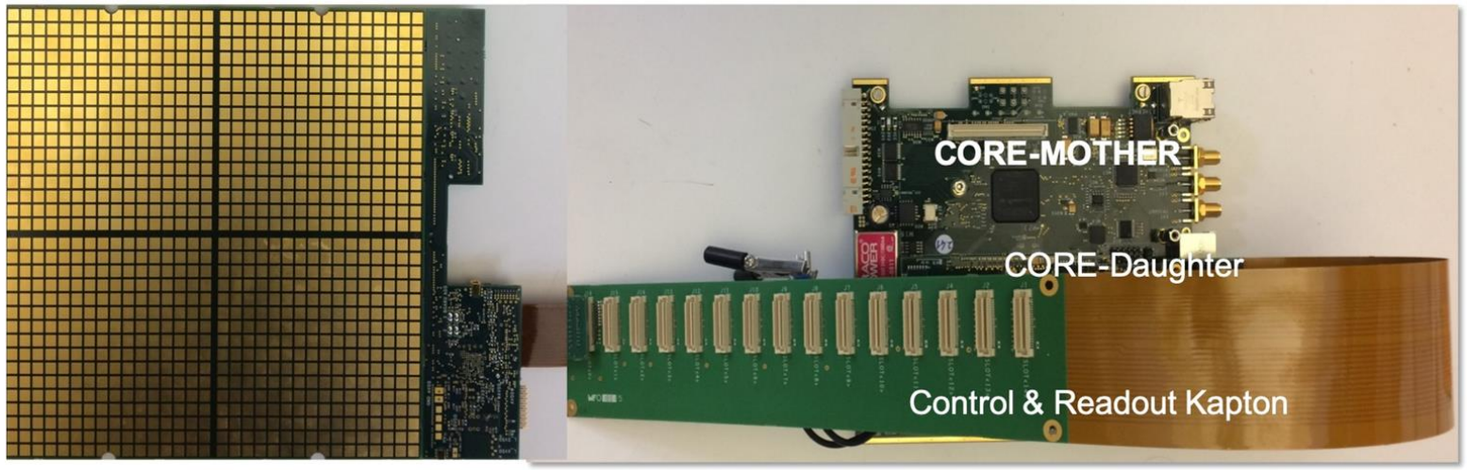
Core Module connector (100 pins):
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

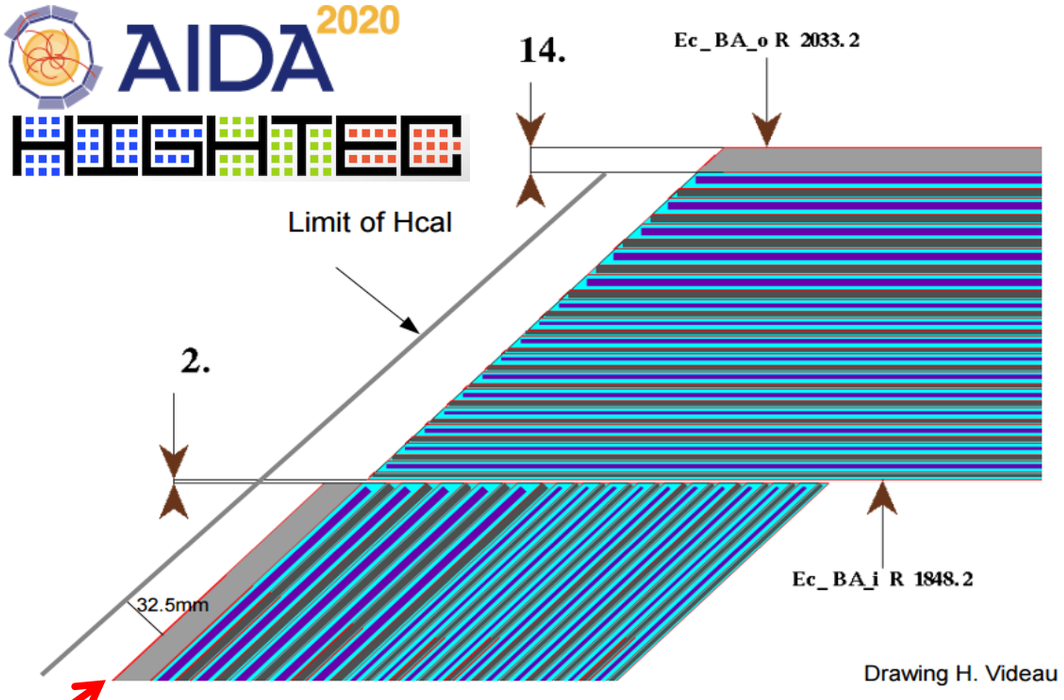
SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

- The **CORE kapton** measures 40 cm. It is the **interface** between the CORE Daughter and the SL-Board. It permits driving and reading out **up to 15 slabs**.
- It transmits all the **clocks and fast signals**, and houses the control and readout links.
- It handles the **synchronisation** of the **15 slabs**.
- The Kapton Interface makes use of **asynchronous serial transmissions** in order to greatly simplify the synchronization of the numerous control and data links.
- The speed of the slow control and the individual readout links is : **40 Mbits/s**
- Reminder : readout link of the ASUs **: 2 x 5 MBits/s**

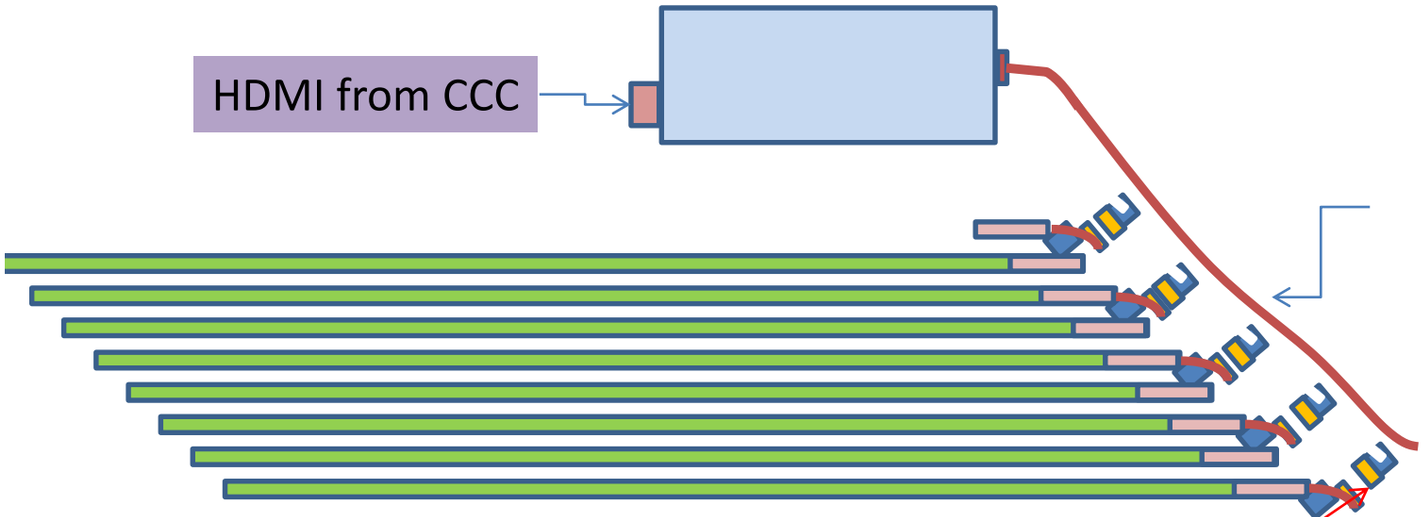
For illustration - System in final detector





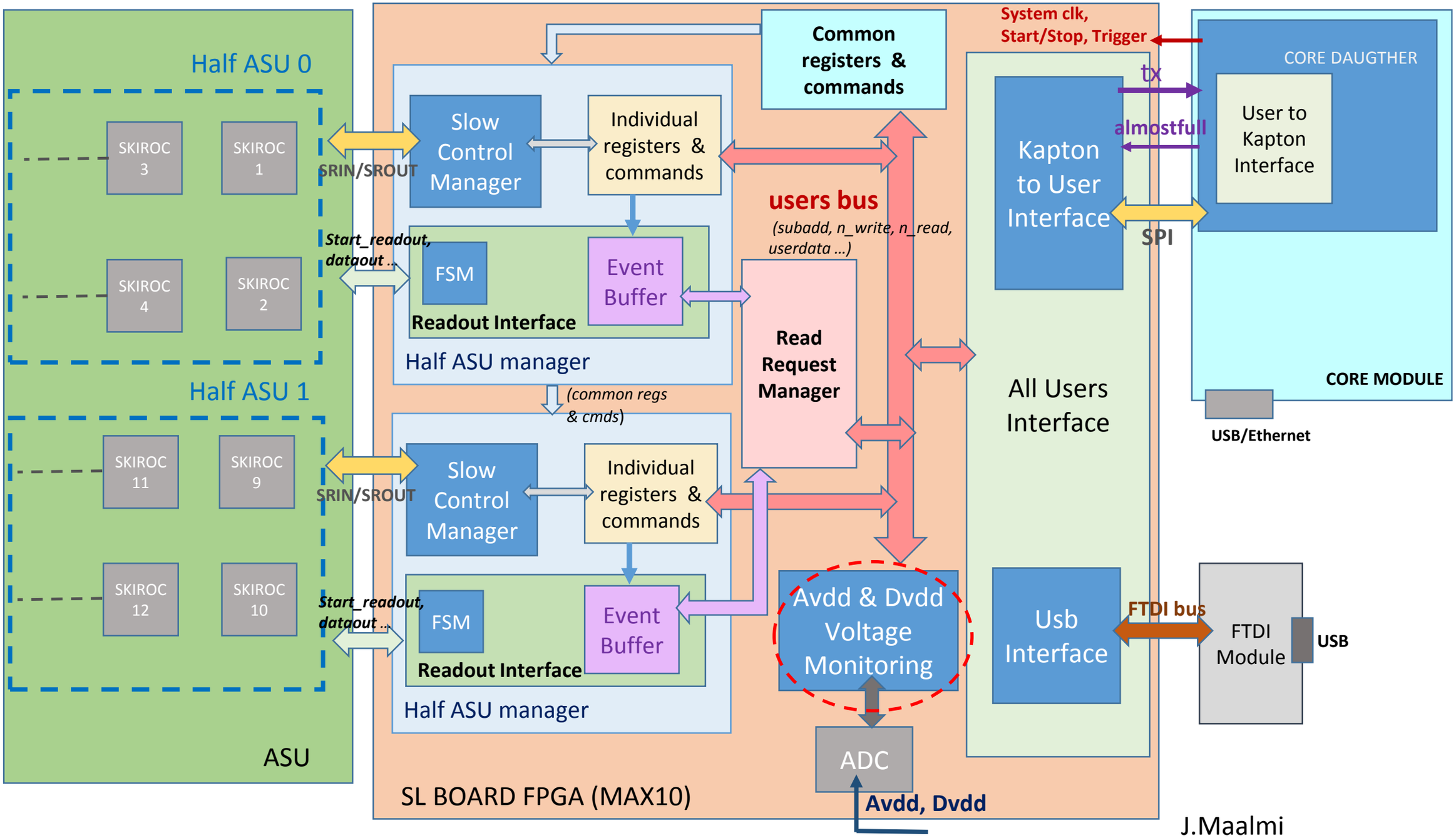


Approximately 6cm between Ecal and Hcal



Guiding/receiving signals to/from slabs

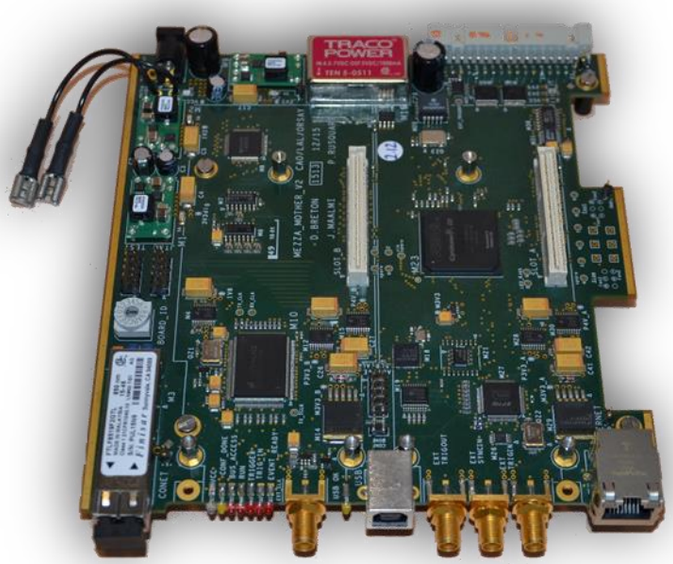
SL Board Firmware diagram:



The CORE Module

The CORE Mother:

- The **Control and Readout Motherboard** have been developed for housing up to 2 **Mezzanines**: it permits separating the **acquisition** part from the specific front end part.
- **External** input and output signals permit **synchronising** or interfacing the module with other systems.
- The CORE mother sends common clocks and fast signals to the Core Daughters to keep the **system synchronised**
- The control and readout is possible through **USB(2.0)**, **UDP or Optical link** (Ethernet over optical)
- The CORE module **power consumption** is **5 W**



The CORE mother

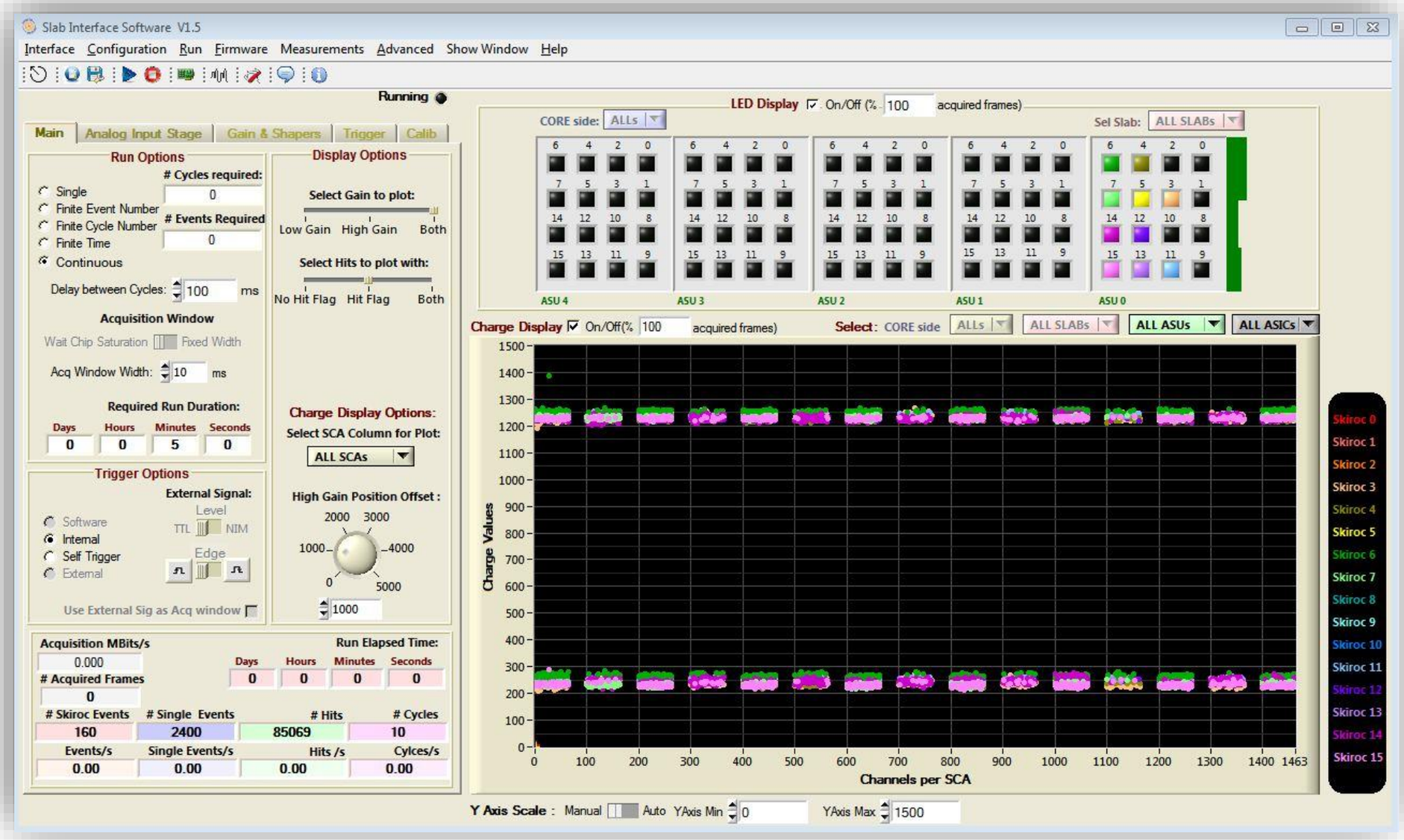
The CORE module

The CORE Daughter:

- The **CORE Daughter** is based on a Cyclone IV FPGA. It is the interface between the CORE motherboard and the Kapton which permits driving and reading out **up to 15 slabs**.
- It buffers all the clocks and fast signals, and deals with the control and readout links through the Kapton Interface.
- It houses the second level of **event buffers** (derandomizers)**.**
- Ctrl & Readout link between CORE Daughter and CORE Mother **: 60 MBytes/s** if USB**, and 125 Mbytes/s** if UDP**.**

The CORE daughter

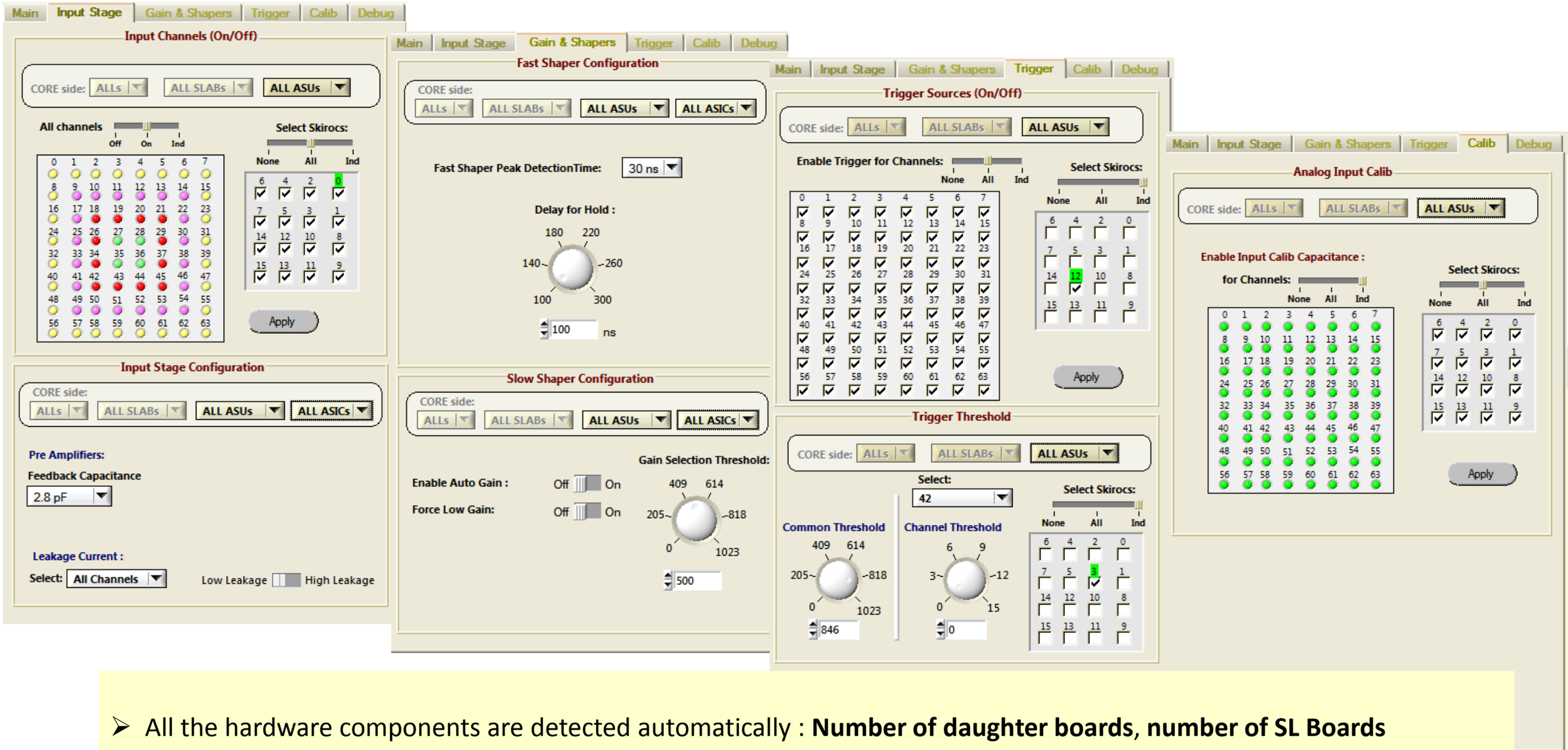
Software Development Status: Main Panel for Acquisition:



- The Software can handle the communication through FTDI connector **or** through **CORE Module**.
- It handles the **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**
- Advanced measurements can be performed Online such as threshold scans…
- The C-functions that handles the communication (readout and configuration) can be used as a a library with any other program that handles C-langage.

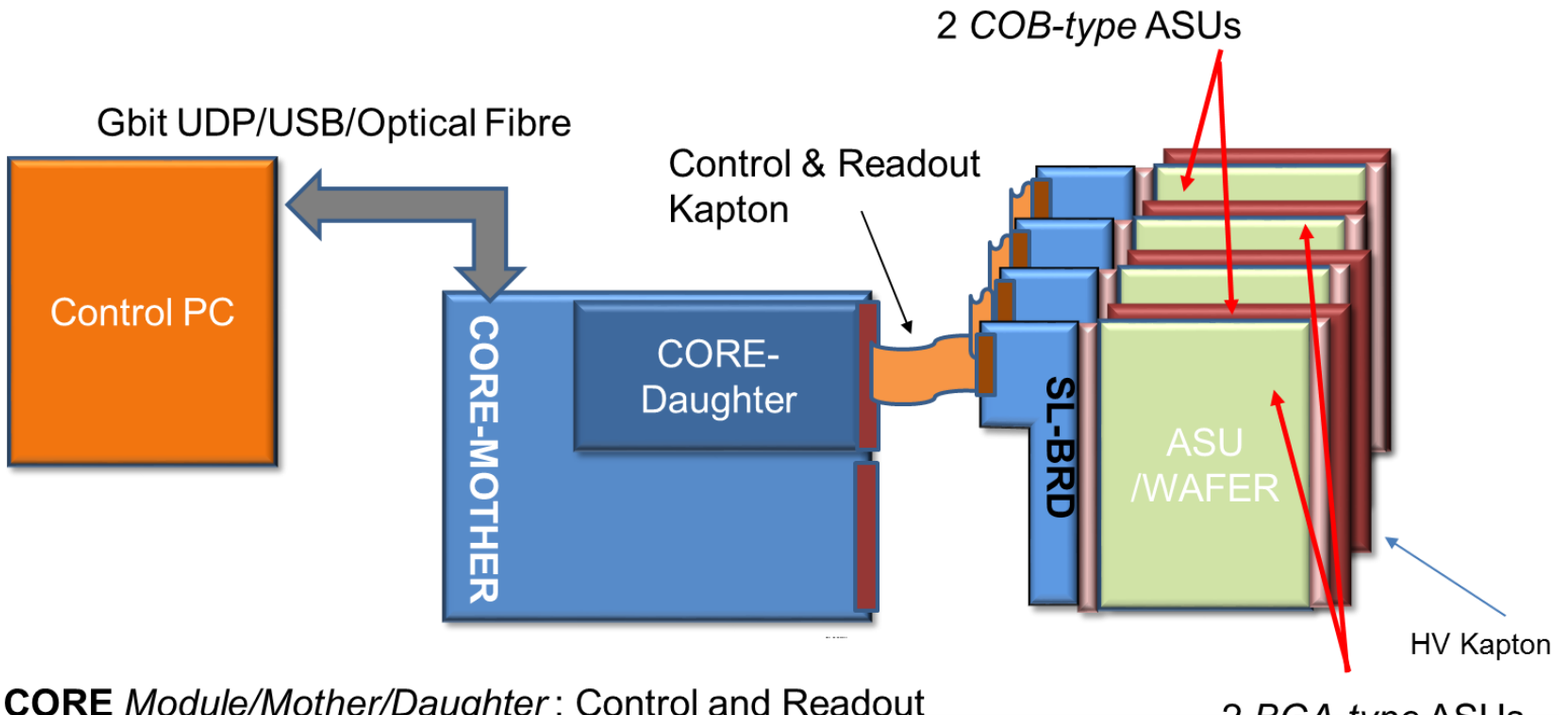
Remaining work to perform: pedestal measurements, online charge histogramming etc...

Slow Control



- All the hardware components are detected automatically : **Number of daughter boards, number of SL Boards** connected to each daughter board, and also the **number of ASUs** on each slab using **slow control readout**.
- **Slow Control**:
  - All necessary slow control **parameters** can be programmed through the Software
  - Slow control configuration is checked by writing twice the same values to the SKIROC shift regiser and reading back the pushed value on the SROUT signal.
- Control and data Readout with **direct connection** to the SL Board via FTDI module or through the **CORE module**.

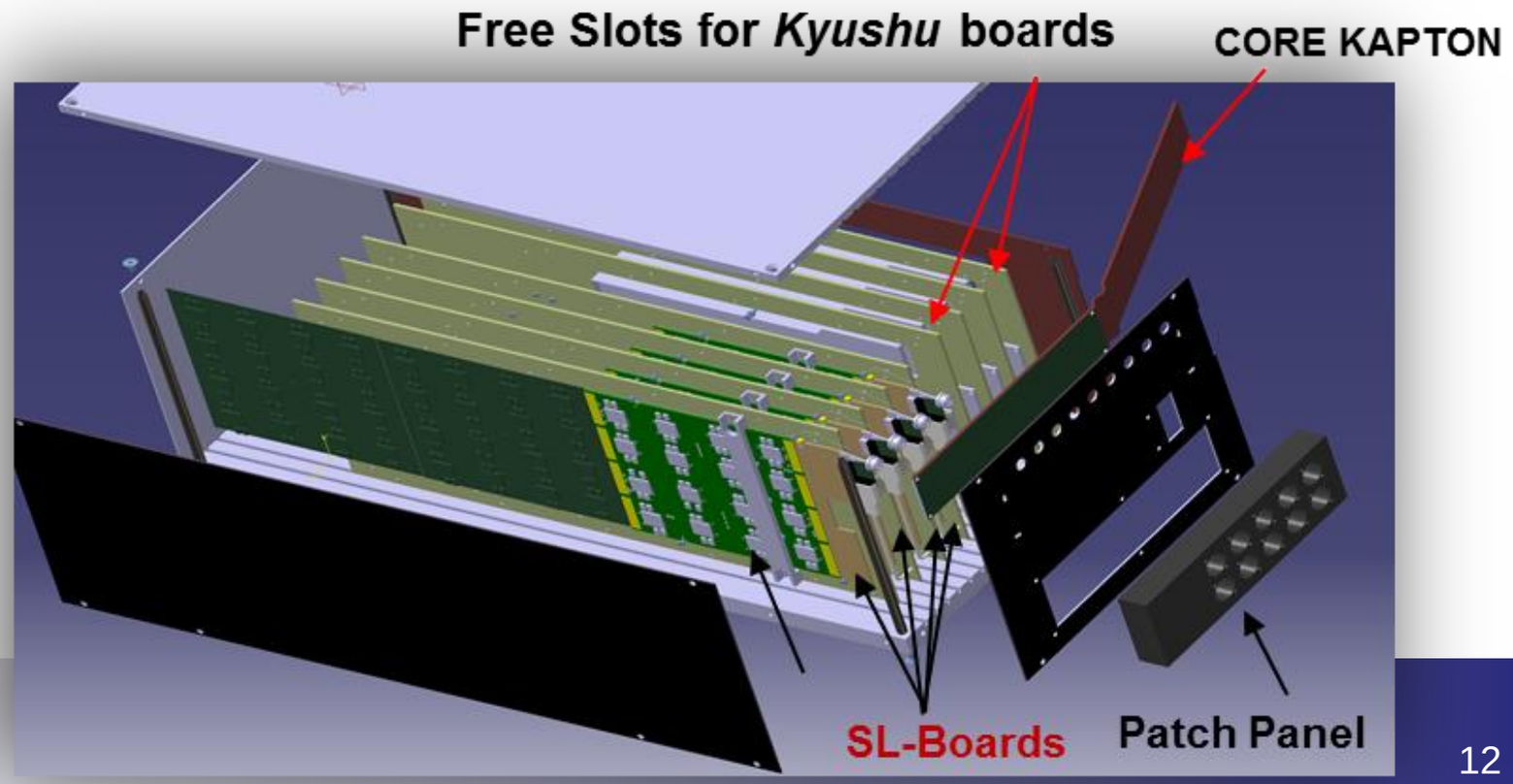
Setup preparation for test beam (1/2)



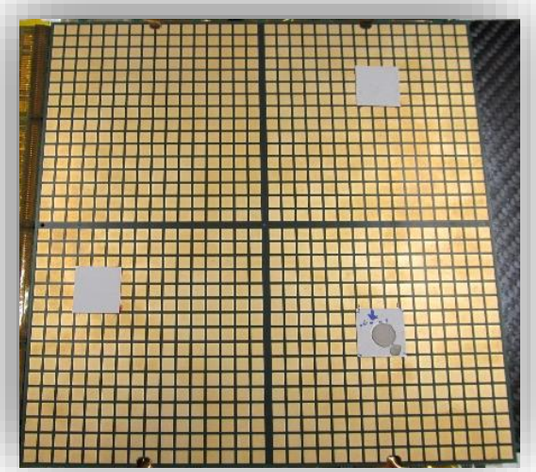
CORE *Module/Mother/Daughter* : Control and Readout
SL-BOARD : Interface board to Slab

- **Cycles** and **acquisition windows** are programmable and generated by the CORE Module.
- All ASUs run **synchronously**.
- Possibility to check **buffer overflow**

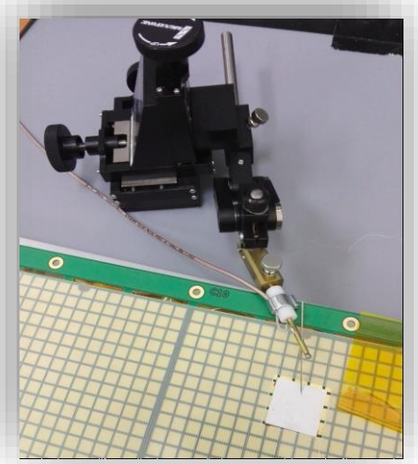
2 *BGA-type* ASUs



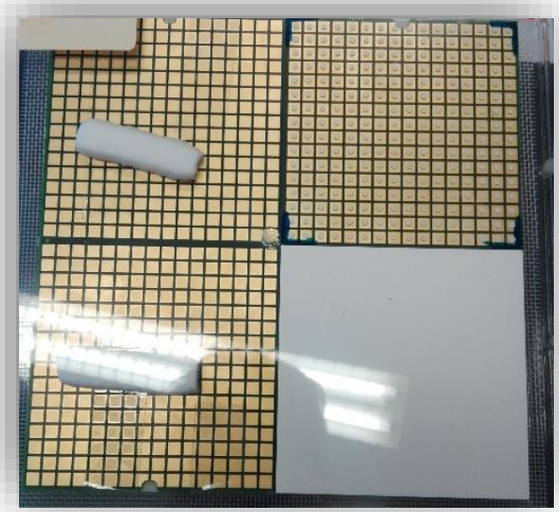
Setup preparation for test beam (2/2)



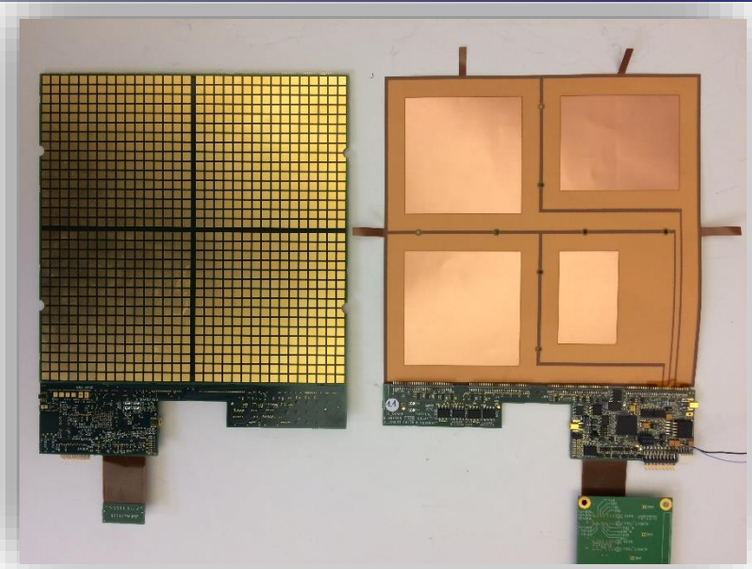
Test of 3 baby wafers



HV via Probe (150Volts)



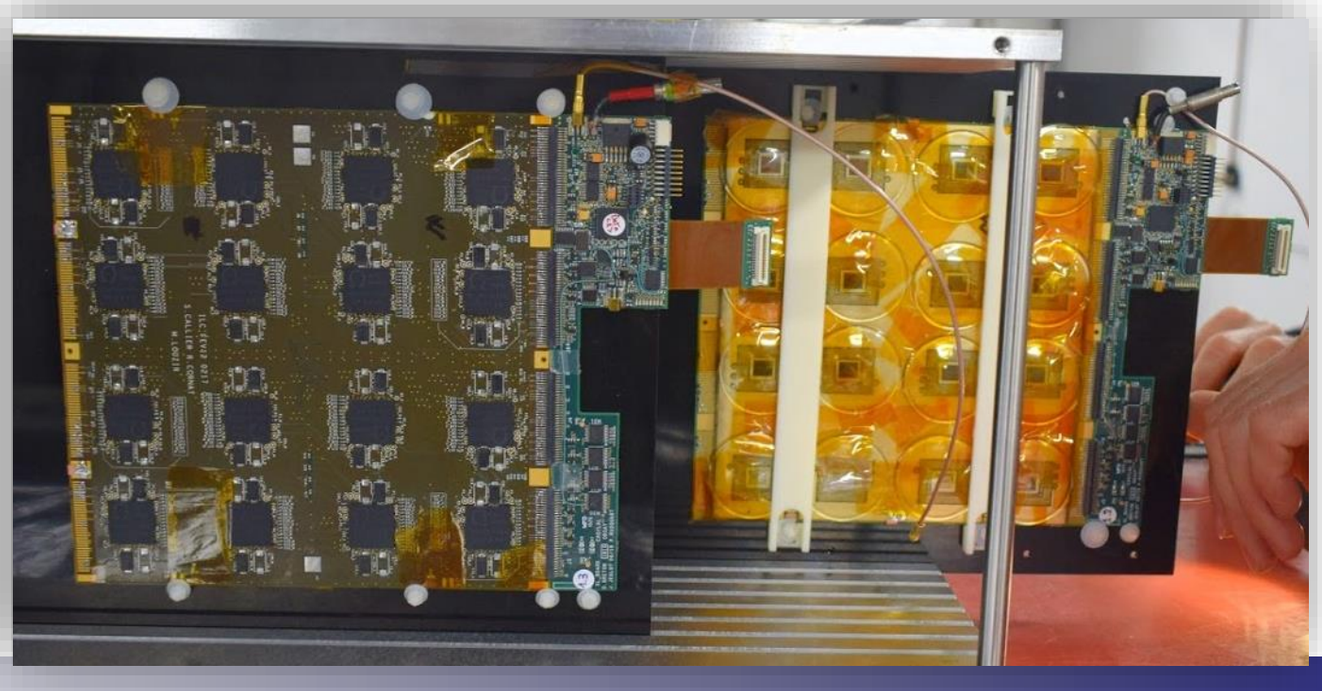
Wafer gluing (500um) made at LPNHE



Mounting of HV Kapton

SL-board + ASU on support

* A particular thank you to Remi Cornat and Patrick Ghislain from LPNHE for the development of the wafer-ASU assembly of both ASU types



Test beam at DESY: June 24th to July 7th

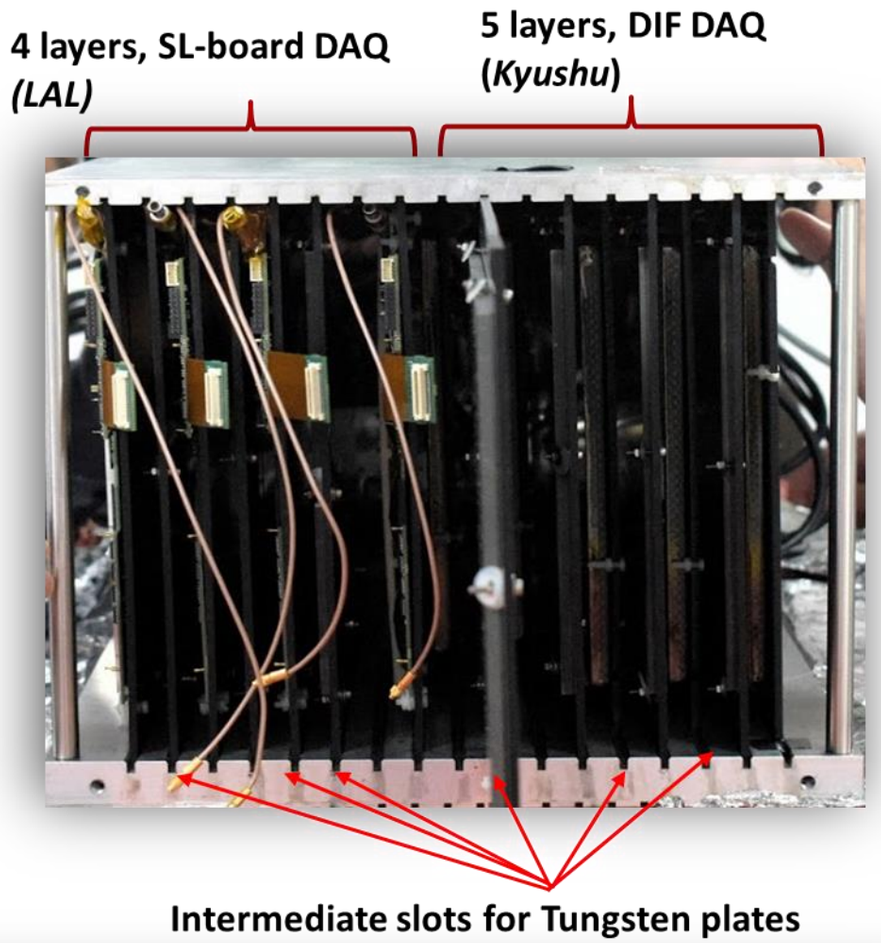
- Number of Layers in the prototype box: **4 Layers** running with SL-Board DAQ, and **5 Layers** with DIF DAQ.
- 4 Layers with SL-Board/Core Module DAQ :
  - 2 ASUs (***COB option***) with **500um Si wafers**
  - 2 ASUs (***FEV12***, *BGA option*) with **500um Si wafers**
- 5 Layers with DIF DAQ (SMBv5):
  - 4 ASUs (FEV13) equipped with **650 um Si Wafers**
  - 1 ASU (FEV13) with **320um Si Wafer**.
- The **Front End** ASICs used are **SKIROC** version **2a**.

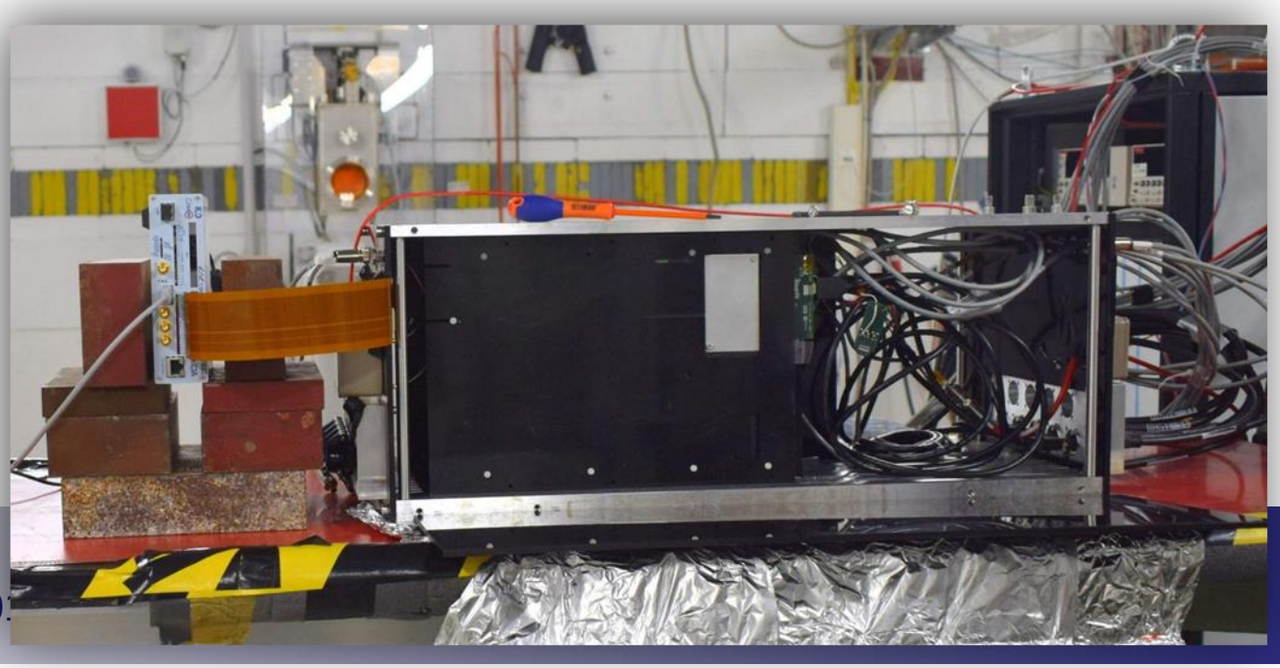
- **Two weeks** of testbeam.

- First **individual runs**, then **common runs** of the 9 Layers using a **common external signal as Start/Stop** of the acquisition window of the Front End ASICs.

- Tungsten plates added during the second week between the 9 Layers.

- Results will be shown in next talk





Future plans

- **Firmware :**

  - Some improvements to be done in the Firmware after some bugs seen during the test beam
  - **JTAG adaptor board** under design in order to **program** the SL Boards firmware through the CORE Module.

- **Software:**
  - Online measurements with the Software: charge histograms …
  - Pedestal Calibrations
  - …

- **Hardware**
  - SL Board V2 → see next slides
  - **Power pulsing mode** : → see next slides

- **Mechanics:**
  - Improvement of the prototype box: modification of the front panel for giving a better access to all connectors of the SL Boards.

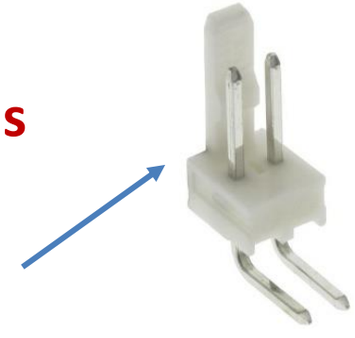
- **Preparation of the next test beam (March 2020 ?):**
  - More layers
  - Calibration of Noisy channels
  - Tests with muons
  - More calibrations before test beam
  - **Full synchronisation** with Layers from Kyushu: same clock, sync signals …

Going from SL_Board V1 to V2

Experience from beam test permitted **upgrading the design** of the SL_Board:

- All useless circuitry has been removed and the rest optimized
- Kapton length will be raised from **40** to **60 mm** (this will **ease the plugging to the kapton**)
- The main input plugs are moved next to the kapton (HV and calibration pulse in MMCX)
- The connector for the FTDI USB module is changed and moved => takes less space, easier to handle
- A **switch** will permit encoding the **slot number**
- Adding of :
  - a **DAC for SKIROC ADC calibration**
  - a **flash EEPROM** for permanent information storage

- The FPGA will produce **pulses** for **autonomous functional calibration of both gains**
- The **HV will be made available on the SL_Board** to ASU connectors (both sides)



- **Design is almost finished** => still need to make a decision on the low voltage power supply connector type (moving to a **more robust** through-hole 2-point connector ?)

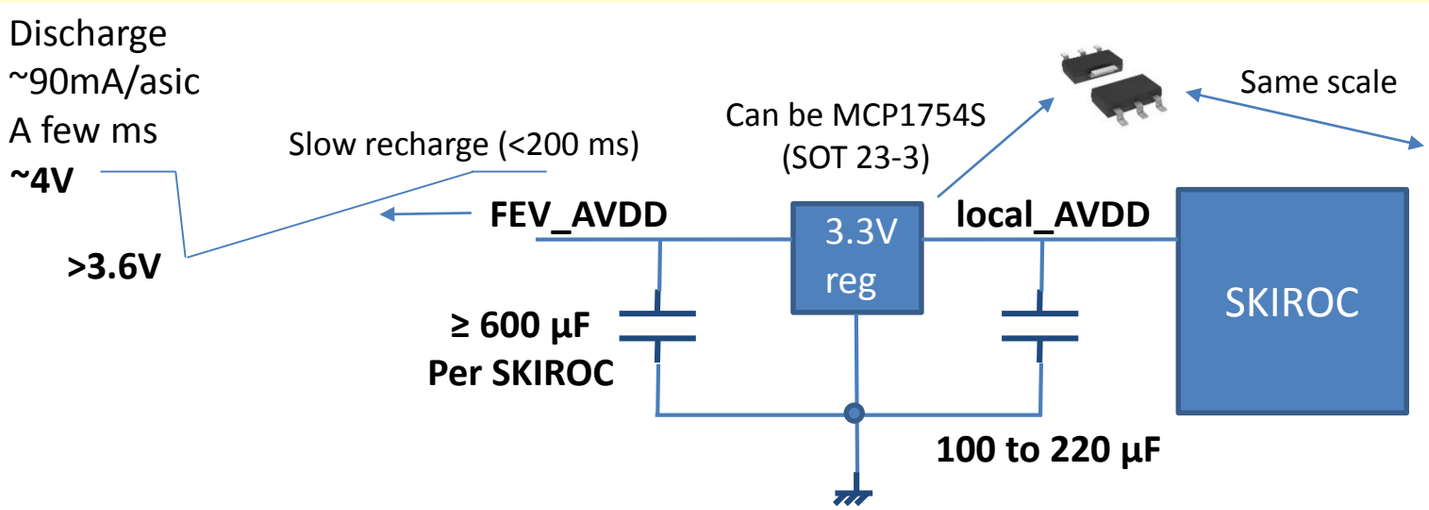
Working on the power pulsing

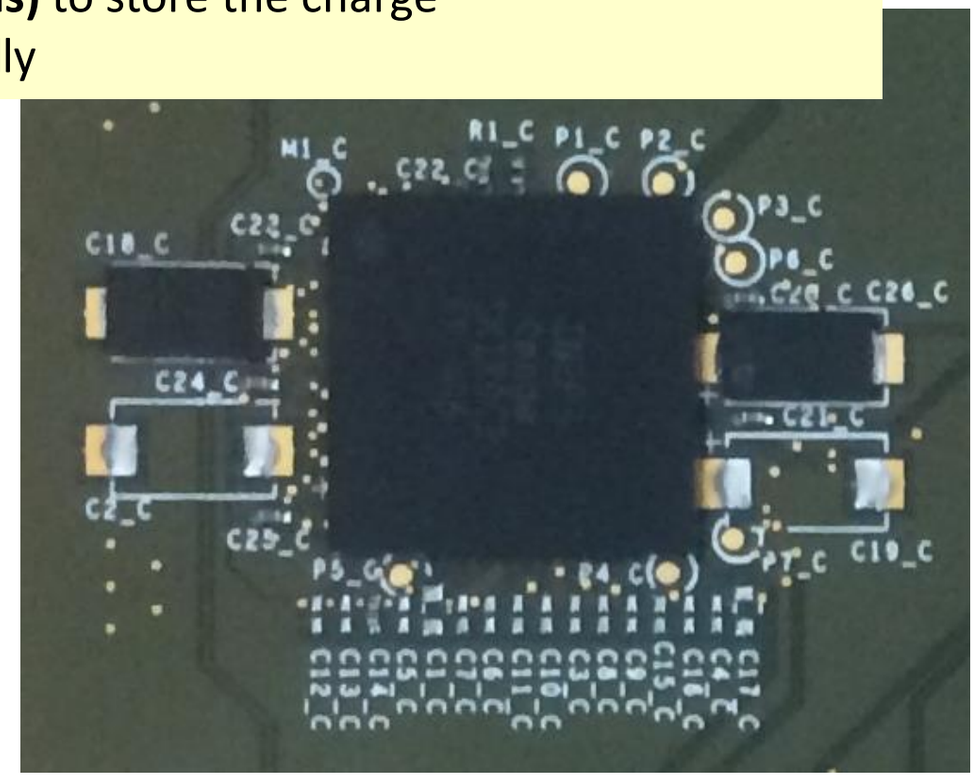
Two remarks:

1) High-value flat capacitors actually have a poor **ESR** (**order of Ohms**) => not adapted to high currents
2) It is better that **the AVDD of the SKIROC chips does not vary** during the power pulsing

⇒ two actions:

1) Put **enough lower-value capacitors** with very **good ESR (~ tens of mOhms)** to store the charge
2) AND add an **individual regulator** for producing each SKIROC's AVDD locally





There are already 4 slots for decoupling capacitors around the SKIROC chips. More can be added if required (space is available).

Example of Discharge/Recharge Cycle for one SKIROC block:

- Current of 90 mA during 2.5 ms in 600 µF => ΔV ~ 0.4V
- Total FEV capacitance ~ 15 000 µF
- Reload current can be as low as 15 mA/ASU

There is **no more effect of the variations of AVDD on the SKIROC chips**
The only constraint is to **keep AVDD > 3.6 V.**
The higher the capacitance, the lower the variations => look for the optimum (~1000 µF ?)…

Conclusion

- The new compact digital electronics for the control & readout of the SiW Ecal is functional
- It worked very nicely during the test beam in June: results will be presented in the next talk
- A lot of experience learned from this test beam: improvements will be realized for the next one in March.
- Improved version of the SL Board is almost ready
- We are currently studying a new version of the FEV in order to work on the optimization of the power pulsing mode.
- Remark: Compact design may lead to spin-offs beyond LC Detectors