

Toward faster and larger monolithic CMOS pixel sensors (CPS) for vertexing and tracking at ILC

Auguste Besson on behalf of Strasbourg-PICSEL group

- ❑ ILC vertex detector requirements with CPS
- ❑ MIMOSIS for CBM MVD
- ❑ R & D challenges

CMOS pixel sensor (CPS) for charged particle detection

Main features

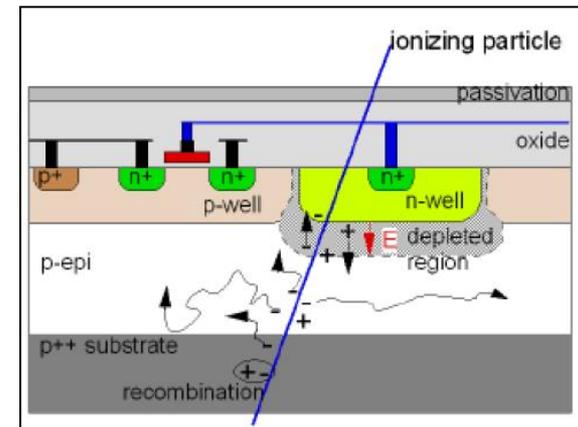
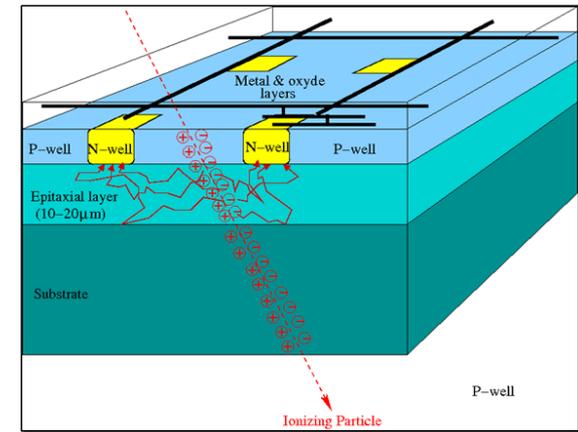
- ✓ **Monolithic** (Signal created in low doped thin epitaxial layer $\sim 10\text{-}30\ \mu\text{m}$)
- ✓ **Thermal diffusion of e^-** (Limited depleted region)
- ✓ **Charge collection: N-Well diodes** (Charge sharing \Rightarrow resolution)
- ✓ **Continuous charge collection** (No dead time)

Main advantages

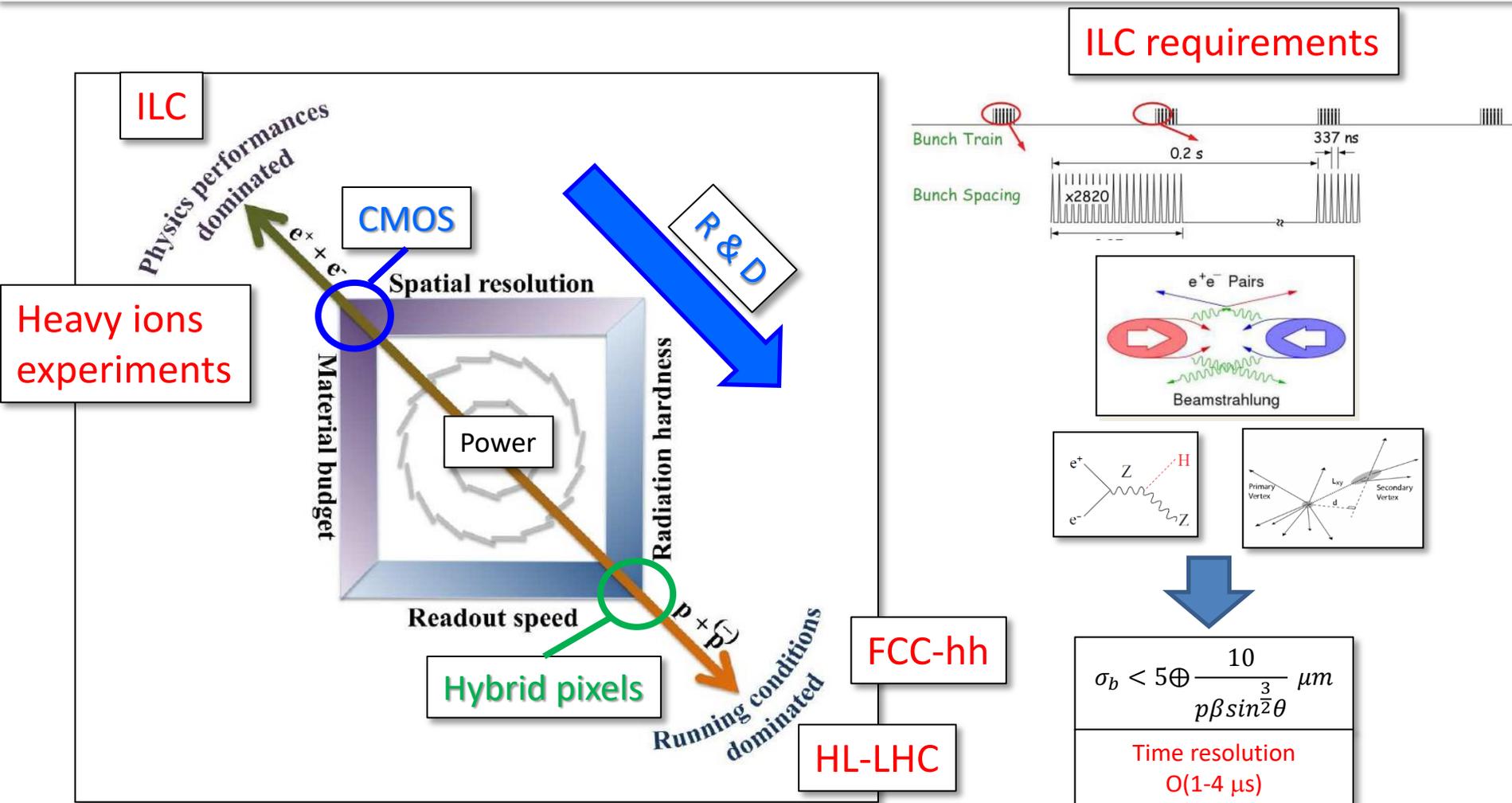
- ✓ **Granularity**
- ✓ **Material budget**
- ✓ **Signal processing integrated in the sensor**
- ✓ **Flexible running conditions** (Temperature, Power, Rad. Tol.)
- ✓ **Industrial mass production**
 - Advantages on costs, yields, fast evolution of the technology,
 - Possible frequent submissions

Main limitations

- ✓ **Industry addresses applications far from HEP experiments concerns**
- ✓ **Needs adapted processes**



Vertex detector technology figure of merit



- ⇒ Keep excellent spatial resolution and push towards better time resolution
- ⇒ Strong synergy between Higgs factories and Heavy ion experiments

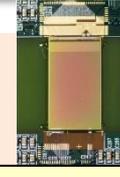
CPS Time resolution

EUDET beam telescope
(Mimosa 26 by IPHC)
2009



HL-LHC
MALTA - 25 ns

MUPIX-X
(Mu3e)
<10 ns



CEPC (Z) bunch
25 ns

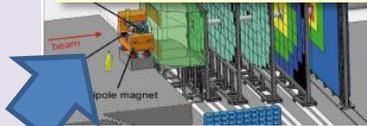
FCCee (Z) bunch
20 ns

CLIC 5 ns

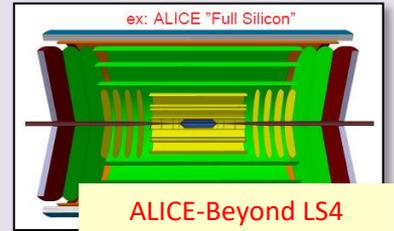
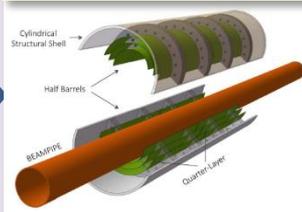
CLIC bunch
500 ps

Others

CBM-MVD
(MIMOSIS by IPHC & IKF)
5 μ s - Under development

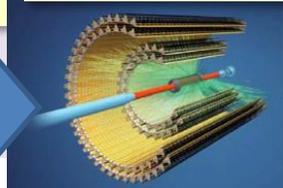


ALICE-Beyond LS3



STAR-PXL detector
(ULTIMATE by IPHC)
185 μ s - 2014

ALICE-ITS2
(ALPIDE by CERN & IPHC)
10 μ s - In construction



Heavy ion experiments

100 μ s

10 μ s

1 μ s

100 ns

10 ns

1 ns

100 ps

10 ps

Time resolution

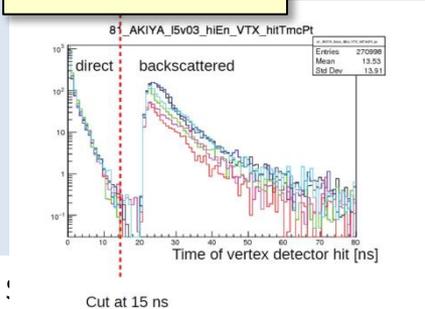
ILC R&D

VXD requirements
2-4 μ s



SIT & Bunch tagging
300-500 ns

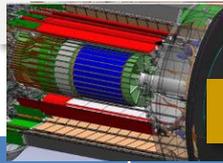
backscattered filter
10 ns



Particle ID

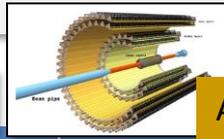
ILC

Evolving CPS



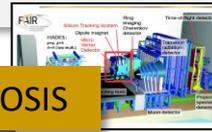
ULTIMATE

STAR-PXL



ALPIDE

ALICE-ITS



MIMOSIS

CBM-MVD

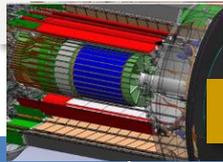
PSIRA proposal



ILD-VXD

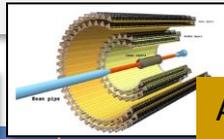
	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	0.18 μm	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, $V_{\text{bias}} \sim -6\text{V}$ Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	Asynchronous r.o. In pixel discri.	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~ 185	5-10	5	1 – 4
Data Flow		$\sim 10^6$ part/cm ² /s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7×10^5 /mm ² /s >2 Gbits/s output (20 inside chip)	~ 375 Gbits/s (instantaneous) ~ 1166 Mbits / s (average)
Radiation	O(50 kRad)/year	2×10^{12} n _{eq} /cm ² 300 kRad	3×10^{13} n _{eq} /cm ² /yr & 3 MRad/yr	O(100 kRad)/year & O(1×10^{11} n _{eq} (1MeV)) /yr
Power (mW/cm ²)	< 150 mW/cm ²	< 40 mW/cm ²	< 200 mW/cm ²	~ 50 -100 mW/cm ² + Power Pulsing
Surface	2 layers, 400 sensors, 360x10 ⁶ pixels 0.15 m ²	7 layers, 25x10 ³ sensors > 10 m ²	4 stations Fixed target	3 double layers 10 ³ sensors (4cm ²) 10 ⁹ pixels ~ 0.33 m ²
Mat. Budget	~ 0.39 % X_0 (1st layer)	$\sim 0.3\%$ X_0 / layer		~ 0.15 -0.2 % X_0 / layer
Remarks	1 st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

Evolving CPS



ULTIMATE

STAR-PXL



ALPIDE

ALICE-ITS



MIMOSIS

CBM-MVD

PSIRA proposal

ILD-VXD



	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
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ILC requirements

⇒ MIMOSIS architecture already allows

2-4 μs time resolution / $\sigma_{\text{sp}} \sim 4 \mu\text{m}$

⇒ Smaller feature size (65nm) would allow

BX time stamping / $\sigma_{\text{sp}} \sim 3 \mu\text{m}$

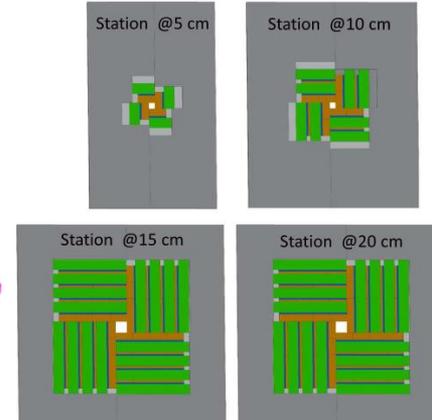
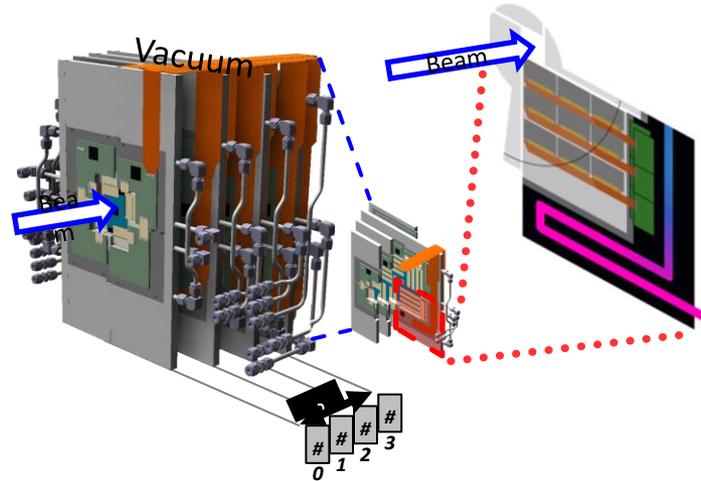
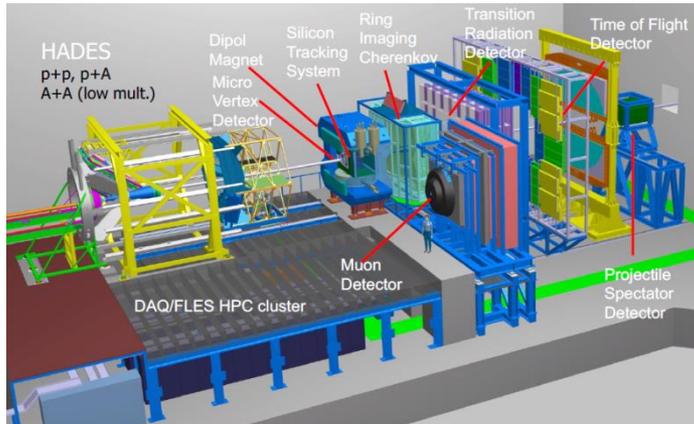
⇒ Power vs read-out speed compromise

Avoiding power pulsing possible ?

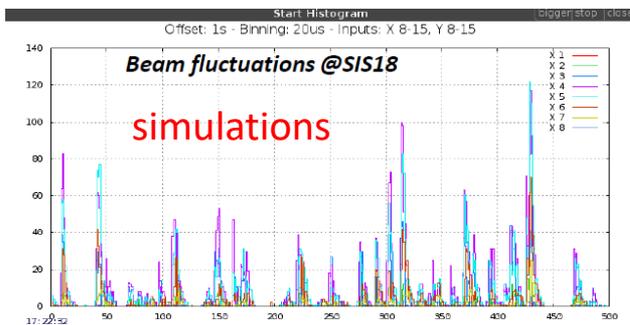
⇒ Stitching

Very low mass detector

Radiation	O(100 kRad)/year & O(1×10^{11} n _{eq} (1MeV)) /yr
Power (mW/cm ²)	~ 50 -100 mW/cm ² + Power Pulsing
Surface	3 double layers 10^3 sensors (4cm ²) 10^9 pixels ~ 0.33 m ²
Mat. Budget	~ 0.15 -0.2 % X ₀ / layer
Remarks	Evolving requirements



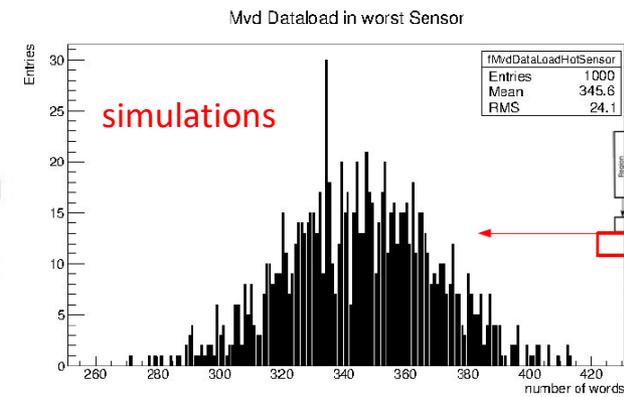
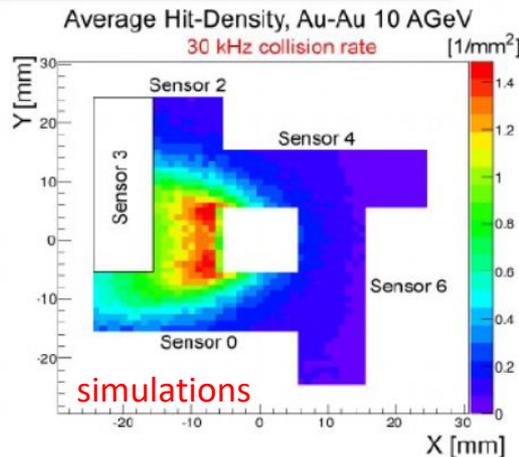
Joachim Stroth | 56th Winter Meeting on Nuclear Physics | Bormio (Italy)



Michal Koziel | deutsche physikalische gesellschaft 2017 | Münster (Germany)

Au/Au 10 AGeV 100kHz

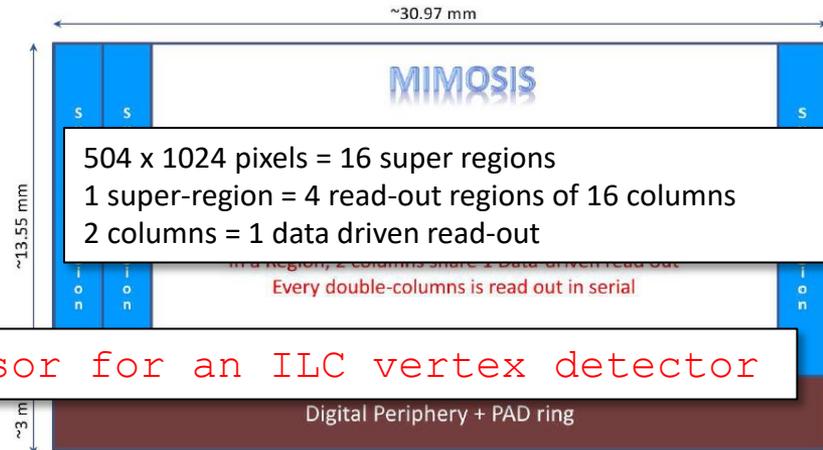
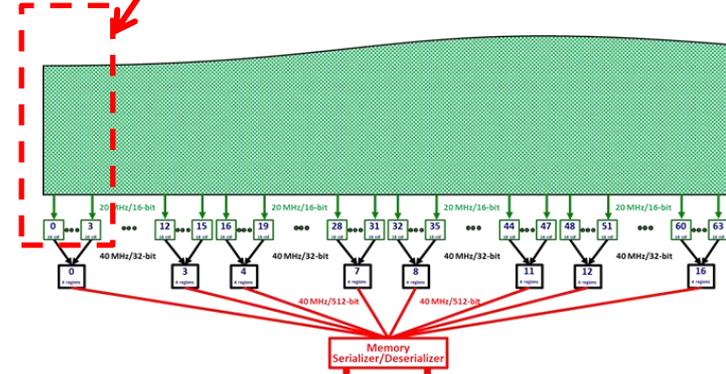
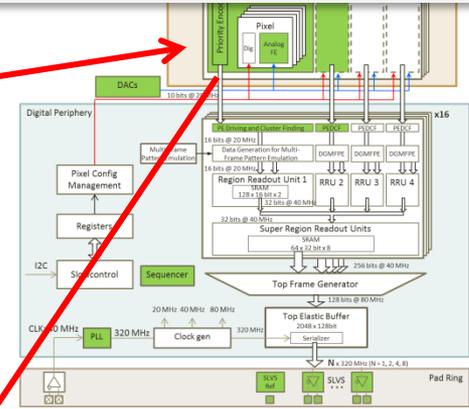
Non uniform hit density in time and space



Data load distribution in most occupied sensor (number of 16 bits words during 5 μ s)

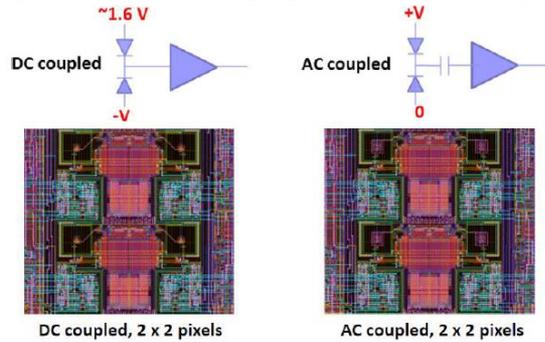
MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
 - ✓ Back from foundry (2017)
 - ✓ Test (2018-2019)
 - Testability
 - Priority encoder frequency
 - Radiation hardness design (SEU)
- MIMOSIS-1: 1st prototype of complete sensor
 - ✓ About to be Submitted
 - ✓ Tested during 2020
- MIMOSIS-2:
 - ✓ 2021
- MIMOSIS-3: final pre-production sensor
 - ✓ >2022

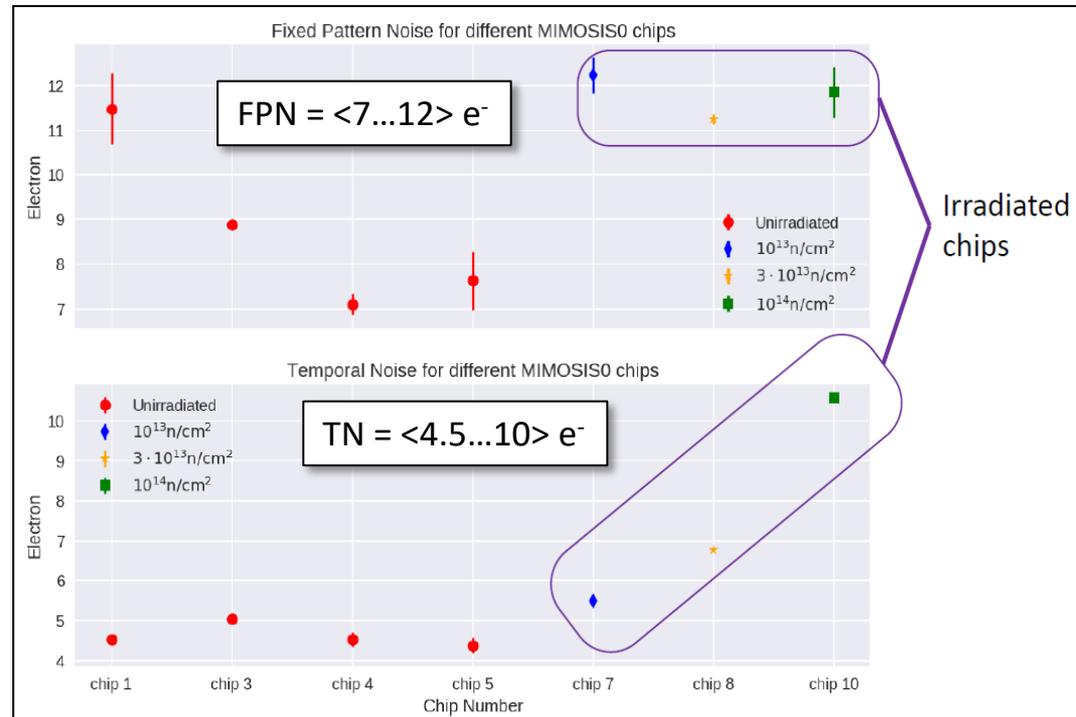
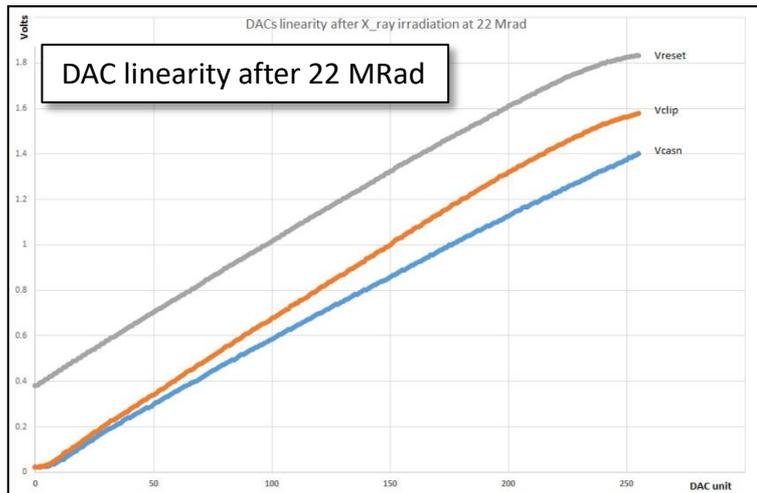


⇒ architecture adaptable to a fast sensor for an ILC vertex detector

Mimosis-0 tests results



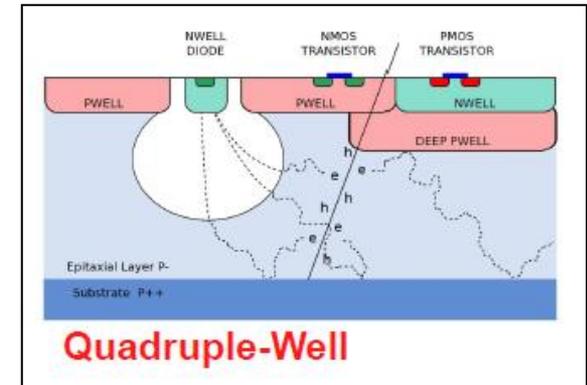
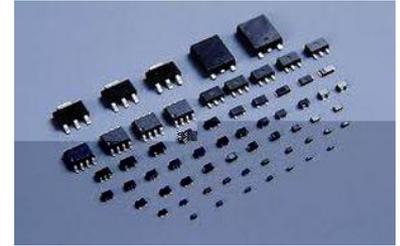
- Temporal noise and fixed pattern noise (room T°C on DC pixels)



Studies: Noise, pixel to pixel dispersion, radiation hardness \Rightarrow works as expected

Challenge 1: towards faster time resolution

- Feature size of the technology
 - ✓ 0.35 μm (yesterday)
 - ✓ \Rightarrow 0.18 μm (today)
 - ✓ \Rightarrow 0.065 μm (tomorrow)
- Smaller feature size allows
 - ✓ More functionalities inside the pixel
 - Keep small pixel dimensions
 - ✓ Faster read-out
 - ✓ Lower Power consumption
 - ✓ Other tech. options matters
 - # metal layers
 - Deep N-well, etc.



- \Rightarrow Relation with foundries and access to options is a key
- \Rightarrow Current technology: time resolution potential of $O(100 \text{ ns})$
- \Rightarrow Ultimate limit down to $O(100 \text{ ps})$

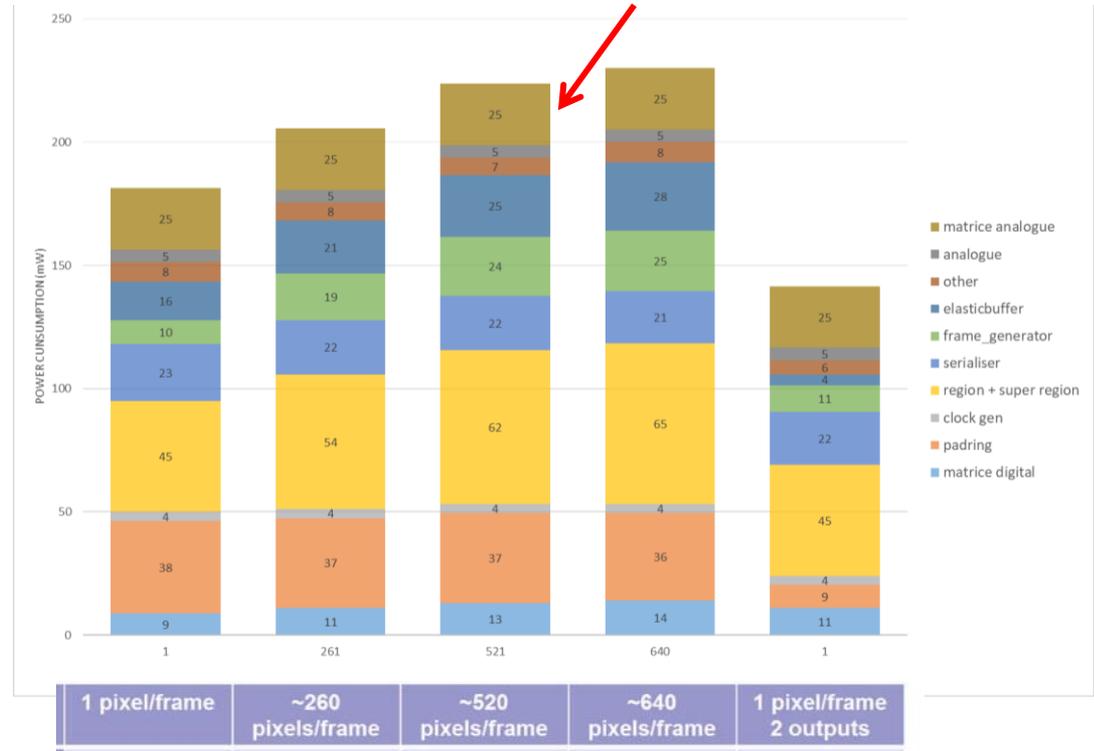
Challenge 2: Power consumption

- Mimosis-1: Detailed Power consumption simulation

✓ Validated previous estimates for ILC VXD Power consumption

- Ultimate challenge

✓ Air cooling only
 ✓ No Power Pulsing



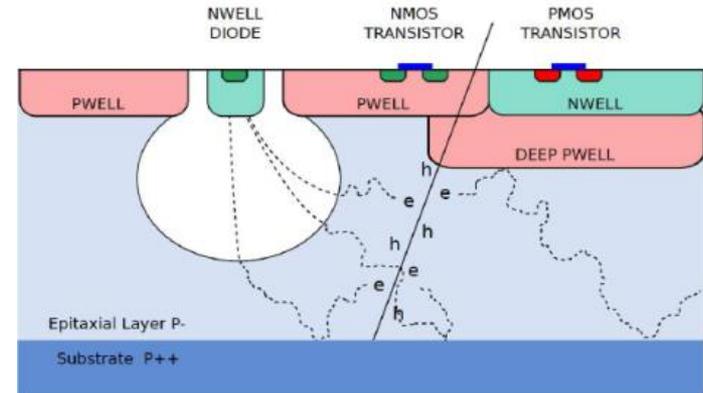
Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

Beam background rate	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
	(μ s)	(W)	Conservative	Ambitious
DBD	4 μ s	102 W	~31 W	~12 W
DBD	2 μ s	122 W		
DBD x 2	4 μ s	107 W		
DBD x 2	2 μ s	127 W		

Challenge 3: Optimizing the sensing element

Epitaxial layer

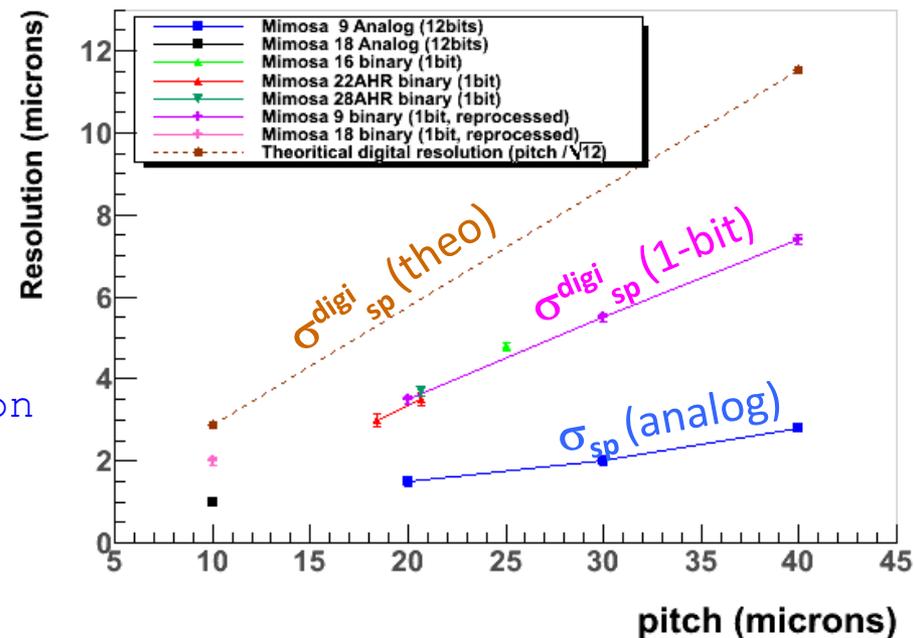
- ✓ Pitch
- ✓ Thickness
- ✓ Depletion
- ✓ doping profile
- ✓ Collecting diode & preamp.
- ✓ N bits to encode the charge



Effects on:

- ✓ Q_{signal} & SNR
- ✓ radiation tolerance
- ✓ Charge collection time
- ✓ cluster size & spatial resolution

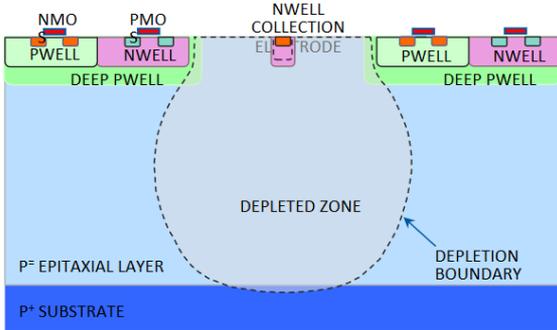
Mimosa resolution vs pitch



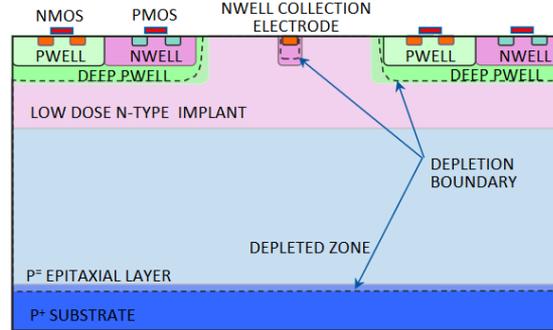
Sensing element simulations with TCAD:

Process Optimisation (CERN-Foundry)

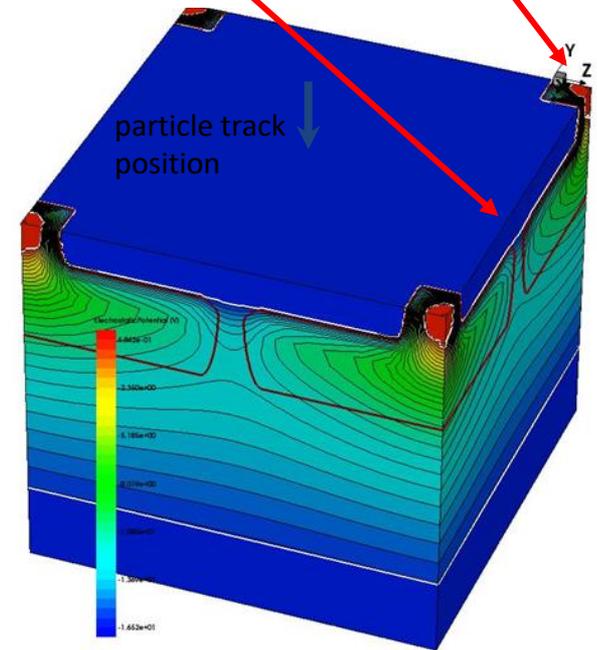
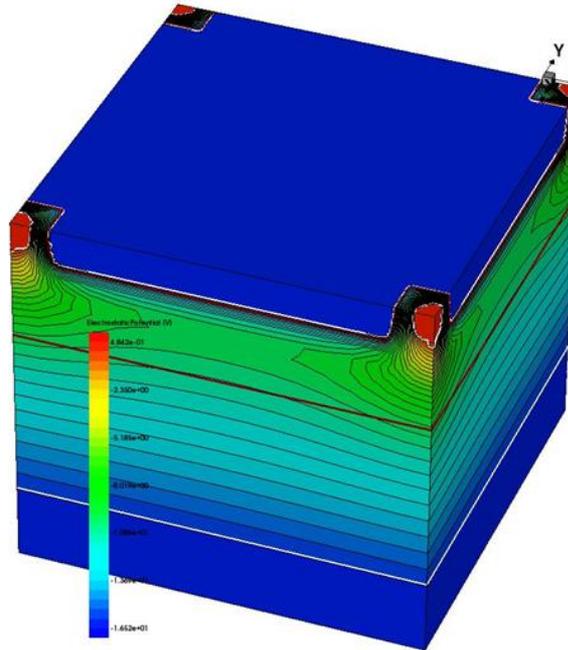
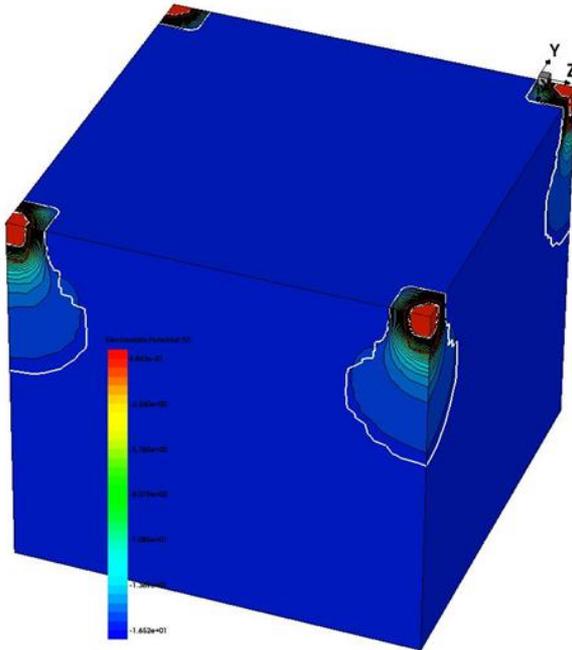
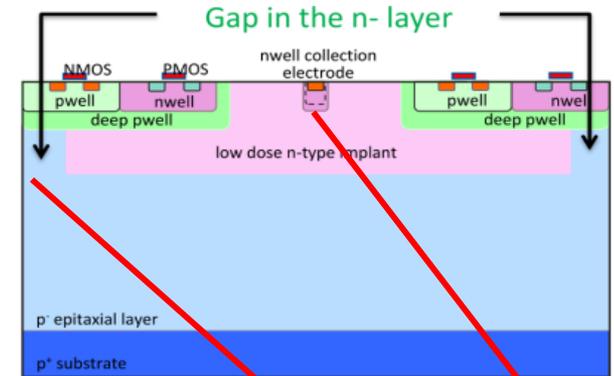
Standard (std): no full depletion



Modified (mod): full depletion, faster charge collection

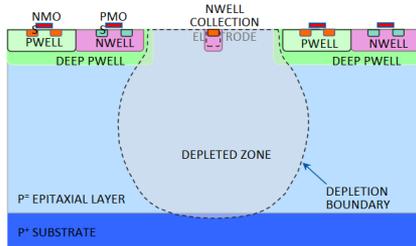


Modified (mod1): full depletion, improve charge collection time in pixel corners

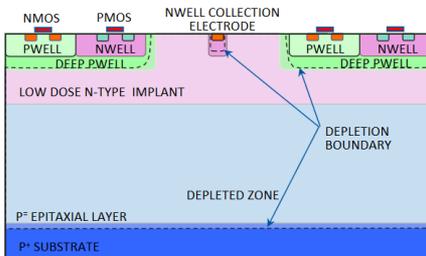


Process/geometry optimization ⇒ Charge sharing and charge collection time

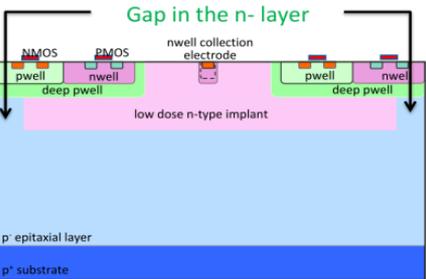
Charge collecting time simulations



std



mod



mod1

Collected charge as a function of time

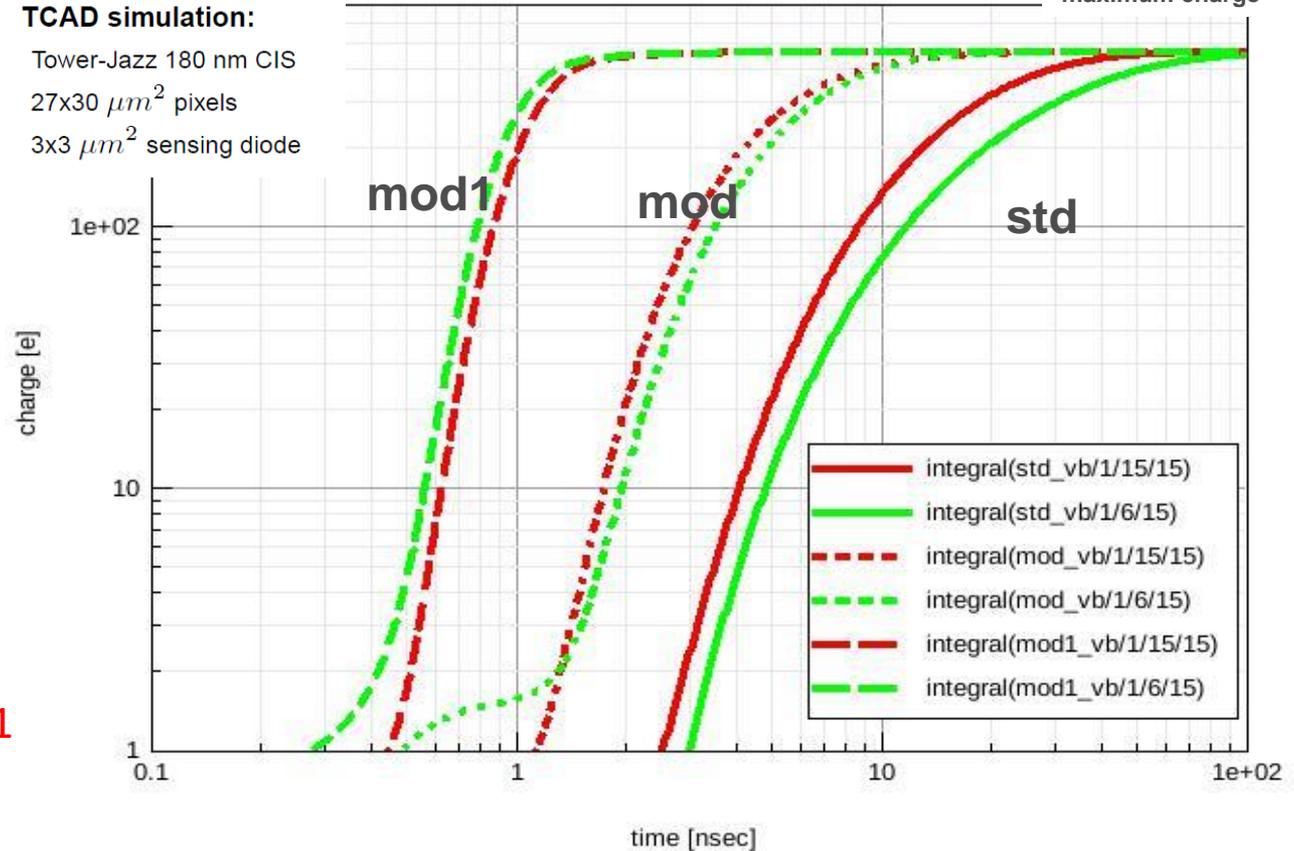
TCAD simulation:

Tower-Jazz 180 nm CIS

27x30 μm^2 pixels

3x3 μm^2 sensing diode

maximum charge ~450e



- Shorter collection time
 - ✓ Improves radiation tolerance
 - ✓ Necessary for ultimate time resolution < 100 ns
 - "QUARTET", R&D transverse project of IN2P3 (IPHC, CPPM, OMEGA)

Challenge 4 : Material budget

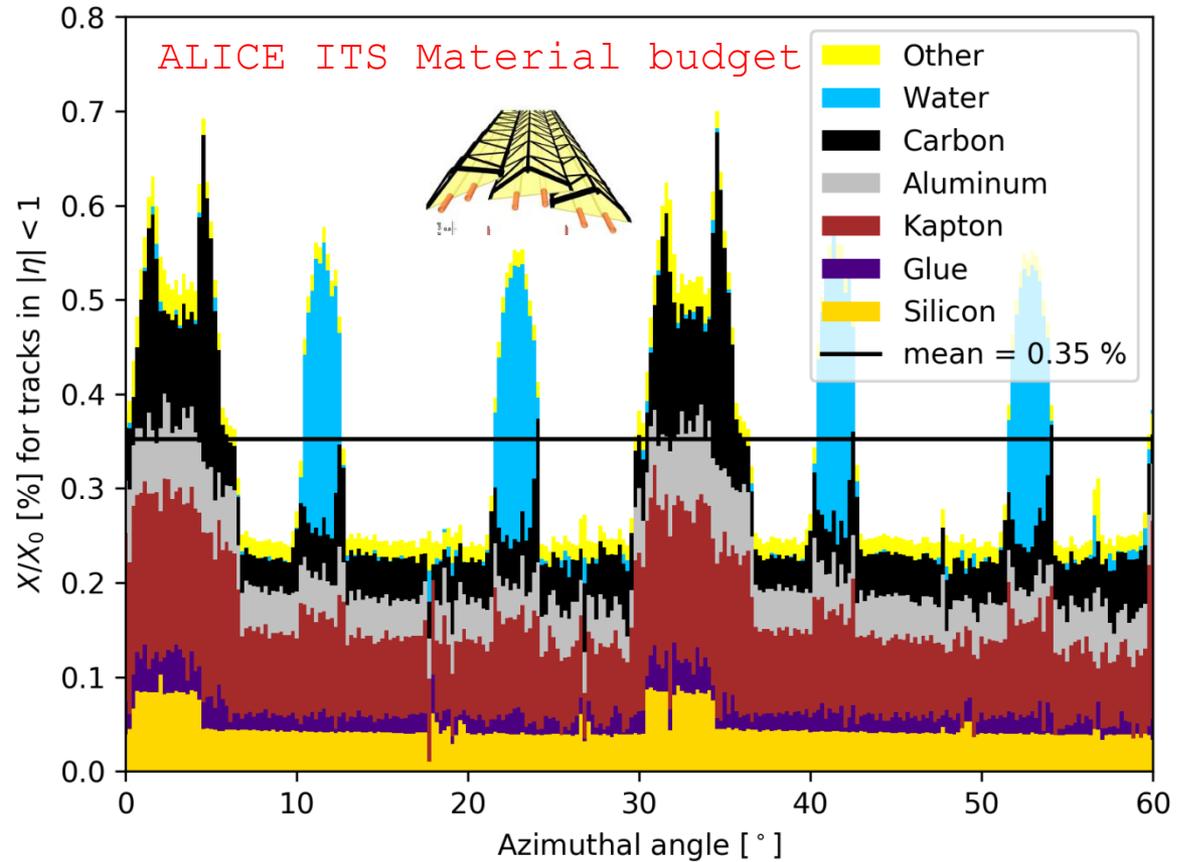
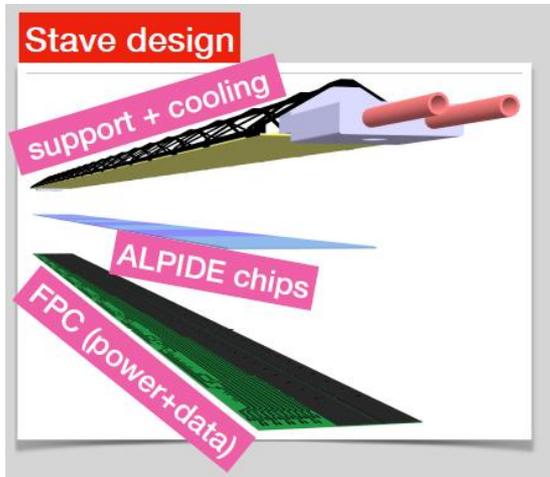
- PLUME double sided ladders
 - ✓ 0.35% X_0 reached \Rightarrow $\sim 0.3 X_0$ doable



- ALICE ITS

Proposal for an ITS upgrade in LS3

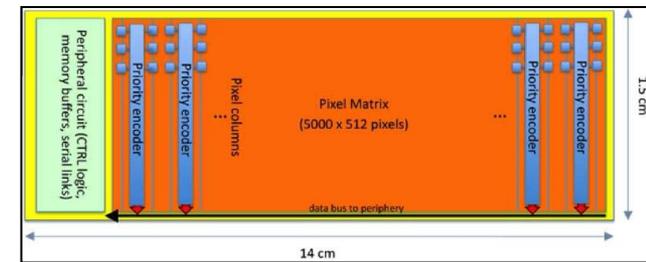
Magnus Mager (CERN)
LHCC 10.09.2019



\Rightarrow Contribution of sensors to total material budget $\sim 20-30\%$
(Majority from cables + cooling + support)

A possible answer: stitching

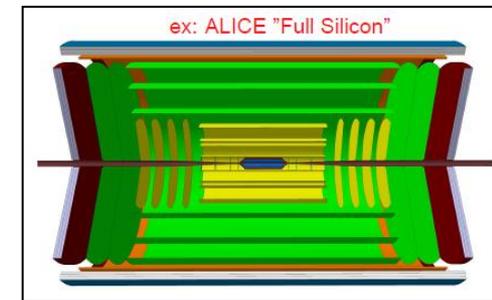
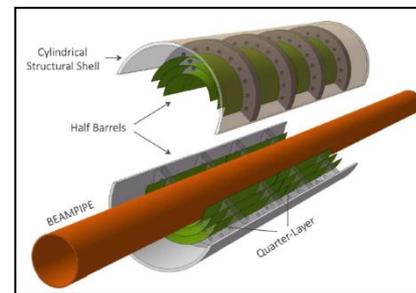
- Silicon is flexible
 - ✓ Self supported and bended circuits + detectors !
- Industry provides stitching
 - ✓ Multi-reticle size ladders
 - ~14 cm in 180 nm, 30 cm in 65 nm
 - Chip-to-chip interconnection
- Added value:
 - ✓ Very low material budget ($\sim 0.05-0.10 \% X_0$)
 - Flex cable ? Cooling ? Support ?
 - ✓ Large area detectors
 - Constant R = No overlaps or acceptance loss
 - Beam pipe as mechanical support



- ALICE R&D program
 - ✓ ALICE ITS upgrade beyond LS3
 - Exploit stitching
 - ✓ Proposal beyond LS4
 - 10 double sided layers
 - 100 m²

Proposal for an ITS upgrade in LS3

Magnus Mager (CERN)
LHCC 10.09.2019



- Challenge & potential issues
 - ✓ Bias voltage drops
 - ✓ Extended signal distance transport

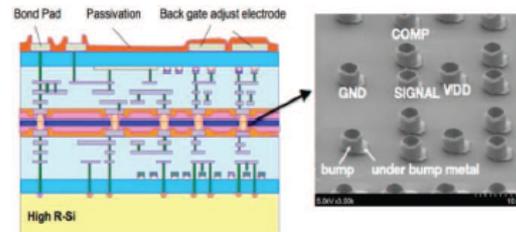
SOI development at IPHC

New features available in the SOI technology

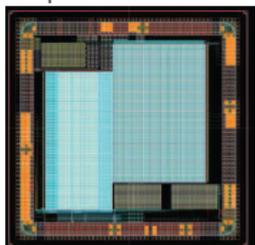
- Double tier “3D” – 5 μm pitch bonding *NIMA A 924 (2019) 422–425*
- Pinned photo-diode – *doi : 10.3390/s18010027*

Prototyping at IPHC

- Developed a Digital Library in cooperation with KEK
- Submitted two sensors in the last MPW run
 - Digital – for the Digital Library characterization
 - Analog



300 μm thick - 6x6 mm²



Analog Sensor features:

- Pixels in 18 μm pitch
- Matrix of Mimosi pixels
- New amplifier architecture
- Pixels with different collecting diodes



Study:

- Charge collection Timing
- Radiation damage influence

Perspectives

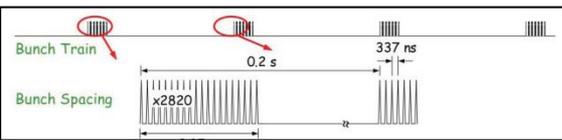
- 20 x 20 μm^2 Mimosi pixel with a digital tier on top
- Assembled structure thinned down to $\sim 50 - 75 \mu\text{m}$

Next MPW submission in May 2020

Conclusion: exploiting synergies

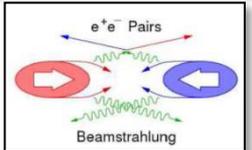
- CPS R&D in its better dynamics than ever
- ILC requirements achievable
 - ✓ Pitch $\sim 18 \times 18 \mu\text{m}$ ($\sigma_{\text{sp}} \sim 3 \mu\text{m}$) & r.o.time $\sim 1\text{-}4 \mu\text{s}$?
 - Doable with smaller feature sizes
- Joined effort inside EU AIDA++ program
 - ✓ CMOS work packages expected:
 - Time resolution & radiation hardness
 - High granularity and low mass devices
 - ✓ Beam telescopes WP
 - EUDET upgrades towards improved time resolution
 - ⇒ 65 nm technology exploration
 - ⇒ Final proposal Q1 2020
- CREMLIN+ (EU-Ru program, funding approved)
 - ✓ WP7.1: Development of fast CMOS pixel sensors
 - IPHC-Strasbourg, FAIR, JINR, Frankfurt univ, BINP, DESY, CERN, KINR
 - ✓ Goal ⇒ CBM-MVD station demonstrator
- ALICE beyond LS3/4 Proposal
 - ✓ Stitching & large surface
 - ✓ Very low mass detectors

Back up



Reminder: ILC VXD requirements

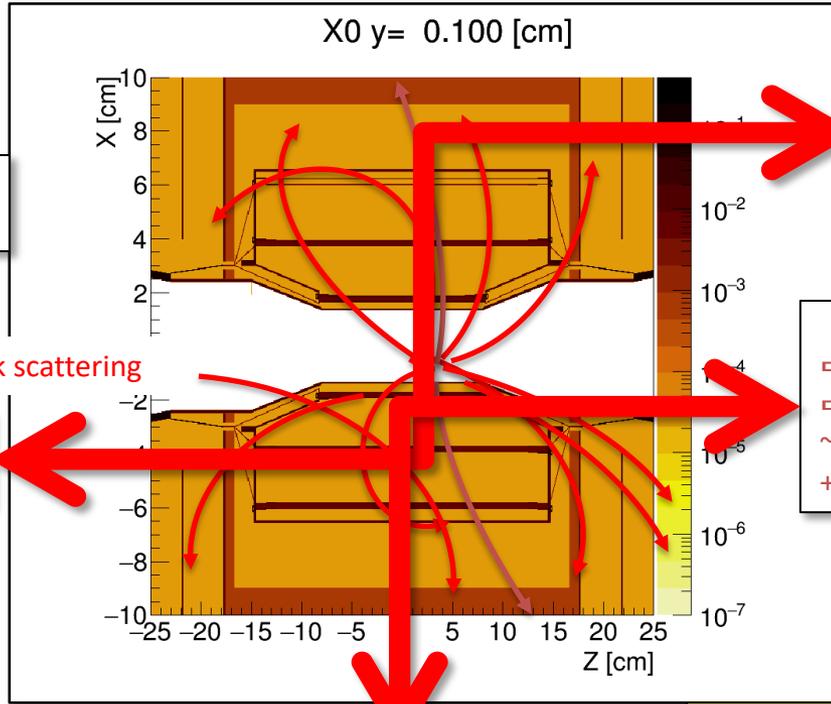
$$\sigma_b < 5\Theta \frac{10}{p\beta \sin^2\theta} \mu m$$



Physics (<Hz/cm²)

Physics
 ⇒ Flavour tagging
 ⇒ Low pT tracks

Beam background (~ 5 hits/BX/cm² on layer 0)



Vertex reconstruction
 ⇒ granularity
 ⇒ Pitch ~17 μm
 ⇒ (σ_{sp} ~3 μm)

Material Budget
 ⇒ ~ 0.15% X₀ / layer
 ⇒ < 1% X₀ for the whole VTX
 ~ 900 μm Si
 + ~0.14% X₀ for the beam pipe

Beam background

Radiation hardness
 O(100kRad/yr) & O(10¹¹)n_{eq}/yr

Rad.Tol. devices

Read-out speed
 O(1-10 μs)

Power consumption
 ~< 50mW/cm²

Fast read-out & low Power architectures

Cooling
 Stiffness / Alignment

Low material detectors & supports structures

Challenge : meet the requirements all together

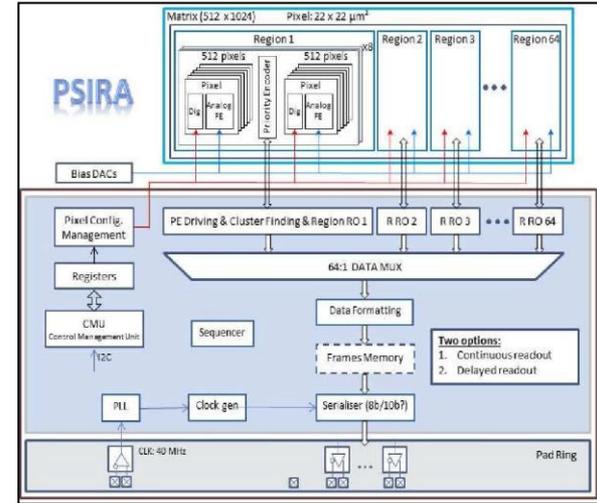
Extension of MIMOSIS to ILC vertexing and tracking

Conservative approach

- ✓ Minimize changes w.r.t. MIMOSIS
 - Keep TJ 0.18 μm technology & a similar architecture
- ✓ 2 sub-systems targeted
 - Vertex detector & Silicon inner trackers (SIT @ ILD)

⇒ PSIRA

⇒ Finalize CPS ~2025

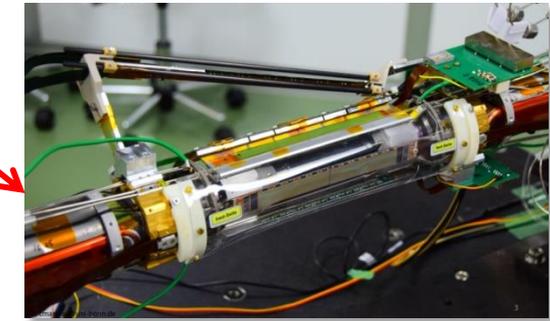
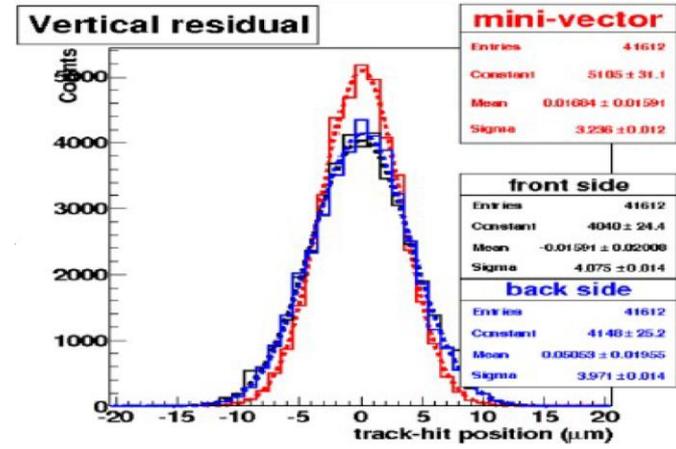
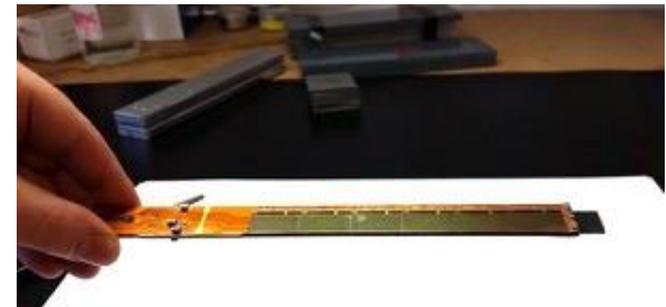
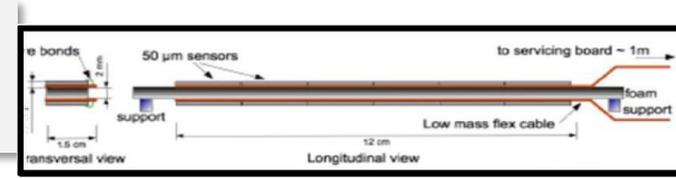


Expected Performances

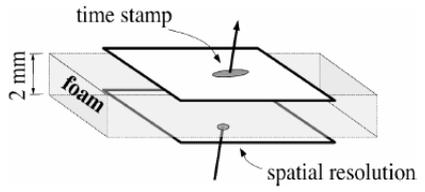
- ✓ $\sigma_{sp} \sim 4 \mu\text{m} \Rightarrow$ Use double sided $\Rightarrow \sigma_{sp} \sim 2.8 \mu\text{m}$
 - 22x22 $\mu\text{m}^2 \sim 20\%$ better spatial resolution % ALPIDE (vertexing)
 - Faster = higher Power consumption
 - ✓ Read-out time: 2-4 μs (ILD-VXD) and 1 μs (ILD-SIT)
 - ✓ Single pixel address read-out = 50 ns
 - (with 20 MHz clock)
 - ✓ Sustainable occupancy (~ 5 pixels/hits)
 - ~ 4 hits/region/ $\mu\text{s} \sim 100$ hits/ $\text{cm}^2/\mu\text{s}$
- Can one reach : Pitch $\sim 18 \times 18 \mu\text{m}$ ($\sigma_{sp} \sim 3 \mu\text{m}$) & r.o.time $\sim 2-4 \mu\text{s}$?
 - Doable with smaller feature sizes

⇒ PSIRA architecture already reaching 4-8 BX read-out time
⇒ Power vs read-out speed compromise
⇒ Avoiding power pulsing possible ?

Integration (example of PLUME collaboration)



- Plume collaboration (Bristol, DESY, IPHC)
 - ✓ Double sided ladders with minimized material budget
- Plume-02 prototypes
 - ✓ Successfully validated in test beam
 - ✓ Cu/Al flex cable (0.42/0.35 % X_0)
 - ✓ 6 ladders fabricated
 - 2 installed in BEAST for Belle-2 commissioning
- Summary
 - ✓ No major issue
 - ✓ 0.3 % X_0 reachable
 - ✓ Possible next step:
 - \neq chips on each side
 - Replace carbon foam by carbon fiber



Know-how acquired \Rightarrow Ladders close to ILC mat. budget specifications

e⁺e⁻ collider beam parameters

Linear

Parameter	ILC		CLIC		
	250 GeV	500 GeV	380 GeV	1.5 TeV	3 TeV
Luminosity L ($10^{34}\text{cm}^{-2}\text{sec}^{-1}$)	1.35	1.8	1.5	3.7	5.9
L > 99% of ν_s ($10^{34}\text{cm}^{-2}\text{sec}^{-1}$)	1.0	1.0	0.9	1.4	2.0
Repetition frequency (Hz)	5	5	50	50	50
Bunch separation (ns)	554	554	0.5	0.5	0.5
Number of bunches per train	1312	1312	352	312	312
Beam size at IP σ_x/σ_y (nm)	515/7.7	474/5.9	150/2.9	~60/1.5	~40/1
Beam size at IP σ_z (μm)	300	300	70	44	44

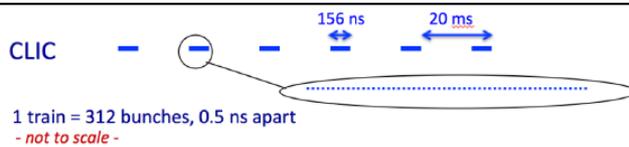
ILC: Crossing angle 14 mrad, e⁻ polarization $\pm 80\%$, e⁺ polarization $\pm 30\%$

CLIC: Crossing angle 20 mrad, e⁻ polarization $\pm 80\%$

Very small beams + high energy
=> beamstrahlung

Very small bunch separation at CLIC drives timing requirements for detector

Very low duty cycle at ILC/CLIC allows for:
Triggerless readout
Power pulsing



Circular

	FCC-ee			CEPC	
	Z	Higgs	ttbar	Z (2T)	Higgs
\sqrt{s} [GeV]	91.2	240	365	91.2	240
Luminosity / IP ($10^{34}\text{cm}^{-2}\text{s}^{-1}$)	230	8.5	1.7	32	1.5
no. of bunches / beam	16640	393	48	12000	242
Bunch separation (ns)	20	994	3000	25	680
Beam size at IP σ_x/σ_y ($\mu\text{m}/\text{nm}$)	6.4/28	14/36	38/68	6.0/40	20.9/60
Bunch length (SR/BS) (mm)	3.5/12.1	3.3/5.3	2.0/2.5	8.5	4.4
Beam size at IP σ_z (mm)					

Beam transverse polarisation

=> beam energy can be measured to very high accuracy (~ 50 keV)

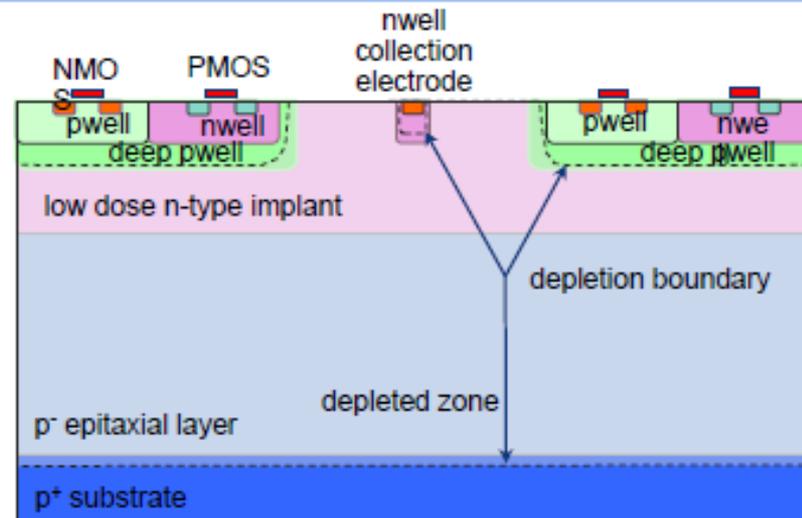
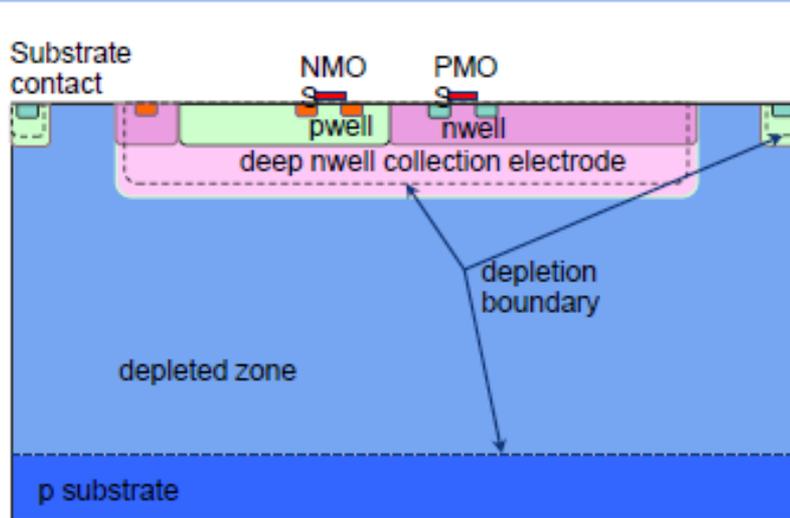
At Z-peak, very high luminosities and very high e⁺e⁻ cross section (40 nb)

- ⇒ Statistical accuracies at 10^{-4} - 10^{-5} level ⇒ drives detector performance requirements
- ⇒ Small systematic errors required to match
- ⇒ This also drives requirement on data rates (physics rates 100 kHz)
- ⇒ Triggerless readout likely still possible

Beam-induced background, from beamstrahlung + synchrotron radiation

- Most significant at 365 GeV
- Mitigated through MDI design and detector design

Large vs Small collection electrode



Large collection electrode (HV-CMOS)

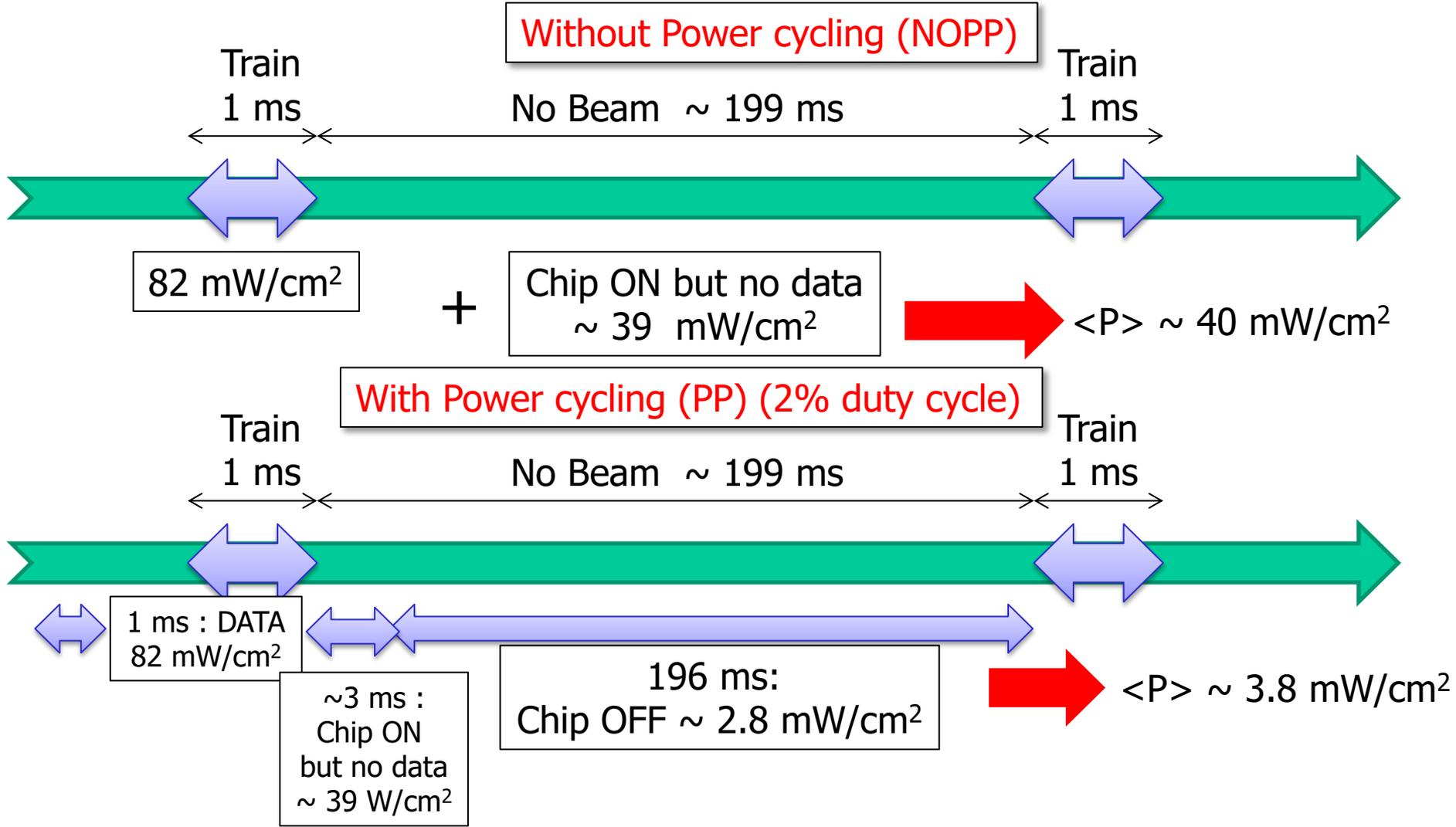
- Large capacitance
- Higher power
- Practically uniform field
- Very high radiation tolerance

Small collection electrode (TJ)

- Small capacitance
- Lower power
- Less prone to coupling
- Longer signal travel path, process modification to increase radiation tolerance

Monolithic Pixel Developments - T. Kugathasan - ACES 2018 - CERN - 25/04/2018

Power scheme for VTX-ILD (inner layer)



Hypothesis: 3 double sided layers (3483 cm²), PSIRA architecture (4 μs / 4 μm), DBD background @ √s = 500 GeV, no safety factor

Power: Results

Power Analog (<i>mW/chip</i>)	49.22
Power Bias (<i>mW/chip</i>)	4.5
Power PriorityEncoder (<i>mW/chip</i>)	4.219
Power DigitalPeriphery (<i>mW/chip</i>)	64.27
Power PLL (<i>mW/chip</i>)	18.5
Power Serializer With Data (<i>mW/chip</i>)	86.06
Power Serializer With No Data (<i>mW/chip</i>)	0
Power LVDS (<i>mW/chip</i>)	56.4

Period	Relative Energy
E during train	225 mJ ~ 4 %
E between train (Power ON)	380 mJ ~ 6 %
E between train (Power OFF)	5740 mJ ~ 90 %

Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

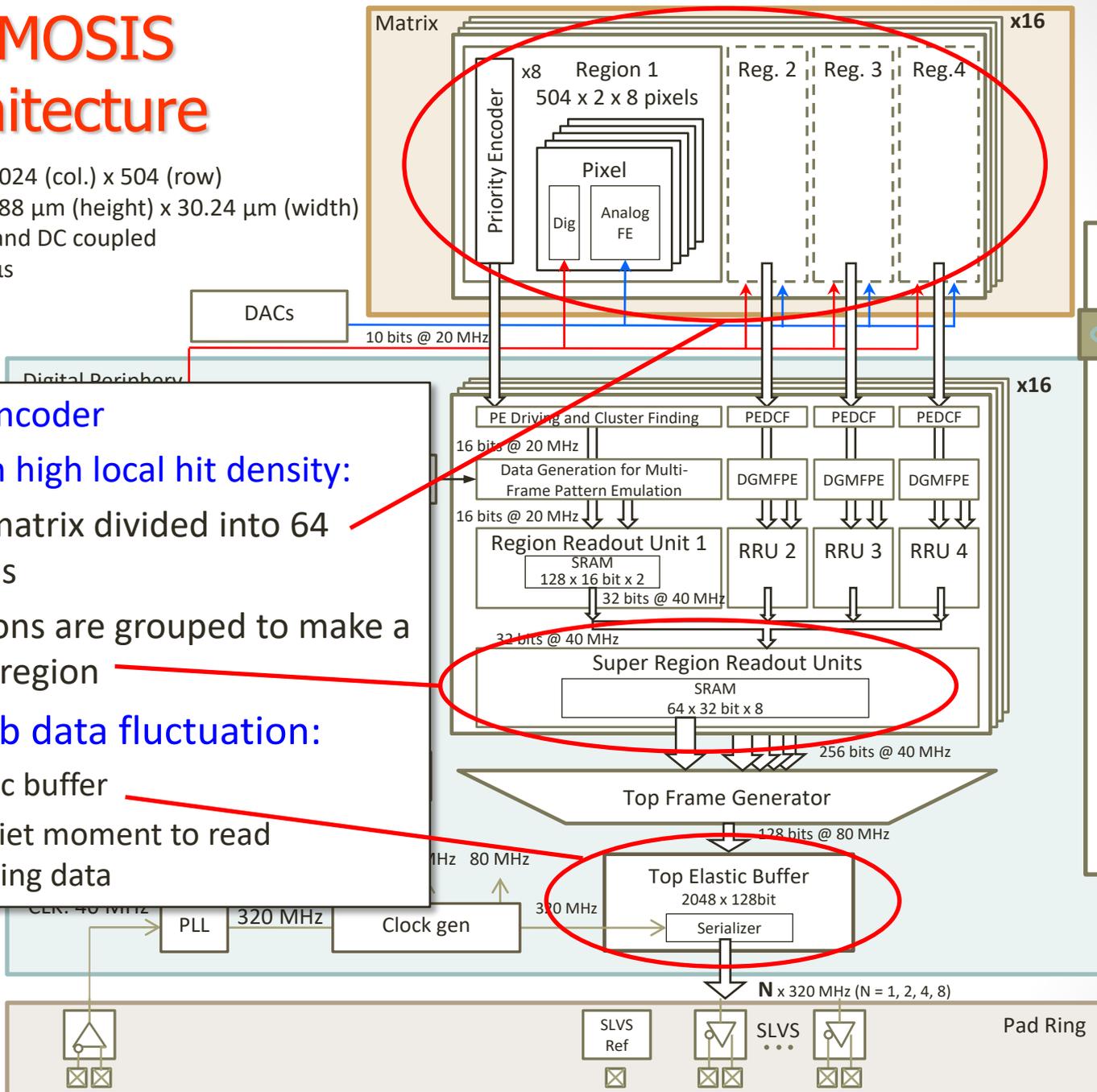
Beam background rate	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
	(μ s)	(W)	Conservative	Ambitious
DBD	4 μ s	102 W	~31 W	~12 W
DBD	2 μ s	122 W		
DBD x 2	4 μ s	107 W		
DBD x 2	2 μ s	127 W		

- Chip read-out speed
 - 2 ms - 4 ms
- Power pulsing
 - Power ON, no beam during 1-3 ms
 - Leading parameter With NO P.P.
 - Power OFF: 10-30 mW/chip
 - Leading parameter with P.P.
- Outer layers
 - Lower occupancy
 - Power is dominated by outer layers
- Beam background rate
 - DBD – DBD x 2



MIMOSIS architecture

Matrix dimension: 1024 (col.) x 504 (row)
 Pixel dimension: 26.88 μm (height) x 30.24 μm (width)
 2 kind of pixels: AC and DC coupled
 Integration time: 5 μs



- Priority Encoder
- To sustain high local hit density:
 - Pixel matrix divided into 64 regions
 - 4 regions are grouped to make a super region
- To absorb data fluctuation:
 - 1 Elastic buffer
 - Use quiet moment to read remaining data