Analysis of SiW-ECAL technological prototype beam test with electron beam

Y. Kato[B], K. Goto[A], T. Suehara[A]
and ILD SiW-ECAL group
Kyushu University[A]
The University of Tokyo[B]

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katou@icepp.s.u-tokyo.ac.jp

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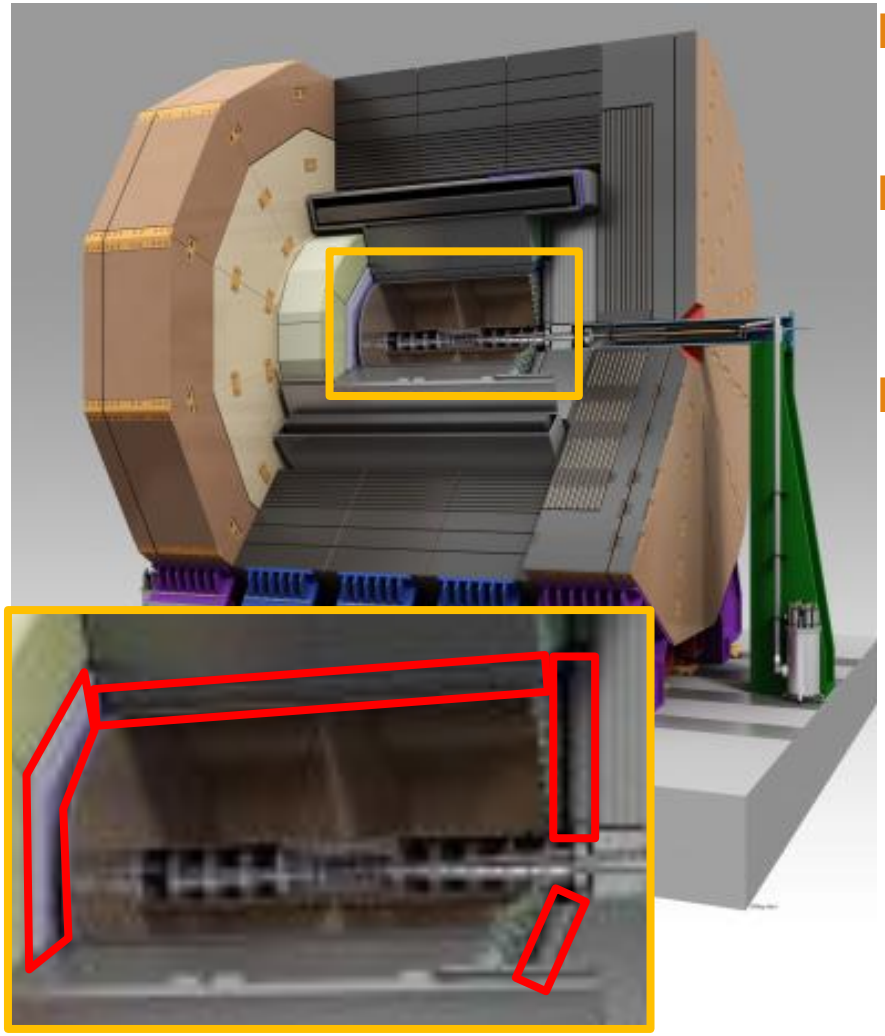
International Large Detector



- One of the detector concepts at the ILC
- Optimized for Particle Flow Algorithm
  - Reconstruct & identify all the particles
- Components
  - Vertex detector
  - Trackers
  - Calorimeters
    - ECAL
      - ScW-ECAL
      - SiW-ECAL
    - HCAL
  - Muon Yoke

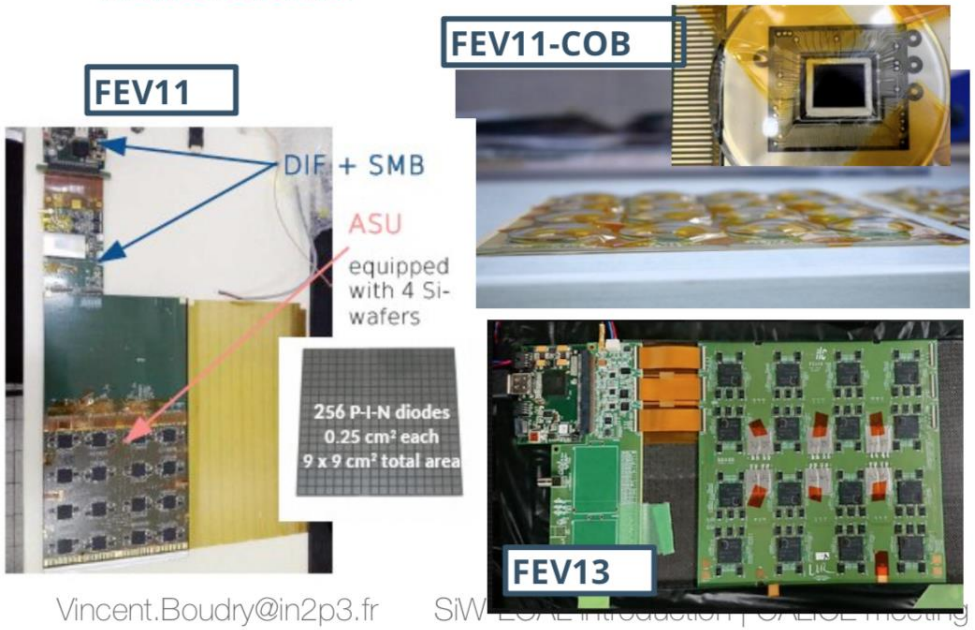
etc.

R&D of SiW–ECAL technological prototypes

ASU: 12 years of R&D

Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints



Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	7 units	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig.}$ 6–8 % masked
1st technological ECAL	2018	SLABvFEV11 & FEV13 SK2a+ Compact stack	SK2 & SK2a (⊃timing)	Improved S/N Timing...

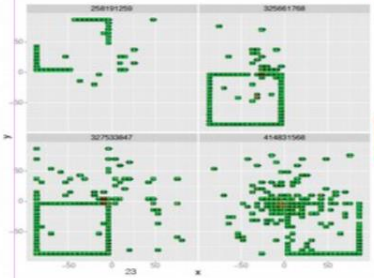
Vincent.Boudry@in2p3.fr

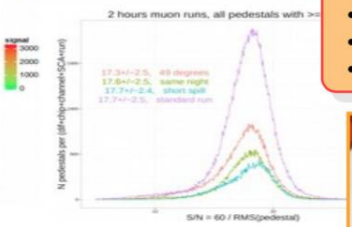
R&D of SiW-ECAL technological prototypes

Beam-test 2015-2018

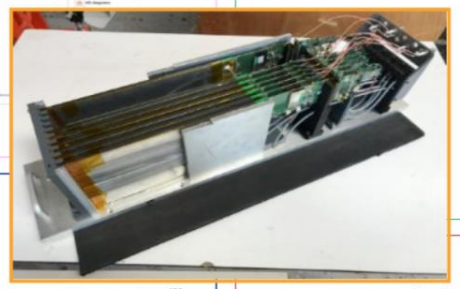
CERN 2015

"Naked FEV11"





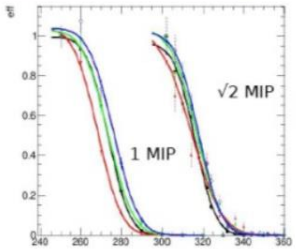
S/N_{ADC} = 16–17
(MIP – ped) / σ_{ped}
Defaults cataract :
- Negative signals
- re-triggers
- ~ high thr.
- sq events / 10



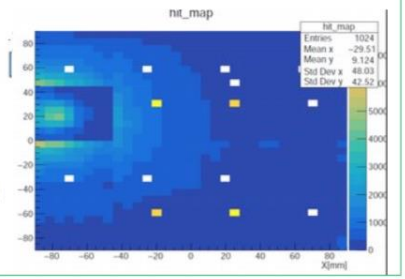
DESY 2018

7 FEV11 + 1 FEV13(650µm)

S/N_{Trig} ~ 11.6.±0.7
Trigger → ~1/3 mip (est.)
First comm. of FEV13

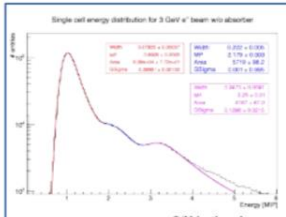


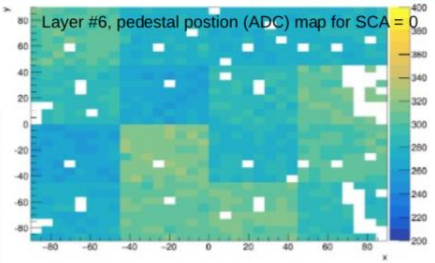
Slab 17, 18, 19, 20
S/N = 11.6 ± 0.7

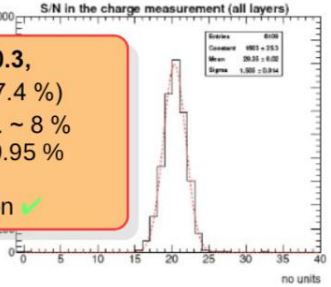


DESY 2017

7 FEV11





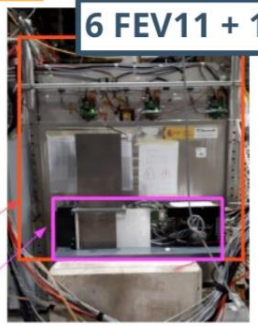


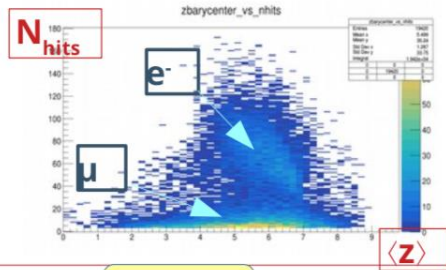
S/N_{ADC} = 20.3,
$\sigma_{S/N}$ = 1.5 (7.4 %)
masked ch. ~ 8 %
Hit eff. ~ 99.95 %
0°, 45° ✔
1T operation ✔

CERN 2018

Masked ch (FEV11) ~ 4 %

6 FEV11 + 1(4) FEV13(320 & 650µm) + 24X_0 W



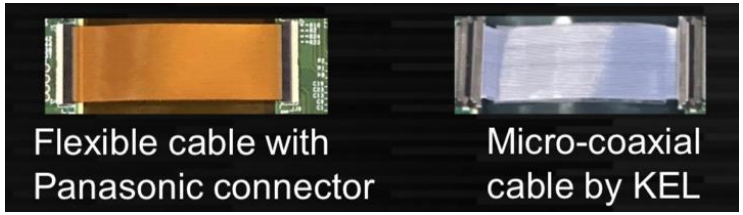


Vince -ECAL introduction | CALICE meeting | Utrecht uni, 10/04/2019 Taikan 11/35

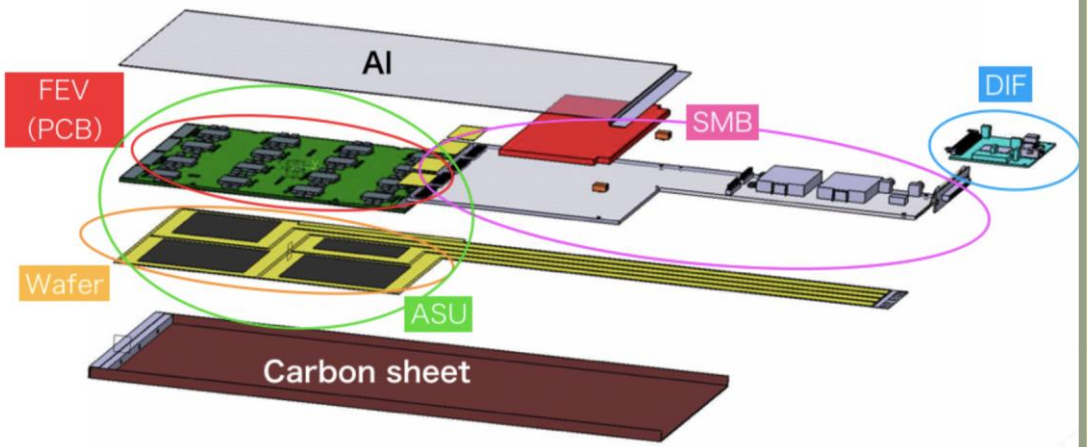
R&D of SiW-ECAL technological prototypes

Major changes in FEV11 → 13 and SMBv4 → v5

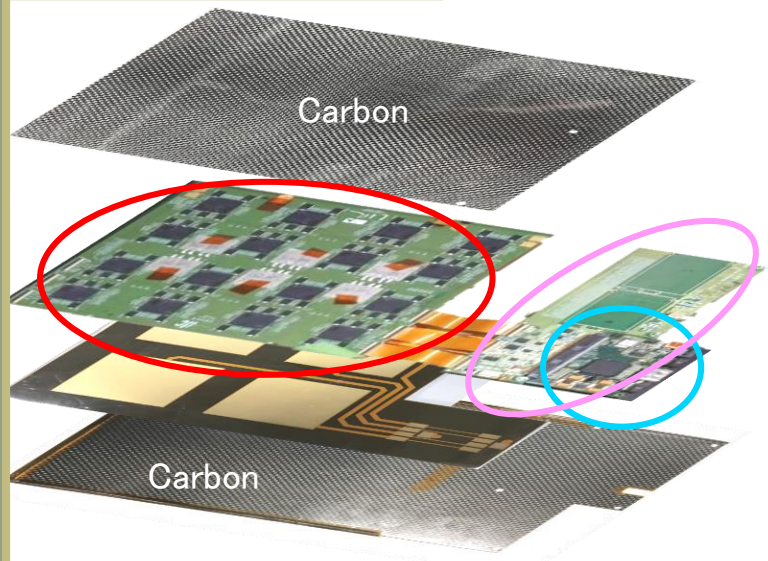
- ASIC: SKIROC2 → 2A
  - Individual threshold control
  - Improvements on TDC
- Smaller SMB footprint
- Connection by 0.4mm-pitch flex cables
  - Two candidates, footprint compatible



FEV11 & SMBv4

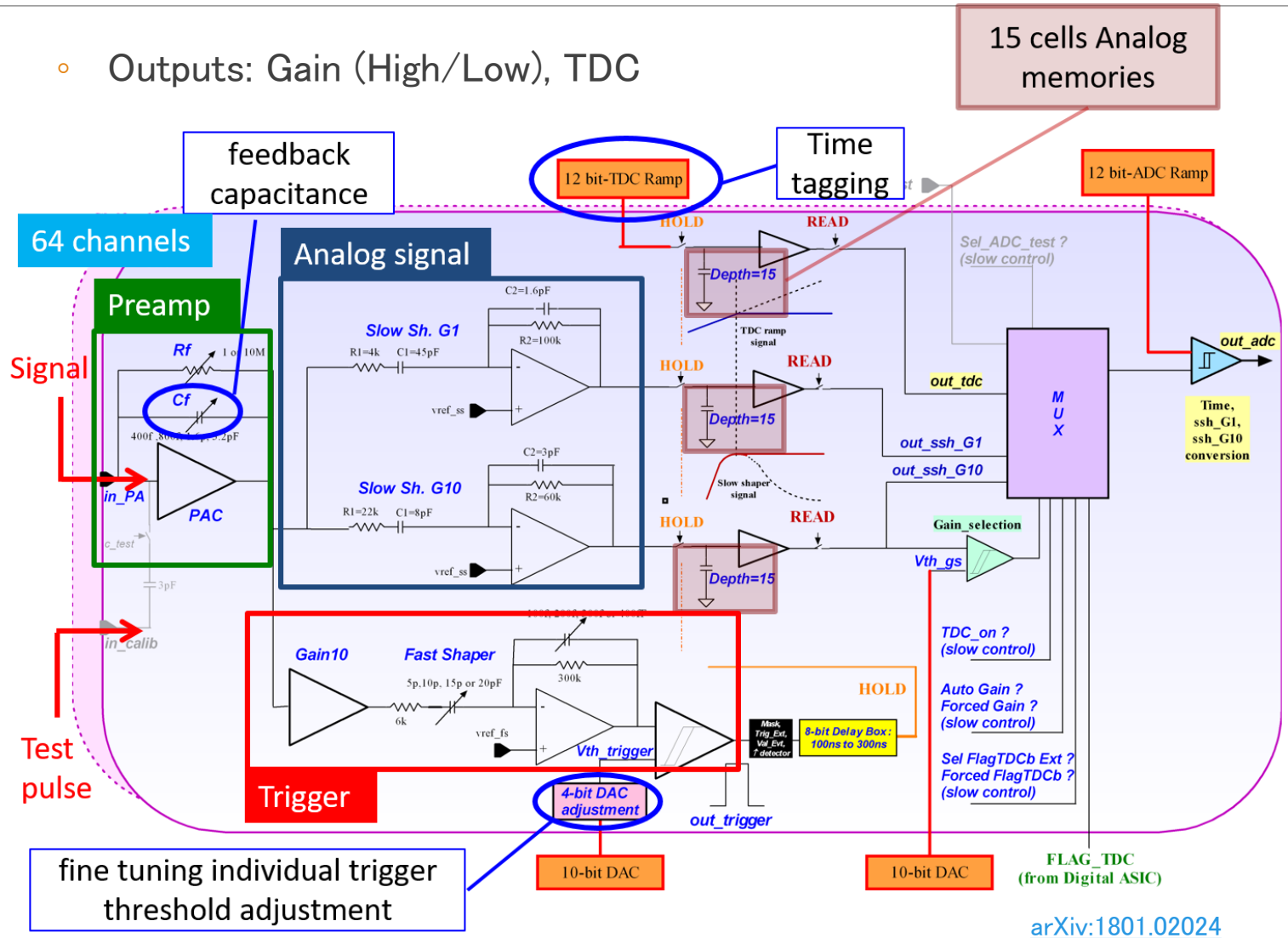


FEV13 & SMBv5



Analogue core: SKIROC2A

- Outputs: Gain (High/Low), TDC

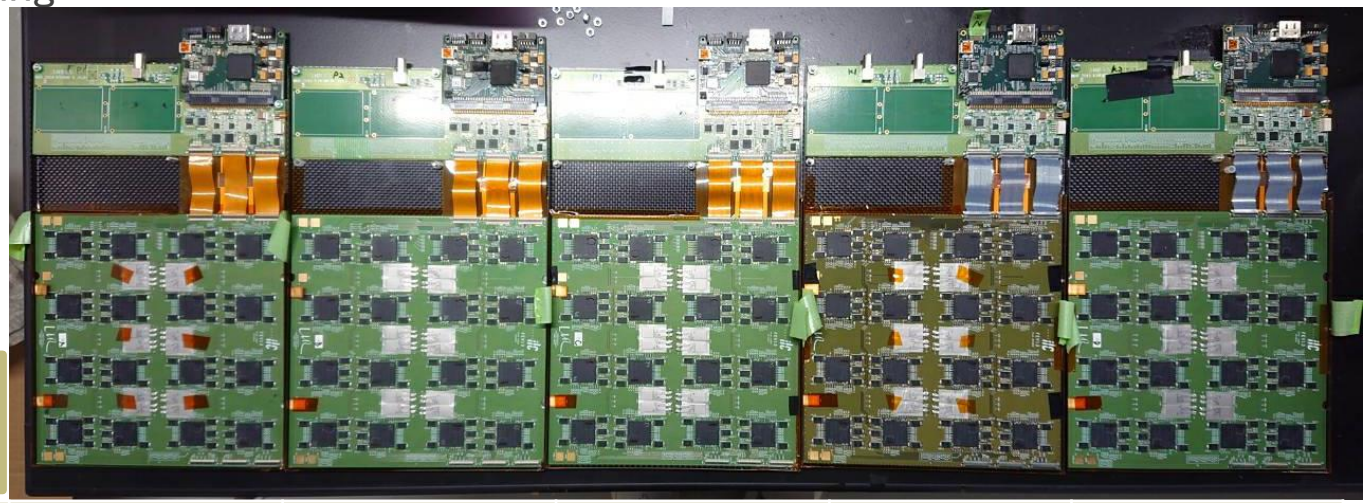


arXiv:1801.02024

FEV13-Jp Status

- ASIC: SKIROC2A
- Si thickness: 320μm & **650μm** New!
  - 256 ch/sensor × 4 sensor/slab
- FEV-SMB Connection: Flexible cable or Micro-coaxial cable
- EM shielding: w/ Carbon frame and cover
- Power Pulsing

➢ See previous talk for details

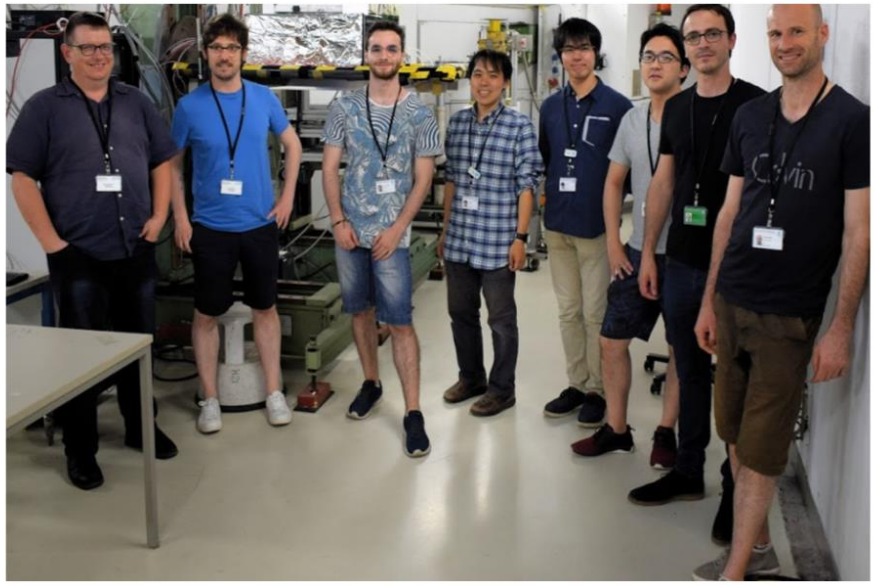


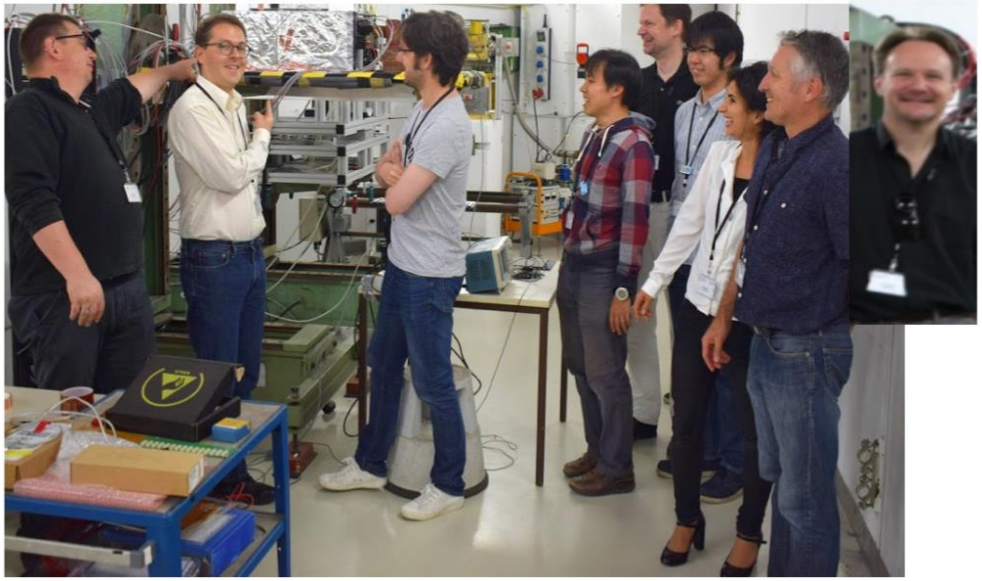
Total 5 slabs in Kyushu U., Japan

slab ID	P1	P2	P3	K1	K2
Si thickness	650 μm	650 μm	320 μm	650 μm	650 μm
Assembly	in Kyushu U.	in Kyushu U.	in Kyushu U.	in LLR	in Kyushu U.

Beam Test 2019 @ DESY

- Beam time:
  - 24th June – 7th July at DESY test beam facility
  - e^- beam: 1 – 5 GeV
- Presence from:
- Support & Hardware from:





Beam Test 2019 @ DESY

- Beam time:
  - 24^{th} June – 7^{th} July at DESY test beam facility
  - e^- beam: 1 – 5 GeV
- Objectives:
  - Comparison of ASU based on BGA and based on Chip-On-Board (COB)
  - Test of new SL-Boards
  - **Validation of FEV13-Jp** ← Target of this talk
- Programs:

MIP program (w/o Tungsten)

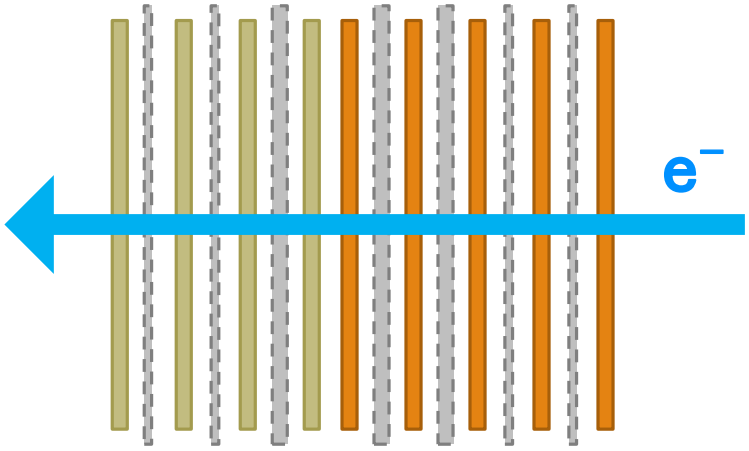
- **Position scan for MIP calibration**
- **TDC test**
- Angled beam: 25 deg.
- **Retriggering / double pedestal**

Shower program (w/ Tungsten)

- **Energy measurement**
- Response from large signal
- TDC / auto gain
- Edge effect

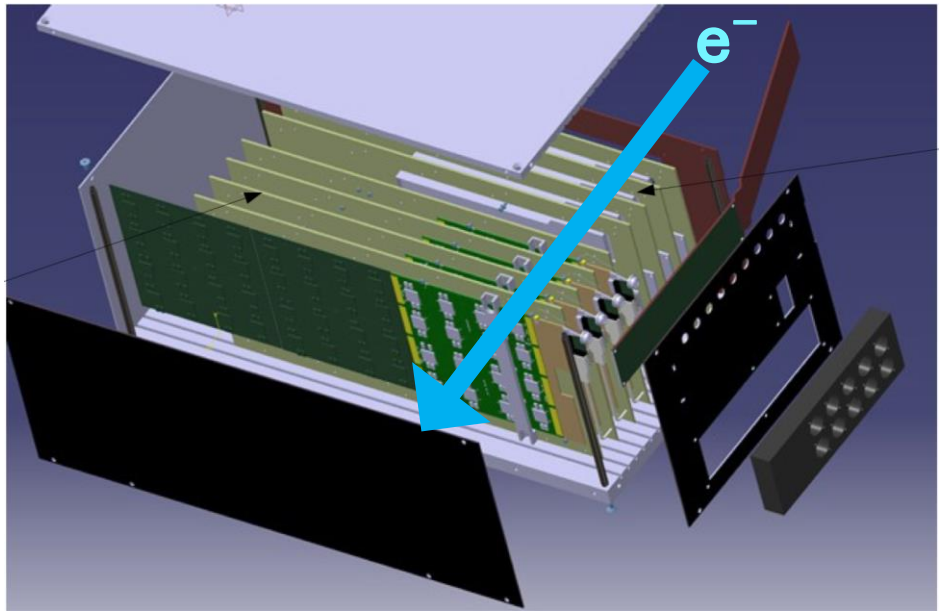
Setup for Beam Test

- Devices: 2 types of readouts
  - DIF based slabs: FEV13-Jp × 5
  - SLB based slabs:
    - COB × 2
    - FEV12 × 2
- Absorber: Tungsten
  - X_0 = 3.5 mm, R_M = 9 mm, λ_0 = 96 mm



SLB slabs DIF slabs

Tungsten (2.1 mm / 4.2 mm)



Procedure for Energy Measurement

Single Slab Analysis

1. Trigger adjustment & Masking of noisy channels
2. Pedestal calibration

   16 chips × 64 channels × 15 memories
3. Gain calibration using MIP

   16 chips × 64 channels
4. (TDC calibration using test pulse)

   time walk correction

Multi Slab Analysis

1. Timing coincidence

   using bunch crossing ID (BCID) $\Delta t = 0.2\ \mu s$
2. Event Building

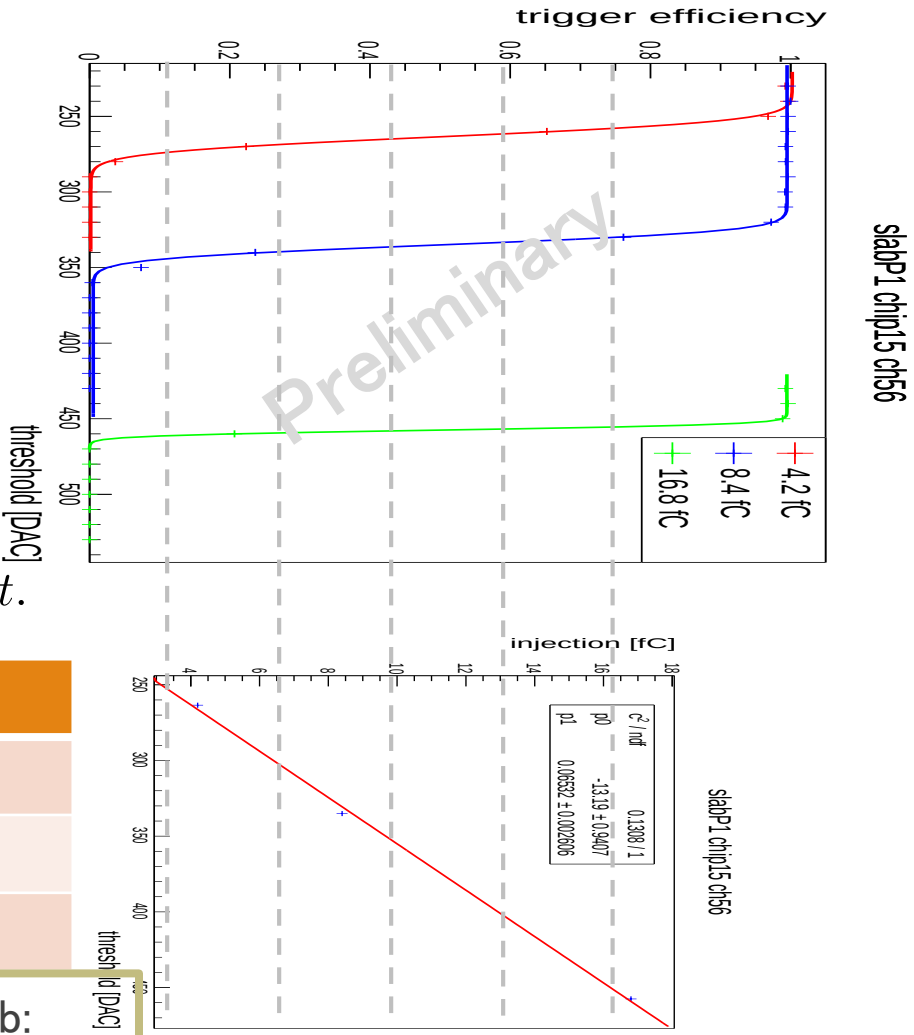
Trigger Adjustment

- Threshold scan is performed for evaluation of S/N_{Trig} and trigger adjustment.

$$S/N_{Trig} \equiv \frac{\mu_{2\mathrm{MIP}} - \mu_{1\mathrm{MIP}}}{\sigma_{1\mathrm{MIP}}}$$

- Test pulse of {4.2, 8.4, 16.8} fC is injected.
  - 320 μm: 1 MIP ~ 4.2 fC
  - 650 μm: 1 MIP ~ 8.4 fC
- S-curve is fitted by Err-function.

$$f(x) = C * Erfc(-\frac{x-\mu}{\sqrt{2}\sigma}) + const.$$

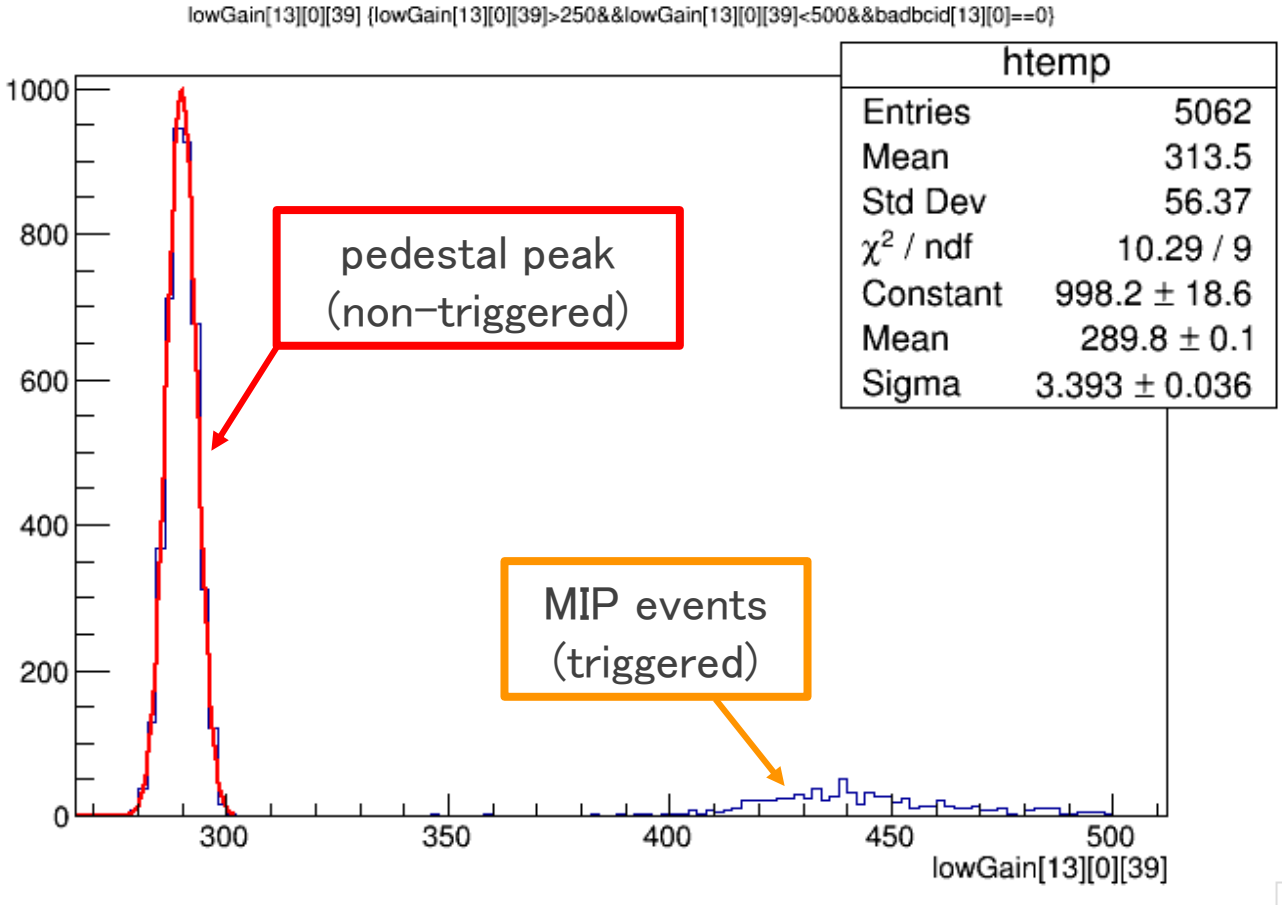


Injection [fC]	4.2	8.4	16.8
mean [DAC]	263.5	335.1	457.5
sigma [DAC]	11.9	10.3	4.3
S/N_{Trig}	6.0		11.9

Trigger is set as 0.5 MIP of 320 μm slab:
~ 230 DAC.

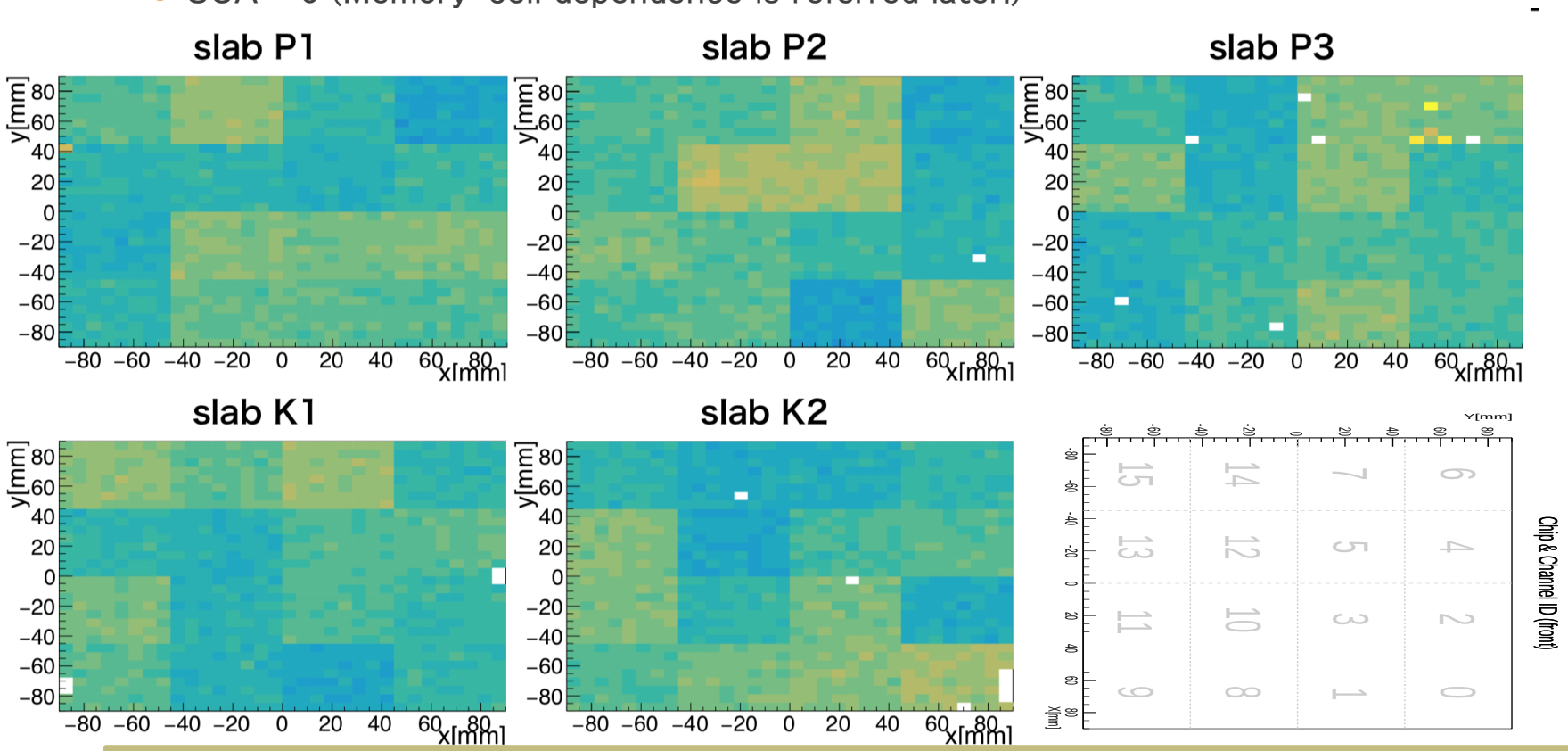
Pedestal Analysis

- Non-triggered ADC output (around ~300 [ADC])
- Fitted by Gaussian



Pedestal Homogeneity: Mean

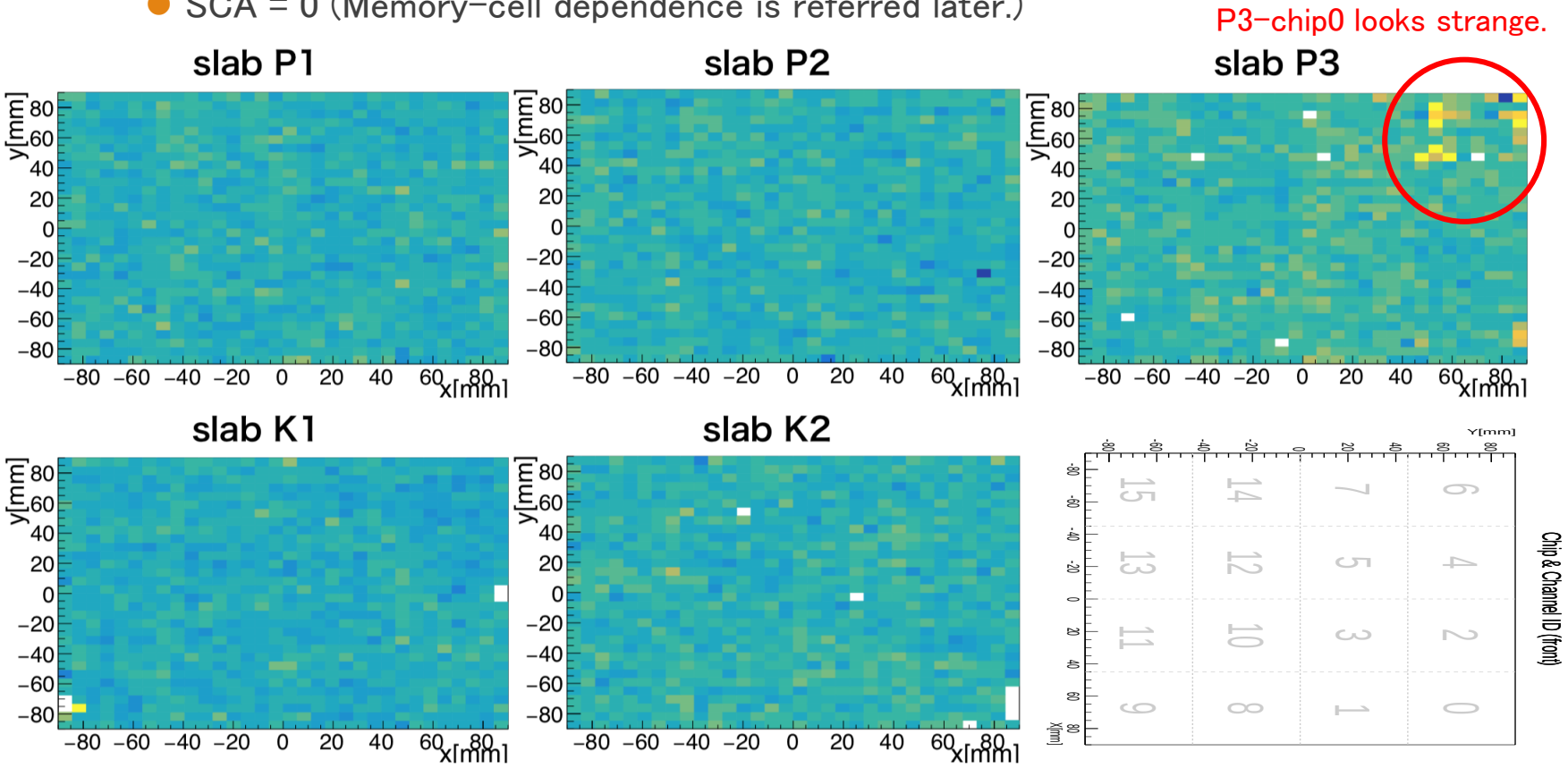
- Mean of Gaussian
- SCA = 0 (Memory-cell dependence is referred later.)



➢ Although there are differences between chips,
mean of pedestals looks generally uniform within the same chip.

Pedestal Homogeneity: Width

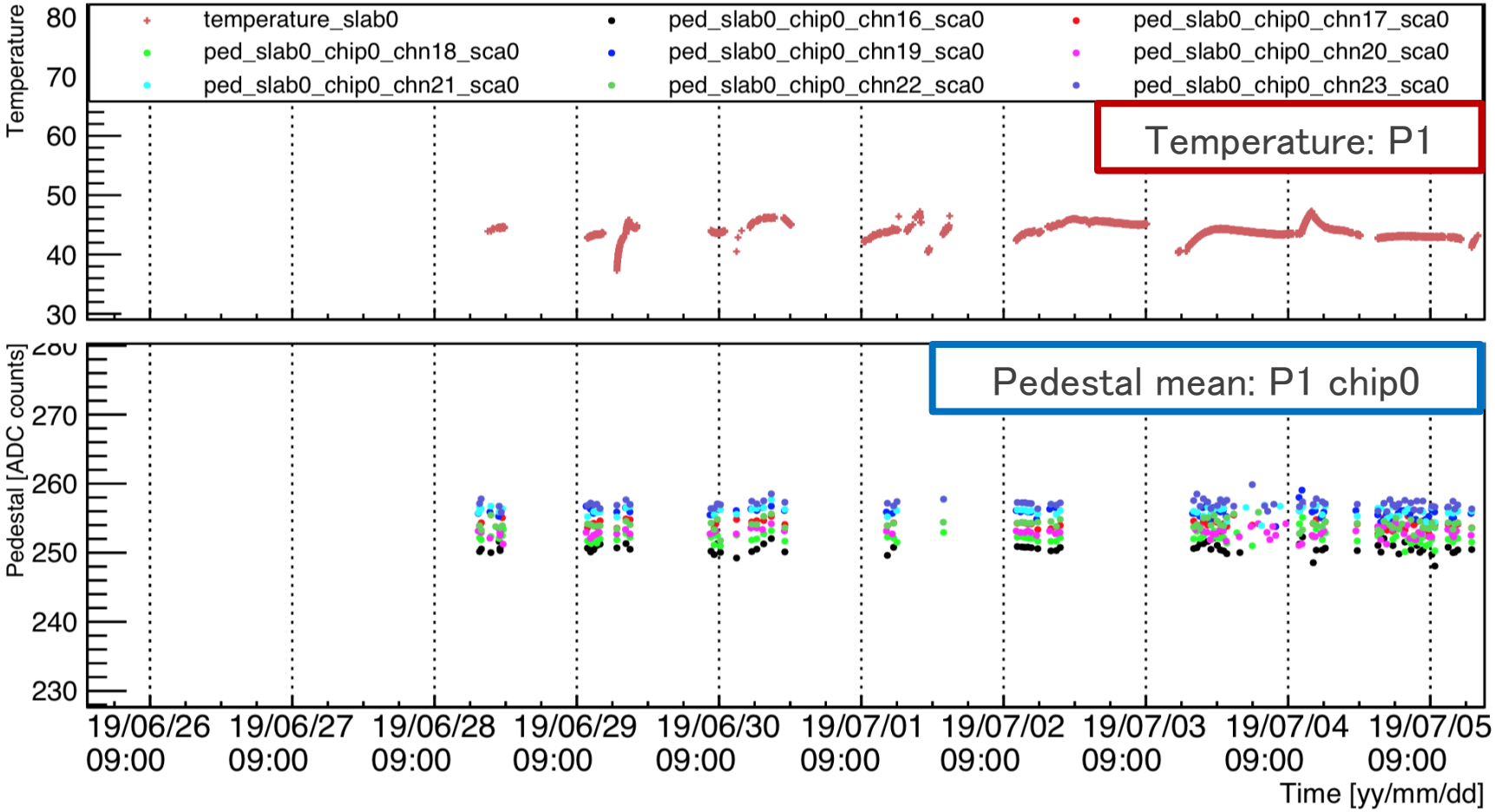
- Sigma of Gaussian
- SCA = 0 (Memory-cell dependence is referred later.)



➢ Width of pedestal is almost uniform (3~4) throughout.

Pedestal Stability

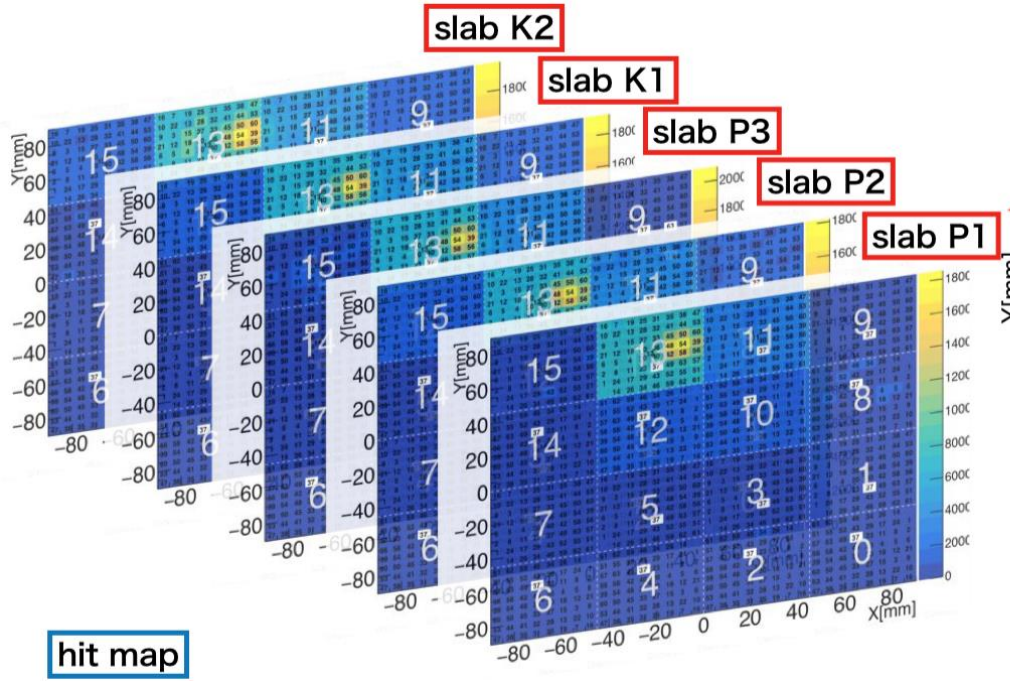
- Pedestal stability is confirmed in this beam time.

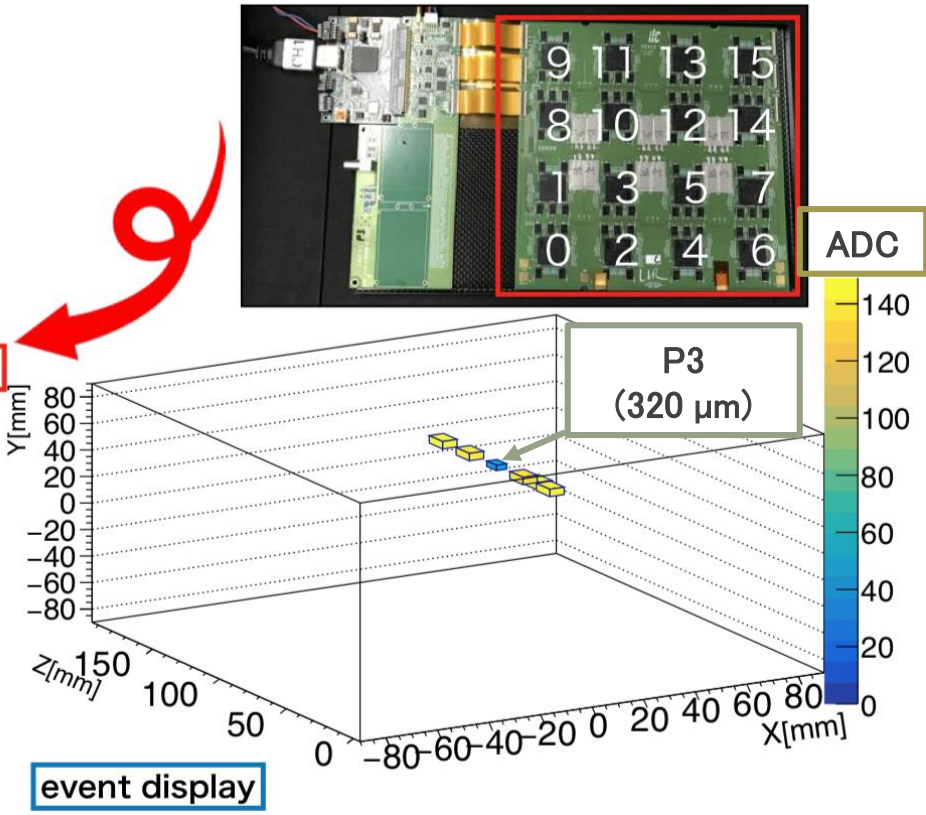


MIP event

- MIP program is performed for mainly energy calibration of all the pixels.
- Hit map: Sum of the triggered events
- Event display: ADC output of single event

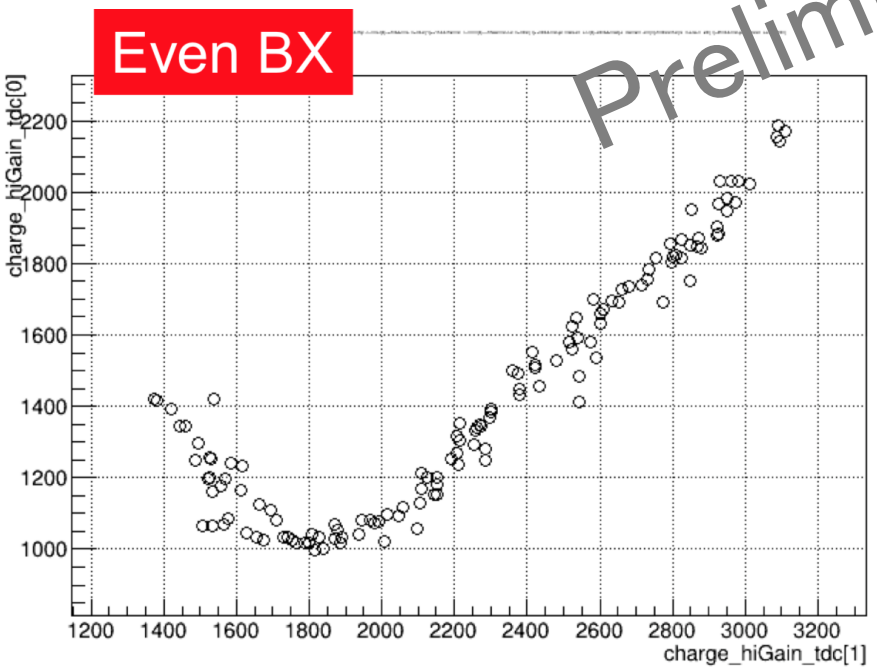
  - Electron energy: 3 GeV

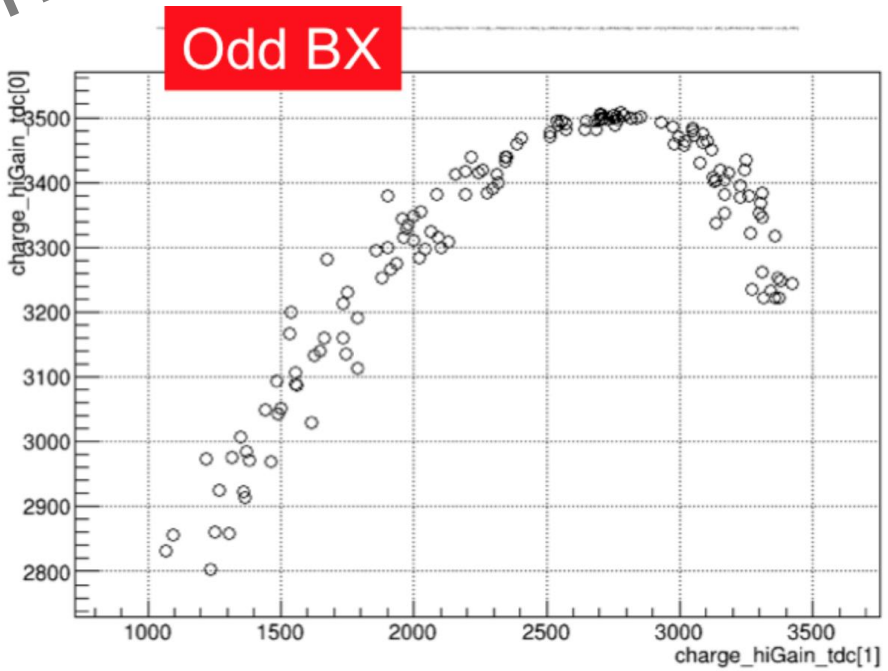




TDC with MIP

Preliminary



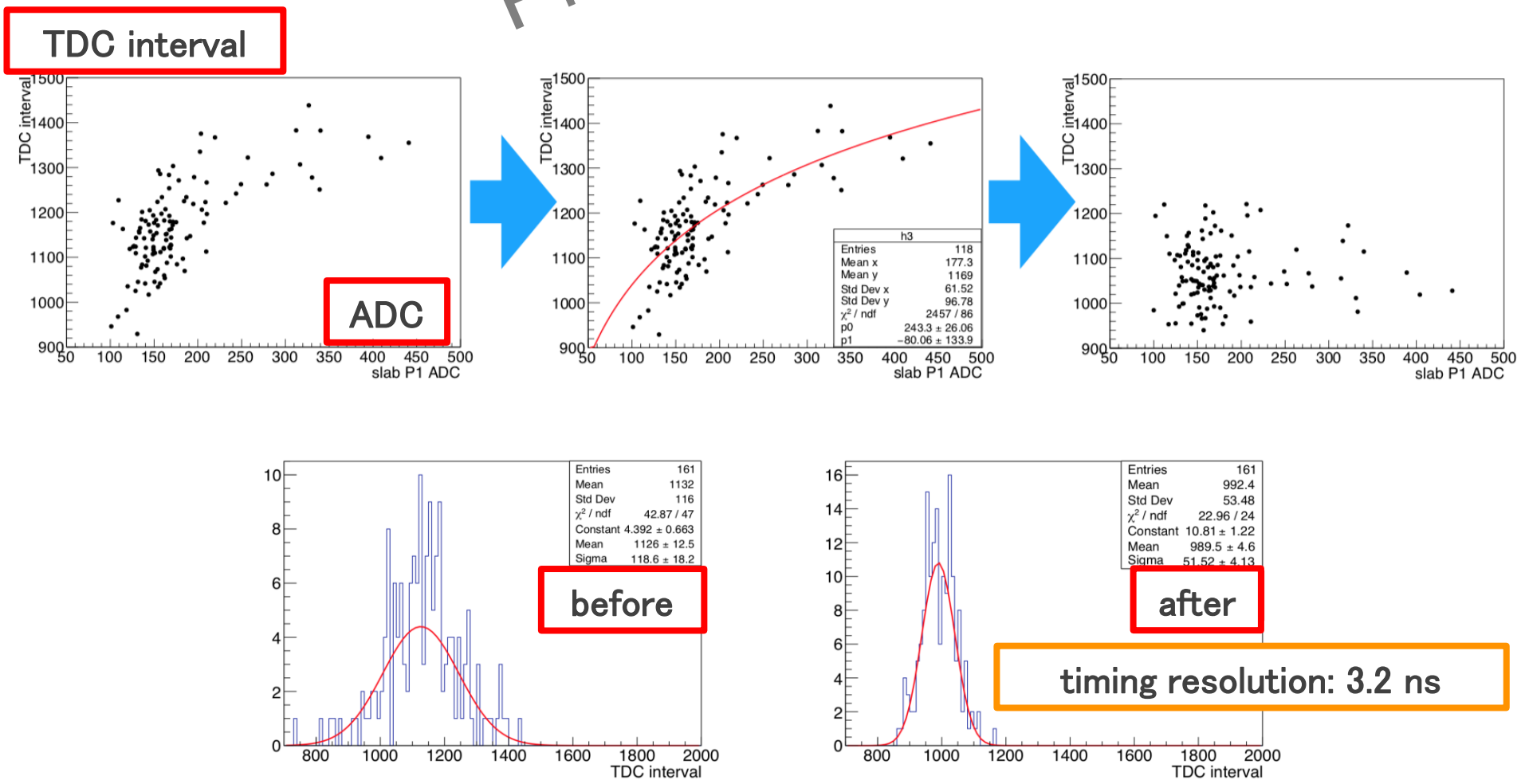


- Correlation of TDC between slab 1 and 2
- Select 1 ch (at the center of the beam), 450 < ADC < 500 (to avoid timewalk)
- ~10 / 1 ns at the normal slope: timing resolution ~ a few ns?
- TDC calibration in progress.

Correction of Time Walk

Preliminary

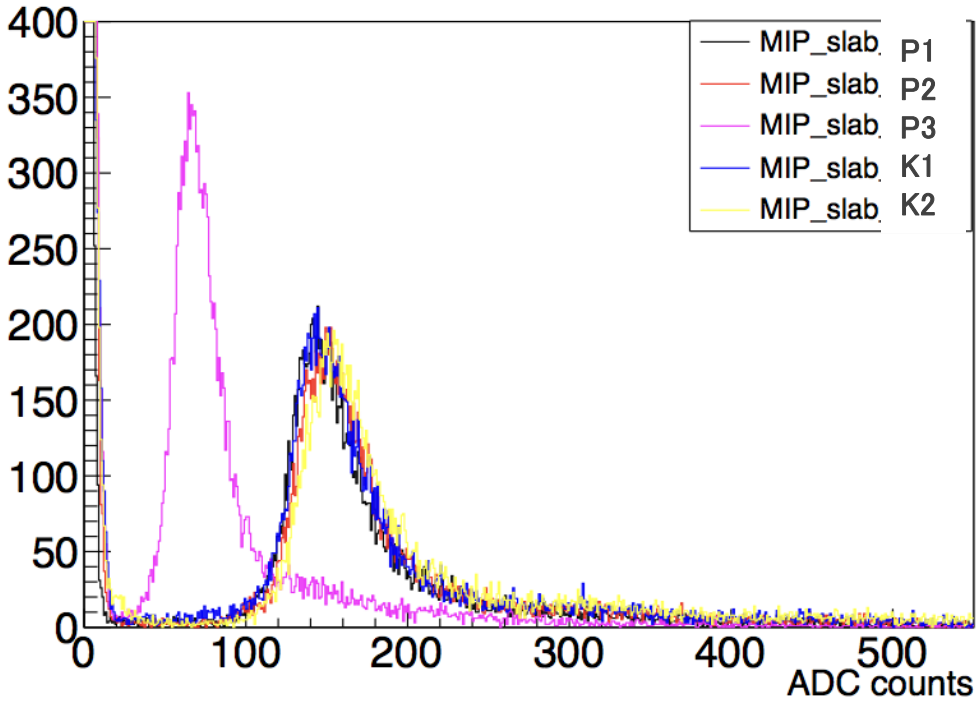
- Time Walk: TDC depends on ADC



MIP spectrum

- MIP spectrums of each slabs are shown.
- Pedestal is subtracted.
- Fitted by Lan-Gaus function.
  - Convolution of Landau × Gaussian
- MPV: Most Probable Value
- Definition of S/N_{ADC}:

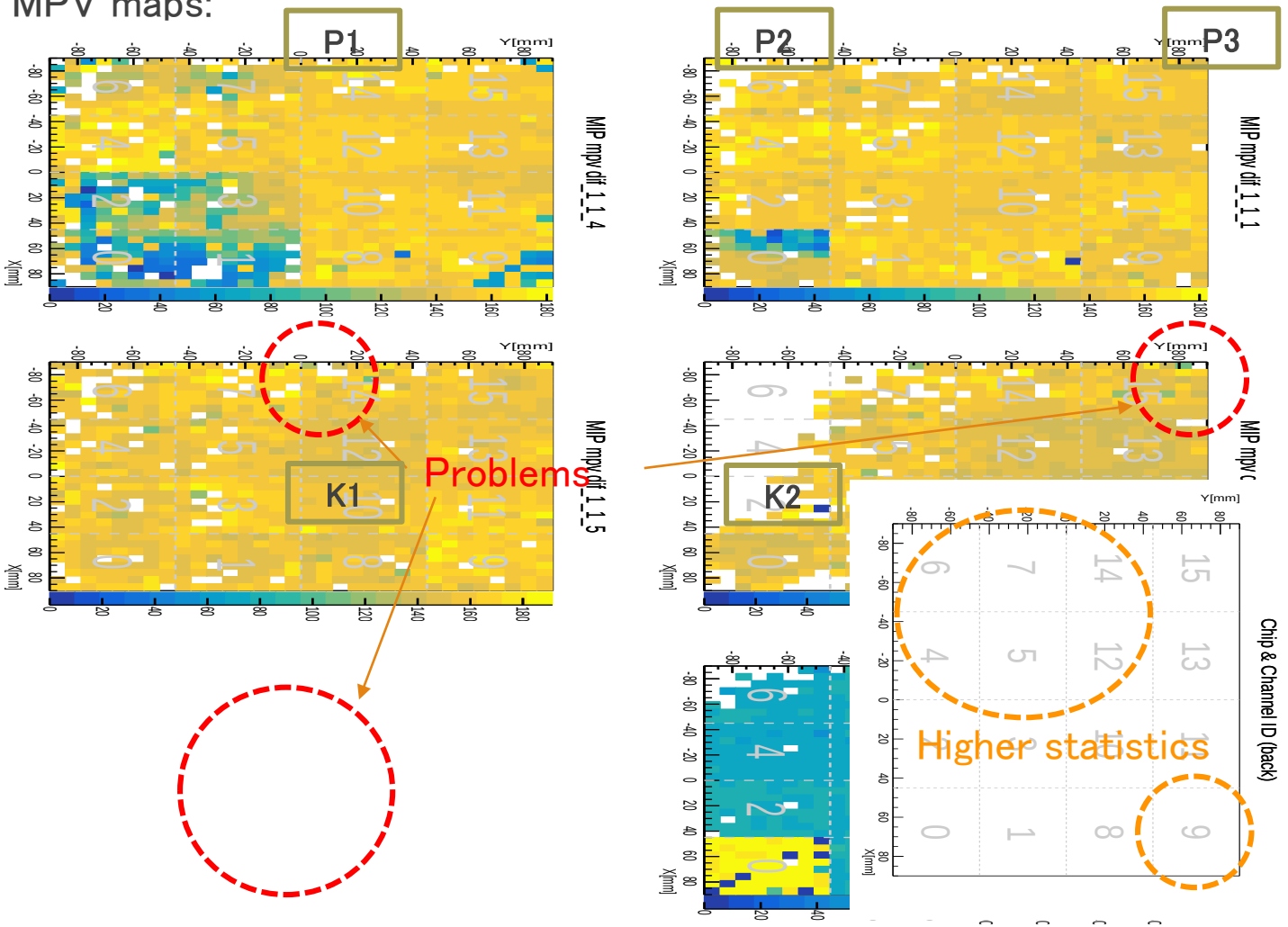
$$S/N_{ADC} \equiv \frac{MPV_{1\mathrm{MIP}}}{Width_{pedestal}}$$



slab	P1	P2	P3	K1	K2
thickness	650μm	650μm	320μm	650μm	650μm
MPV	146.5	144.9	71.3	141.4	146.1
Ped_width	3.0	3.0	3.3	2.8	3.1
S/N	49.0	48.9	21.7	50.2	47.5

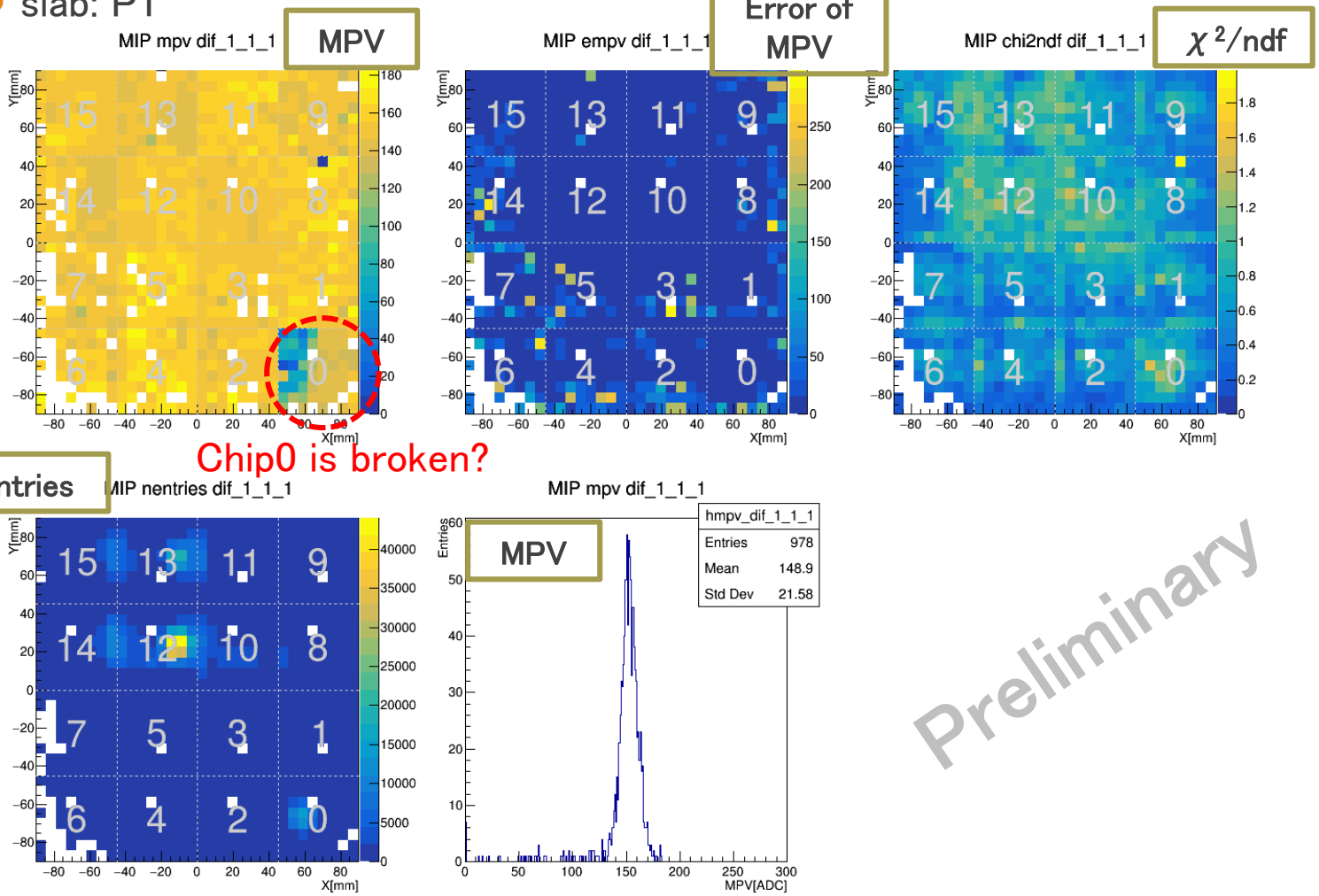
MIP calibration: Summary

- MPV maps:



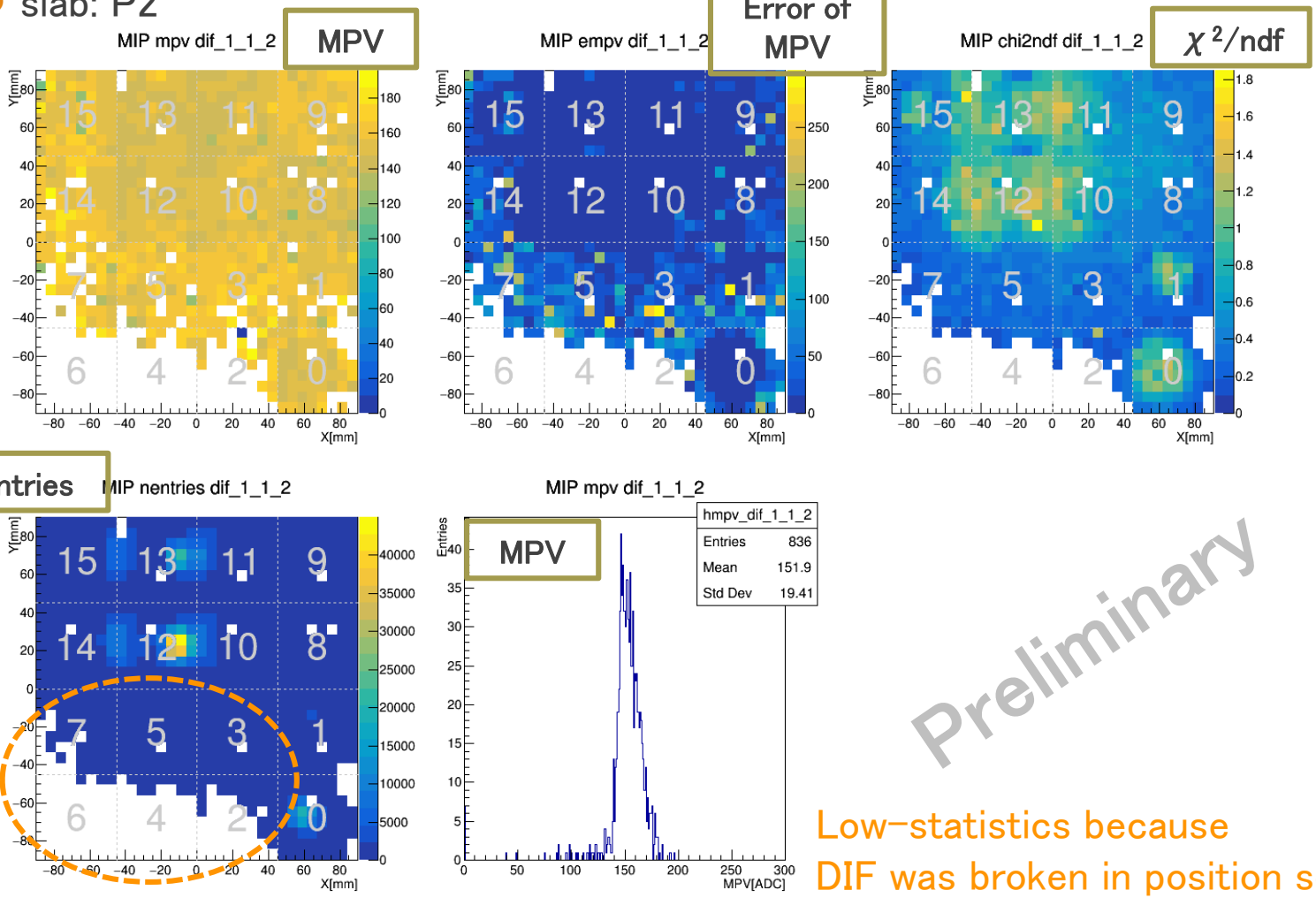
MIP calibration

- slab: P1



MIP calibration

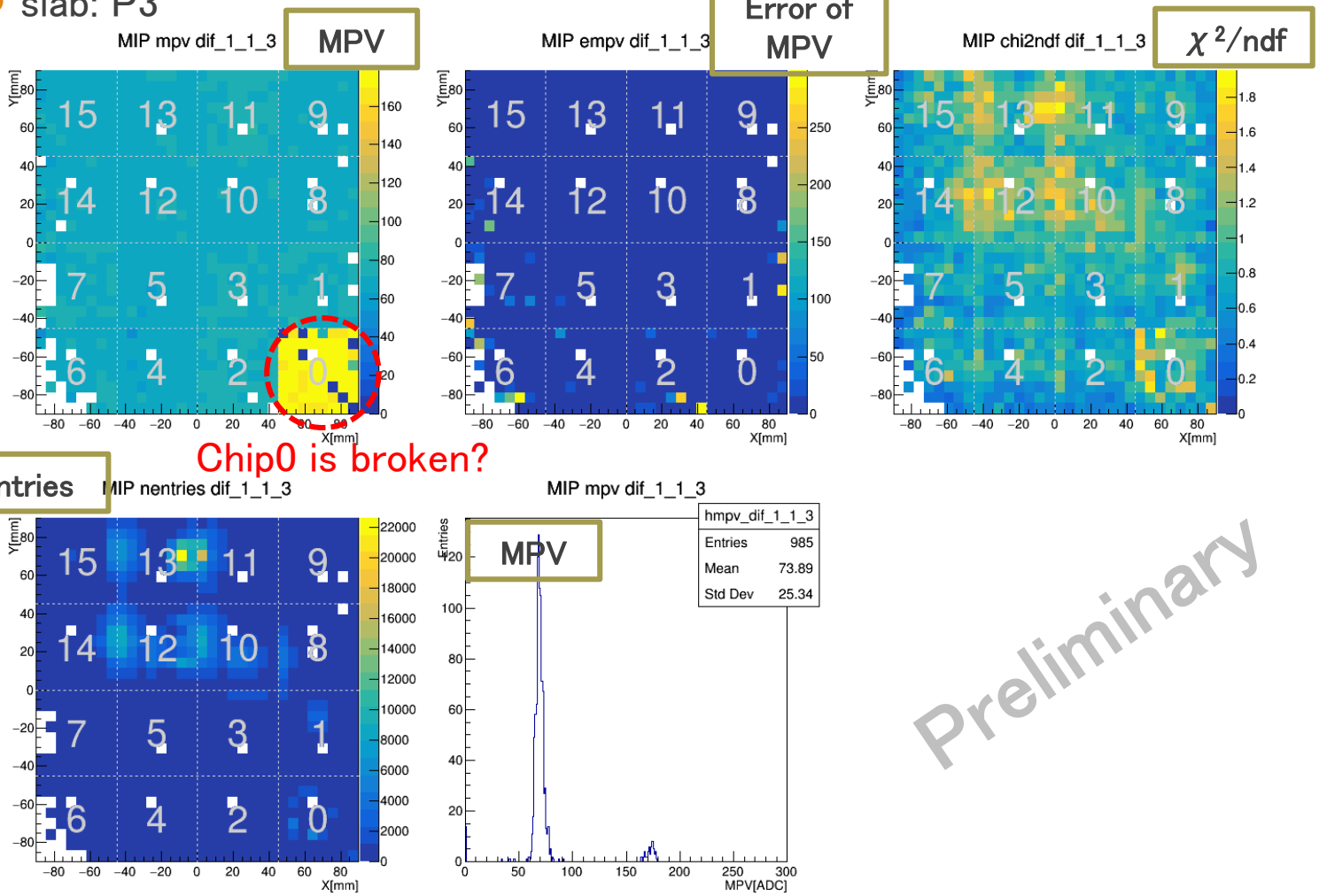
- slab: P2



Low-statistics because
DIF was broken in position scan

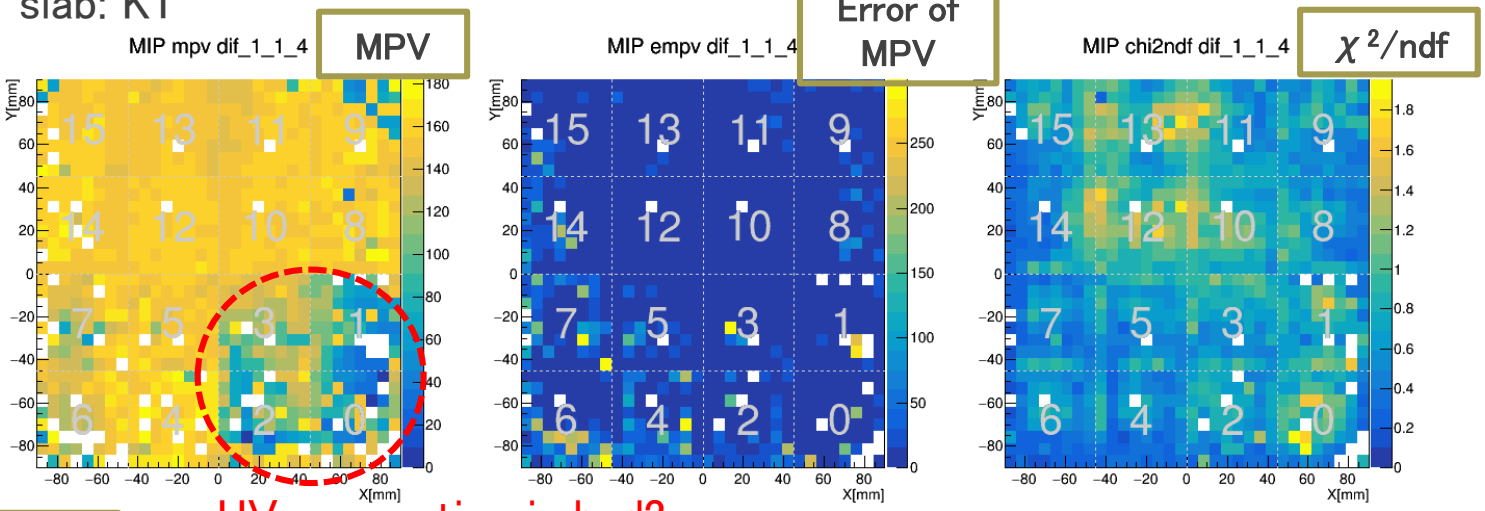
MIP calibration

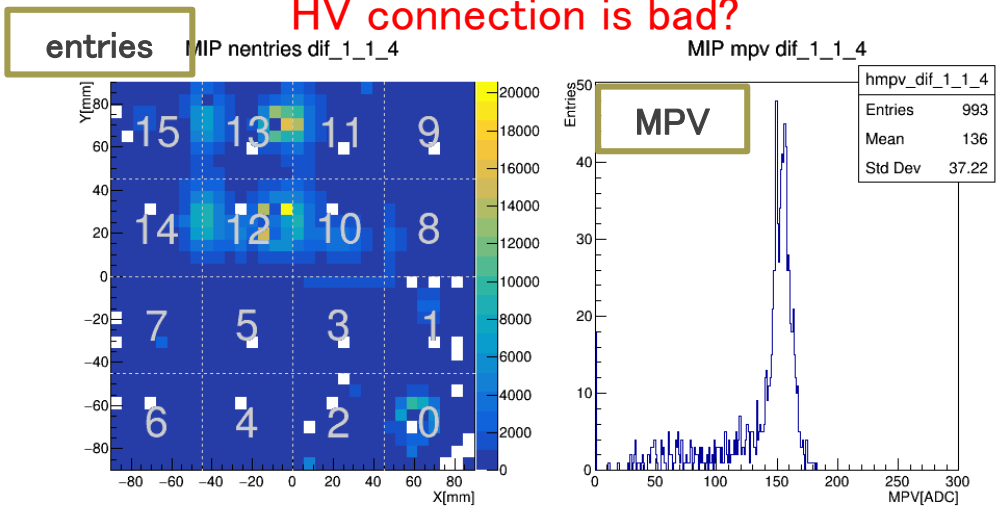
- slab: P3



MIP calibration

- slab: K1

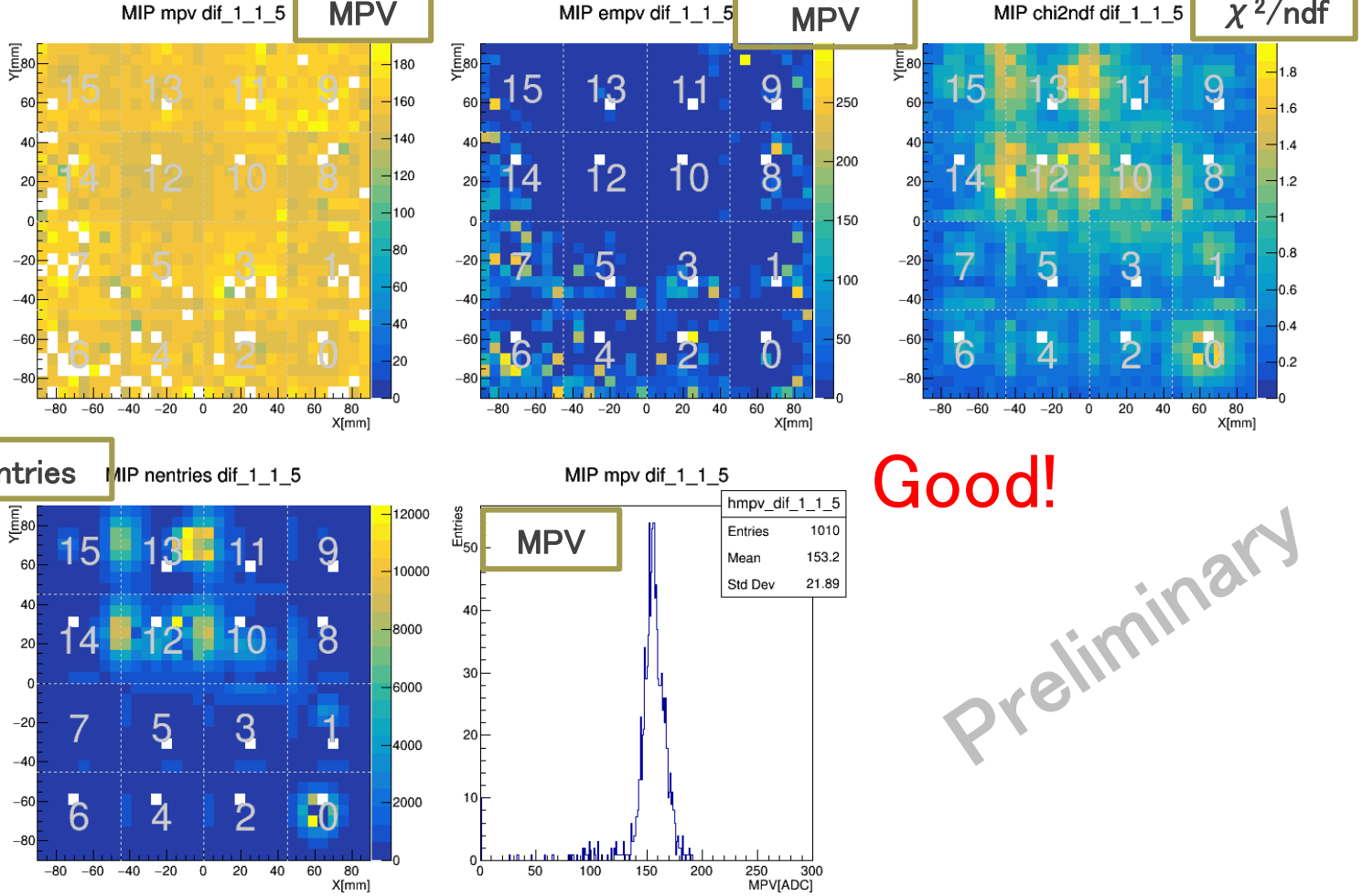




Preliminary

MIP calibration

- slab: K2

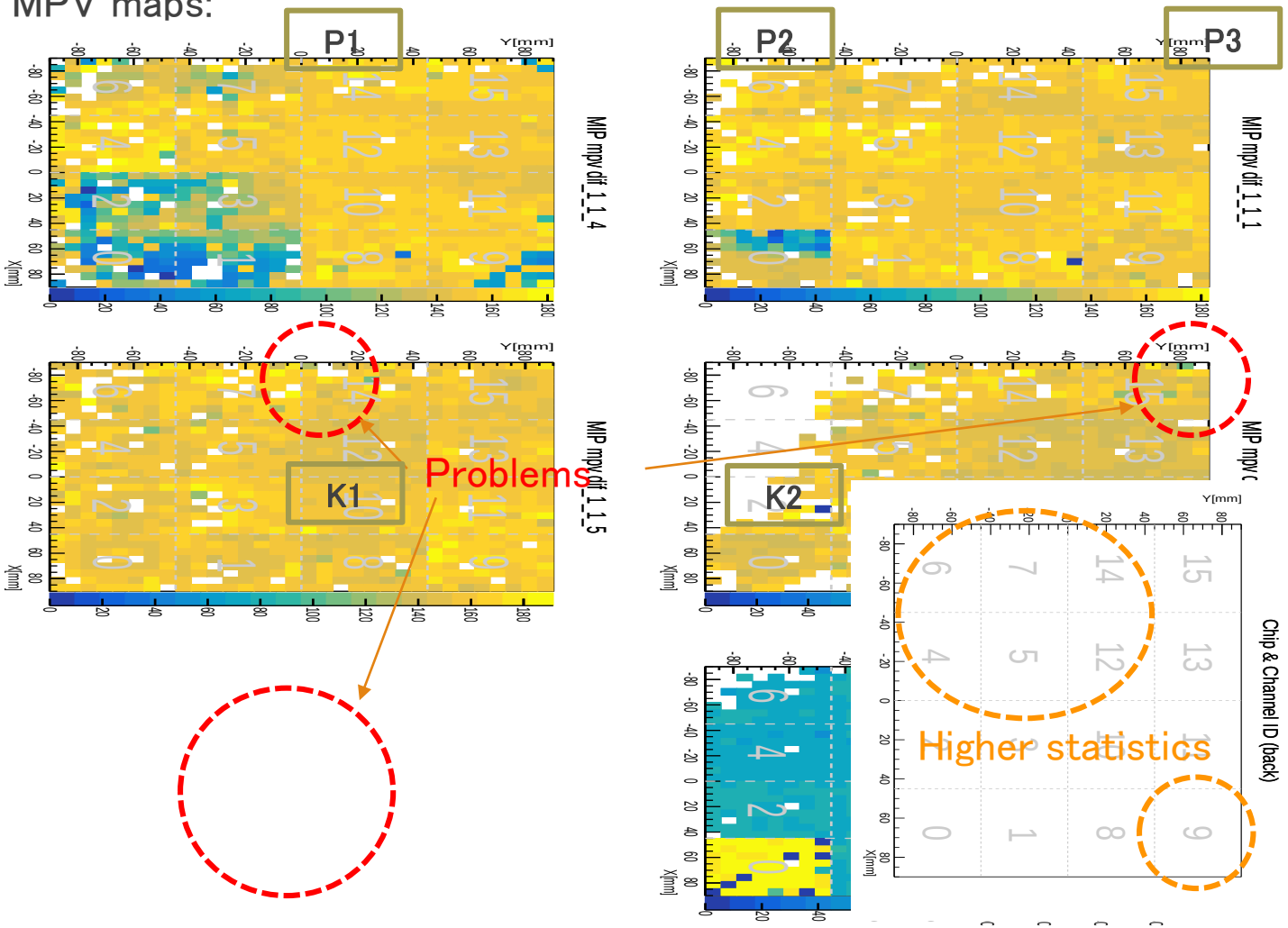


Good!

Preliminary

MIP calibration: Summary

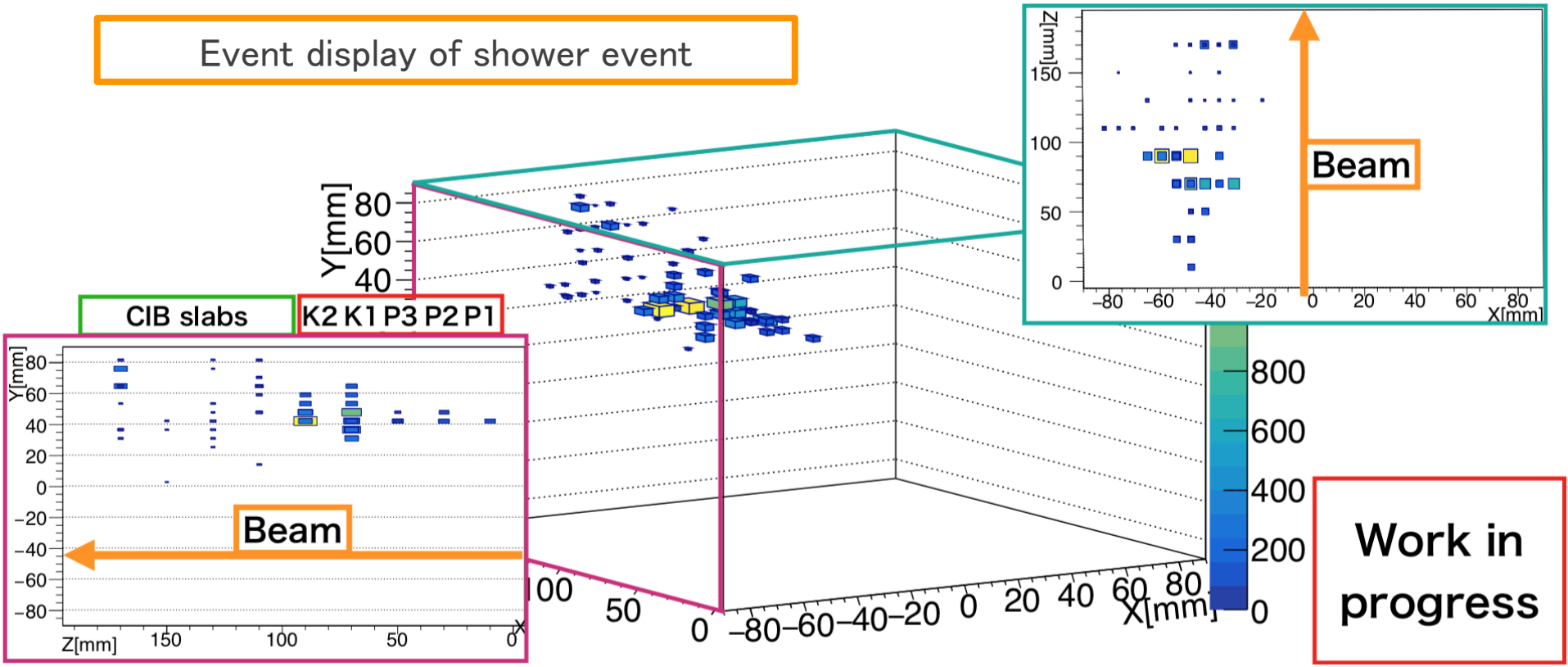
- MPV maps:



Shower event

Preliminary

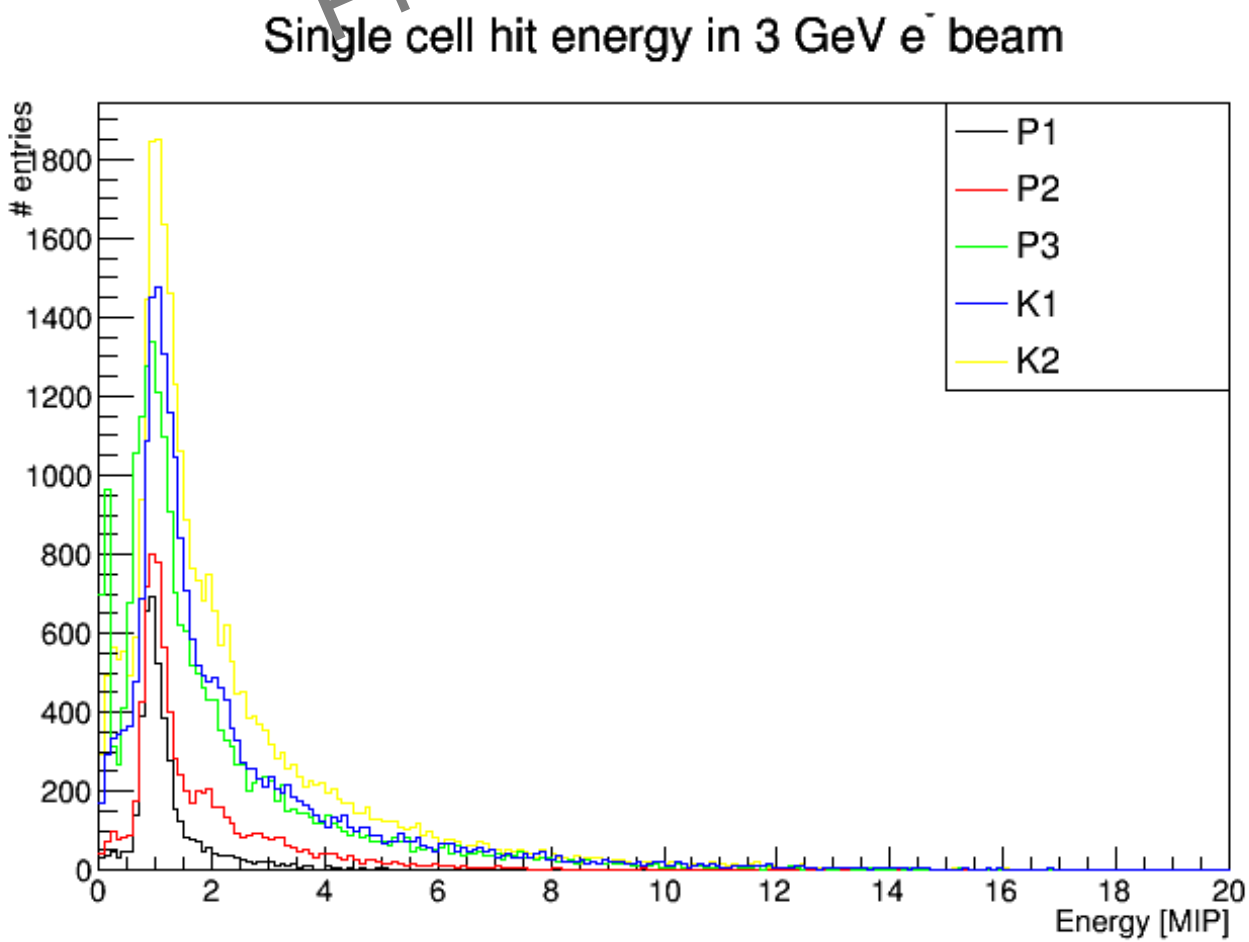
- TBD



Hit Energy

Preliminary

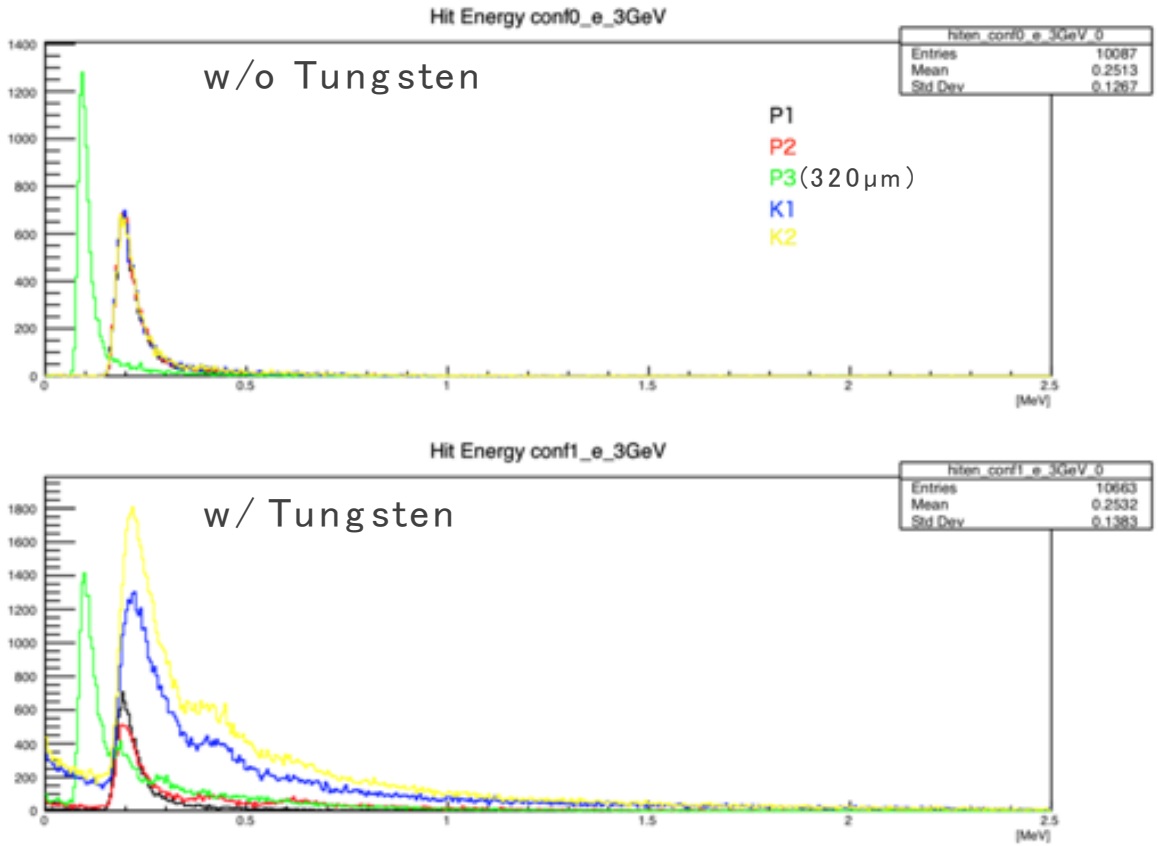
- Hit energy after MIP calibration



Simulation with DDSim in iLCSoft

Preliminary

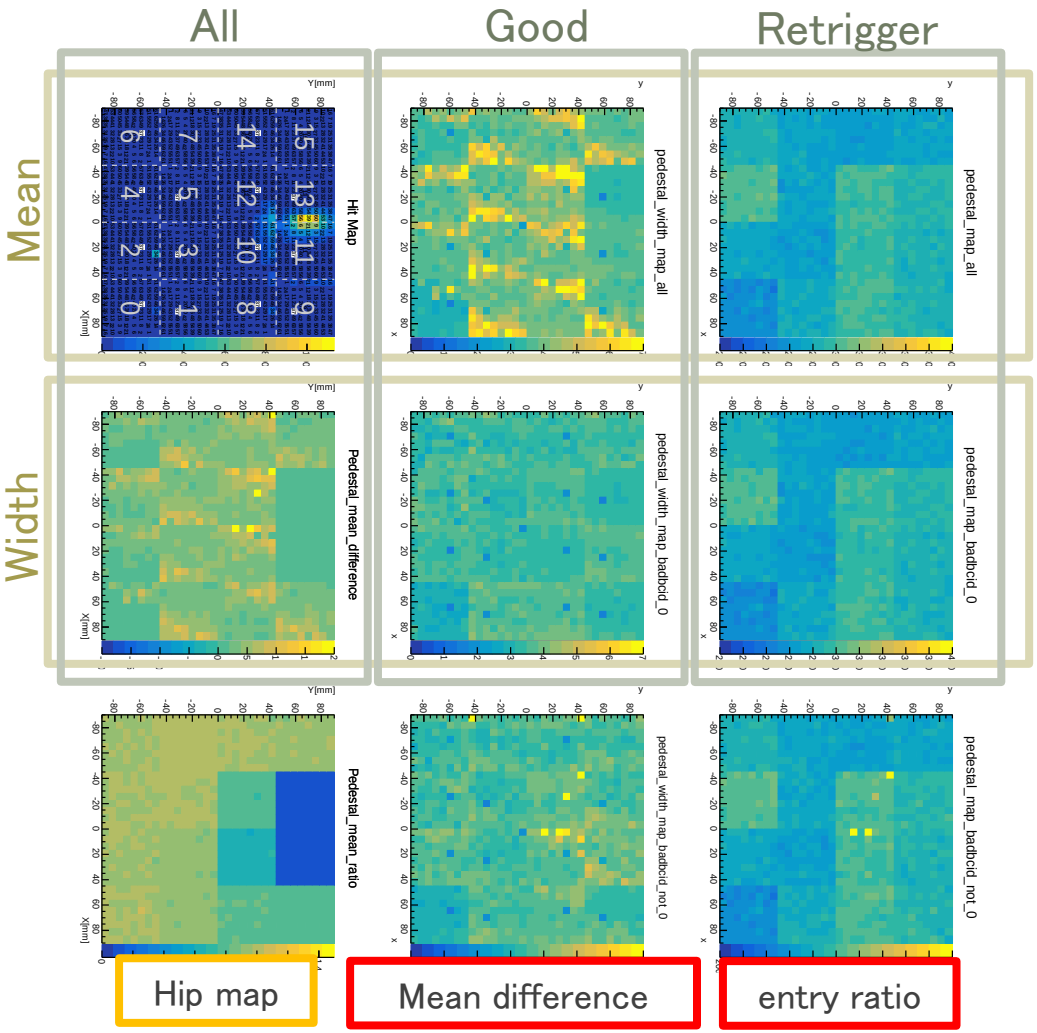
- We performed detector simulation for this beam test.
- FEV13:
  - CF: 0.6mm
  - Electronics(Air)
  - PCB: K1: 1.6mm, others: 1.8mm
  - Glue(Air): 0.08mm
  - Si: 0.32mm or 0.65mm
  - Glue(Air): 0.08mm
  - Kapton(Cu): 0.06mm
  - CF: 0.6mm
  - Plastic(polyethylene): 5mm



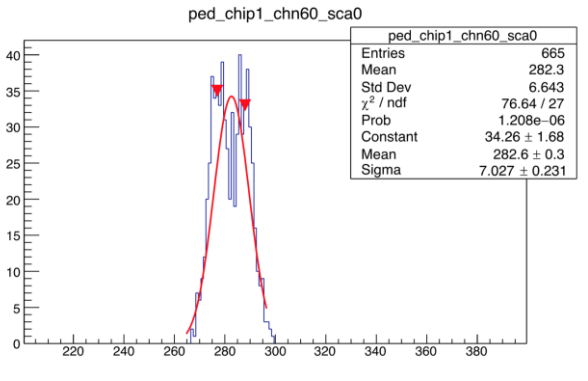
Remaining Issues

Double pedestal / Retrigger

- run 32015, slab P1



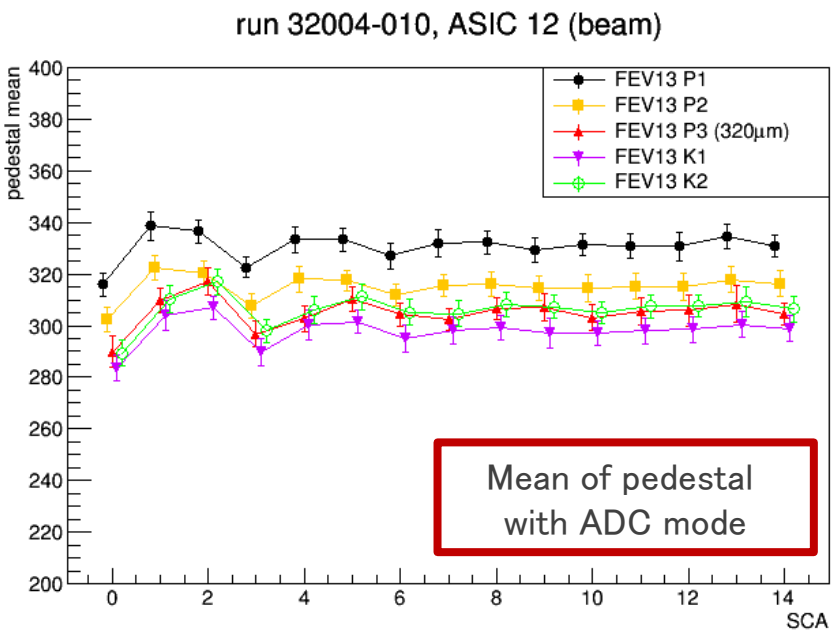
Retrigger event:
BCID is consecutive.
(badbcid≠0)

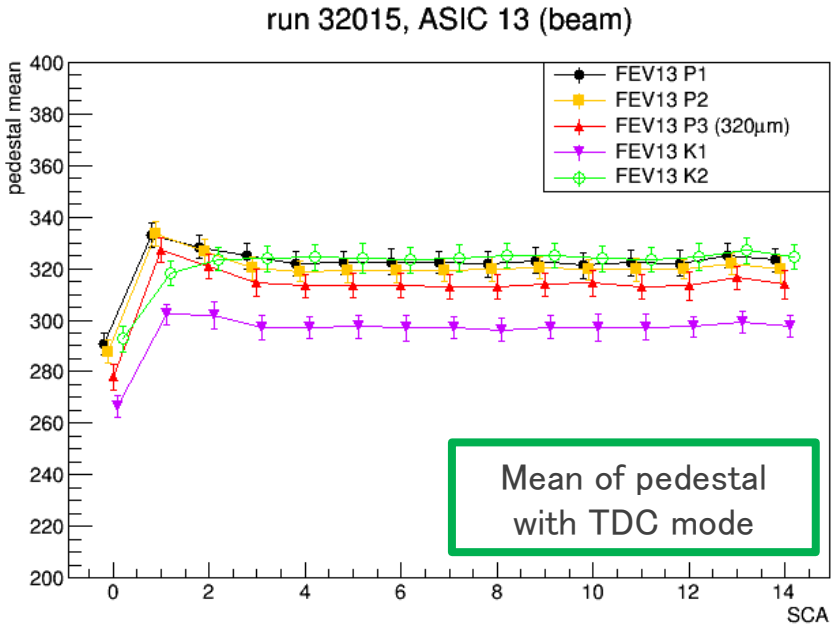


Double pedestal
by retrigger

Pedestal difference between ADC/TDC mode

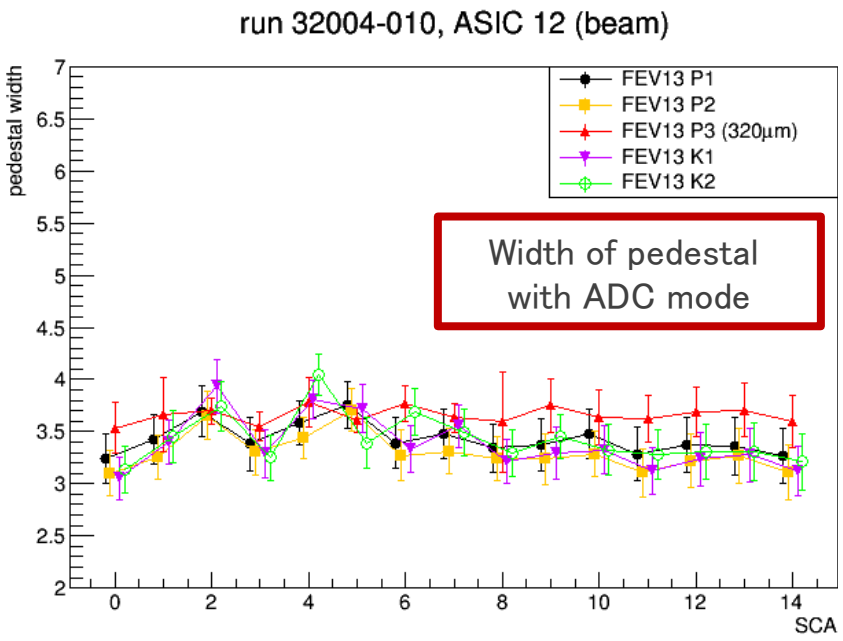
- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In the first memory cell, the difference of typical Ped_mean is ~15.

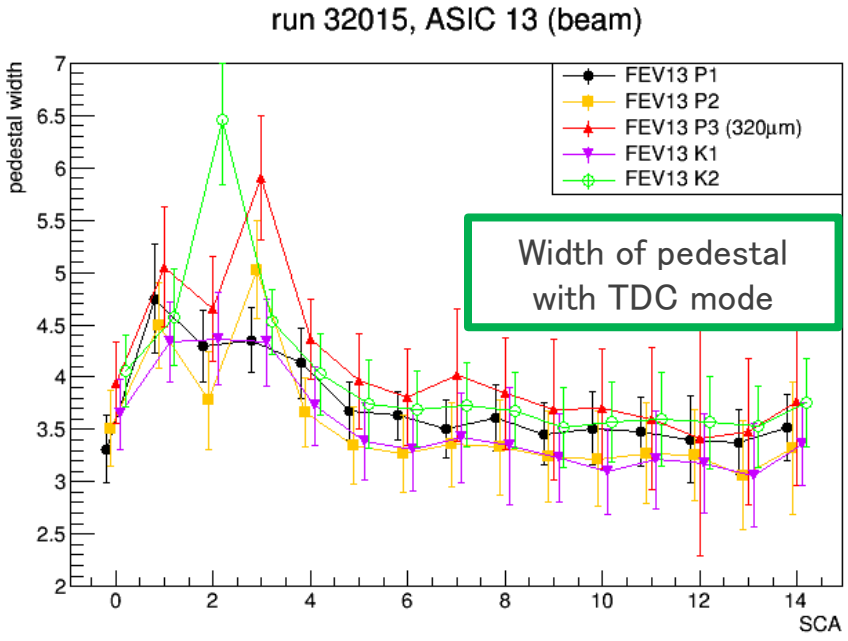




Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In TDC mode, SCA~2 is worse.





Pedestal difference between ADC/TDC mode

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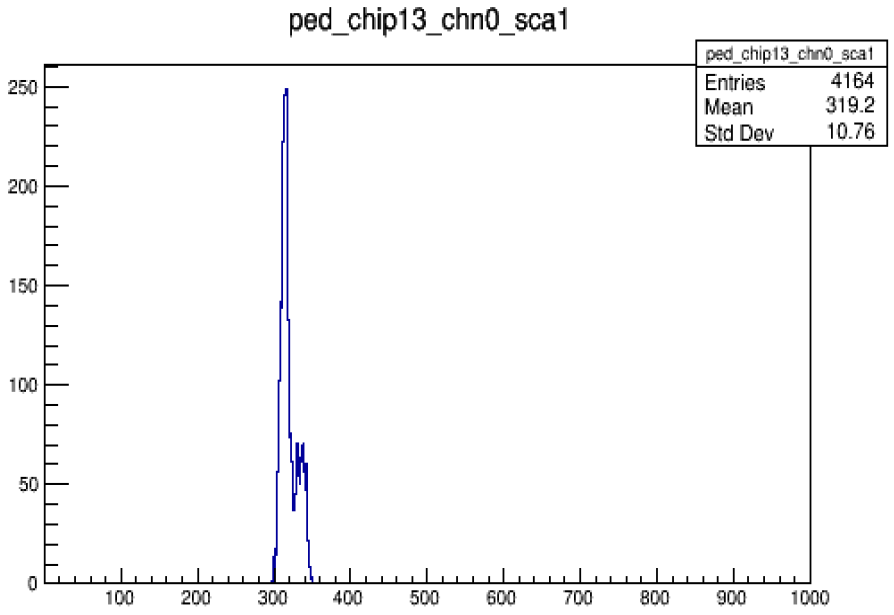
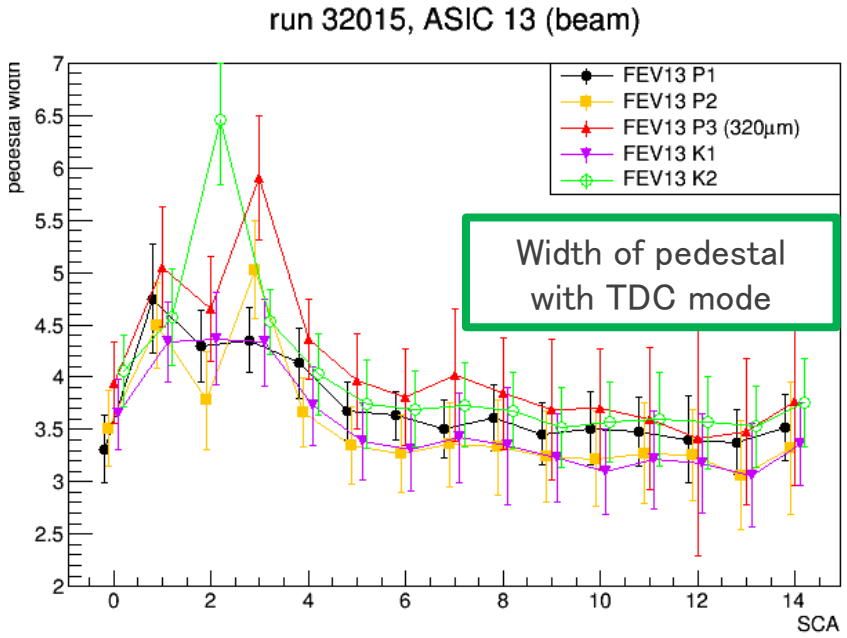




➢ There are double pedestal even after bcid selection in TDC mode.

Work in progress...

Summary

Preliminary

- FEV13: P1, P2, P3, K1, K2 in Kyushu
- BT 2019 DESY: 5 slabs fully working finally
- Pedestal study
  - Homogeneity and Stability is verified.
  - In TDC mode, pedestals become worse probably because of retriggers.
- MIP study
  - MIP calibration is almost completed.
  - S/N is obtained for 5 slabs

slab	P1	P2	P3	K1	K2
thickness	650μm	650μm	320μm	650μm	650μm
S/N	49.0	48.9	21.7	50.2	47.5

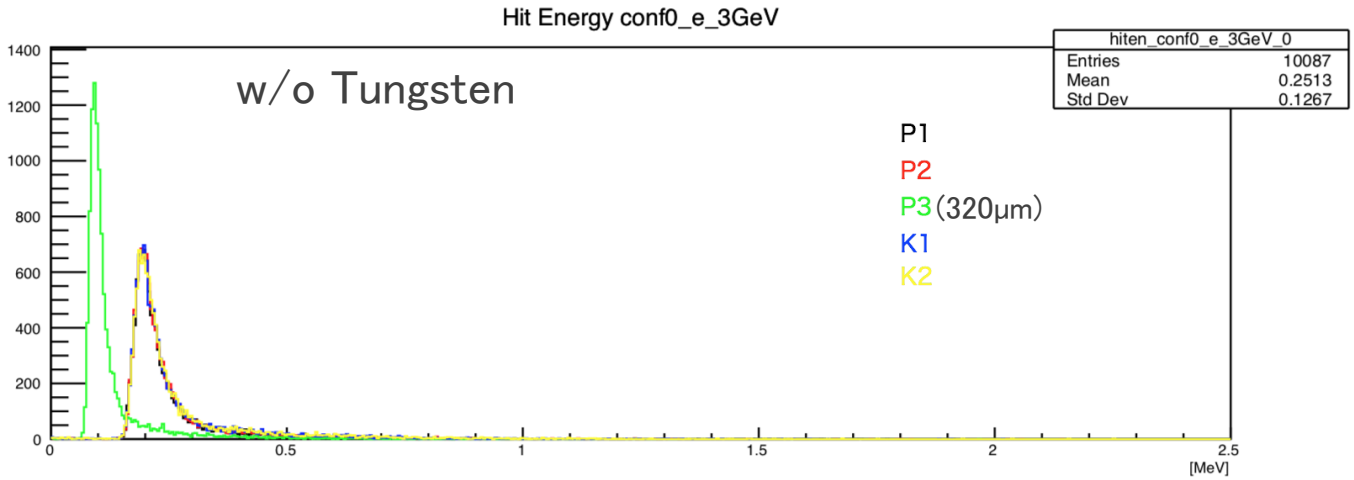
- TDC study
  - Time walk is corrected.
  - Timing resolution is obtained, however we need more detail study using injection.
- Shower study
  - Simulation setup is in progress.
  - Event building is done and shower event is confirmed.

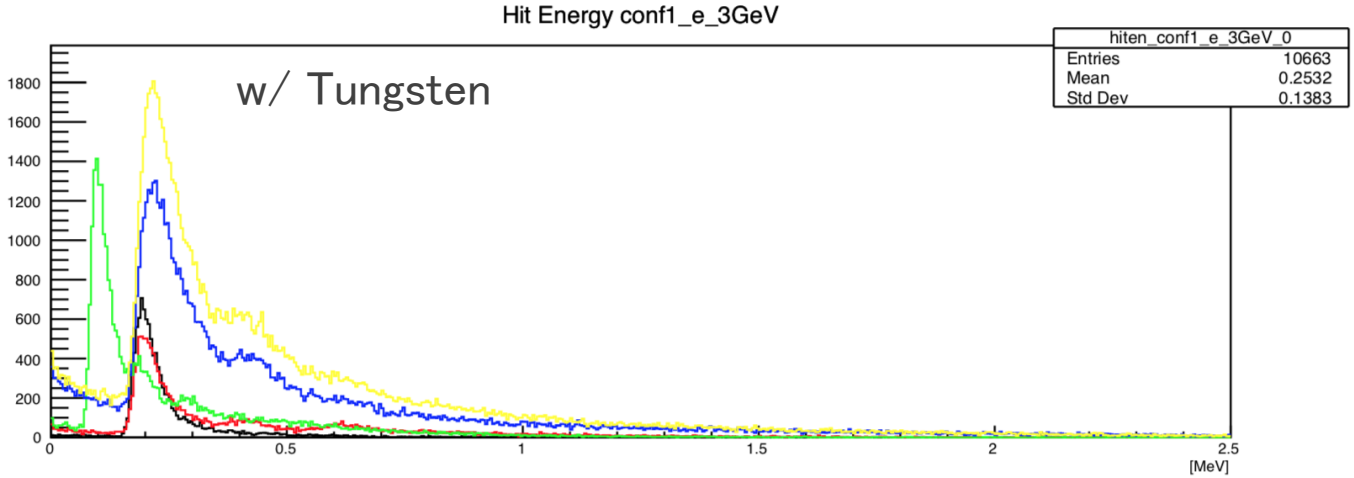
backup

Preliminary

Simulation outputs

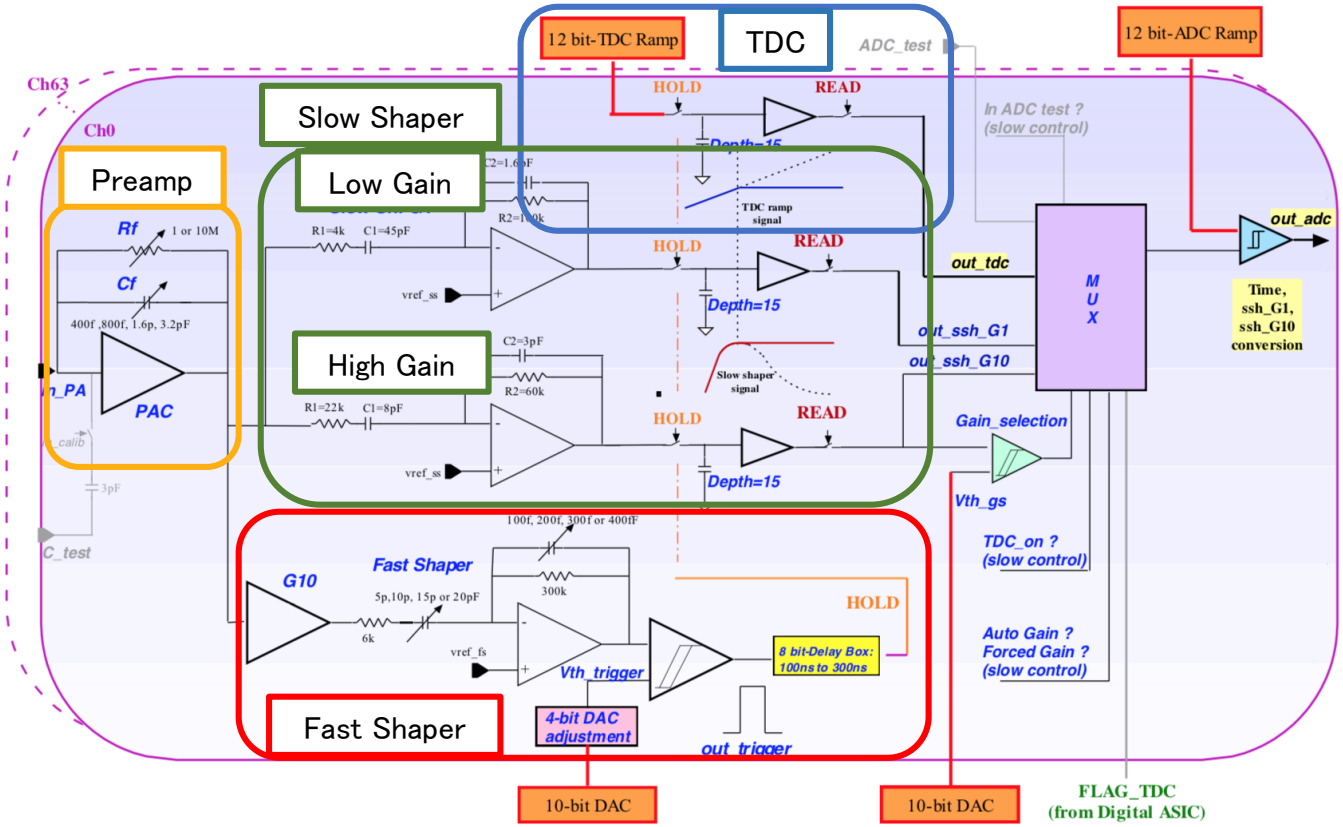
- Hit energy distribution in each slabs



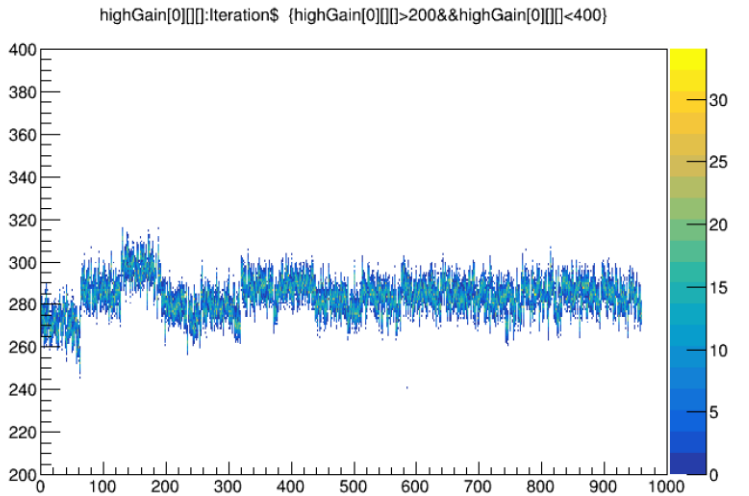


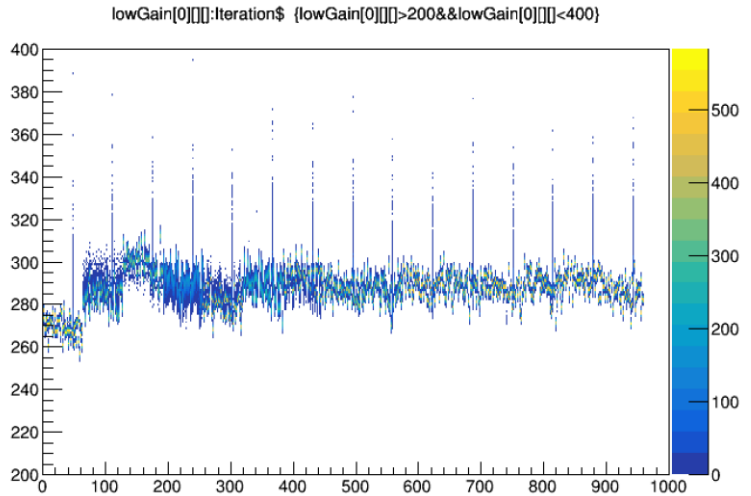
SKIROC2A

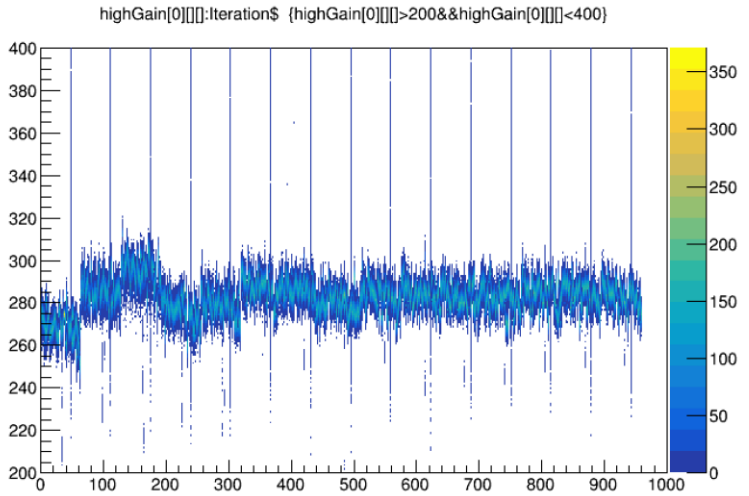
- 64ch / chip × 16 chip / slab
- Self trigger: Individual threshold control is available.
- 3 types of output: ADC with high/low gain & TDC
- 3 types of DAQ mode:
  1. ADC high & ADC low 2. TDC & ADC [high or low] 3. TDC & Auto Gain

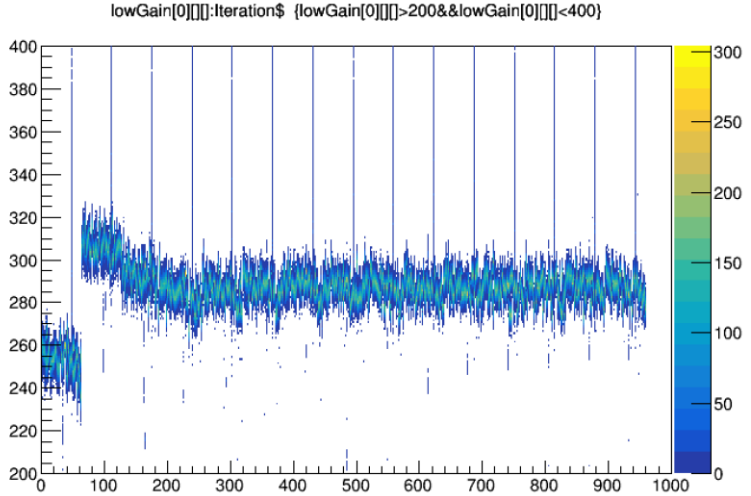


Pedestal difference between ADC/TDC mode





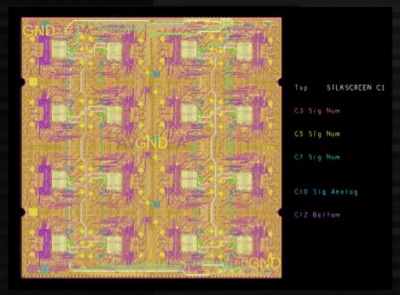


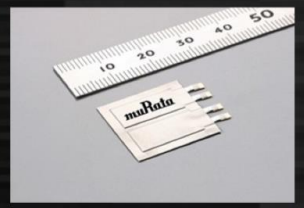


FEV13: SiW-ECAL technological prototype

Major changes in FEV11→13 and SMBv4→v5

- ASIC: SKIROC2 → SKIROC2A
  - Individual threshold control
  - Improvements on TDC
- Dedicated power planefor AVDD_PA
  - Power layers: 2→3
  - Total layers: 10→12
- Smaller SMB footprint
- Connection by 0.4mm-pitch flex cables
  - Two candidates, footprint compatible
- PP capacitor on FEV
  - 0.4 mm thickness, 40 mF x 6





Discontinued!

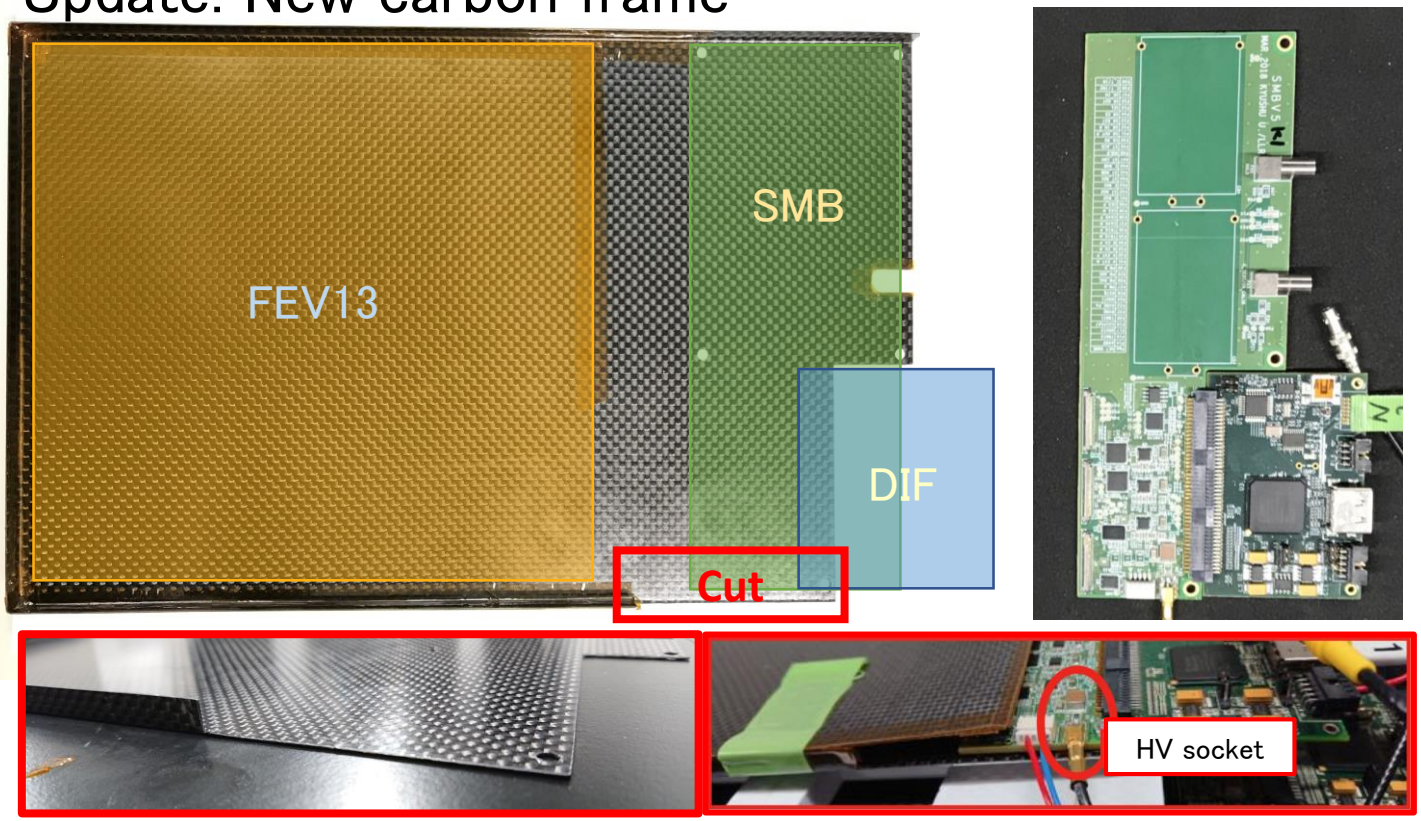
Flexible cable with
Panasonic connector

Micro-coaxial
cable by KEL

Taikan Suehara, CALICE collaboration meeting at CERN, 1 Oct. 2019 page 2

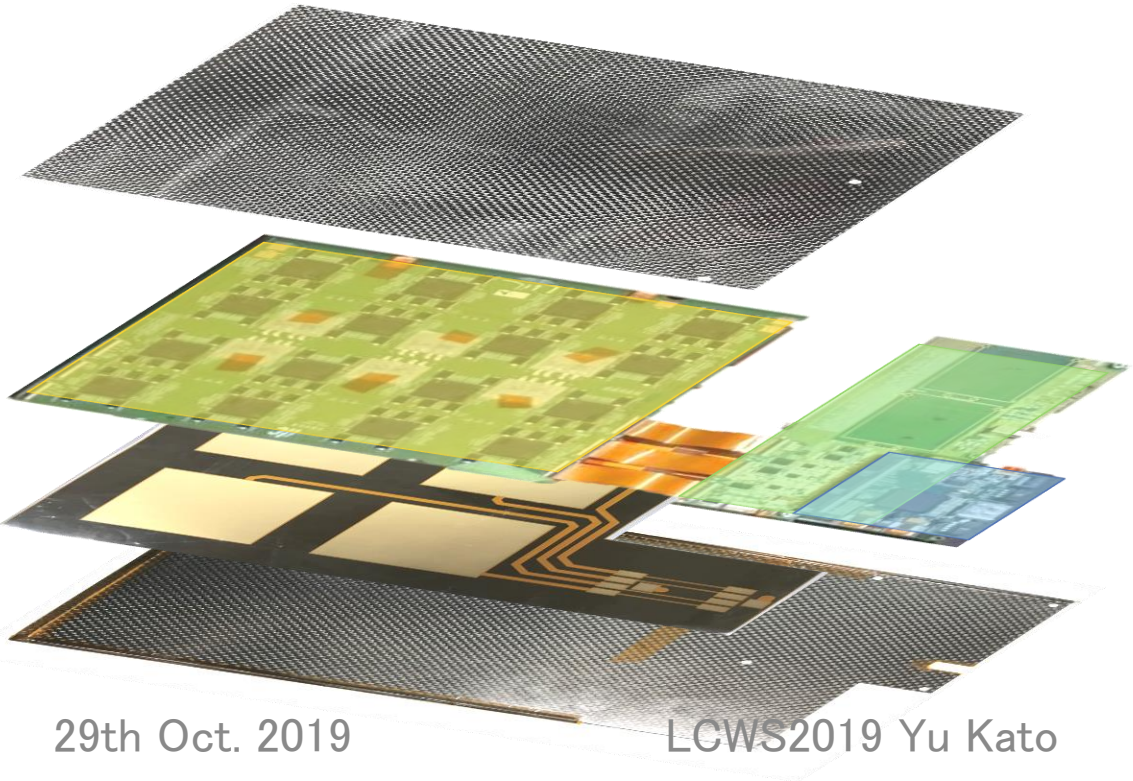
Hardware update

- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.
- Update: New carbon frame

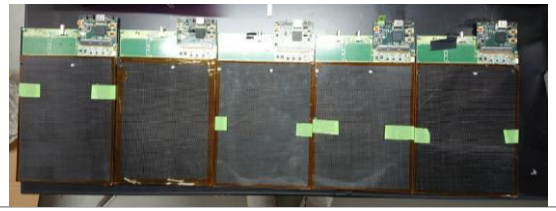


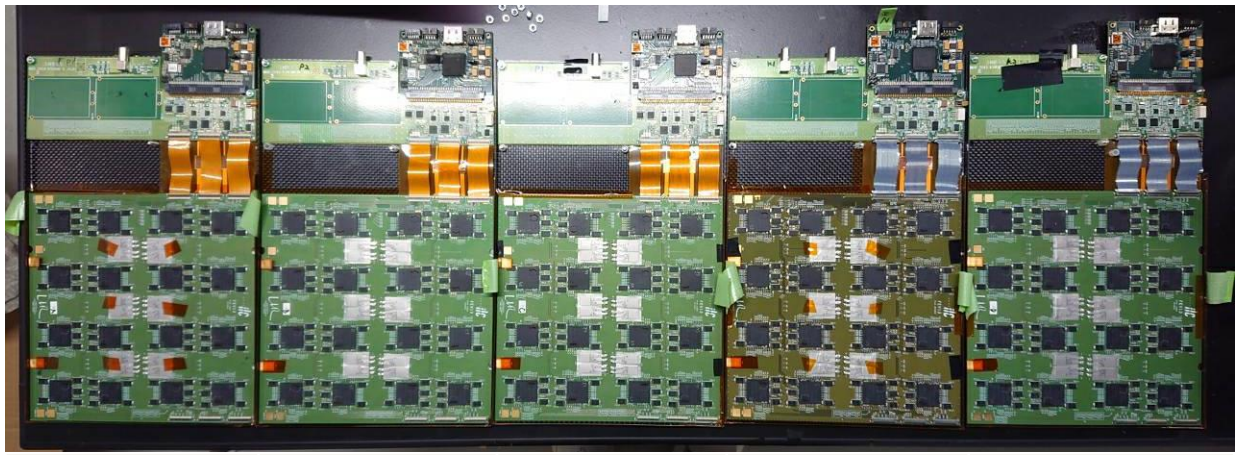
Hardware update

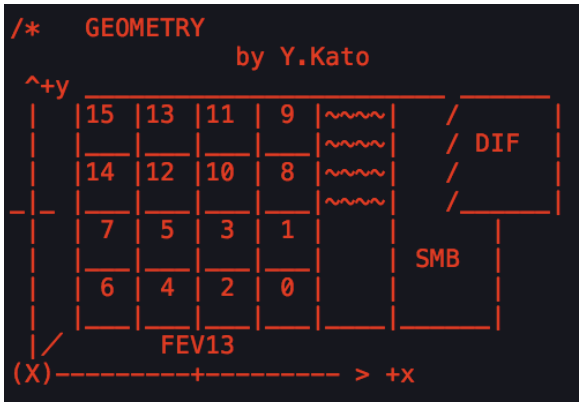
- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.
- Update: Conductive adhesion



FEV13



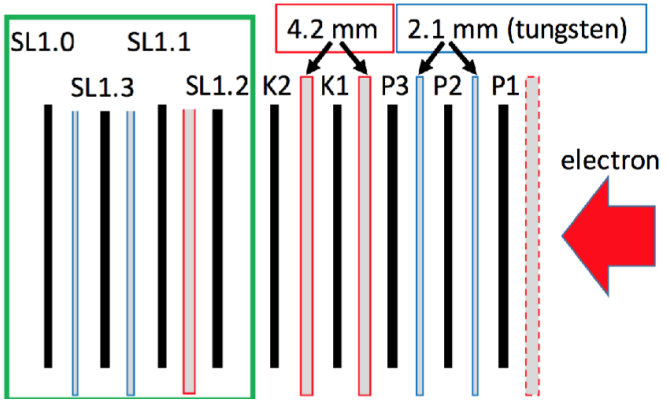




↑ beam direction is from front to back

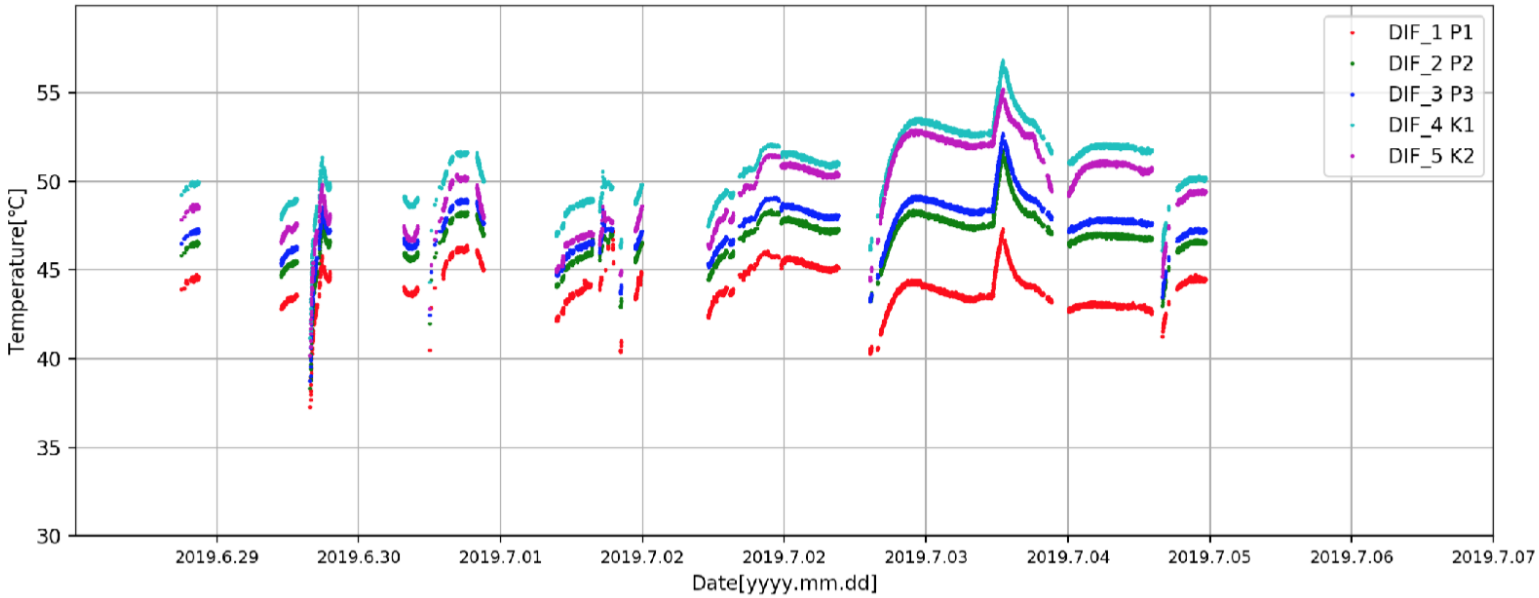
P1	P2	P3	K1	K2
dif_1_1_1	dif_1_1_2	dif_1_1_3	dif_1_1_4	dif_1_1_5
650 µm	650 µm	320 µm	650 µm	650 µm

- We used 5 FEV13 slabs.
- There are 2 types of Silicon thickness.
- Slab position against e− beam: →



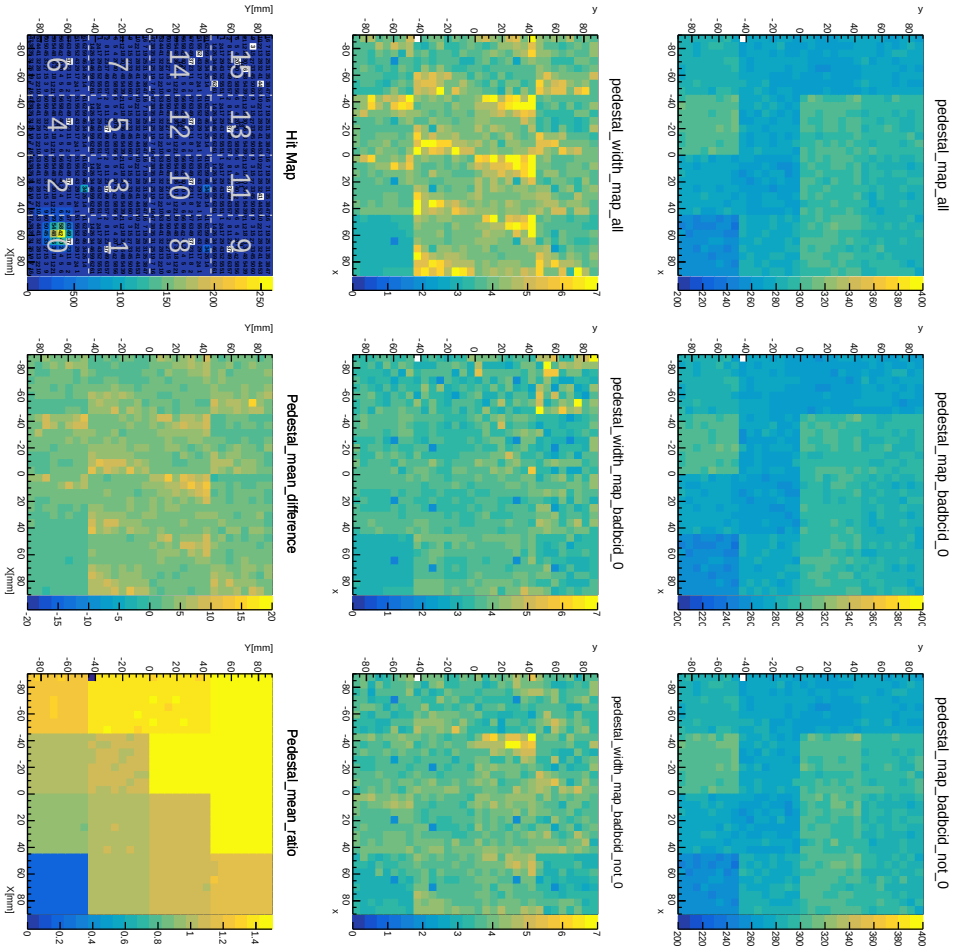
Data Summary

- All the run information is summarized on
  https://drive.google.com/file/d/1uQojIu9KlS9badhVrBf1LRFNt-kz62vV/view?usp=sharing .
  - not perfect, could be improved.
- June 27: DIF on P2 had broken down → June 28: replaced DIF and recovered
- June 28: made script to record temperature & start measurement
- July 1: Data transition from P1 was sometimes lost because of bad connection of HDMI



Pedestal Analysis

- We generated pedestal maps for all runs.



run_30003-006
_dif_1_1_1 (P1)