Summary R&D Detector

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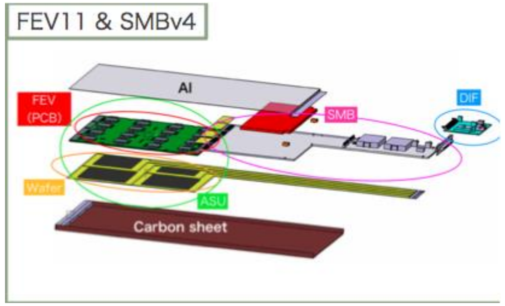
LCWS2019 – Sendai (Japan)

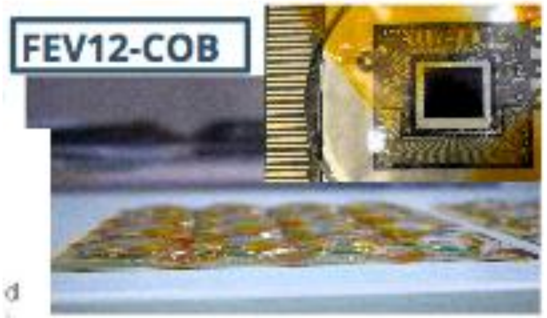
R&D Detector
selected topics

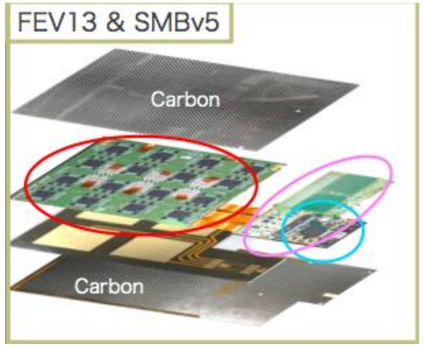
- Calorimetry
  - Si-W ECAL
  - Scintillator ECAL
  - HCal, Muon shielding
- TPC tracking
- Silicon pixel detectors

R&D for Si-W ECAL

Three ASUs tested:

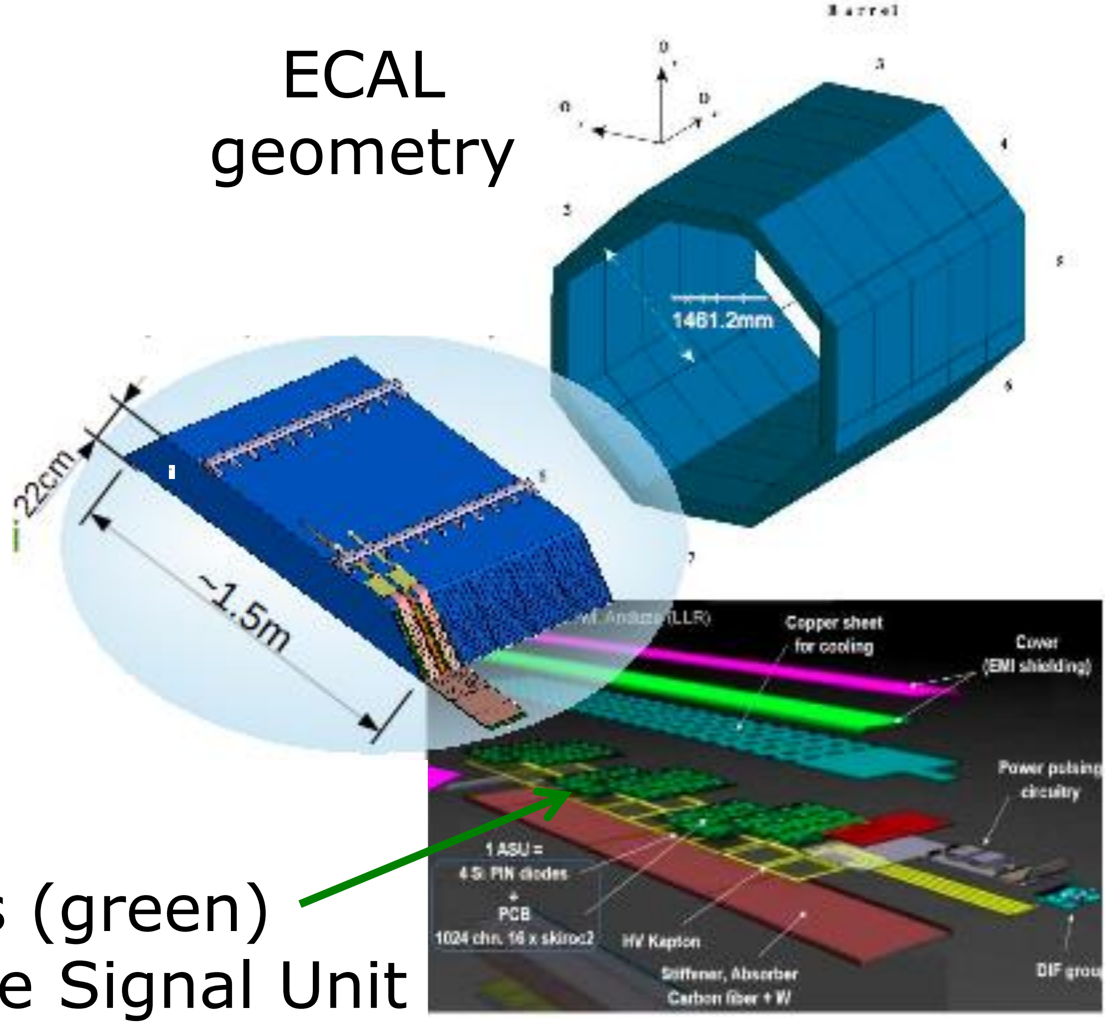






ECAL geometry

SLAB



ASUs (green)
Active Signal Unit

ASU: 12+ years of R&D

Next steps:

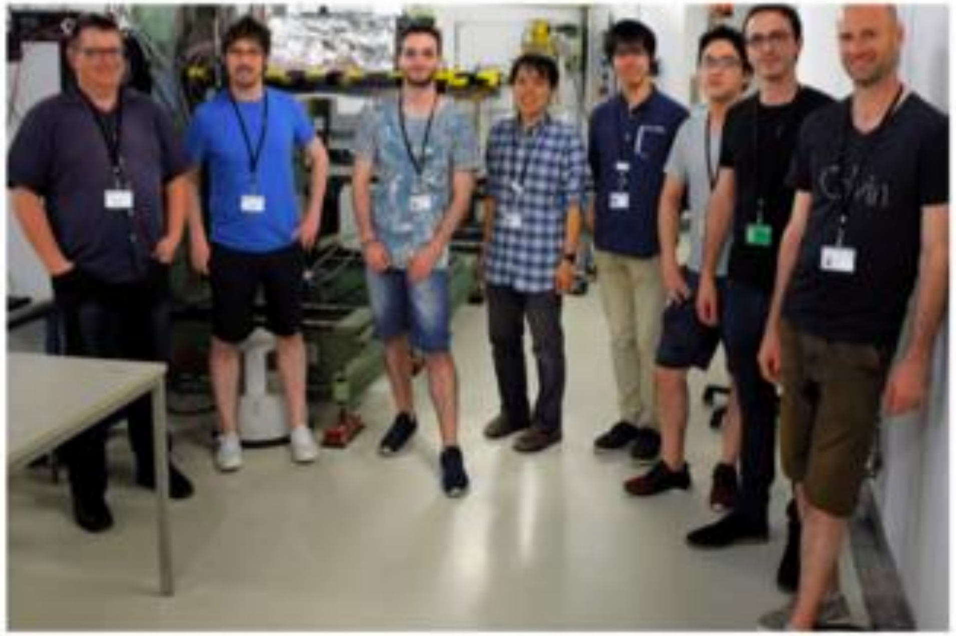
- Study of 8″ 725 μm wafers
  - Thicker: will give better S/N
- ASICs with zero suppression
- Passive/Active cooling (see back up slide) in particular relevant for high luminosity phase
- Continuing high level integration

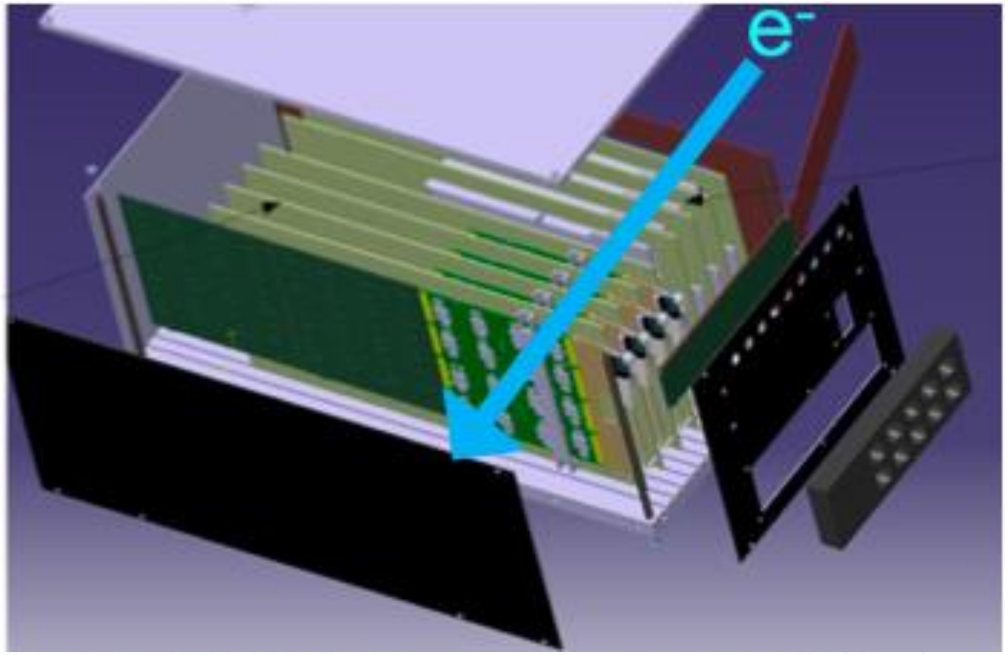
Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	Slab:FEV11	10 units, 320μm	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 (12)trig, 6–8 % masked
1st technological ECAL	2018	10 SLAB: 5 FEV11 320μm 5 FEV13 650*μm Compact stack	SK2 & SK2a (⊃timing)	Improved S/N (1/64 masked ch.) Timing...
1st COB	2019	FEV12-COB	1 wafer, 500μm	S/N ~ 22

Vincent.Boudry@in2p3.fr ILD SiW-ECAL Adaptative design | LCWS

Beam Test 2019 @ DESY

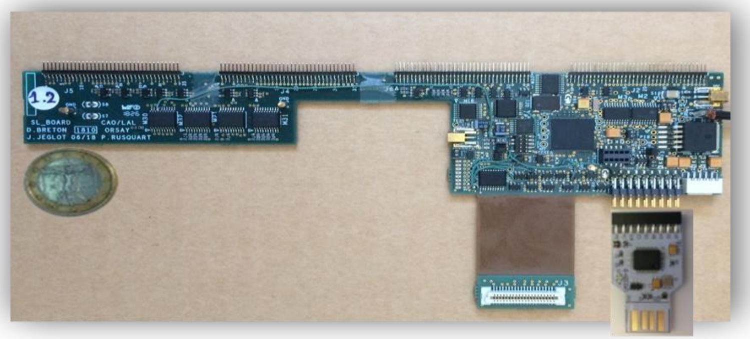
- Beam time:
  - 24^{th} June - 7^{th} July at DESY test beam facility
  - e^- beam: 1 - 5 GeV
- Presence from:
- Support & Hardware from:

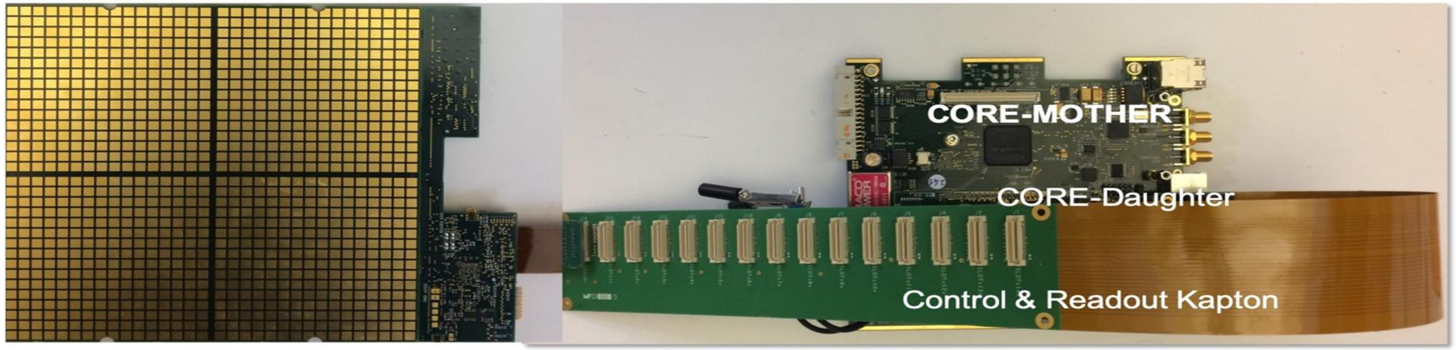


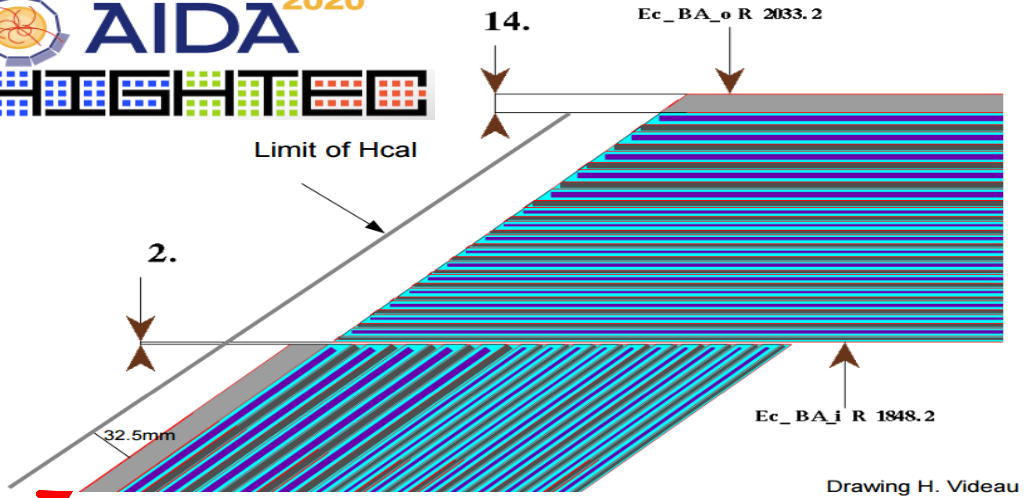


Towards a system for a final detector

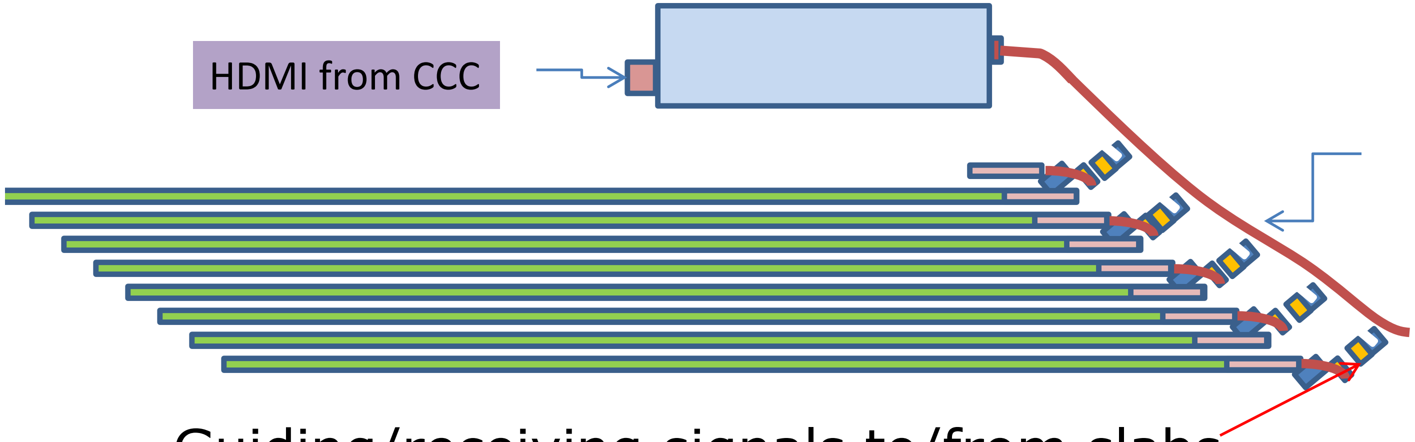
NEW: SL board







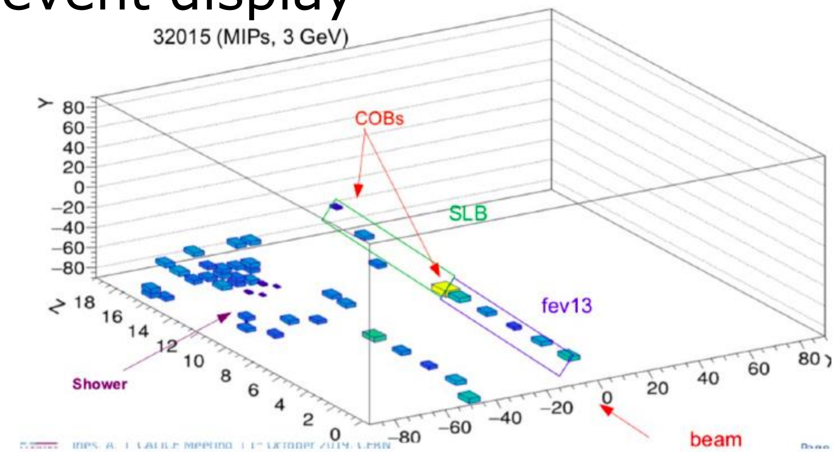
Approximately 6 cm between Ecal and Hcal

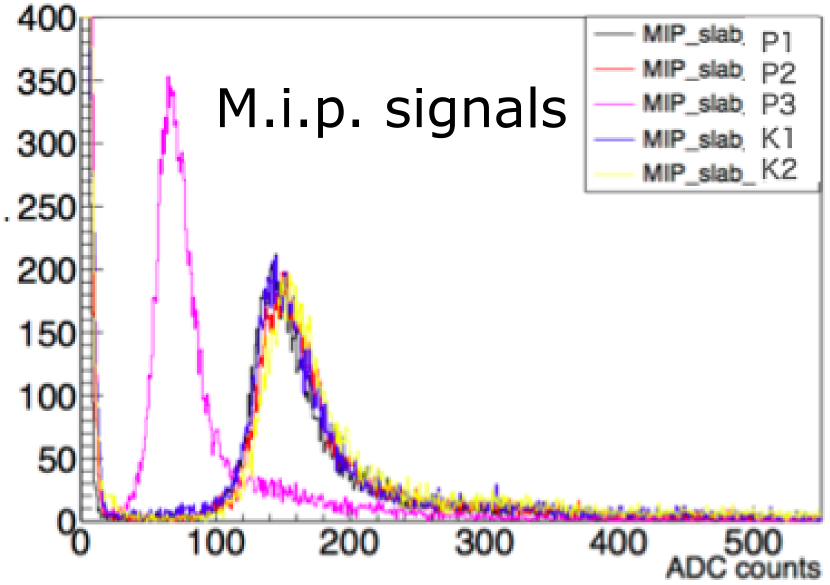


Guiding/receiving signals to/from slabs

Testbeam results for Si-W ECAL

event display





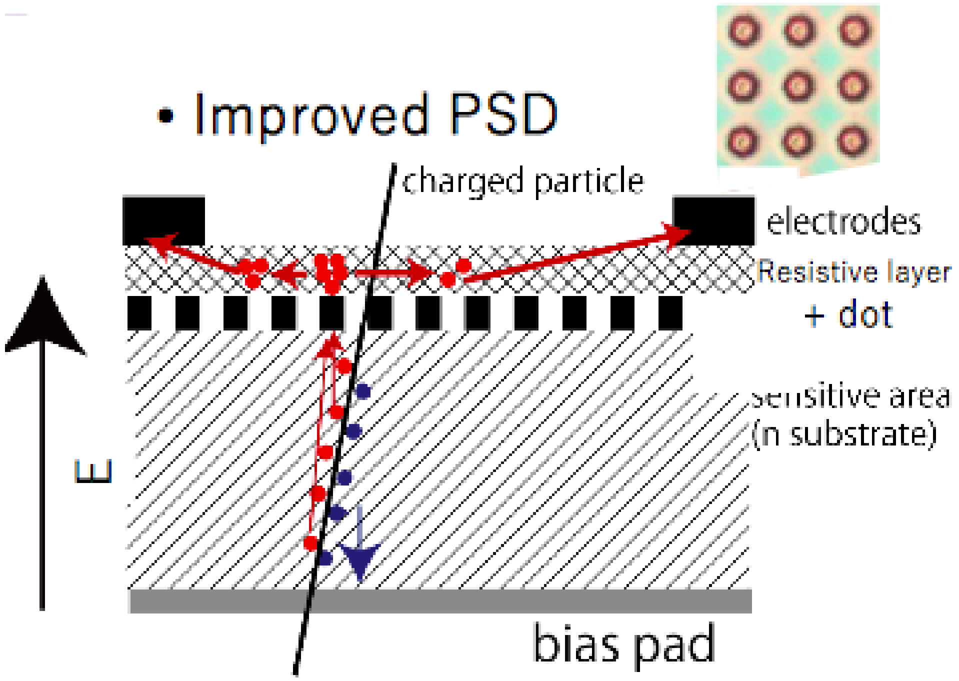
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

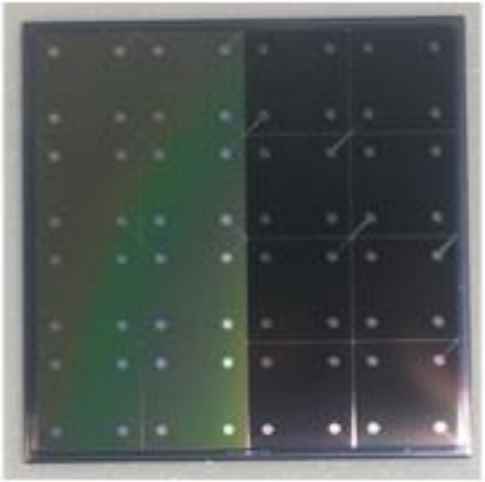
Summary and outlook

- Successful beam test 2019
  - Smooth operation of readout
- First systematic study of Chip-on-Board PCB in beam
  - Flatness good enough for wafers gluing (critical item of R&D)
  - Encouraging results
  - No serious issues discovered
  - Good MIPs w/o additional capacitances
  - Additional capacitances improve performance
- Still a number of tests to be done
  - 1 wafer -> 4 wafers
  - Tests with power pulsing
- Towards new design
  - Integration of stabilising capacitances
  - New SKIROC design (Flip-Chip dixit de la Taille)
  - Discussions with EOS (Korea) beginning of December
    - No immediate new production but rather feedback and brainstorming

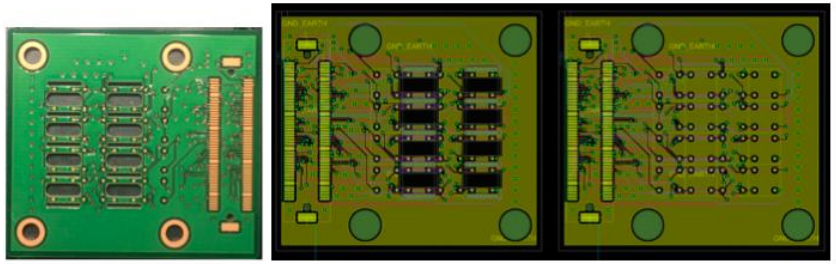
Position sensitive silicon detector

- Part of the Si-W calorimeter
- Reconstruct the position & direction of the photon
- PSD1 cell size : 5.5×5.5 mm^2; sensor thickness : 650 μm





PSD 1



New boards

- Preparations for test beam
- Different versions of PSDs

Scintillator ECAL

- Sensor layers of ScECAL consists of segmented scintillator strip with SiPM
  - **Scintillator strip**

    Plastic scintillator wrapped by reflector film

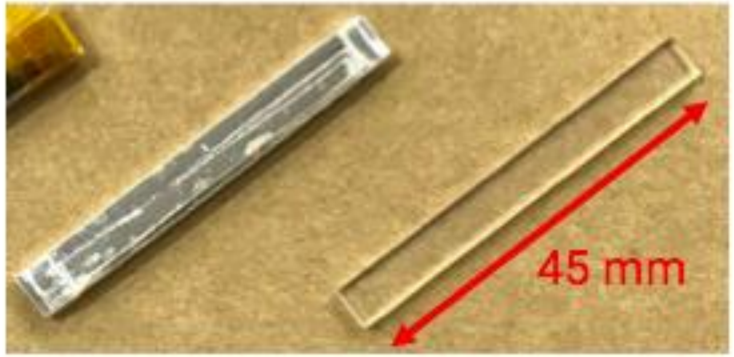
    Size: 45 mm x 5 mm x 2 mm
  - **SiPM** (MPPC®, PPD, GAPD, ...)

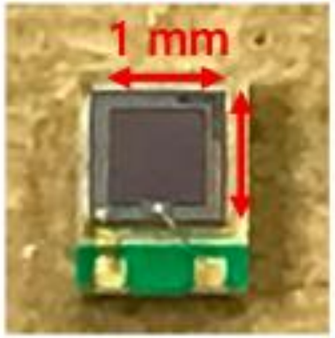
    Photosensitive area : 1 mm x 1 mm

    Gain: **10^5** (PMT : 10^6–10^7)

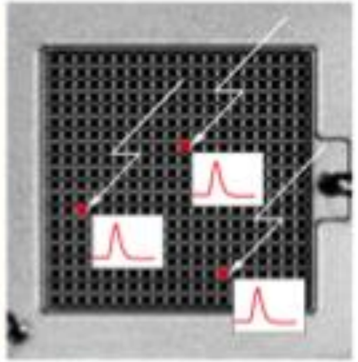
    Pixel pitch: **10 um** or **15 um**
    - The smaller pixel pitch SiPM has, The larger dynamic range it has. So small-pitch SiPM has less effects of saturations.

Advantage: low operation voltage (<100 V), high magnetic filed resistance

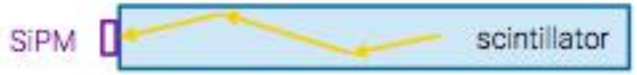




SiPM: S12571-015P (HAMAMATSU)



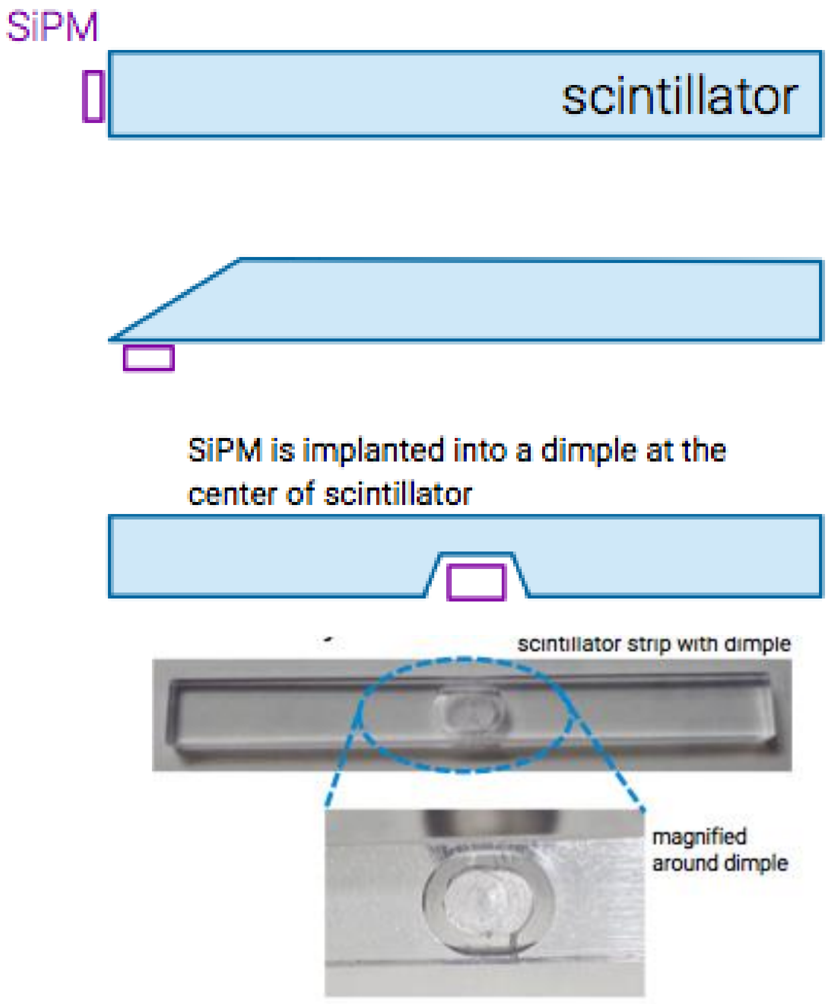
HAMAMATSU, Opto-semiconductor hand bool



E_{loss} ∝ # of detected photon

Scintillator ECAL

- **Side readout**
  - Good light yield for MIP
  - Dead space about 2%, bad light yield uniformity
- **Bottom readout**
  - No dead space, good light yield uniformity
  - Less light yield for MIP
- **Dimple readout (NEW: proposed by USTC & IHEP)**
  - **No dead space**
  - **Easy to mass-produce**

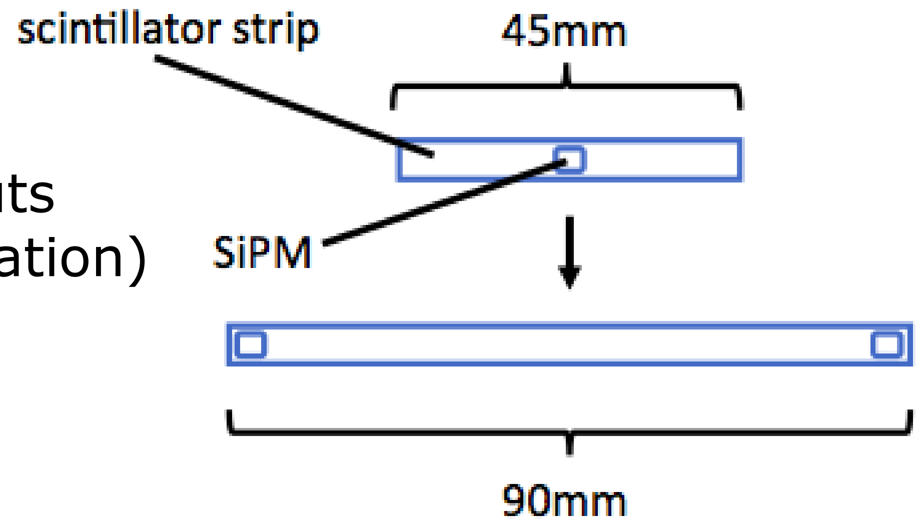


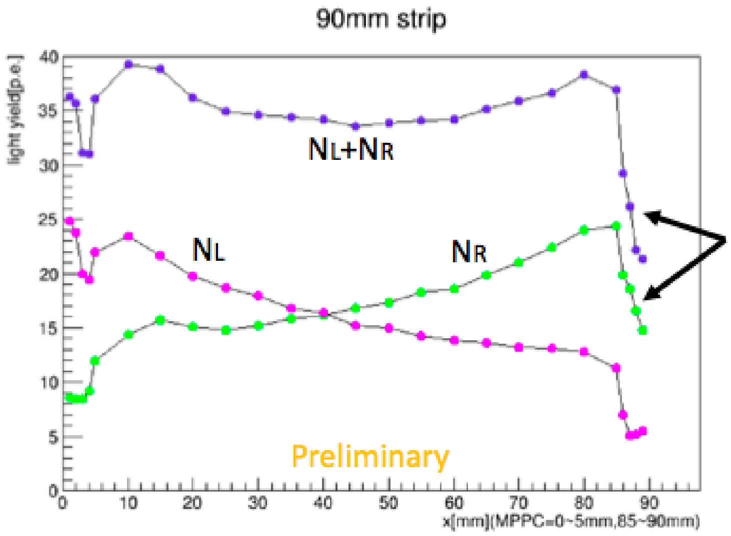
The dimple readout scintillator has good light yield and good uniformity

Sc ECAL with double SiPM readout

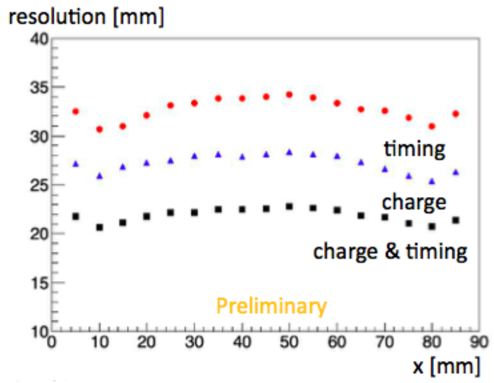
Some possible advantages:

- Eliminating noise by coincidence
- Higher light yield by summing two SiPMreadouts
- Even lower light yield for each SiPM(less saturation)
- Operational even if one of SiPMs is dead
- Position by charge or timing differences

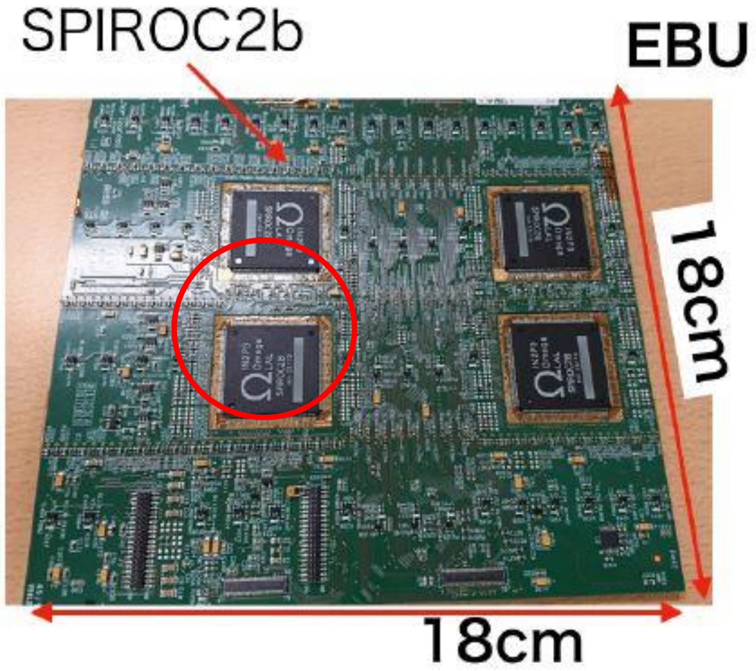


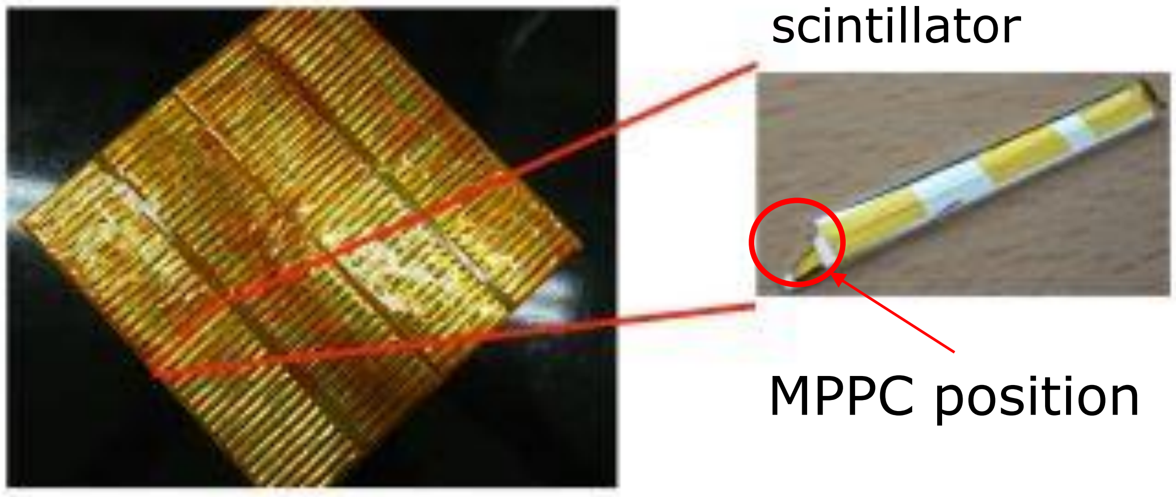


- Large N p.e. 35
- Single readout N p.e. 20
- Edge effect not yet understood
- Position resolution ~20 mm



DAQ for the Sc ECAL: EBU





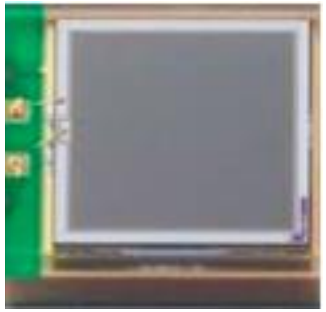
Scintillator surface

- EBU (ECAL Basic Unit) is fabricated by DESY.
- EBU consists of SPIROC surface and scintillator surface.
- One EBU is a PC board with 144 MPPCs and 144 scintillators.
- One EBU is equipped with four ASICs called SPIROC2b developed by OMEGA group.
- One SPIROC2b can control 36ch of MPPCs and adjust each applied voltage for a channel.

Scintillator Tiles MPPCs

Both hexagonal and squared tiles
Using 4th generation MultiPixelPhotonCounter

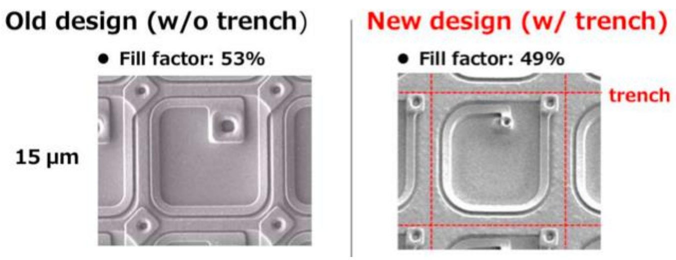
MPPC	S14160-1310	S14160-3010	S14160-1315	S14160-3015
Sens. area	1.3 x 1.3 mm^2	3 x 3 mm^2	1.3 x 1.3 mm^2	3 x 3 mm^2
Pixel size	10 μ	10 μ	15 μ	15 μ
# pixels	16675	90000	7296	40000
V_b	~43	42.1	42.5	42.2
Dark rate	120 kHz	700 kHz	120 kHz	700 kHz
gain	$1.8x10^5$	$1.8x10^5$	$3.6x10^5$	$3.6x10^5$
C at Vop	100 pF	530 pF	100 pF	530 pF

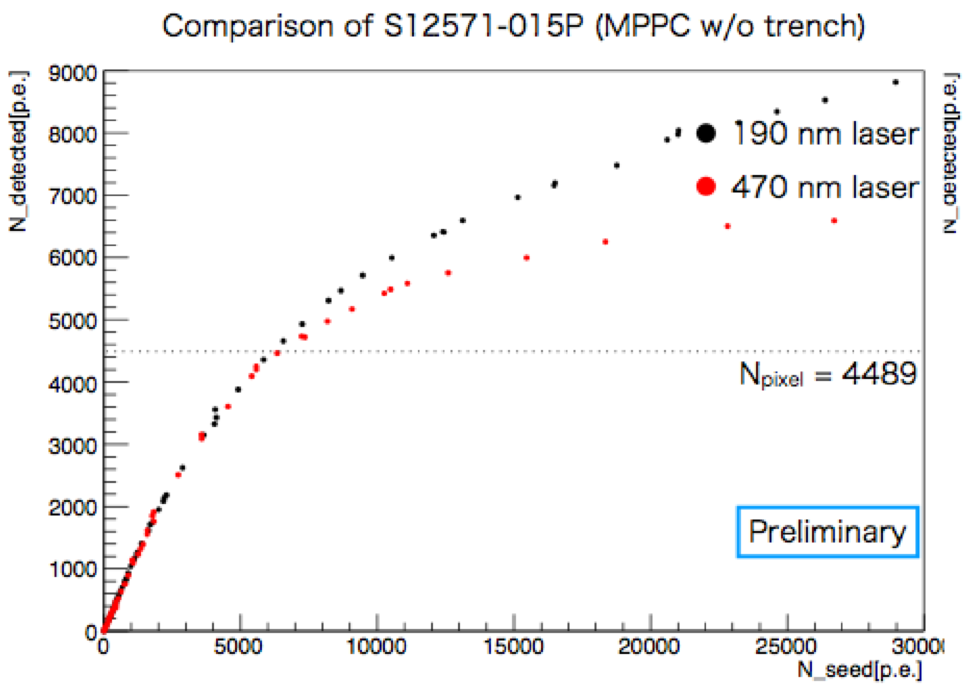


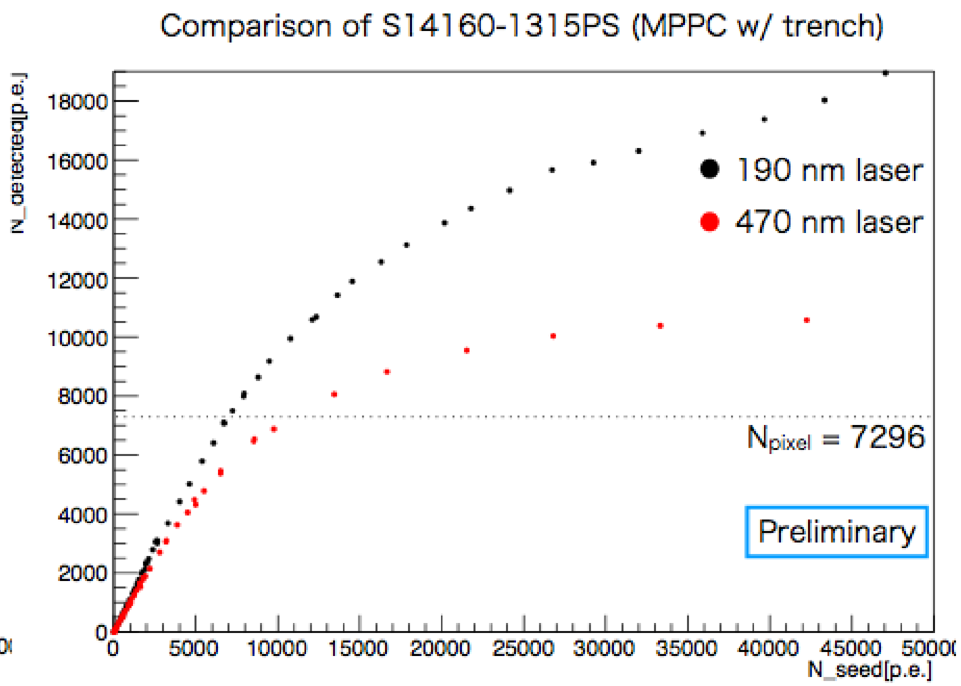
- Readout of hexagonal tiles look promising
- Performance of hexagonal tiles with center-mount readout
  - Uniformity within ±6% except for center position
  - Dimple was too small to insert MPPC fully, ➔ light yield in the center is 1.68 times larger than the average ➔ need to enlarge dimple and redo measurements

Saturation of SiPM

SiPM saturation can be an issue for Sc-ECAL
Studied for two MPPCs w(w/o) trench

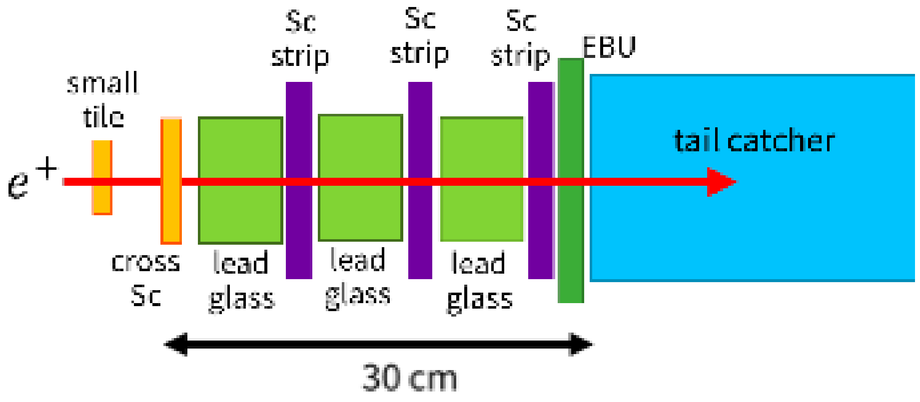


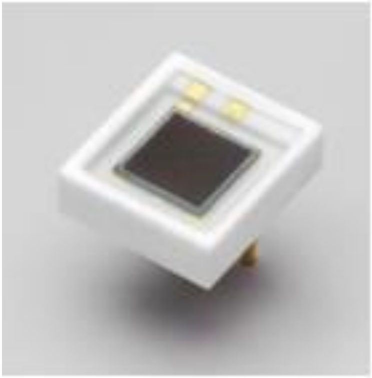




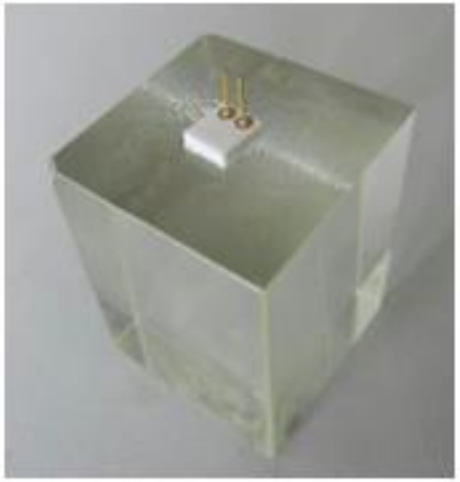
Sampling Calorimeter AACAL

Lead glass segmented 3x3x4 cm^3
MPPC size 3x3 mm^2
Active Absorber CAL (AACAL)



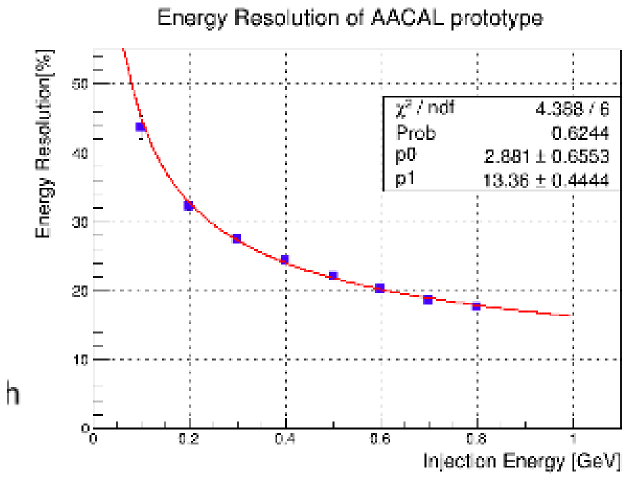


MPPC



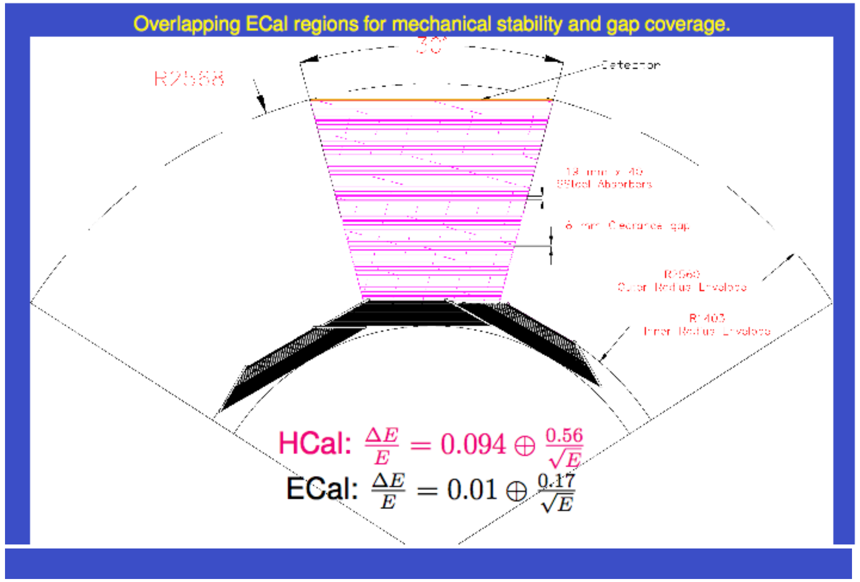
Lead Glass

- The prototype shows good linearity.
- The energy resolution of prototype is $13.4\ \%/\sqrt{E} + 2.9\ \%$.



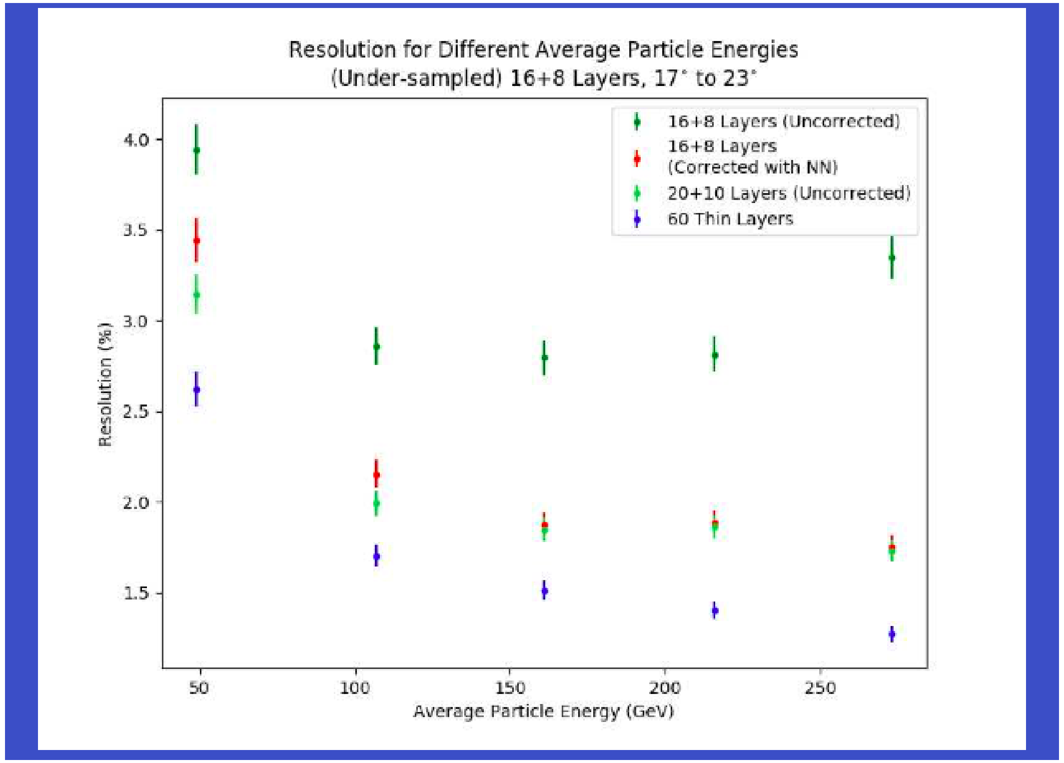
Leakage correction for SiD

Geometry of Calorimeters



Note special overlap zone

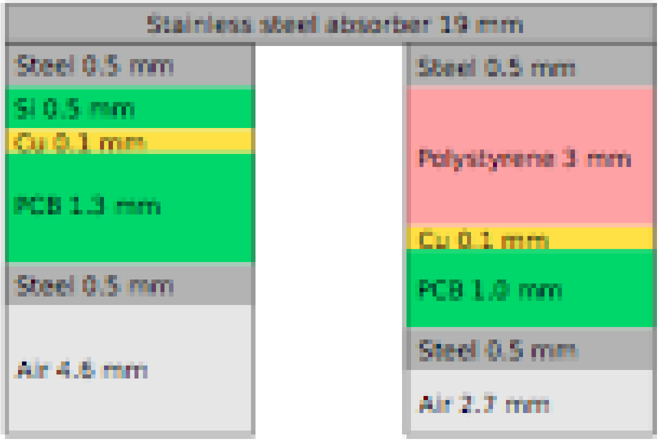
Problem bad e.m. E resolution not whole e.m. shower measured



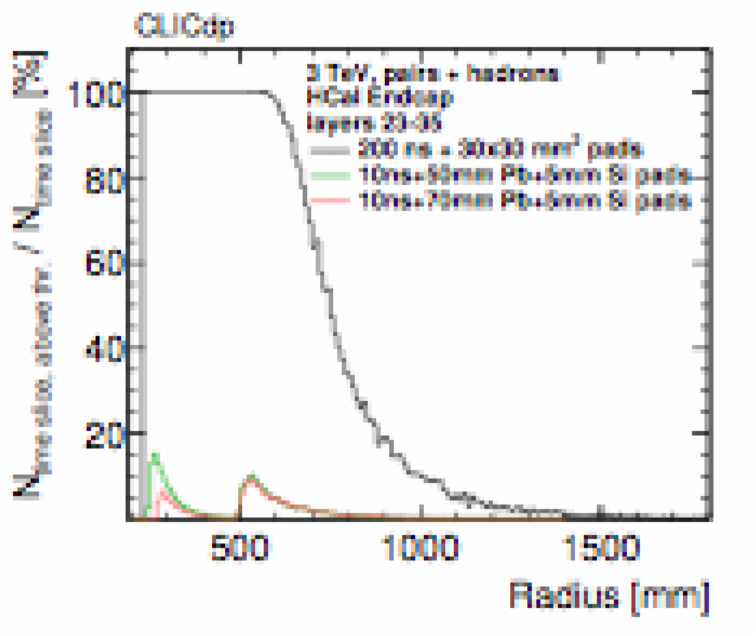
After correction (NN) improved

HCal shielding for CLIC

HCal endcap - two granularity regions



Silicon sensor cell Scintillator sensor cell

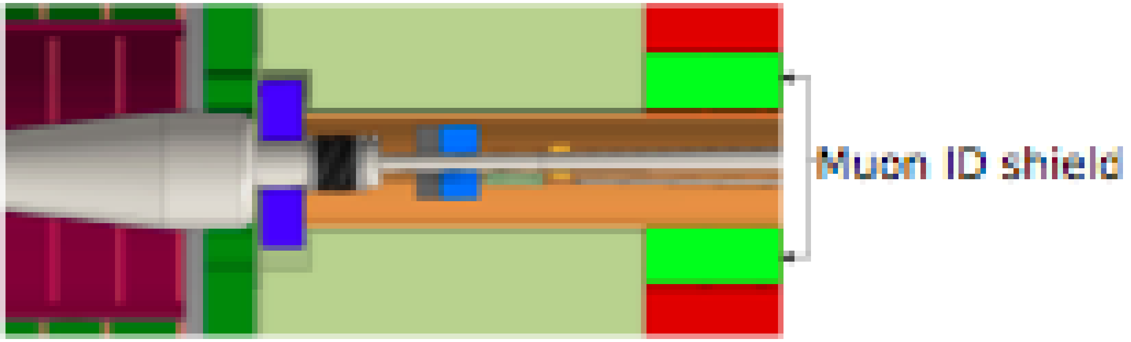


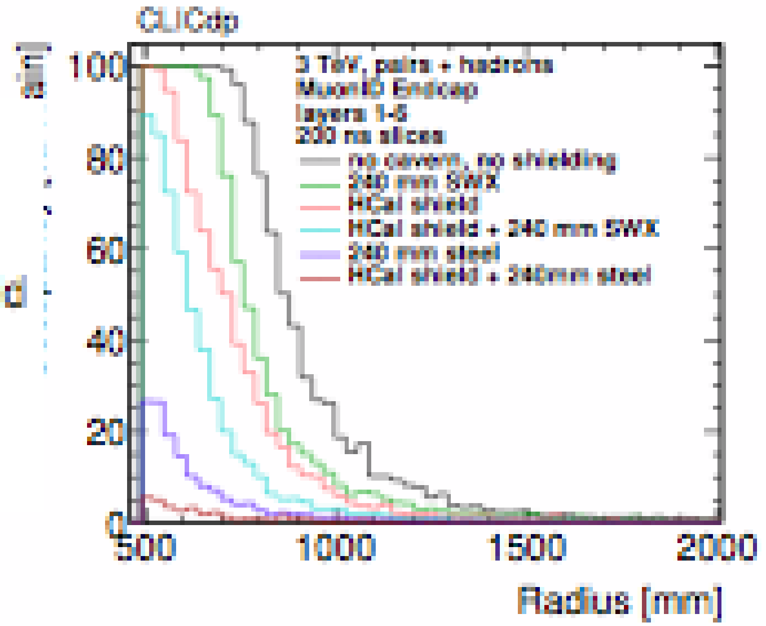
- Two granularity regions for HCal endcap: one with scintillator, one with silicon sensors

Dominik Arominski | HCal and MuonID occupancies mitigation - 29-10-2019 | 17 / 21

Muon shielding for CLIC

MuonID shielding options





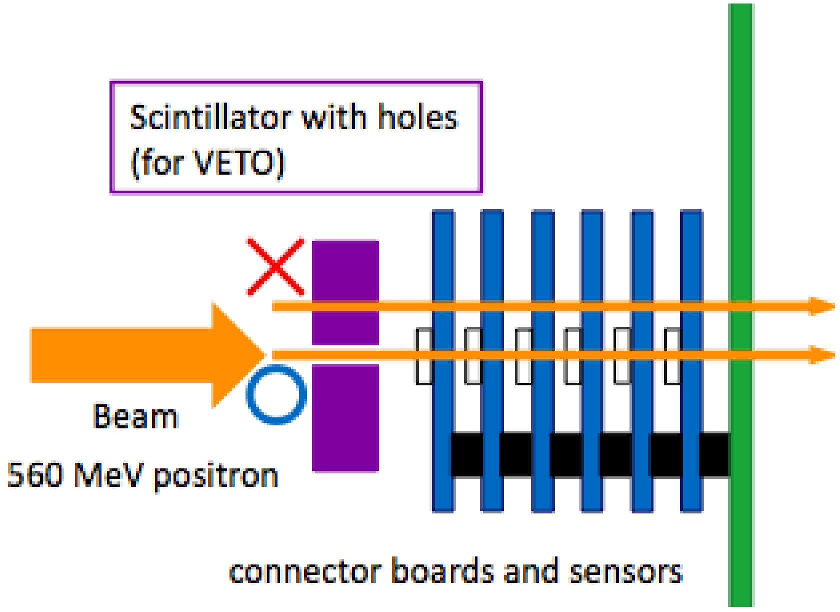
- Borated polyethylene (SWX) does not provide efficient shielding, even when layered with lead as in the HCal shield
- Best solution: the HCal endcap shield + 240 mm of stainless steel

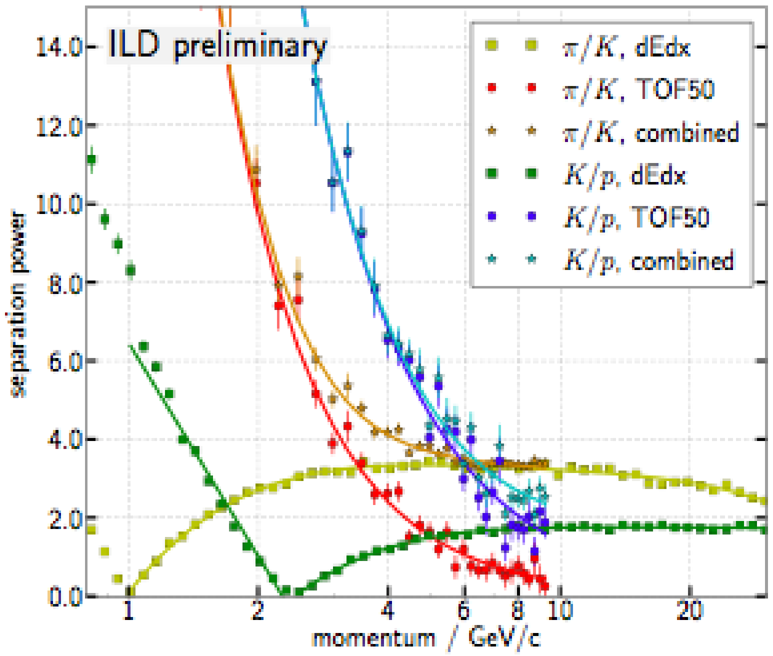
Dominik Arominski | HCal and MuonID occupancies mitigation - 29-10-2019 | 19 / 21

Precise timing with silicon sensors

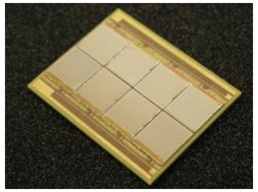
- Low Gain avalanche photo diode (LGAD)
- Allows particle ID using Time of Flight
- LGADs are part of LHC upgrades σ~30 ps
- Several (8) avalanche photo diodes tested
- Preparations for a test beam

stacking connector boards

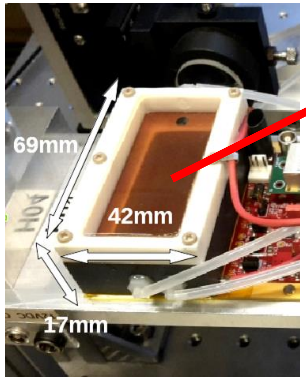


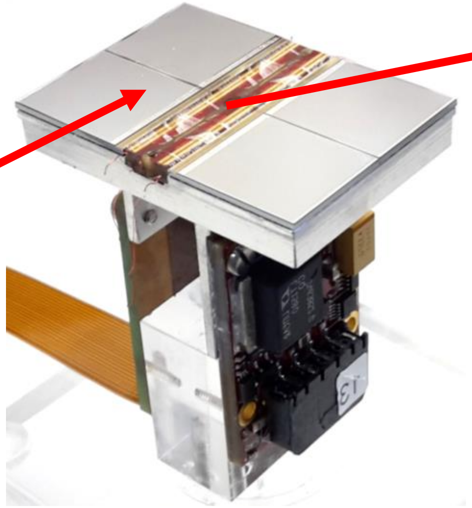


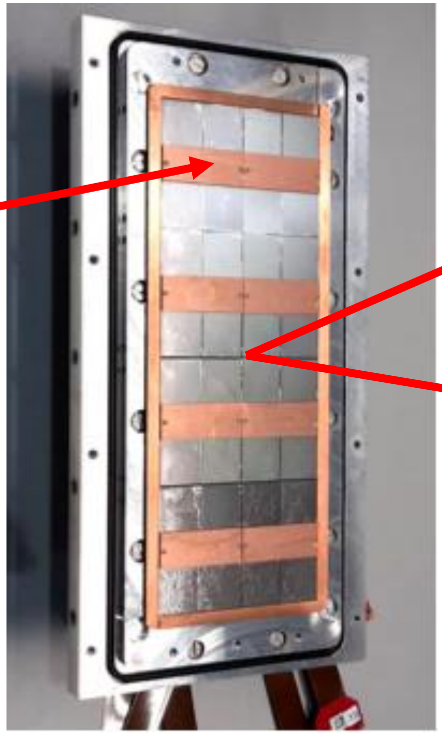
Pixel TPC

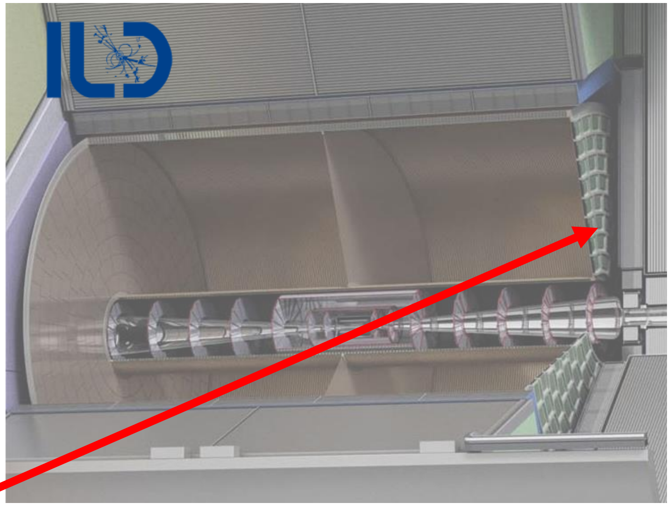


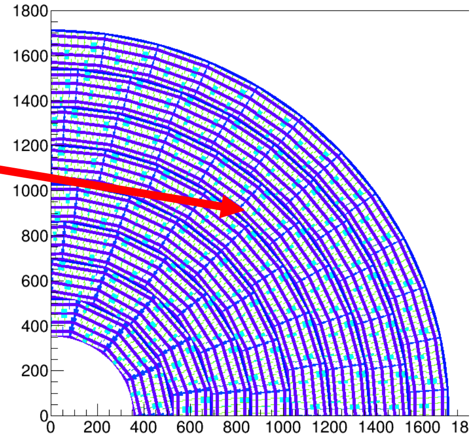
(Octopuce)











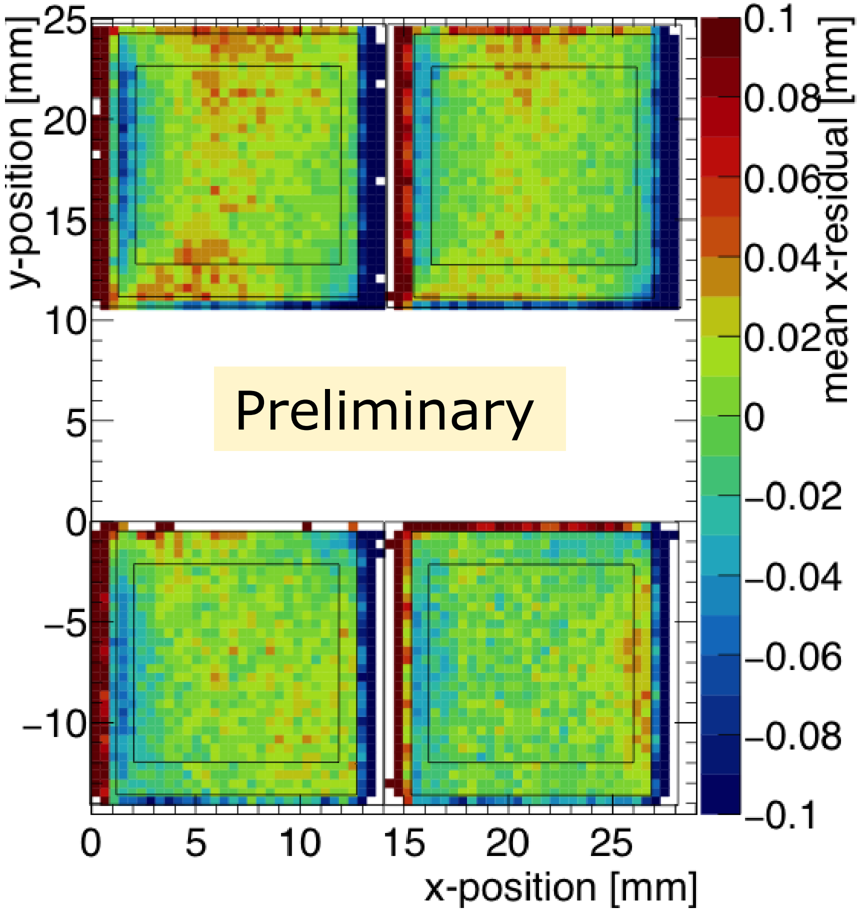
(TimePix1) TPX3 chip Quad Module TPC plane

(2007-14) 2017 2018 2019

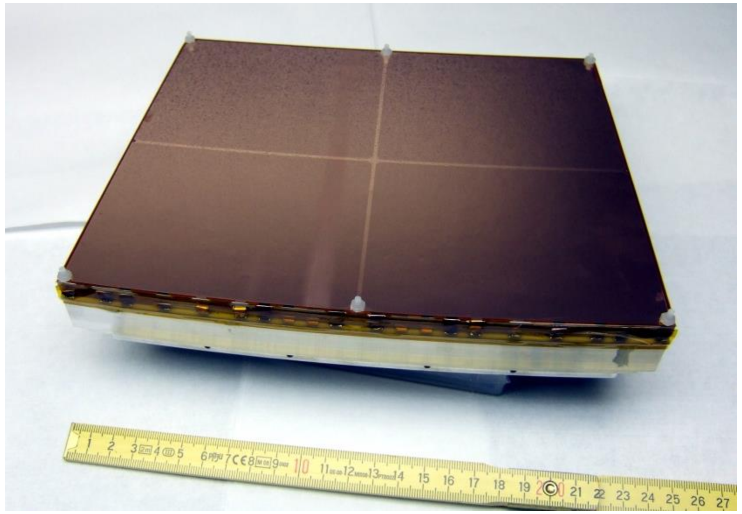
Quad and 8-Quad module

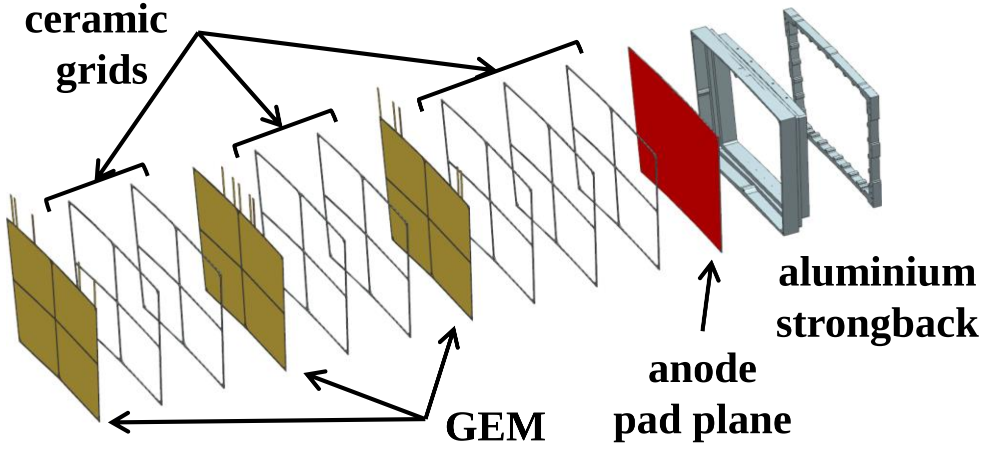
- A Quad detector was designed and the results from the 2018 test beam presented
  - Small edge deformations between two chips are observed
    - added guard wires to the module to obtain a homogeneous field
  - After correcting the deformations in are less than 15 µm
- An 8-Quad module has been designed with guard wires
  - Deformations (no corrections) are shown to be < 15 µm
  - Test beams are being planned at DESY and Bonn
- A pixel pixel TPC has become a realistic viable option for experiments
  - High precision tracking in the transverse and longitudinal planes, dE/dx by electron and cluster counting, excellent two track resolution, digital readout that can deal with high rates

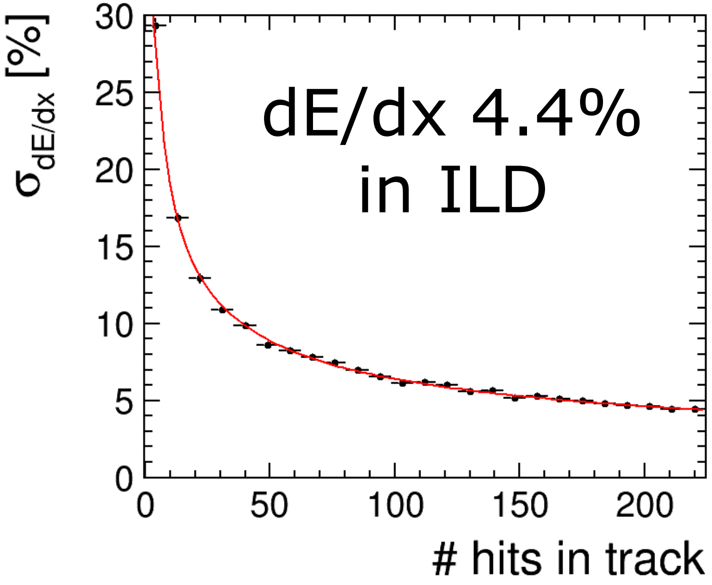
One quad in 8-Quad module



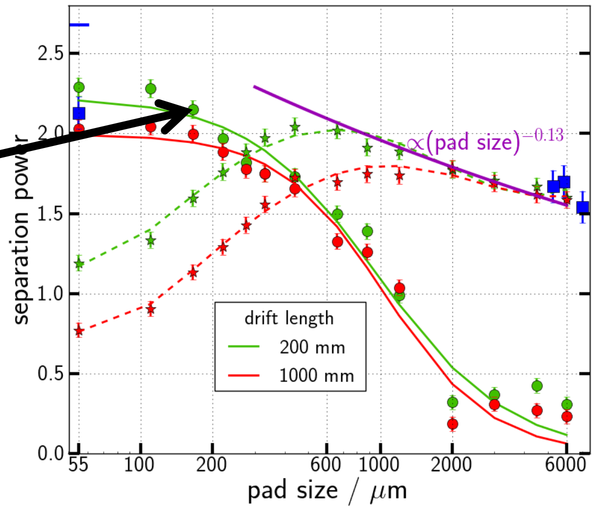
DESY GEM module





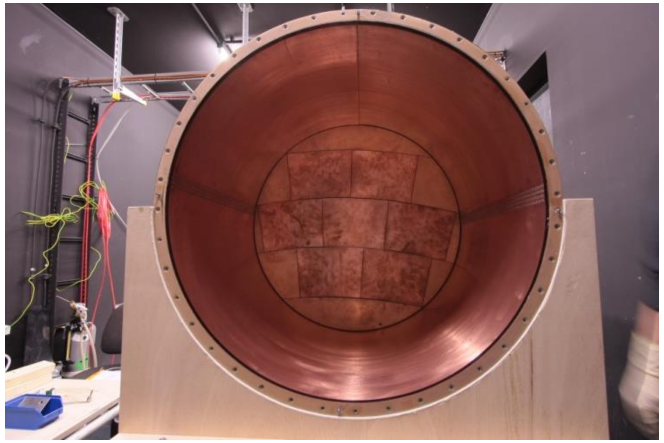


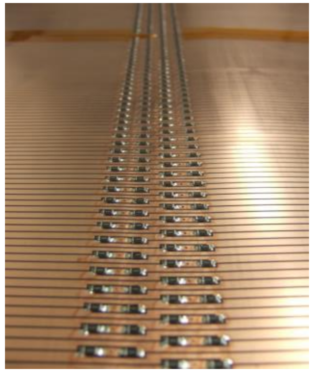
- A better dEdx resolution?
  - smaller pad size



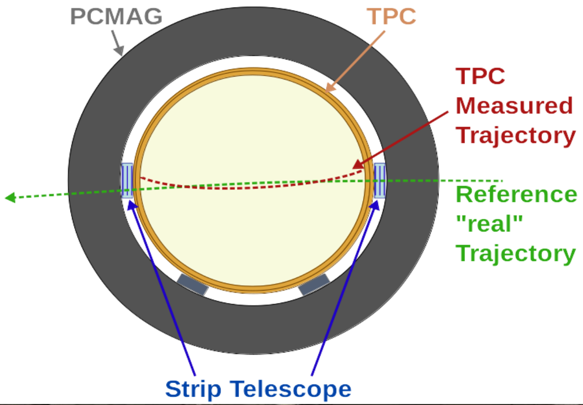
DESY Large Prototype TPC

New version field cage



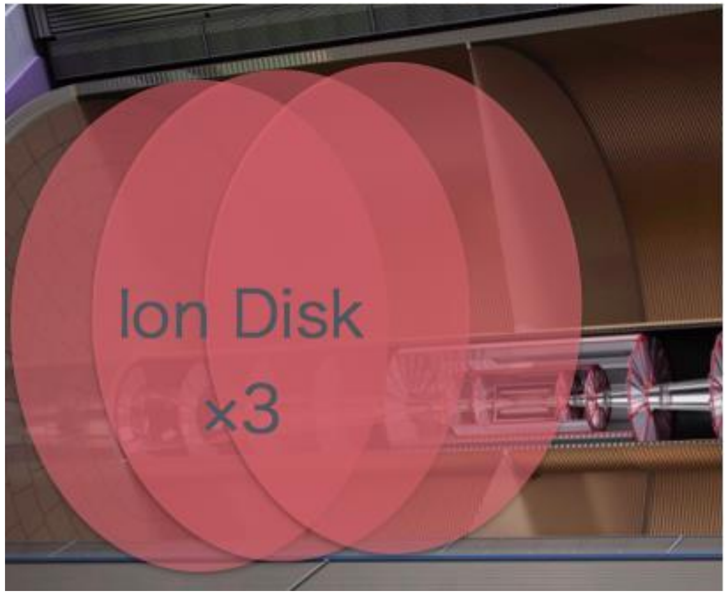


Silicon Beam telescope PCMAG



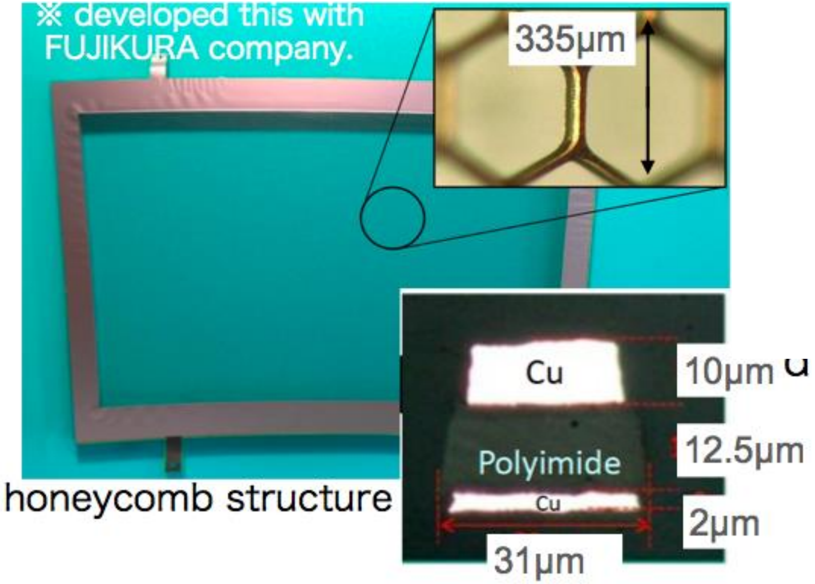
GEM Gating device

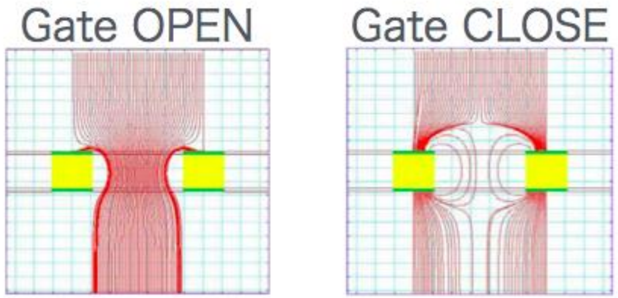
Ion Feed back problem

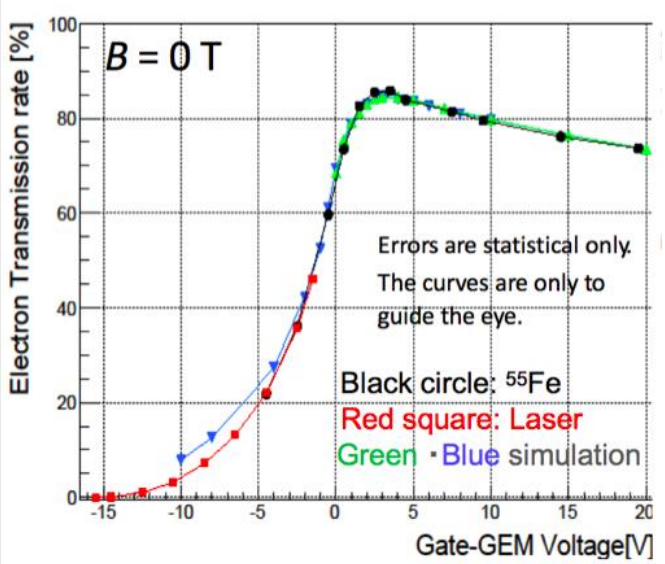


yumia@post.kek.jp

Gating device







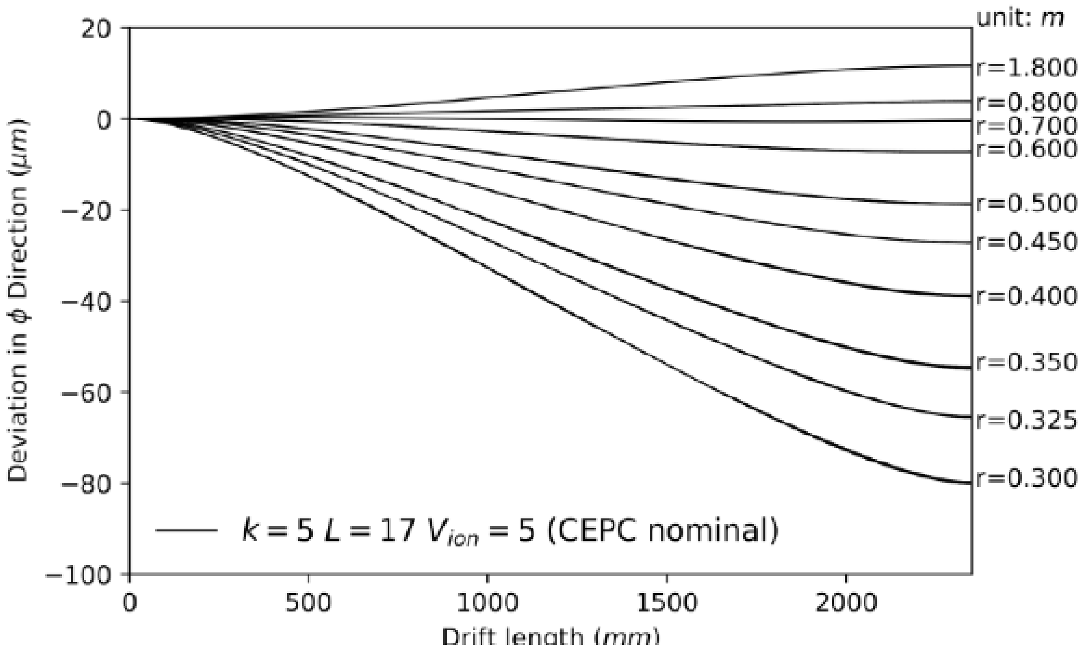
Electron transmission

Measured to be ~86 % with gating GEM.

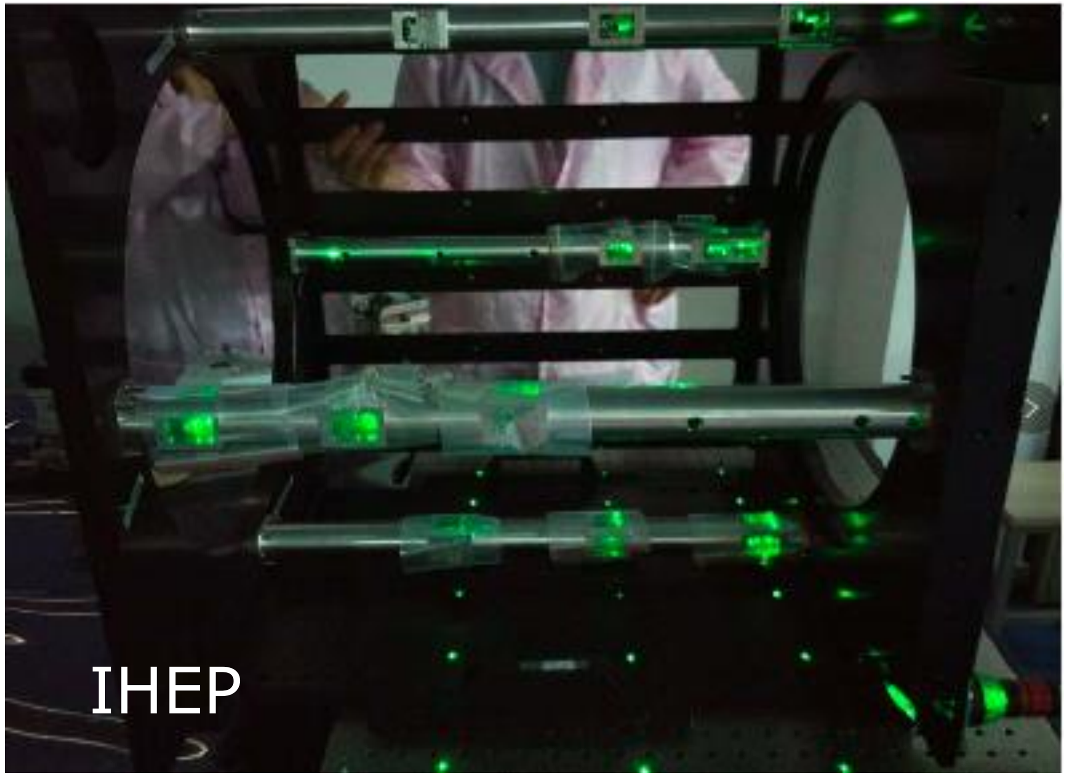
TPC for CEPC

CEPC running at the Z
Deformations due to Ion back flow

Simulation of deviation with IBF (k=Gain×IBF) @CEPC

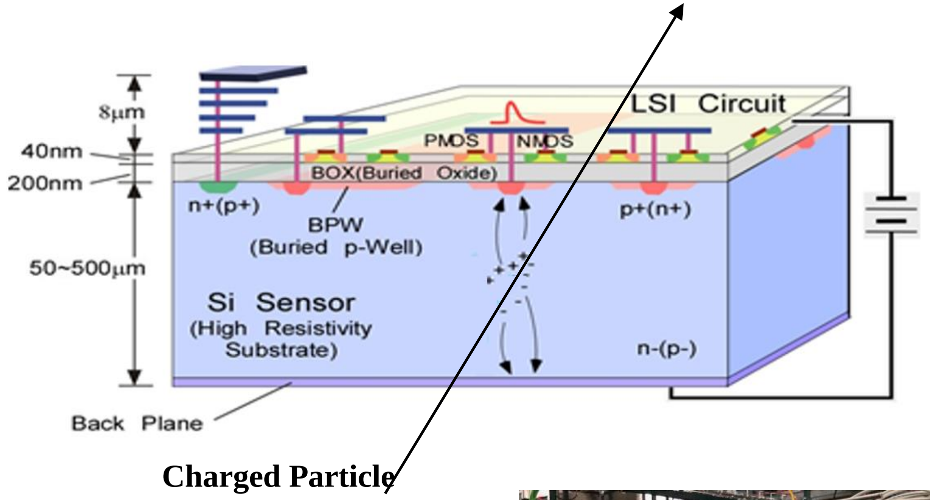


Laser calibration of a TPC

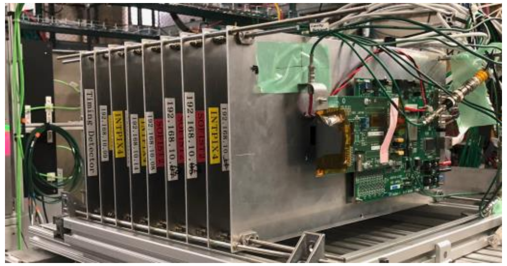


Silicon: SOI based pixel detector

Monolithic sensor using silicon-on-insulator (SOI) technology:
Lapis 0.20 mm FD-SOI Pixel nodes (in handle Si) are electrically connected to readout circuit (SOI layer) through small vias fabricated in a conventional LSI process. Pixel size v4 20 μm x 20 μm



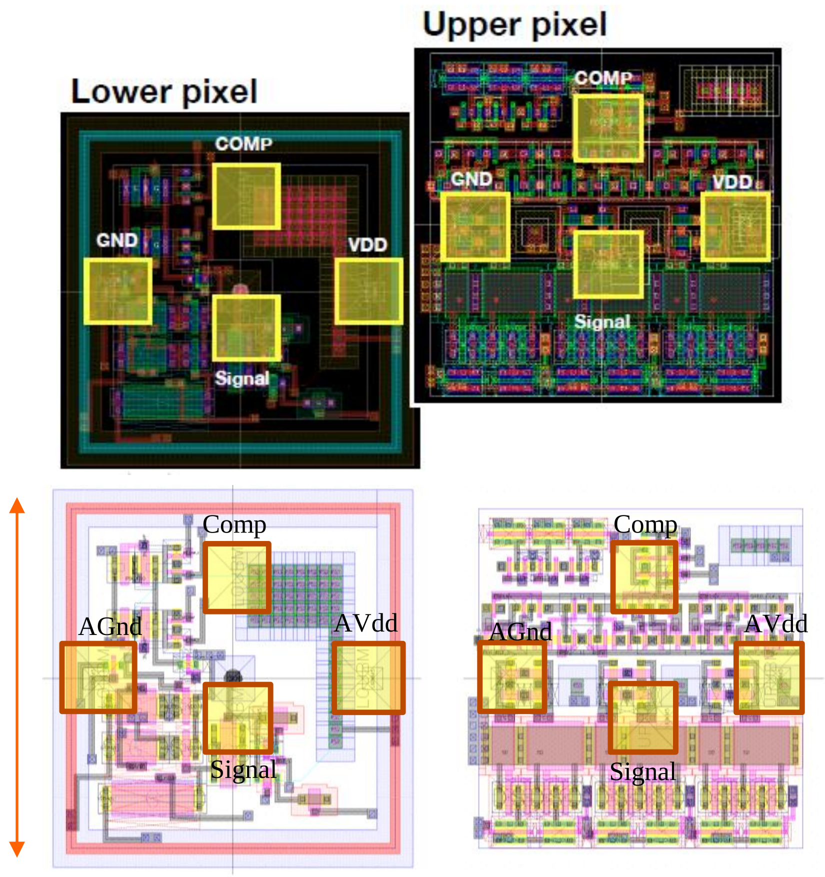
Yearly test beam activities FNAL



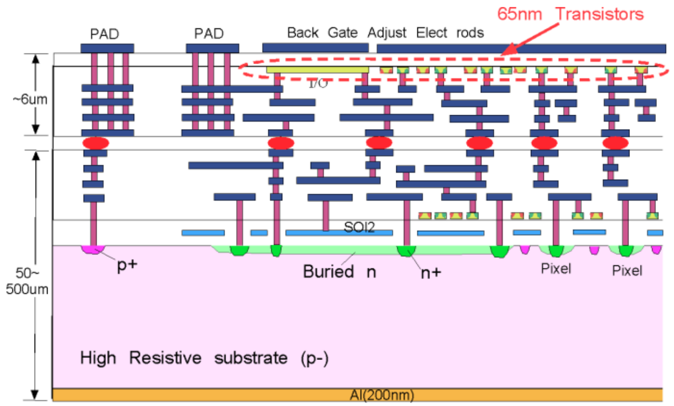
	Ver. 1	Ver. 2	Ver. 3	Ver. 4
Produced /Tested*	2016/2017	2017/2018	2018/2019	2018/2020
Wafer	SOI	DSOI	DSOI	DSOI
Pixel size (μm^2) (μm)	20x20	25x25	30x30	20x20
Chip size (mm^2) (μm)	3x3 500	4.5x4.5 75	6x6 300	4.5x4.5 300

Silicon: SOFIST-4 3-D stacking

Electronics circuits in two chips are fused using cylindrical micro-bumps to extend the circuit functionality in limited space.

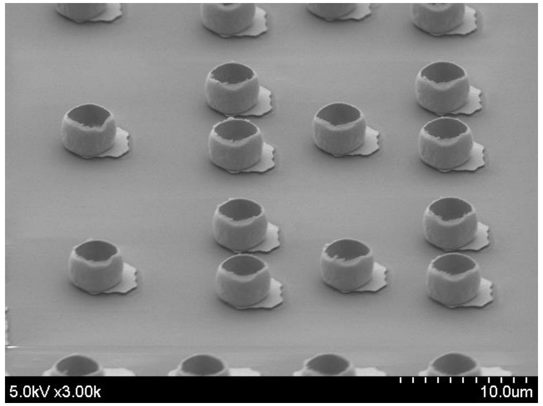


4 mm



upper

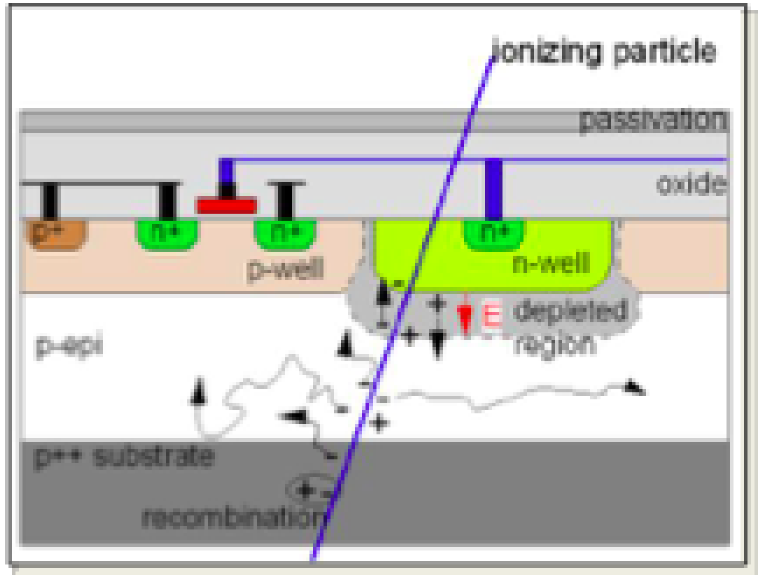
lower

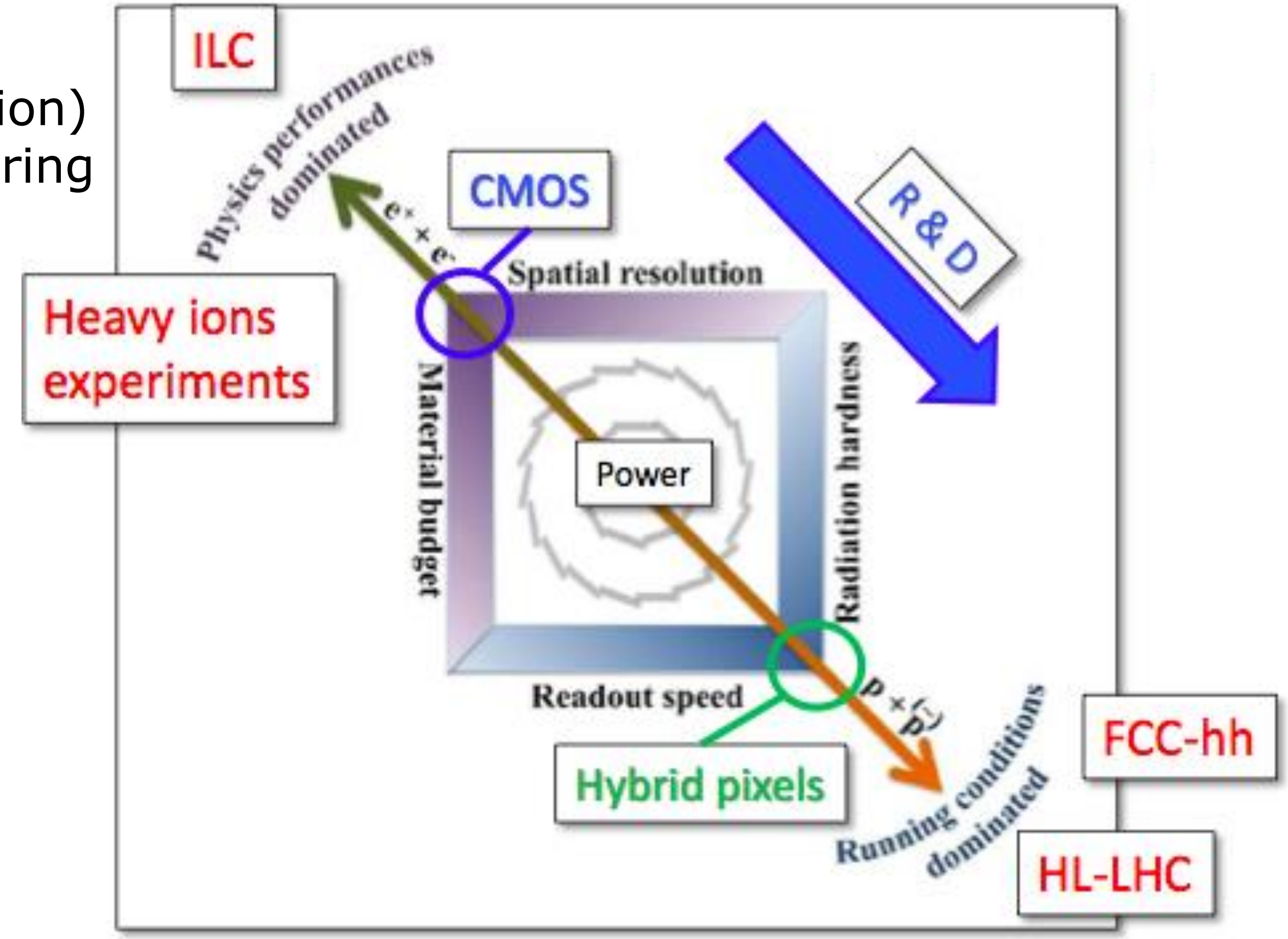


micro-bumps

Silicon: CMOS pixel detector

- Monolithic (Signal created in low doped thin epitaxial layer ~10-30 μm)
- Thermal diffusion of e- (Limited depleted region)
- Charge collection: N-Well diodes (Charge sharing resolution)
- Continuous charge collection (No dead time)

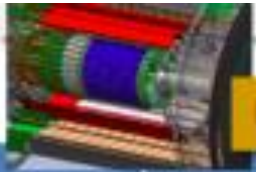




Silicon: CMOS pixel detector

Keep excellent spatial resolution and push towards better time resolution

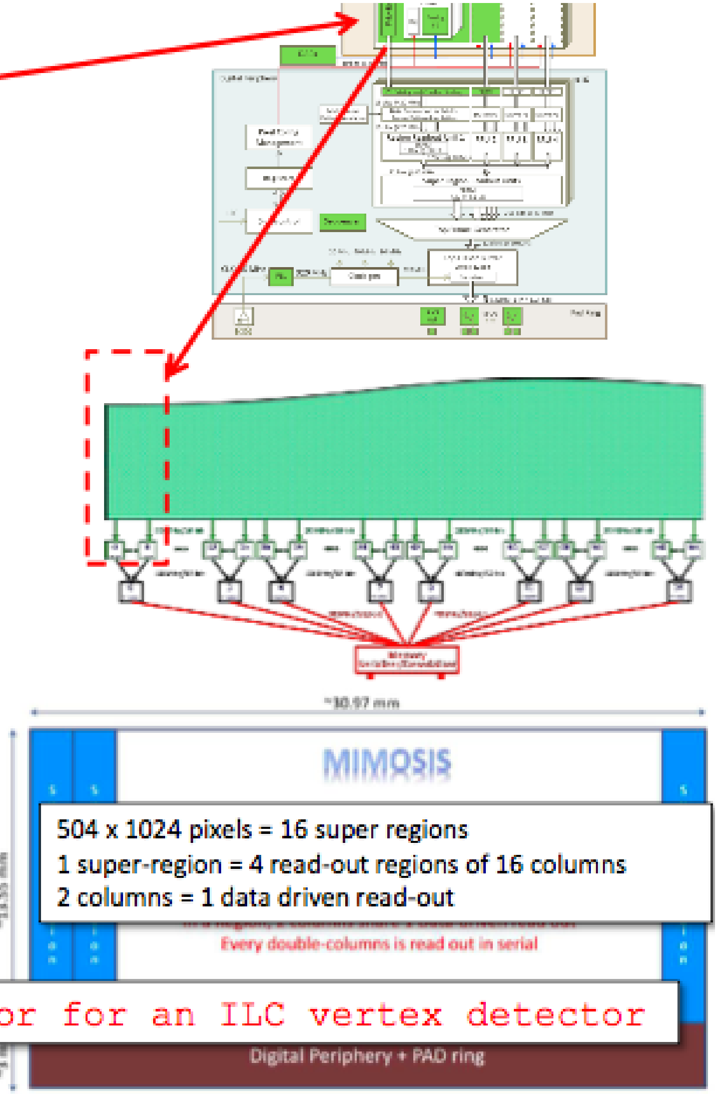
Strong synergy between Higgs factories and Heavy ion experiments




	ULTIMATE STAR-PXL	ALPIDE ALICE-ITS	MIMOSIS CBM-MVD	PSIRA proposal ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 µm	0.18 µm	0.18 µm	0.18 µm (conservative) < 0.18 µm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	synchronous r.o. In pixel discri.	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (µs)	~185	5-10	5	1 – 4

MIMOSIS towards ILC vertex detector

- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - ✓ Back from foundry (2017)
  - ✓ Test (2018-2019)
    - Testability
    - Priority encoder frequency
    - Radiation hardness design (SEU)
- MIMOSIS-1: 1st prototype of complete sensor
  - ✓ About to be Submitted
  - ✓ Tested during 2020
- MIMOSIS-2:
  - ✓ 2021
- MIMOSIS-3: final pre-production sensor
  - ✓ >2022



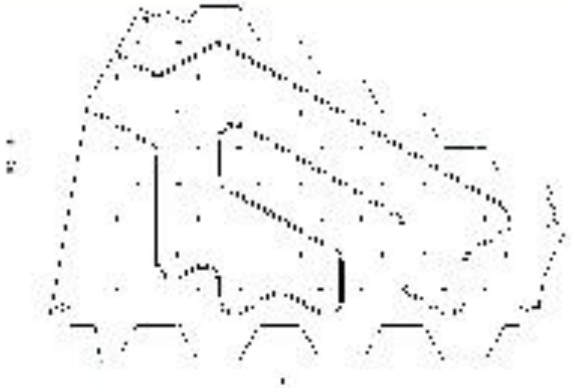
⇨ architecture adaptable to a fast sensor for an ILC vertex detector

LCWS 2019, Sendai A.Besson, Strasbou

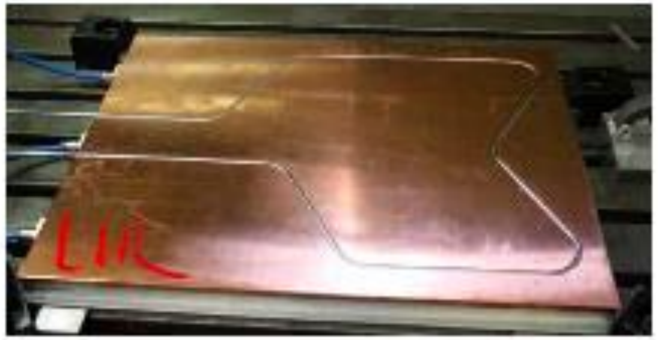
Active cooling → 'Continuous colliders'

R&D using CMS studies (Courtesy of Th. Pierre-Emile from CMS-LLR group)

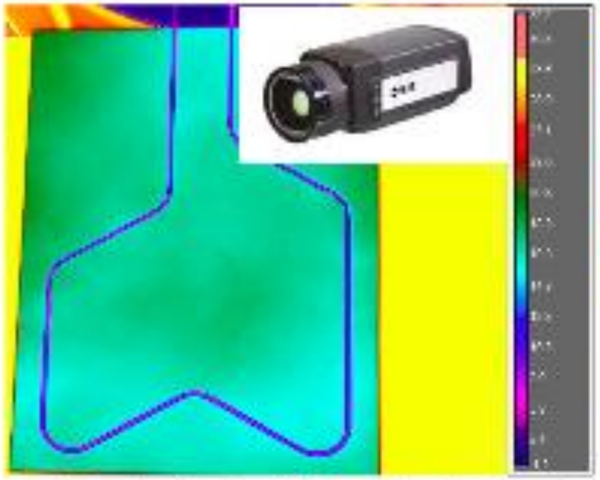
Si-W ECAL

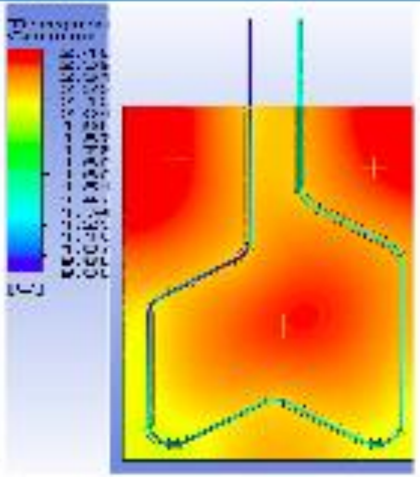


Copper plate prototype dimensions information



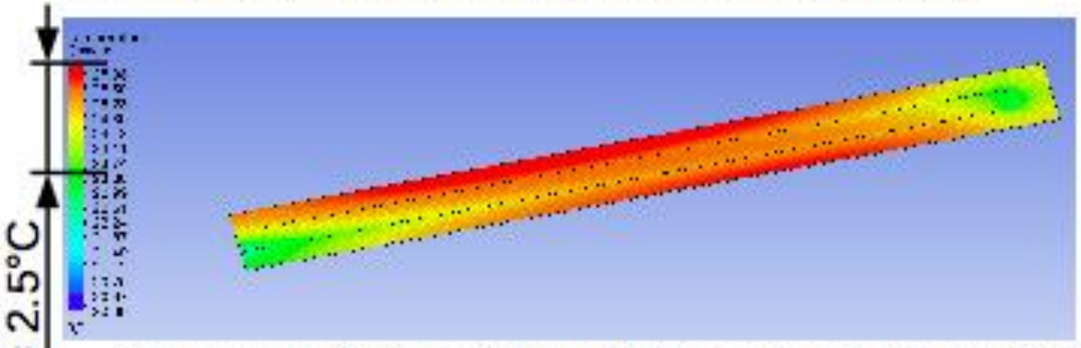
Pipe insertion on a cooling prototype for FEA correlation





Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling



Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

+3mm of Copper/Layer

= 2× cont. operation of a SLAB