

# Photon-to-Digital Converters for precise timestamping and/or large area noble liquid experiments

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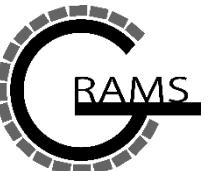
\*TRIUMF, Vancouver, Canada

CALICE Collaboration Meeting

March 4<sup>th</sup> 2020



Arthur B. McDonald  
Canadian Astroparticle Physics Research Institute



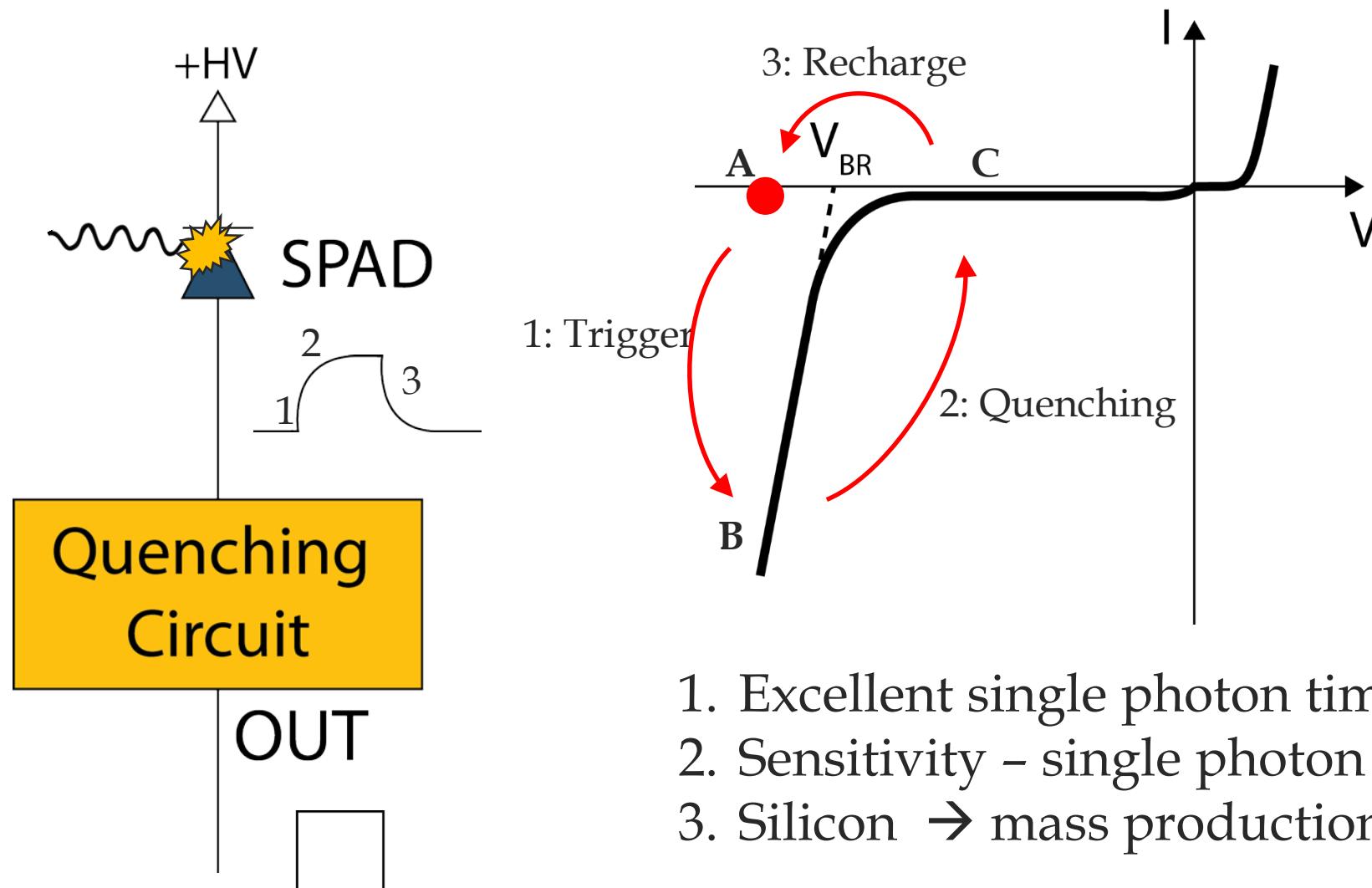
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# What is a Single Photon Avalanche Diodes (SPAD)?



# Single Photon Avalanche Diode (SPAD) Operation Cycle

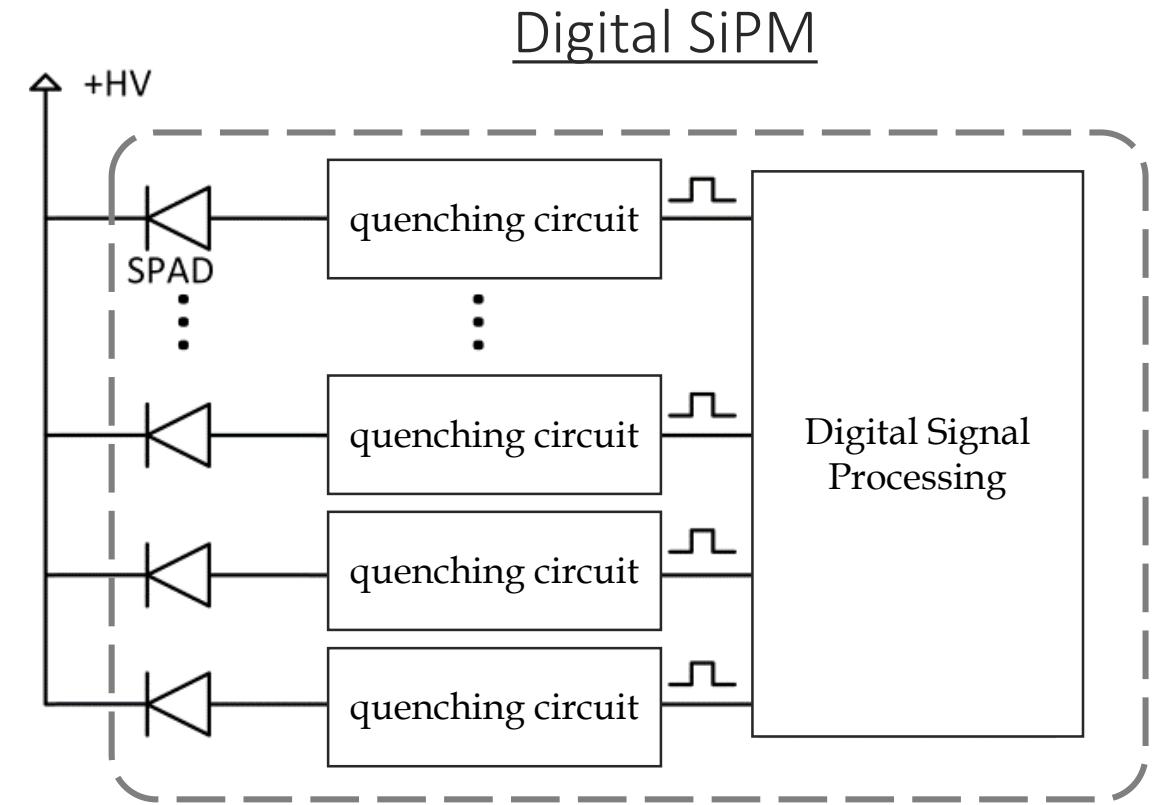
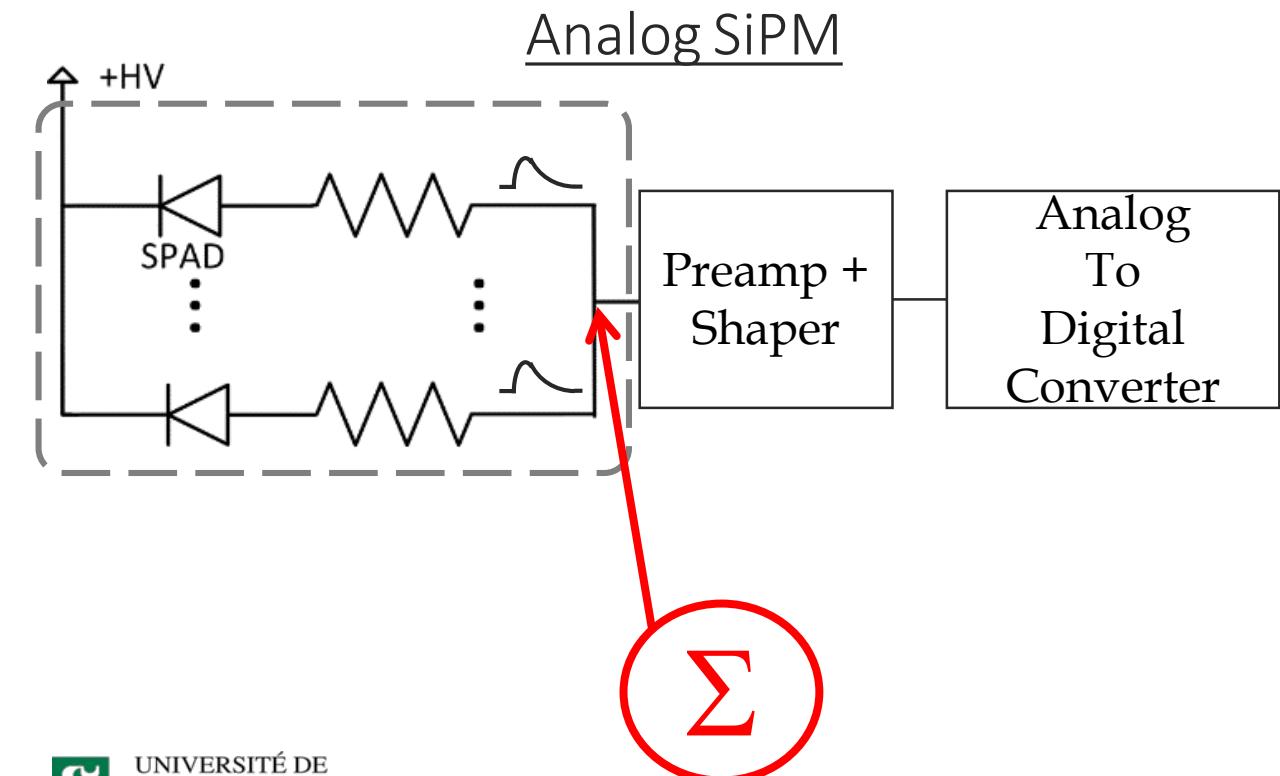


# Analog VS Digital Silicon Photomultiplier (SiPM)



# Analog and Digital Silicon PhotoMultiplier (SiPM): The Definition

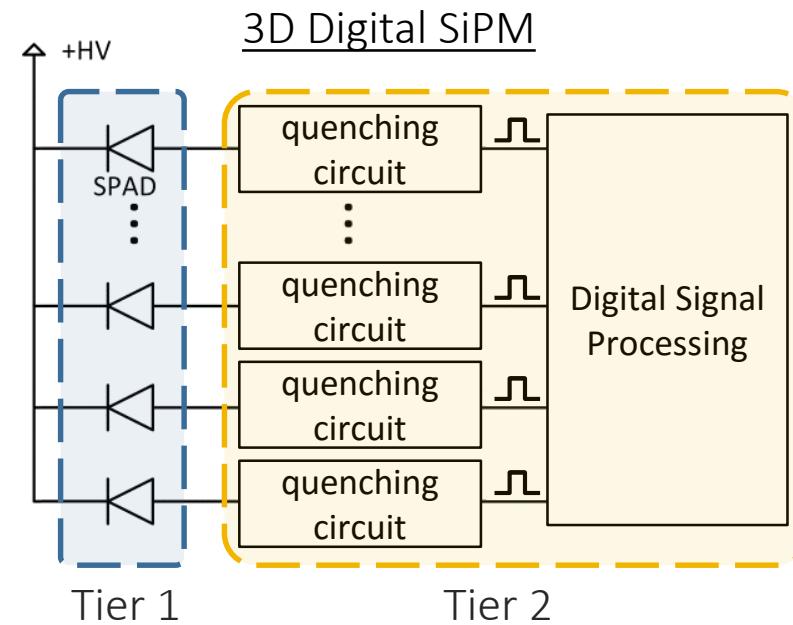
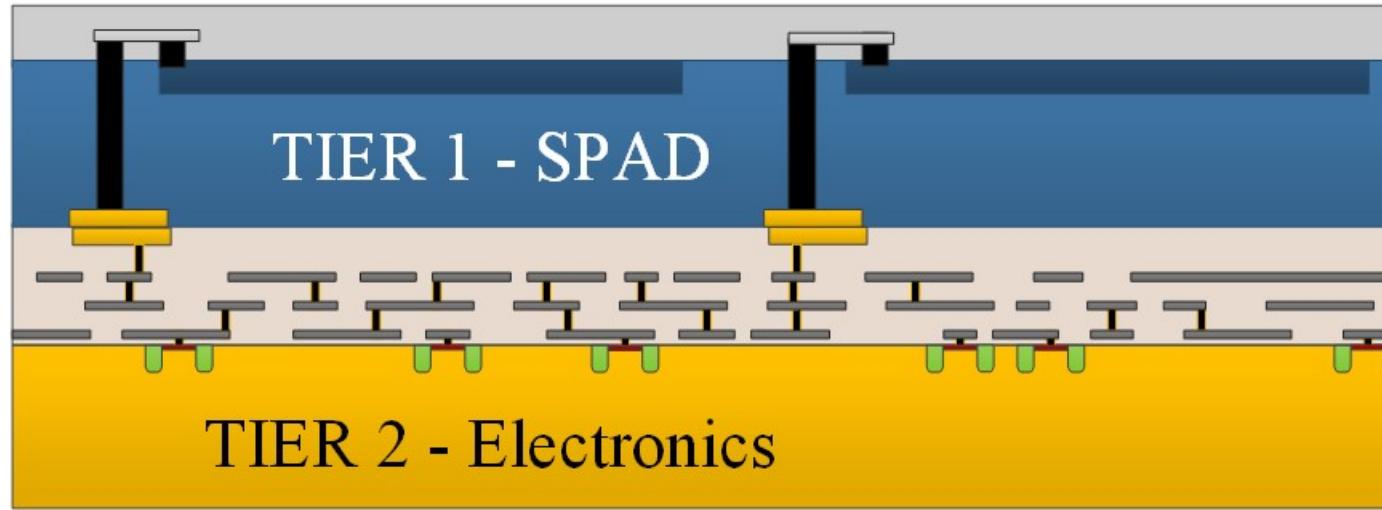
**Single photon avalanche diode (SPAD)** is the basic unit cell of **analog and digital SiPM**



# Analog and Digital SiPM

- A SPAD is a Boolean detector: **digital information available at the sensor level**
- With an **analog SiPM** we sum Boolean detectors (an array of SPAD) to get a linear response...
  - Then, use a current/transimpedance amplifier + shaper + ADC
- To digitize the data... again!**
- With a **digital SiPM**, each SPAD is coupled **one-to-one** with its individual readout circuit.
  - Photon to bit conversion at the sensor level
  - Improved noise immunity
  - Output capacitance is not an issue (compared to SiPM)
  - Single photon counting mitigated
  - Control over each SPAD: **faulty or radiation damaged = shut off**
  - Lower dead time (sense-quench-recharge < 10 ns)
  - Mitigates afterpulsing noise
  - No trigger = Low power consumption

# 3D Digital SiPM / Photon-to-Digital Converter Concept

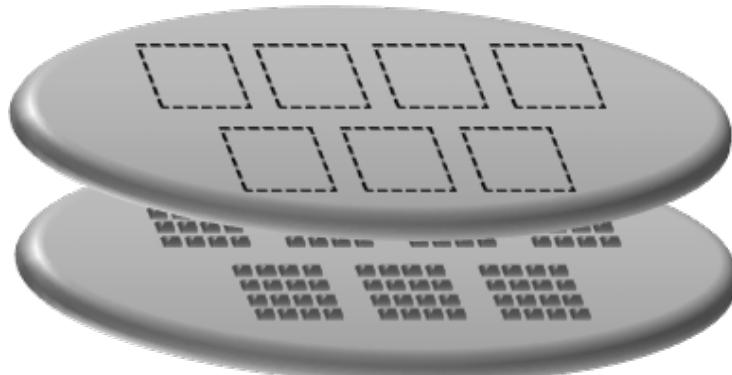


# How to Build a Fully Industrial 3D Digital SiPM ?

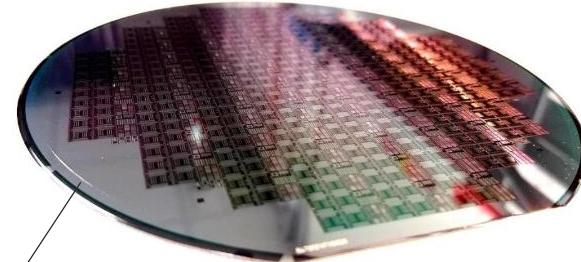
Partnership with Teledyne DALSA Semiconductor Inc.  
(Bromont QC, Canada)



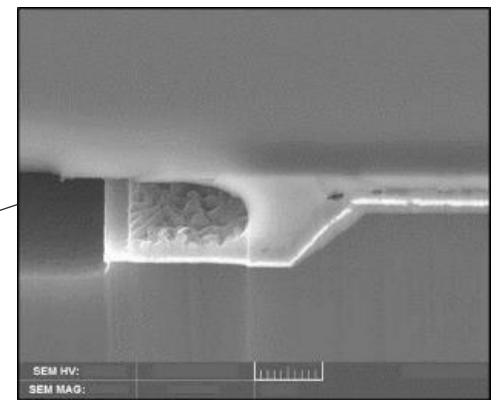
Wafer scale 3D digital SiPM technology



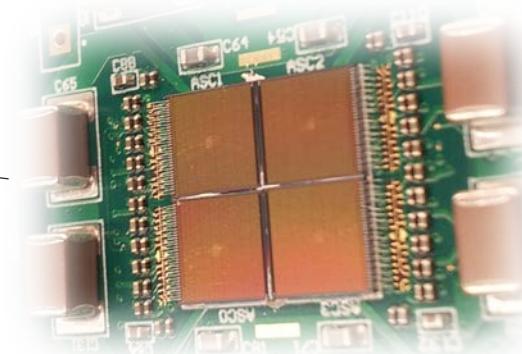
SPAD array layer  
Wafer level process  
CMOS readout



SPAD process



3D process



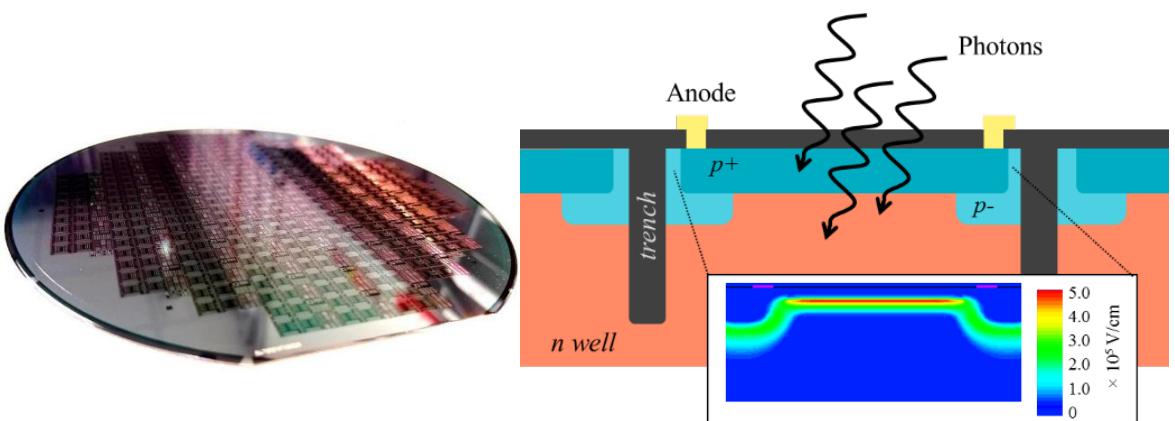
TSMC CMOS readout

# Development of the 3DdSiPM Technology: The SPAD Array and the 3D Vertical Integration Process

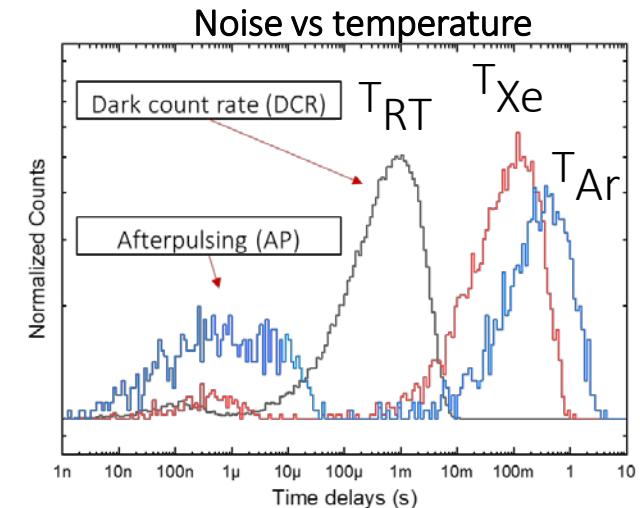
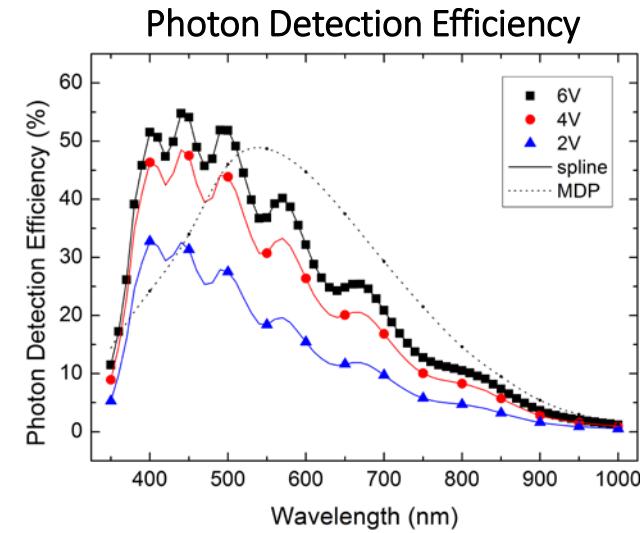
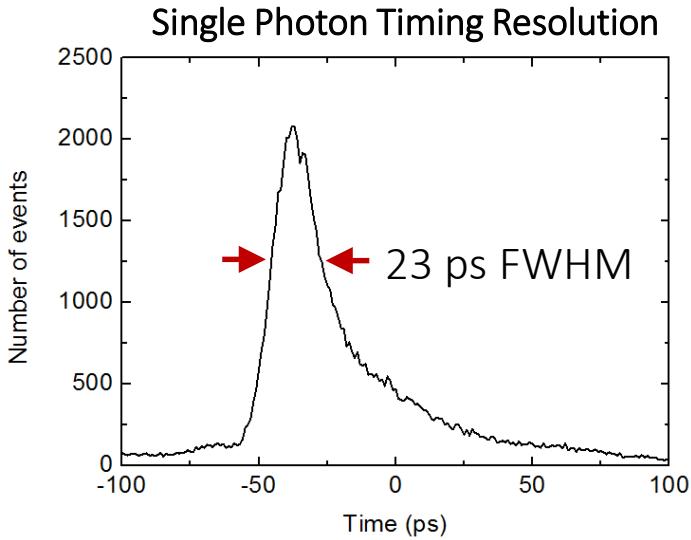
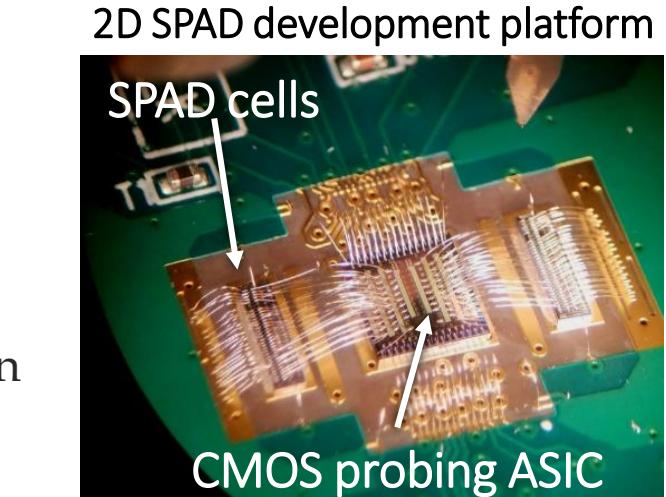


# Review: 2D SPAD characterization

- 150 mm wafer (custom process using DALSA CCD production line)
- 1x1 to 5x5 mm<sup>2</sup> SPAD array
- 50-100  $\mu\text{m}$  diameter **front-side illuminated** shallow P+N type SPAD ( $\sim 0.4 \mu\text{m}$  depth)
- 4  $\mu\text{m}$  width / 22  $\mu\text{m}$  depth optical/electrical isolation trench (highly doped polysilicon filling)
- 2D process for SPAD development



Front-side illuminated  
shallow p<sup>+</sup>n type SPAD



# Enhancing VUV sensitivity



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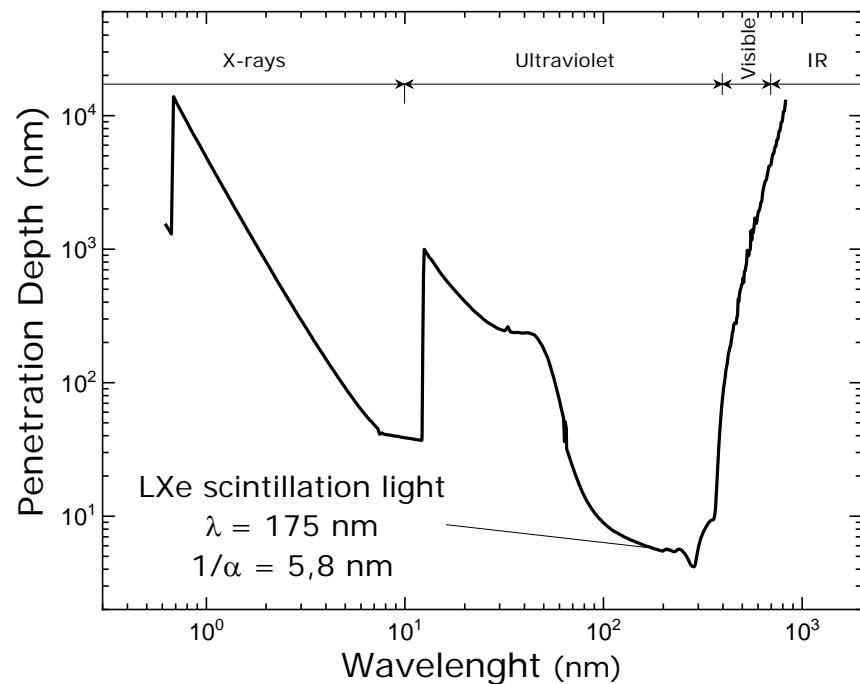
# Challenges of VUV direct detection

Very short penetration depth in Si

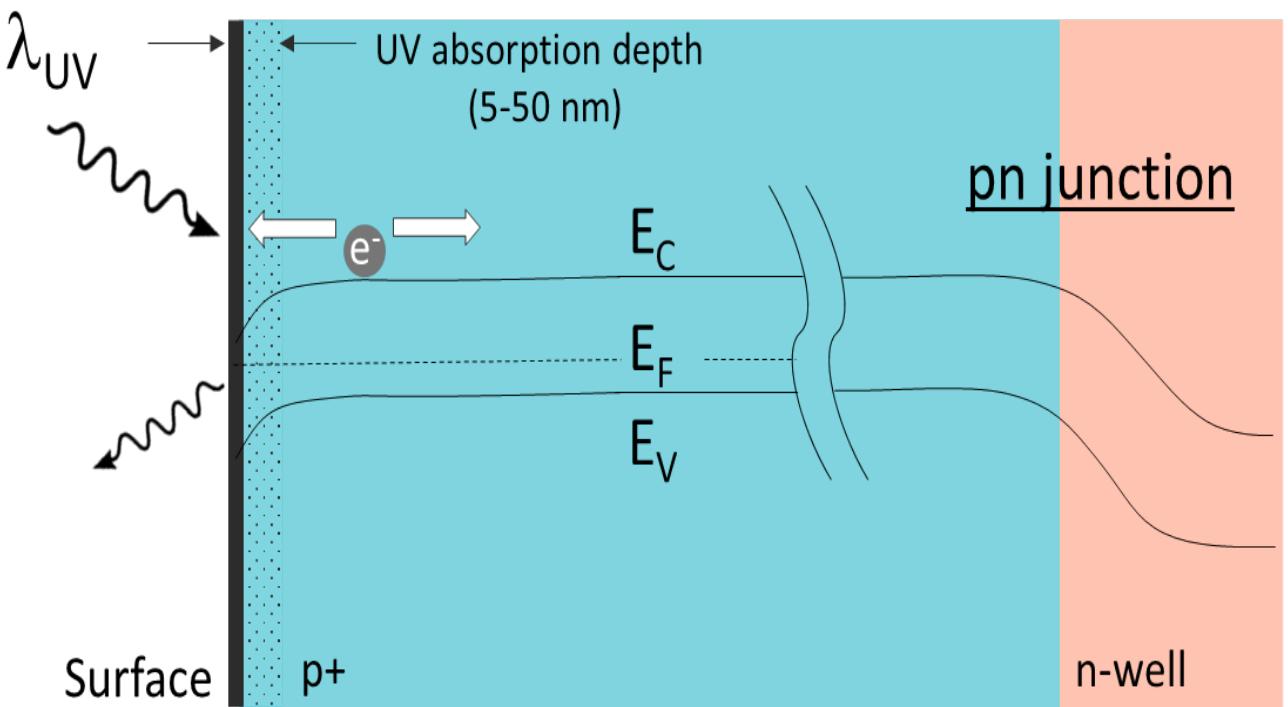
- Poor charge collection efficiency -> energy band engineering

Most passivation layers are absorbtive

- Poor surface transmission -> antireflective coating

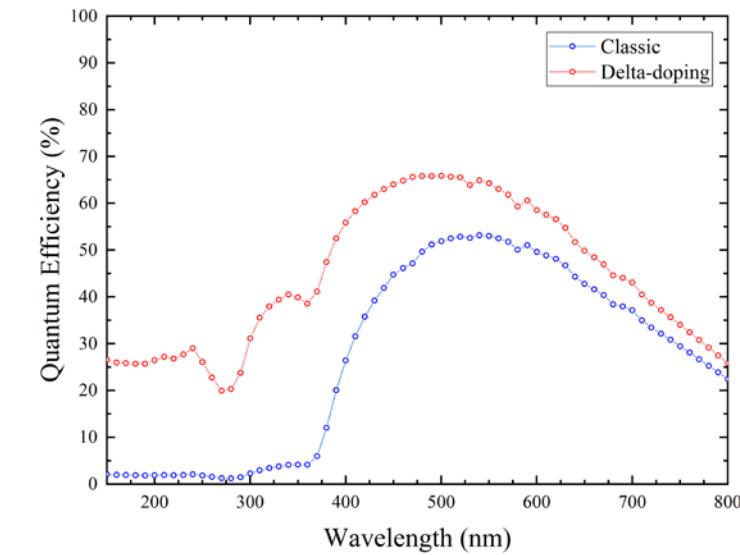
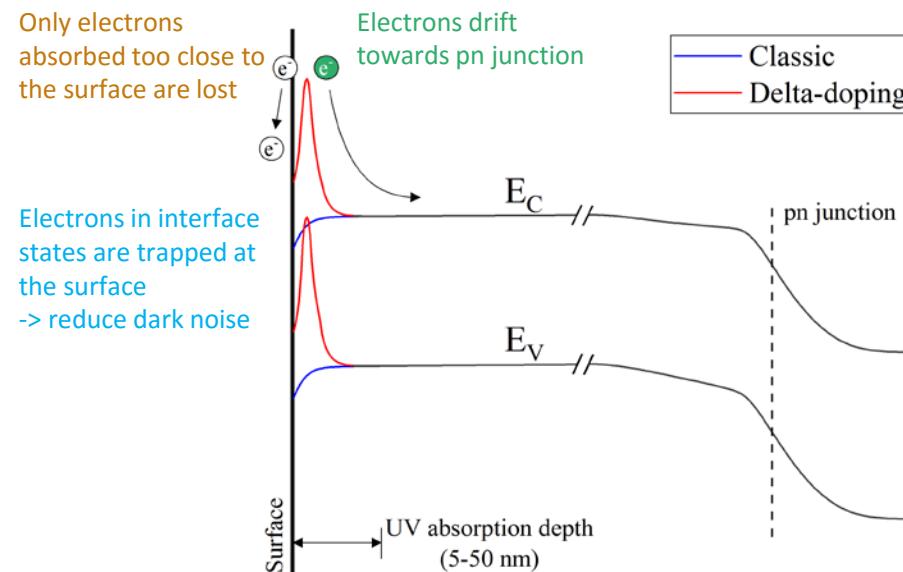
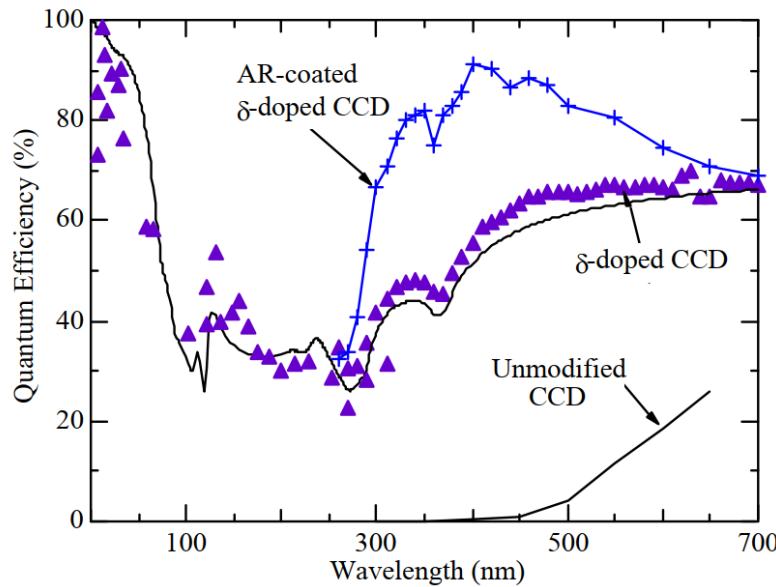


Energy band cross-section



# VUV sensitivity enhancement

- Delta-doping: surface energy band engineering to cause electron drift
- Increase internal quantum efficiency ( $\sim 100\%$  IQE in CCDs  $\blacktriangle$ )
- Delta doping + anti-reflective coating ( $+$ ) : major PDE improvement in VUV range
- UdeS-TRIUMF-Lawrence Berkeley Lab collaboration « Towards high efficiency single VUV photon detectors »



*Delta-doped back-illuminated CMOS imaging arrays: progress and prospects.*  
M.E. Hoenk (In Infrared Systems and Photoelectronic Technology IV 2009)

Simulation of energy bands with delta-doping

Simulation of SPAD internal efficiency with delta-doping

# Development of the 3DdSiPM Technology: Microelectronic Readout Integrated Circuit for Low Power 3DdSiPM and Large Area Detectors



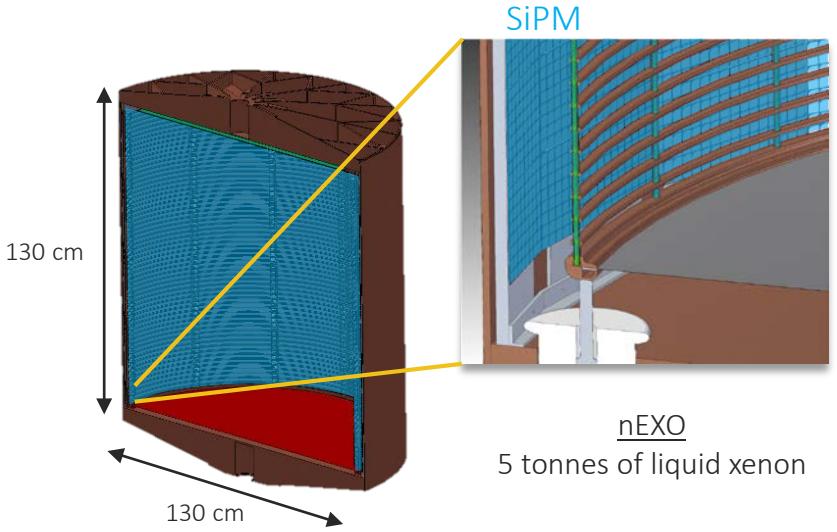
# Low-Background Experiments in LXe and LAr

nEXO : next Enriched Xenon Observatory

- Xenon scintillation : search for  $0\nu\beta\beta$  decay
- $\sim 4 \text{ m}^2$
- $\lambda = 175 - 178 \text{ nm}$
- Slow readout
- **Very low power < 100W**

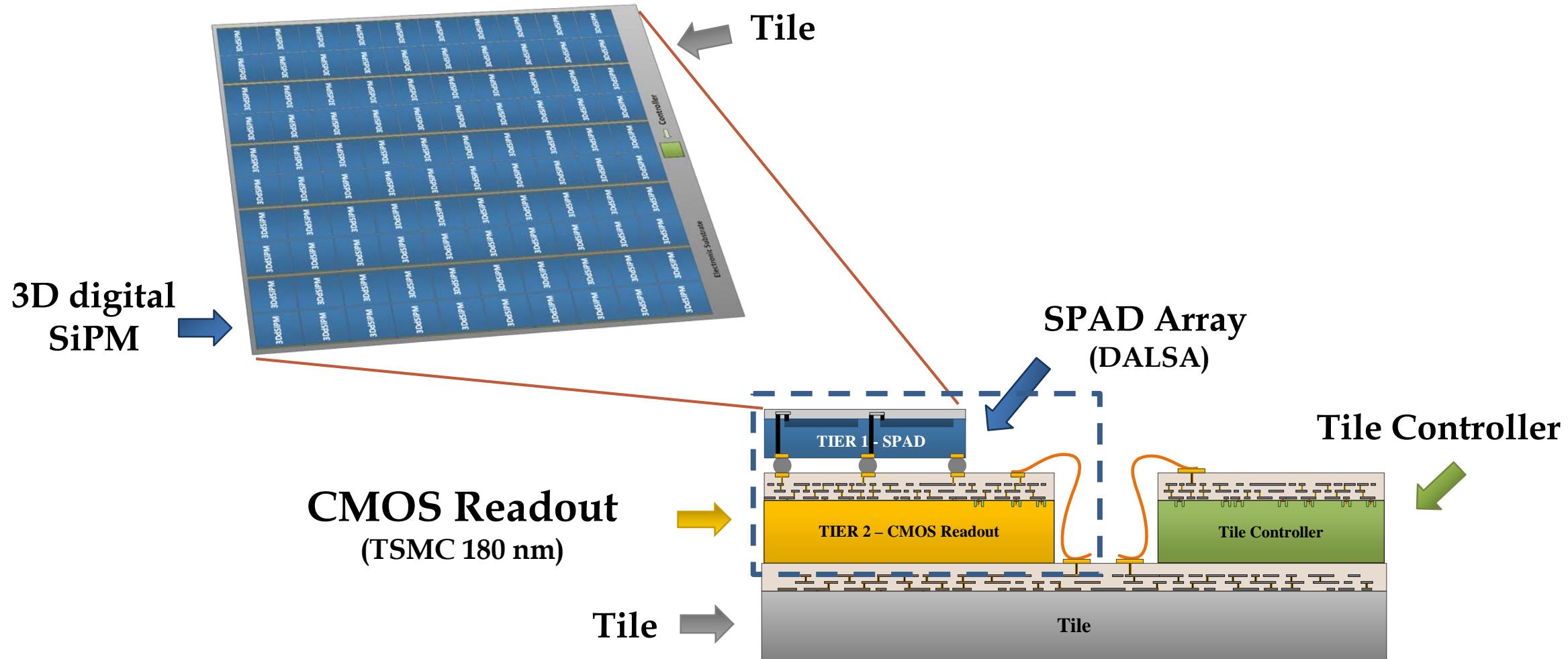
Dark matter Experiment using Argon Pulse-shape discrimination

- Argon scintillation : search for WIMP scattering
- $\sim$ hundreds of  $\text{m}^2$  (next generation)
- $\lambda = 128 \text{ nm}$
- PSD enabled
- Timing resolution < 250 ps (RMS)



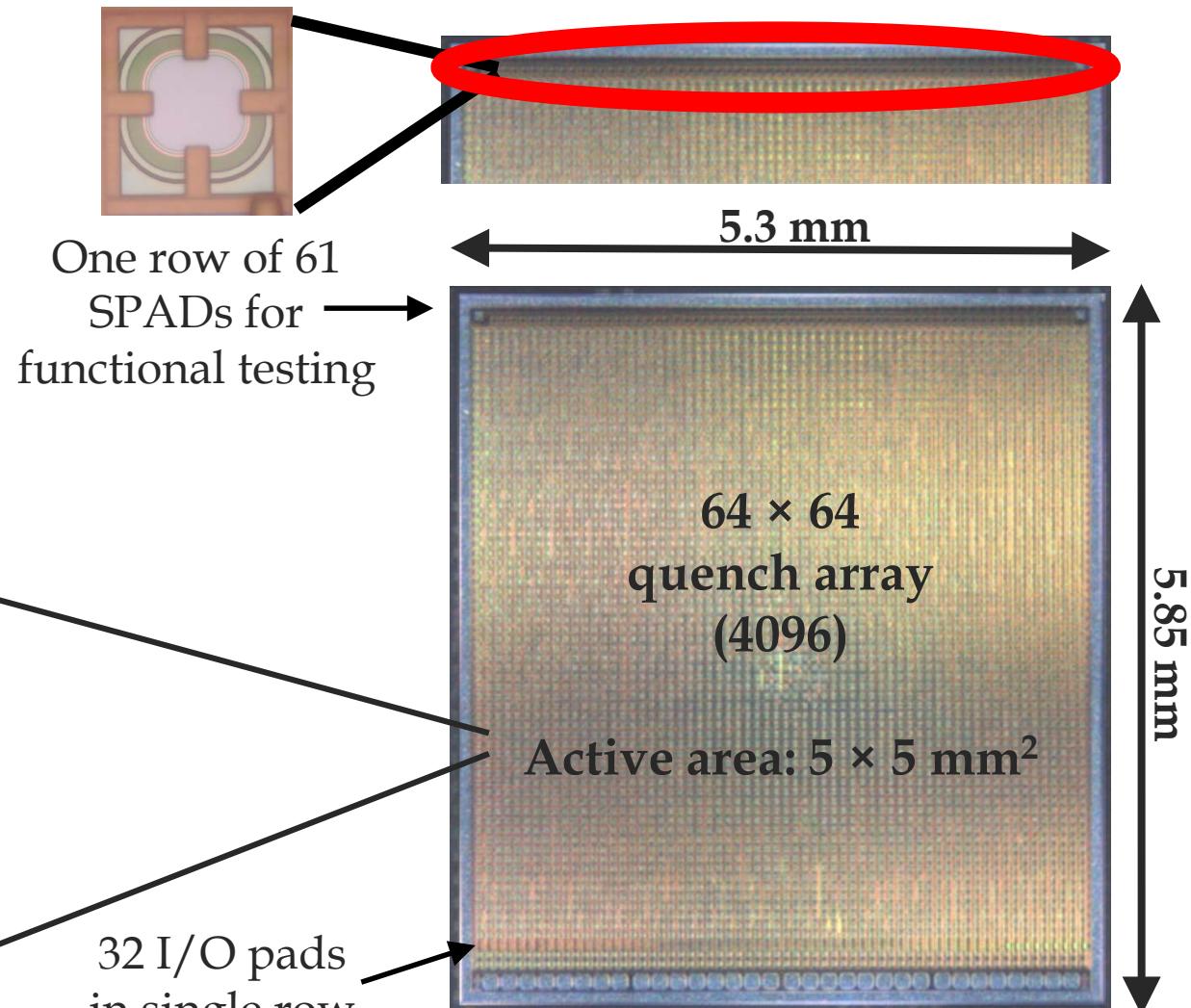
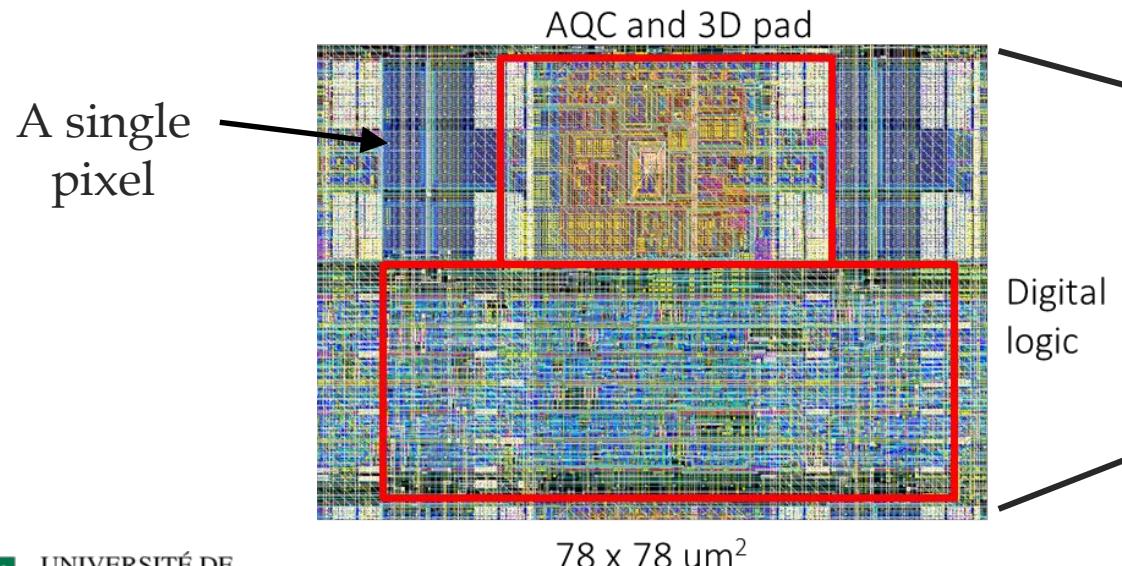
*nEXO Pre-Conceptual Design Report, 2018  
Design and Construction of the DEAP-3600 Dark Matter Detector, 2017*

# 3DdSiPM on a Tile with a Controller for Cryogenic Systems



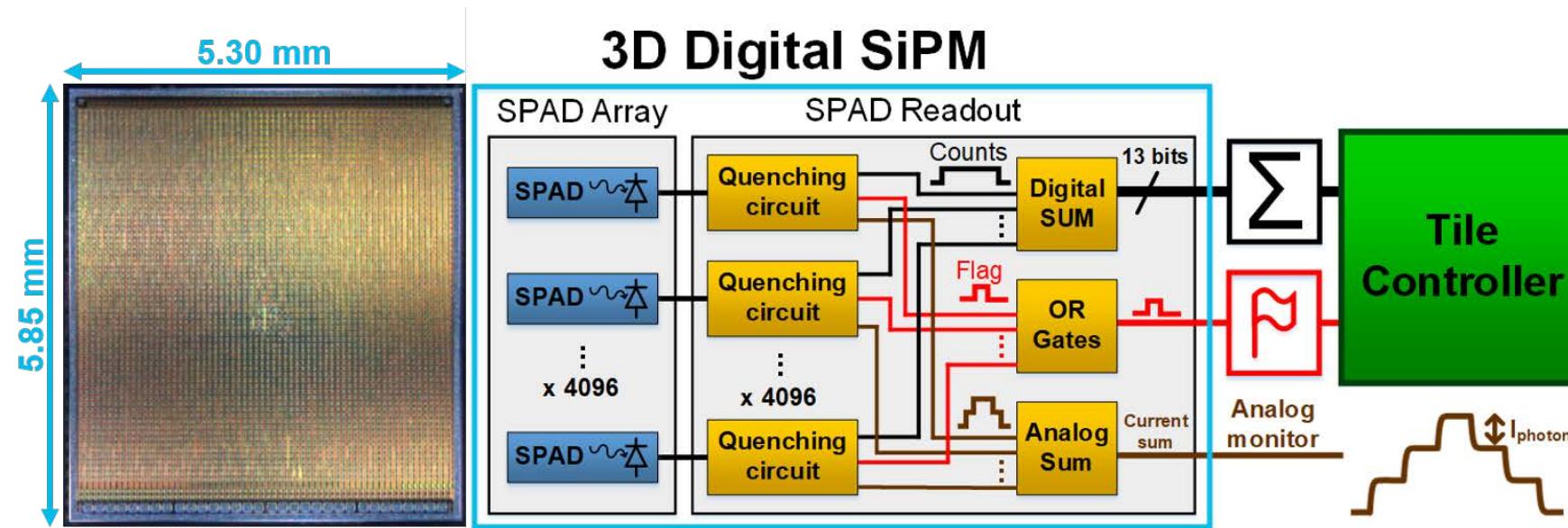
# CMOS Readout for 3DdSiPM – Overview

- TSMC 180 nm BCD process
- $5 \times 5 \text{ mm}^2$  active area
- $64 \times 64$  pixels (4096) – 61 SPAD
- $78 \mu\text{m}$  pixel pitch
- Digital-on-Top design flow



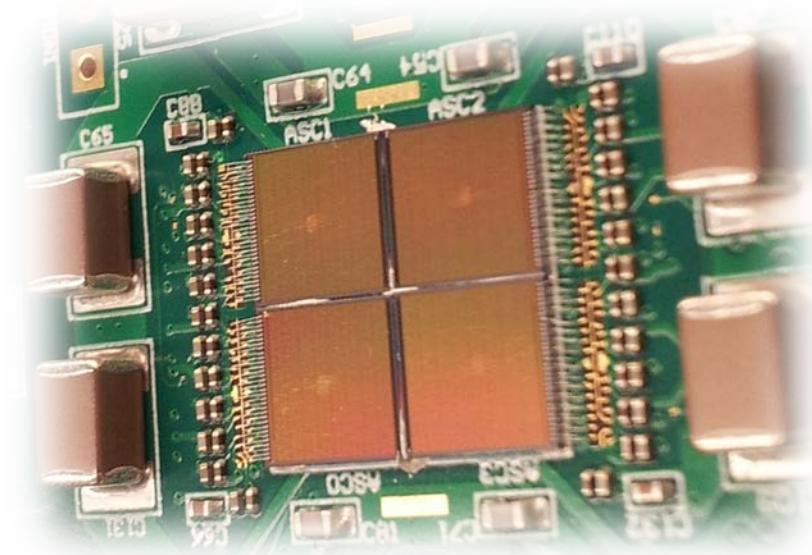
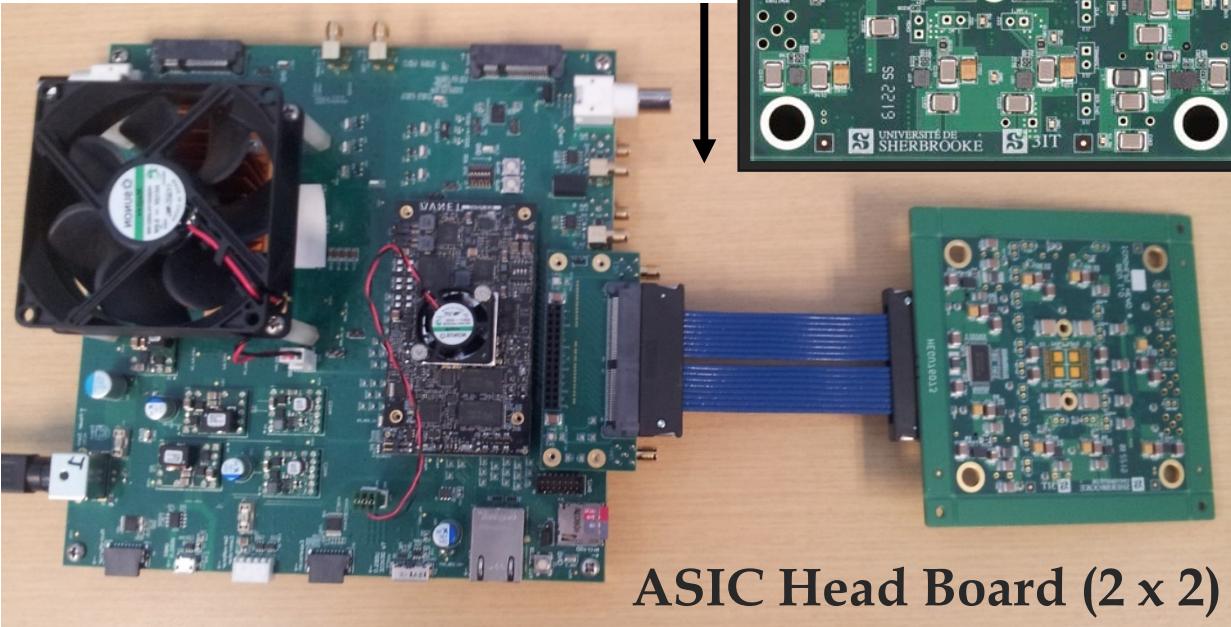
# CMOS Readout for 3DdSiPM – Low Power Architecture

- nEXO operation mode: **INTEGRATION**
  - Event driven: each 3DdSiPM signals the tile controller when a SPAD triggers
  - **Asynchronous (no event no clock - low power)**
  - Integration time from 10 ns to 1  $\mu$ s
  - Transmission of total counts (over integration time) when requested by the tile controller
  - Analog monitor for demonstration
- LAr operation mode: **CONTINUOUS SAMPLING**
  - Synchronous operation by a clock
  - Flags the controller to signal counts
  - Low flag jitter (<250 ps) to allow time-of-flight
  - 128 FIFO depth for transmission on request
  - Sampling bins: short (10 ns) and long frames (1  $\mu$ s) to allow PSD (Pulse Shape Discrimination)



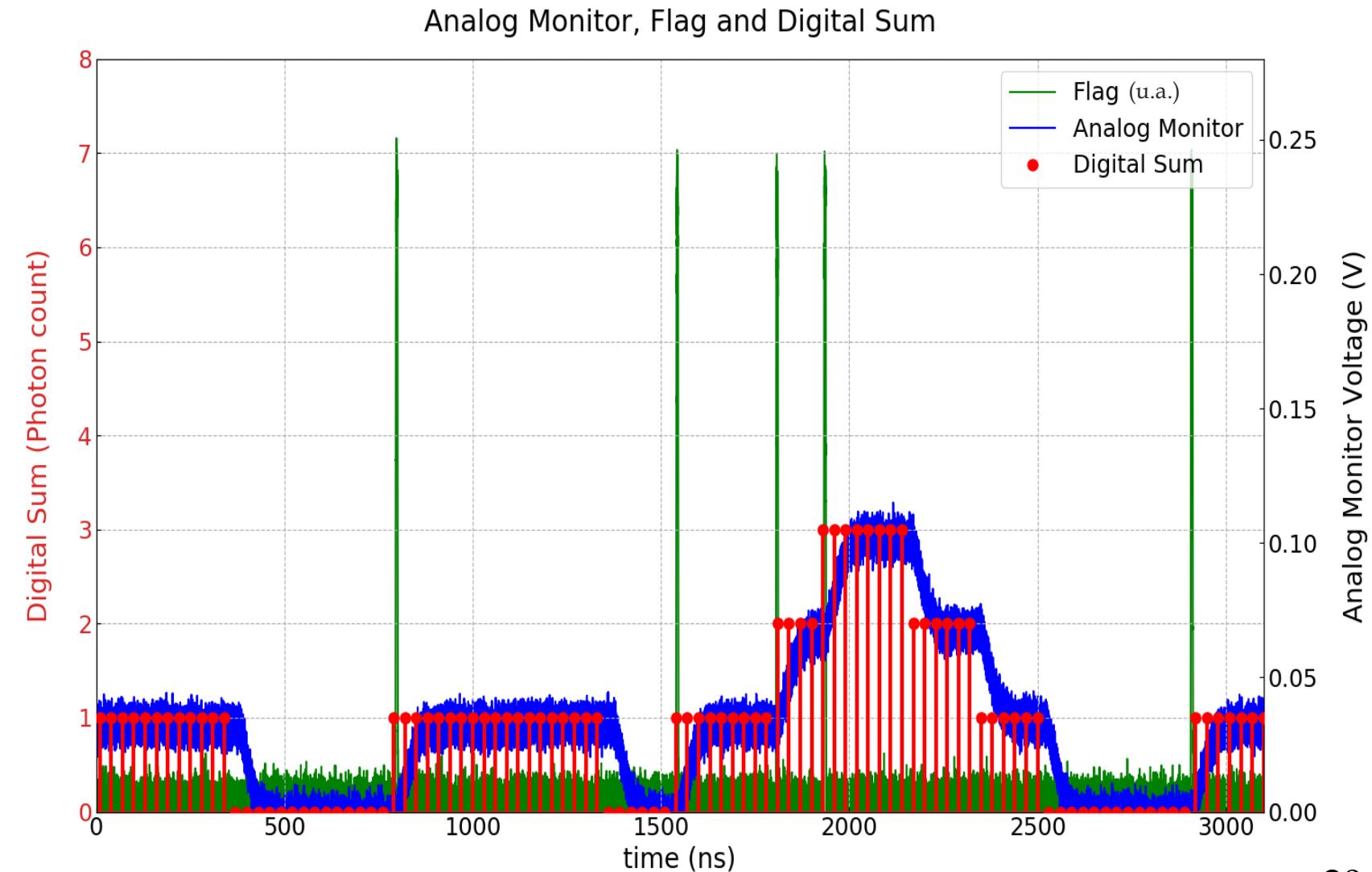
# Measurement Testbench - Toward Tile Integration

**Tile Controller:**  
UltraZed-EG SOM Board  
(ARM + FPGA)



# CMOS Readout - Flag, Digital Sum and Analog Monitor Corroborated

- ADC like acquisition
    - Number of pixels triggered at the moment of the acquisition
  - Flag signals every detected event
  - Analog monitor confirms the digital output
- 22.4 W / 4 m<sup>2</sup>**

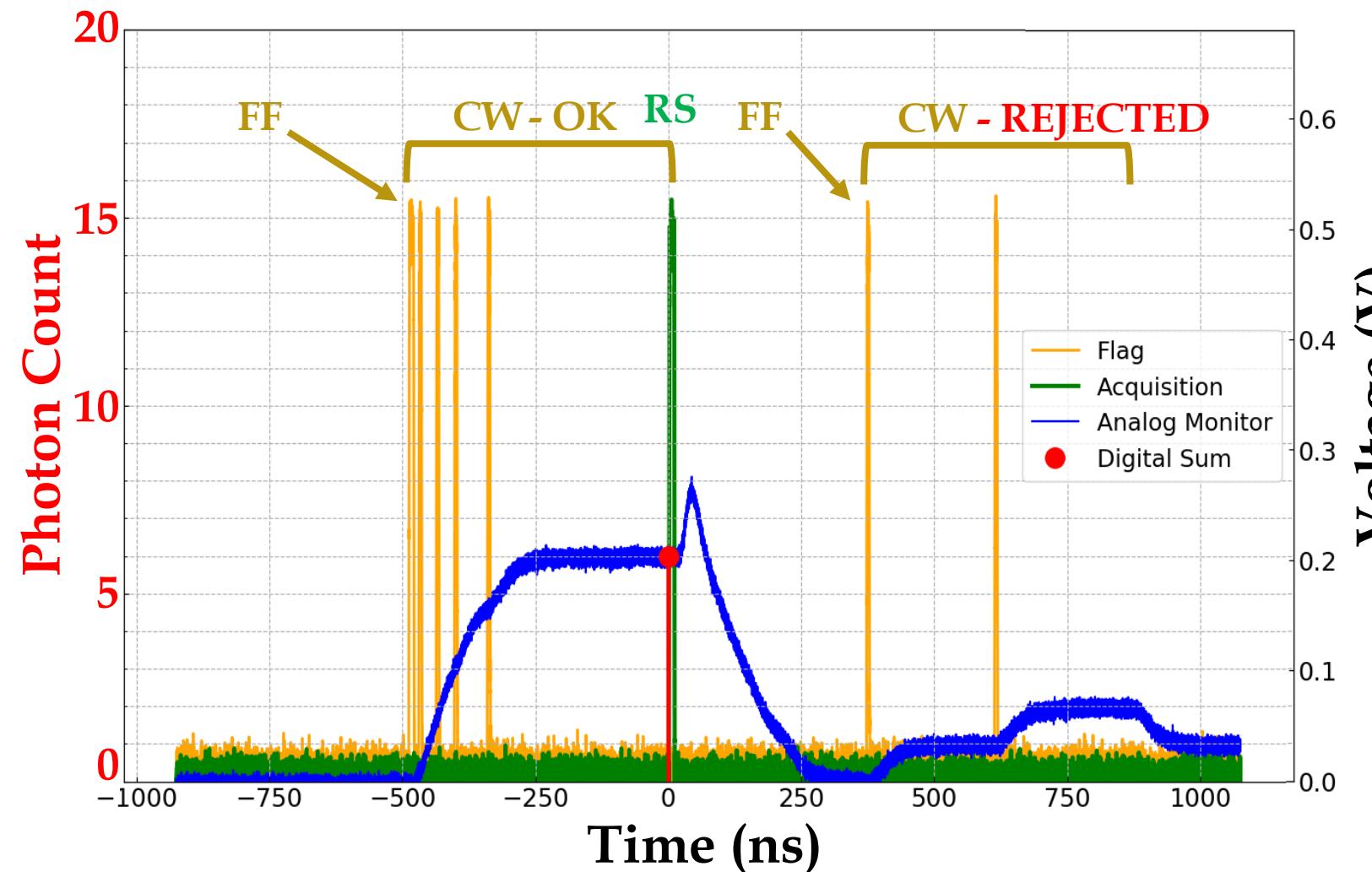


# next Enriched Xenon Observatory



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# nEXO - Single Sample Acquisition (Measurements)



Input source: green LED (565 nm)

SML-LX15GC-RP-TR

LED on for 100 ns

Pulse duration set to ~500 ns

Coincidence implemented in FPGA

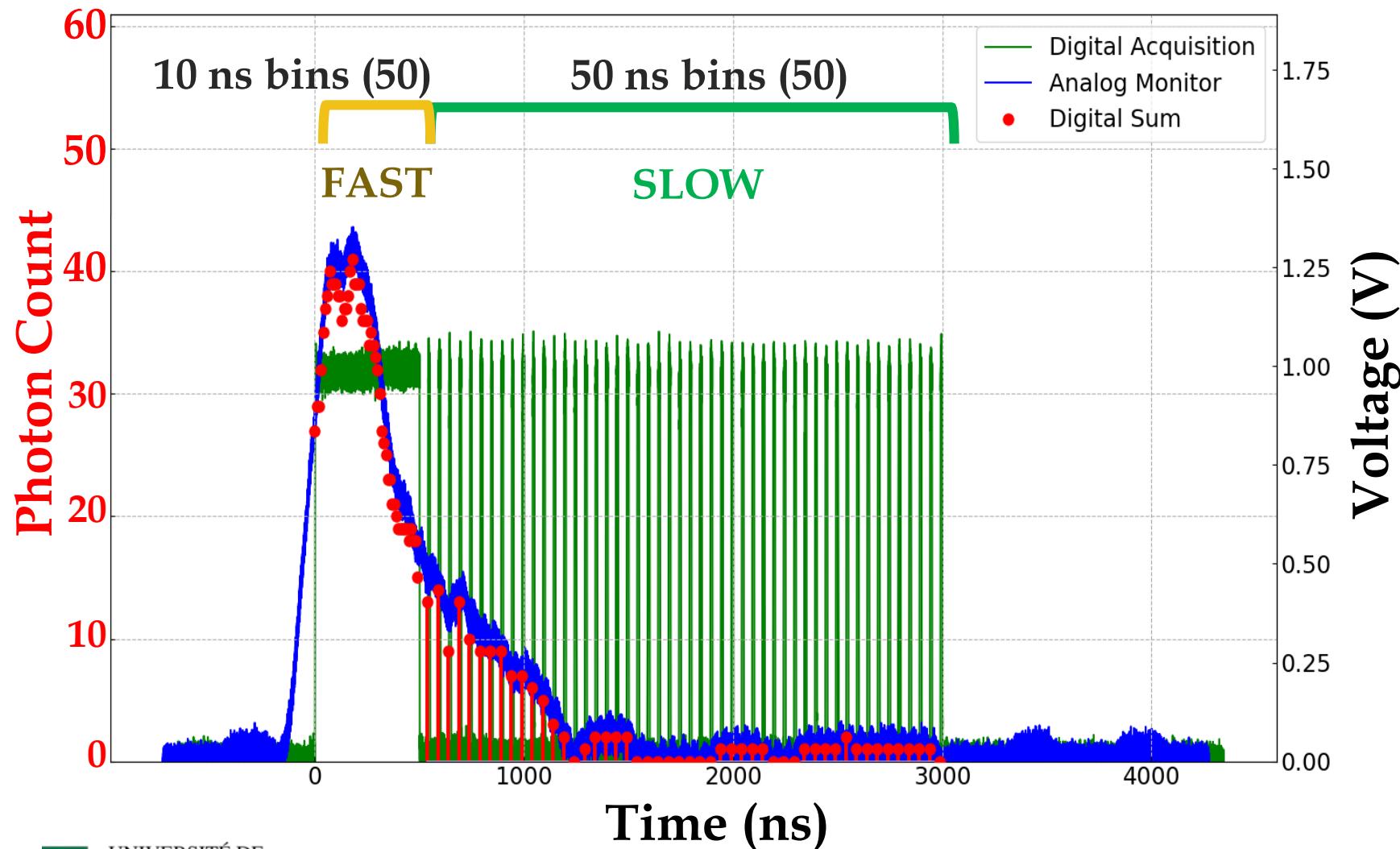
1. LED Flash → First Flag (**FF**)
2. Coincidence Window for 500 ns (**CW**)  
(Flags + Analog Monitor)
3. More than 3 Flags, start a read (**OK**)
4. Reading the Sum (**RS**)
5. First Flag (**FF**)
6. Coincidence Window for 500 ns (**CW**)
7. Less than 3 Flags (**REJECTED**)
8. Event considered as noise  
and rejected

# Pulse Shape Discrimination in Liquid Argon



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# PSD in LAr – Time Binning in Frames (Measurements)



Input source: green LED (565 nm)  
SML-LX15GC-RP-TR  
LED on for 200 ns  
Pulse duration set to  $\sim$ 500 ns  
Coincidence implemented in FPGA

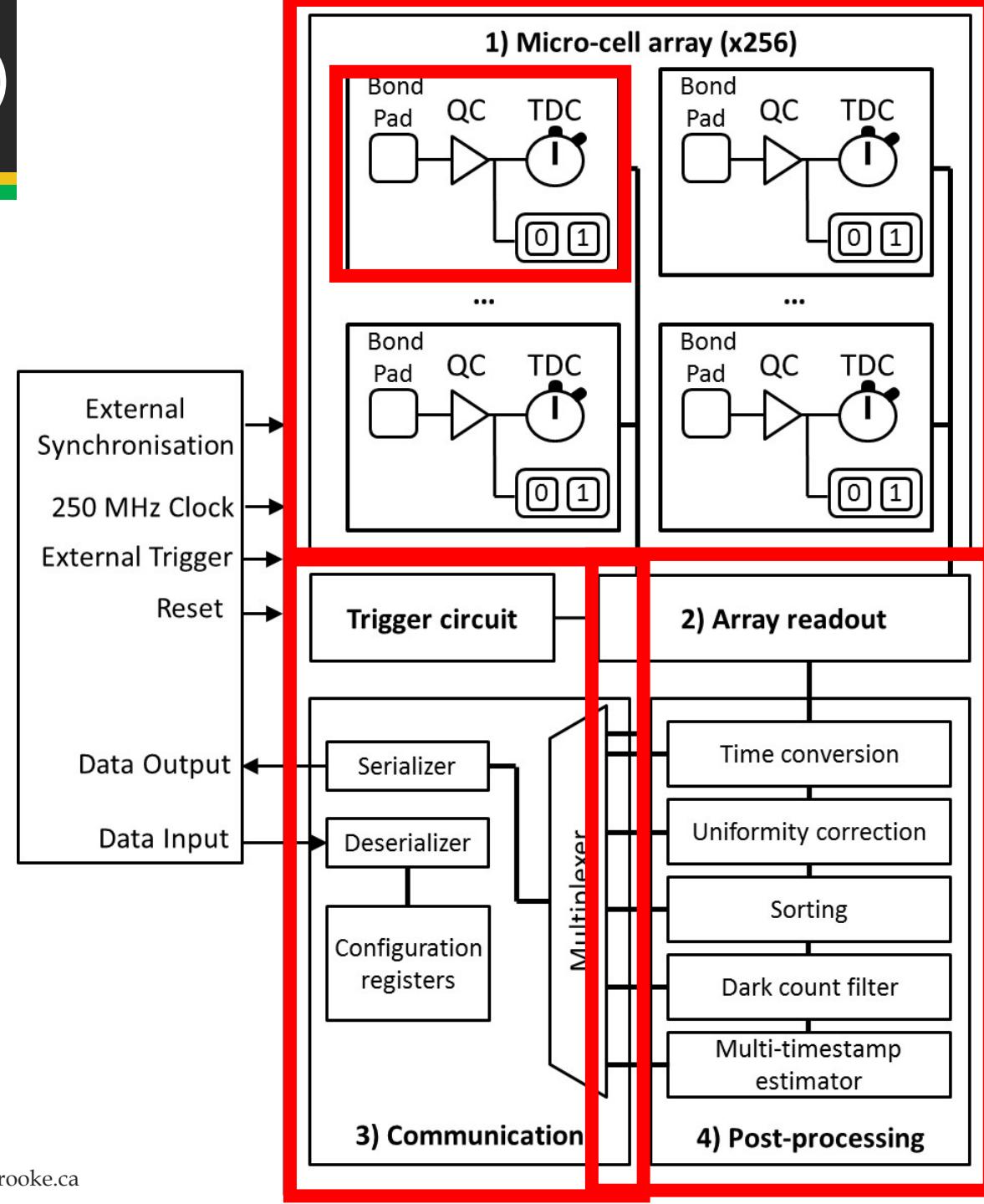
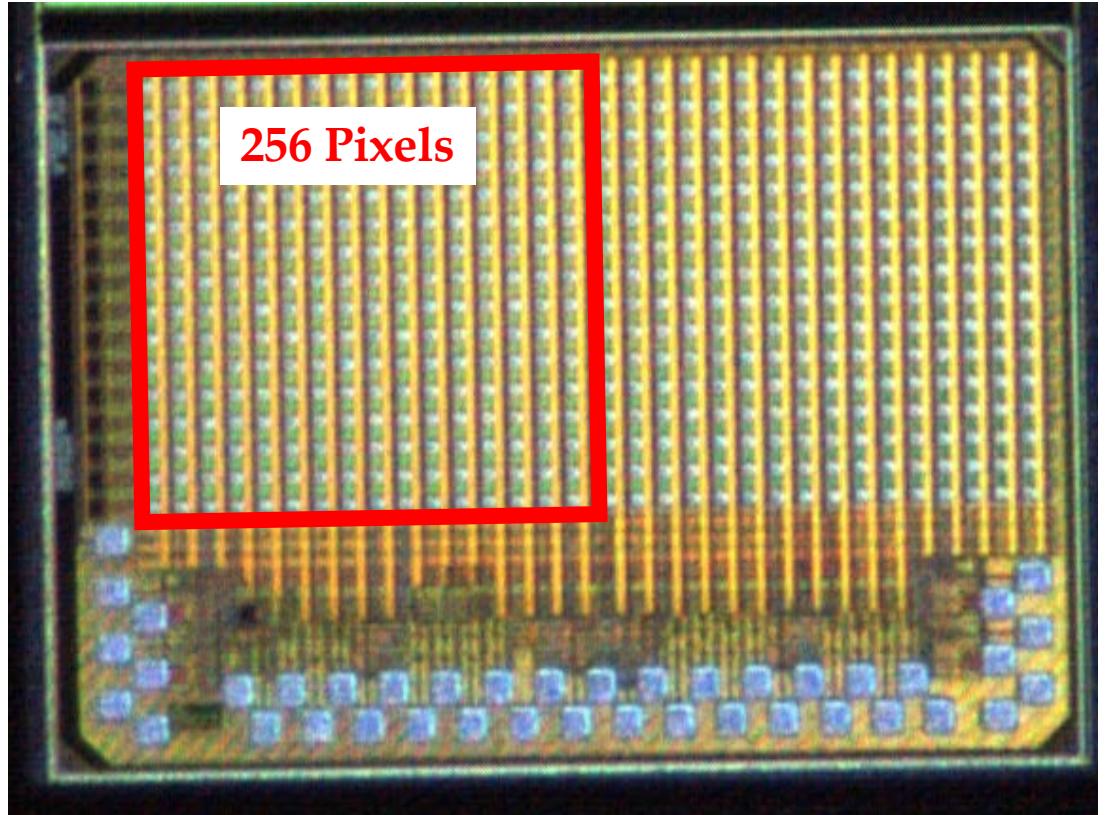
1. Sampling firsts photons with a 10 ns period
2. Sampling the decay with a 50 ns period
3. Counts are stored into the ASIC FIFO then transmitted to the controller

# Development of the 3DdSiPM Technology: Microelectronic Readout Integrated Circuit for Precise Single Photon Timing Resolution (sub 20 ps)

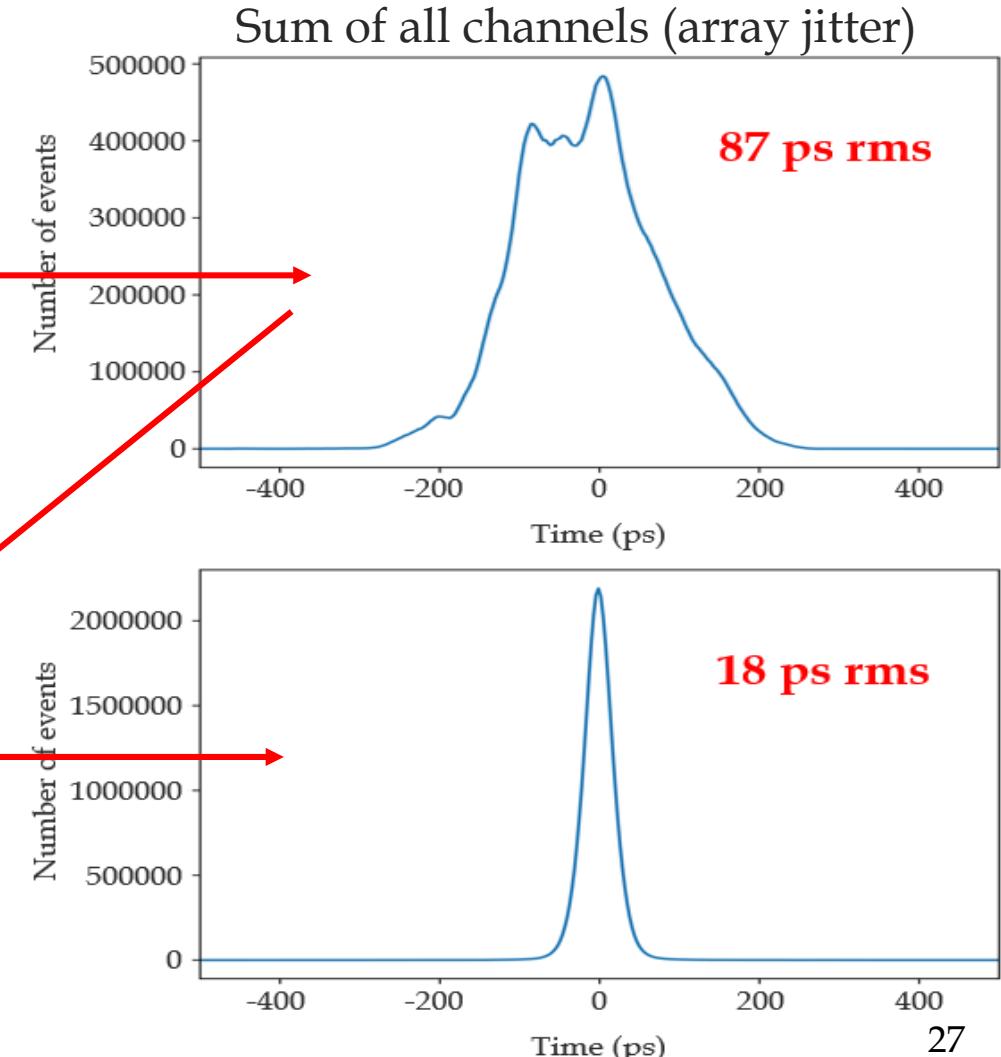
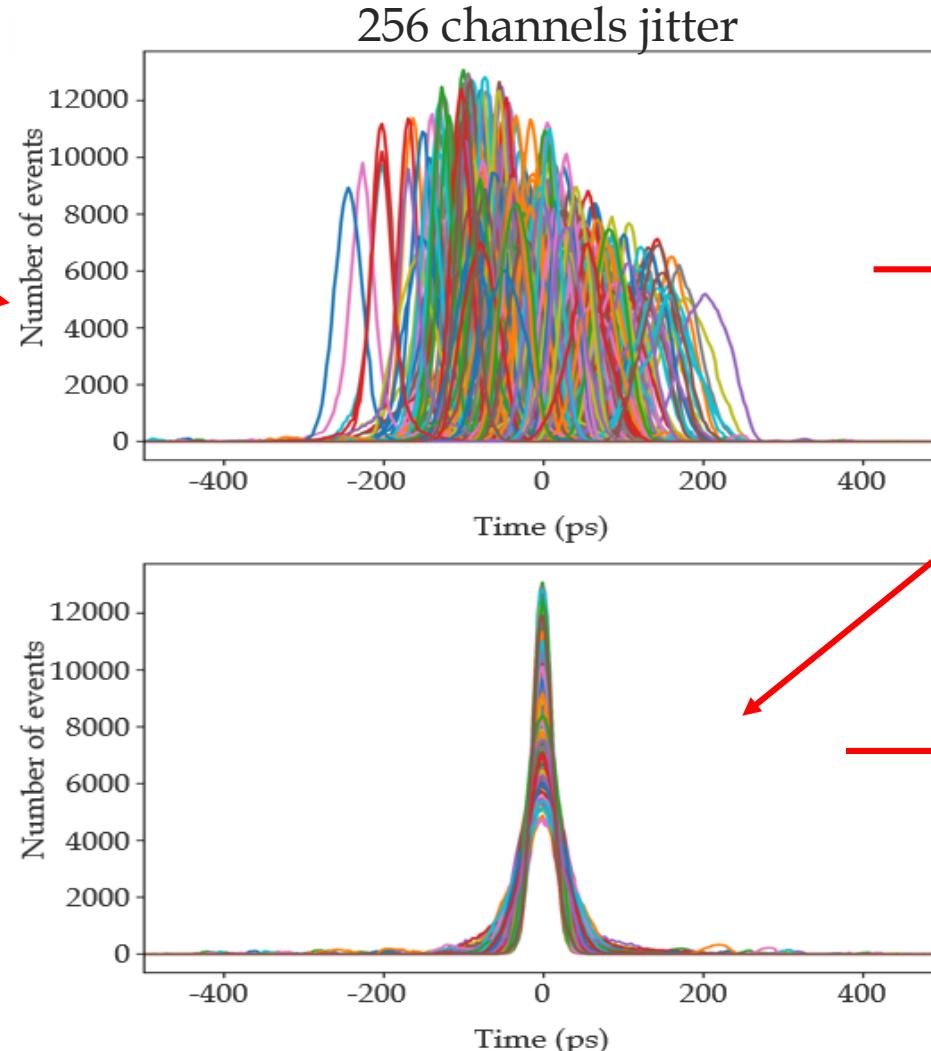
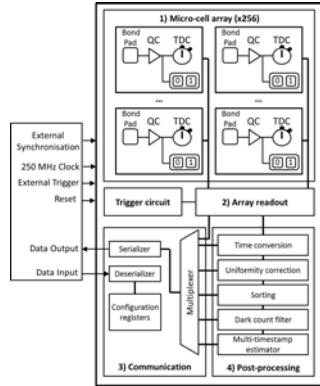


# ASIC Overview (originally for PET)

- TSMC 65 nm CMOS (GP)
- $16 \times 16$  pixels in  $1.1 \times 1.1 \text{ mm}^2$  (red box)

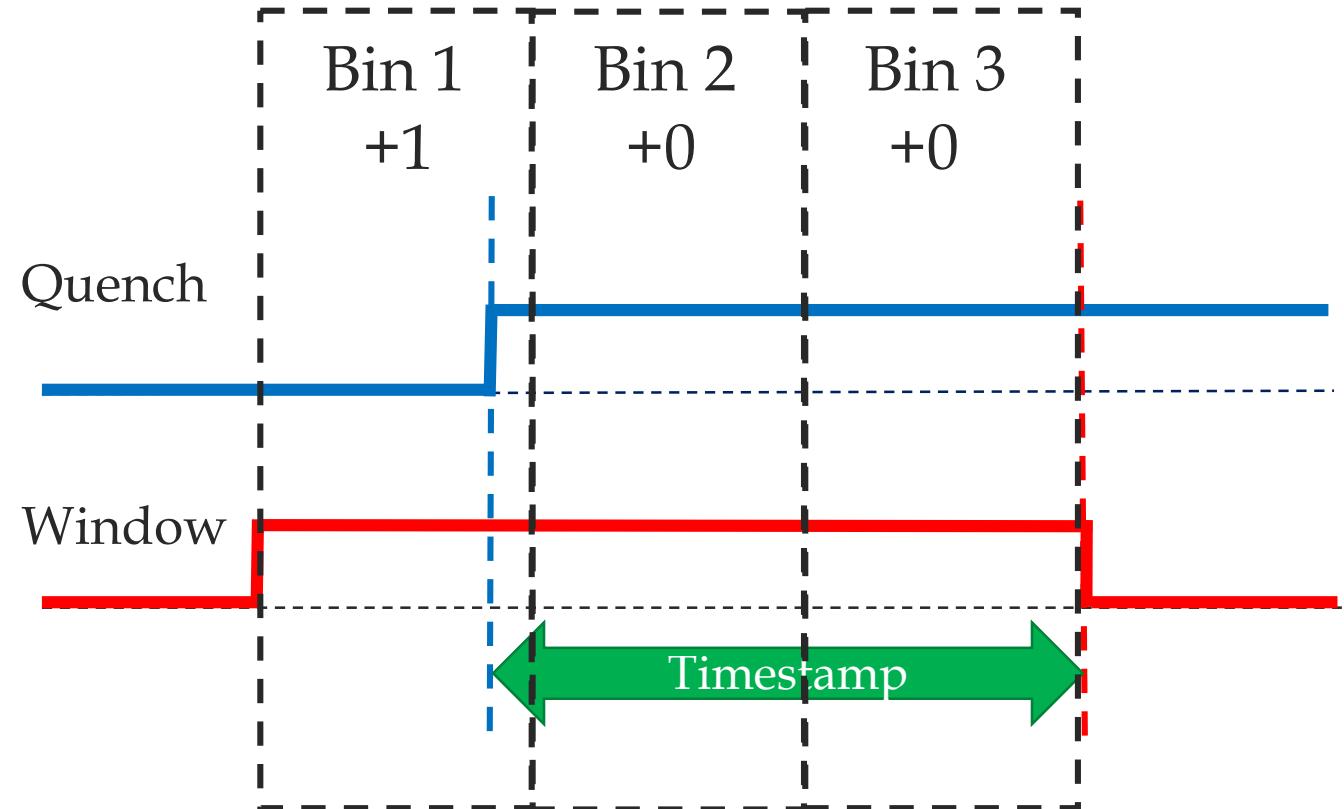


# Embedded Digital Signal Processing Example: Uniformity Correction



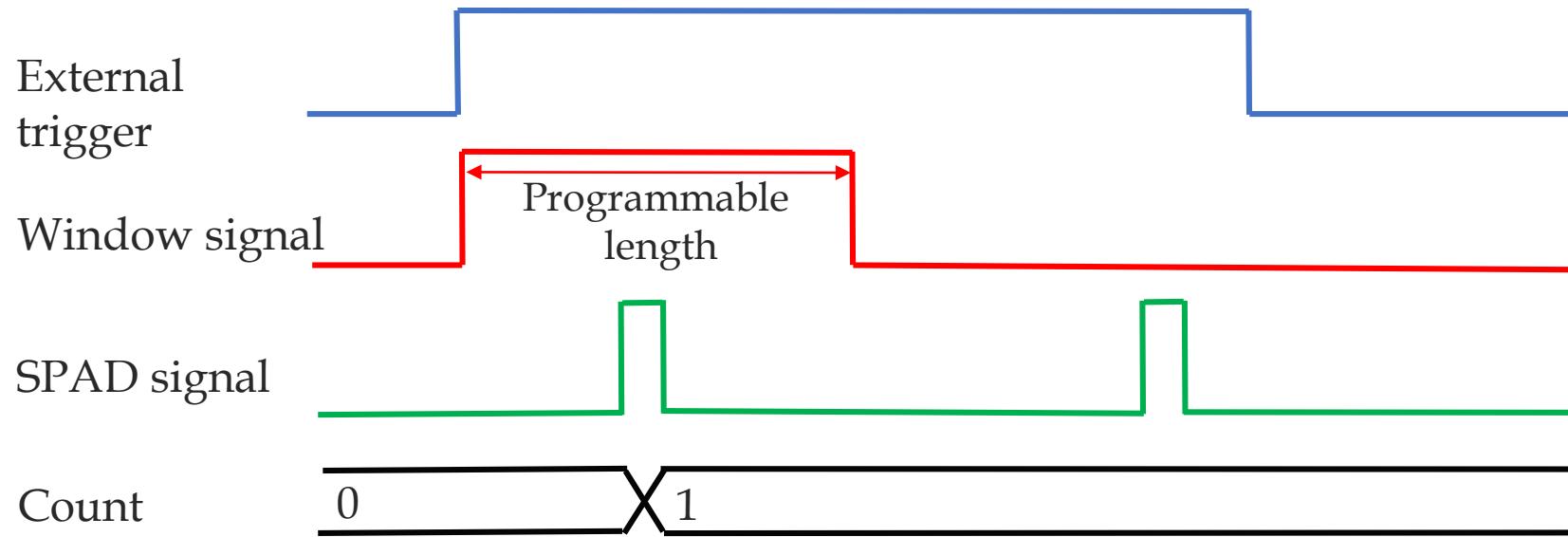
# New Functionalities: Time binning

- Count the number of events that fall within certain windows of time (histogram)
- Done on-chip to reduce readout time
- Number of bins can be adjusted



# New Functionalities: Gated Counting

- External signal triggering a detection window
- Programmable window length (100 ps – 4 ns)
- Count events that occurred during a window

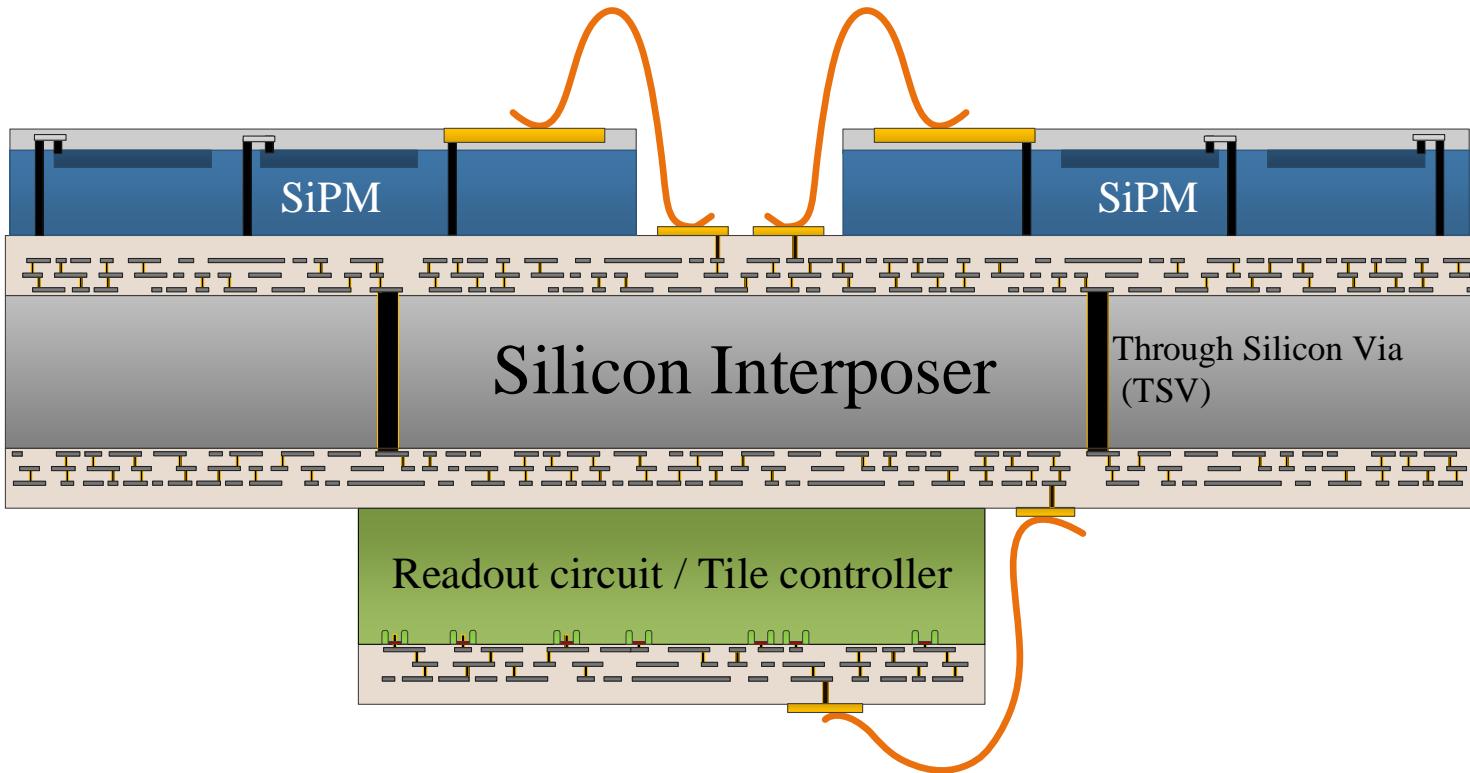


# Silicon Interposers for Cryogenic Detectors



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# Interposer requirements



- $5 \times 5 \text{ cm}^2$  to  $10 \times 10 \text{ cm}^2$
- Long transmission lines:  
Detector to Readout
- Low resistivity, low capacitance
- Analog and Digital lines
- Unknown # of layers

# Sherbrooke – IZM Fraunhofer Berlin Collaboration

World's leading institutes in

- Applied research and development
- System integration

Flexible cooperation models

Industry-compatible high-tech equipment

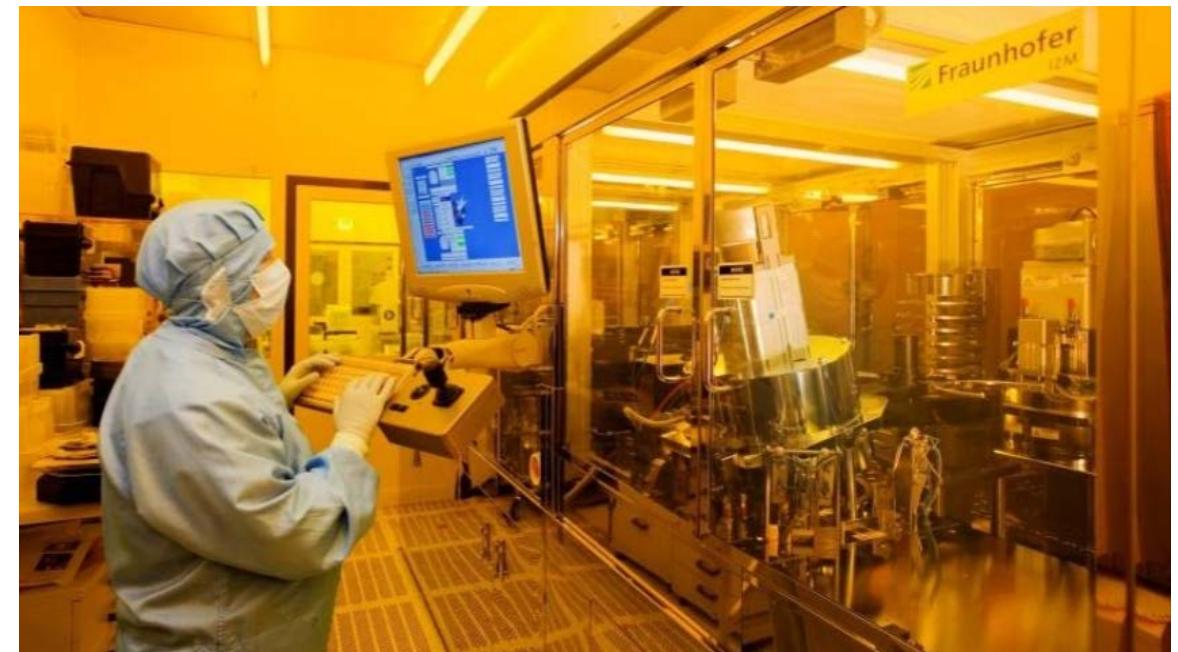
System Integration & Interconnection  
Technologies

RF & Smart Sensor Systems

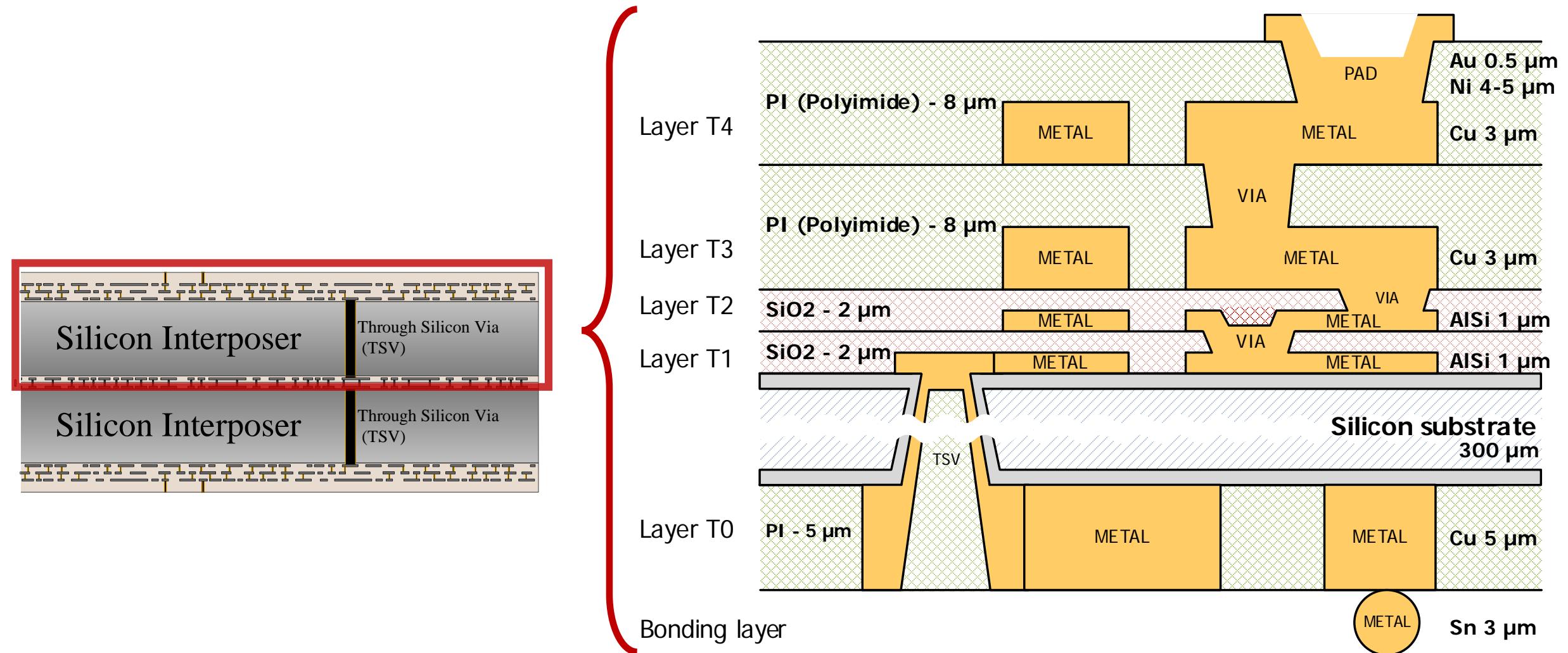
**Wafer Level System Integration**



**Institute for Reliability and Microintegration**



# Selected architecture - collaborative work with IZM



# Conclusion

- No fundamental limitation to build 3D digital SiPM, but it is a great engineering challenge.
- First 3D Digital SiPM expected in 2020.
- SPAD array, 3D integration and readout electronics developed and optimized in parallel.
  - Microelectronics readout soon ready for wafer level production.
  - SPAD R&D as fast as we can within Teledyne-DALSA.
- (We are recruiting! Ph.D. and postdoc.)
- In parallel with particle physics instrumentation, electronic readout for:
  - Positron Emission Tomography (PET) aiming at sub-10 ps FWHM coincidence timing resolution.
  - Photon gating Computed Tomography (CT) scanner.
  - Quantum key distribution.

# A team's work

## Université de Sherbrooke

- Serge Charlebois
  - Réjean Fontaine
  - Roger Lecomte
  - Henri Dautet
  - Julien Sylvestre
  - David Danovitch
  - Caroline Paulin
  - Catherine Pepin
  - Danielle Gagné
  - Étienne Paradis
  - Étienne Grondin
  - Konin Koua
  - Simon Carrier
  - Philippe Martel-Dion
  - Valérie Gauthier
- Nicolas Roy
  - Frédéric Nolet
  - Samuel Parent
  - Audrey Corbeil Therrien
  - Benoit-Louis Bérubé
  - Marc-André Tétrault
  - Frédéric Vachon
  - Tommy Rossignol
  - Gabriel St-Hilaire
  - Jacob Deschamps
  - Xavier Bernard
  - Thomas Dequivre
  - William Lemaire



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FIRST**  
RESEARCH  
EXCELLENCE  
FUND

**APOGÉE  
CANADA**  
FONDS  
D'EXCELLENCE  
EN RECHERCHE

## Collaborators

- Paul Lecoq
- Fabrice Retiere
- nEXO Collaboration
- nEXO Canada
- Simon Viel

## Teledyne-DALSA Semiconducteur Inc

- Claude Jean (CEO)
- Stephane Martel
- Robert Groulx



Arthur B. McDonald  
Canadian Astroparticle Physics Research Institute



Regroupement Stratégique  
en Microsystèmes du Québec



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Back up / clean up

# Publications

- A.C. Therrien; W. Lemaire; P. Lecoq; R. Fontaine; J.-F. Pratte. (2018). Energy discrimination for positron emission tomography using the time information of the first detected photons. *Journal of Instrumentation*. 13(1): p01012.
- Nolet, F.; Parent, S.; Roy, N.; Mercier, M.-O.; Charlebois, S. A.; Fontaine, R. ; Pratte, J-F. (2018). Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution. *MDPI - Instrument - Special Issue Advances in Particle Detectors and Electronics for Fast Timing*. 2(4)
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- Tetrault, M.-A.; Lemaire, W.; Corbeil-Therrien, A.; Fontaine, R.; Pratte, J.-F. (2017). TDC Array Trade-Offs in Current and Upcoming Digital SiPM Detectors for Time-of-Flight PET. *IEEE Trans. Nuclear Science*. 64(3): 925-932.
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- Nolet F, Rhéaume V-P, Parent S, Charlebois SA, Fontaine R, Pratte J-F. (2016). A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS with Low Output Capacitance. *IEEE Transactions on Nuclear Science*. 63(4): 2293-2299.
- Berube BL., Rhéaume V-P., Parent S., Maurais L., Corbeil Therrien A., Charlebois SA., Fontaine R., Pratte J-F. (2015). Implementation study of Single Photon Avalanche Diodes (SPAD) in HV CMOS 0.8  $\mu$ m technology. *IEEE Transactions on Nuclear Science*. 62(3): 710-718.
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- Tétrault M.-A., C. Therrien A., Desaulniers Lamy A., Boisvert A., Fontaine R., Pratte J.-F. (2014). Dark Count Impact for First Photon Discriminators for SPAD Digital Arrays in PET. *IEEE Transactions on Nuclear Science*. 62(3): 719-726.
- Tétrault M.-A., Desaulniers Lamy É., Boisvert A., Thibaudeau C., Dubois F., Fontaine R., Pratte J.-F. (2014). Real-Time Discrete SPAD Array Readout Architecture for Time of Flight PET. *IEEE Trans. Nucl. Sci.* 62(3): 1077-1082.