

#### Adrián Irles & Roman Poeschl (IJCLab CNRS/IN2P3) on behalf of the SiW-ECAL team

Slides and material from A. Gallas, A. Thiebault, D. Breton, J. Maalmi, J. Jeglot, Vincent Boudry, R. P, A.I. and many more







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#### **Outline**



- New Modules equipped with the new compact DAQ
  - 2 x FEV12
  - 2 x FEV11\_COB
- Adaptation of the FEV10/11 slabs to the new compact DAQ
- Adaptation of the FEV13 slabs to the new compact DAQ
- Cabling and mechanics
- Commissioning
- Beam Test 23/03 29/03 2020 at DESY
- Common beam test



#### 2 x FEV12 (1 500 um wafer glued in 2019, 3 more in 2020)

Both equipped with 16 Skiroc2a

- Threshold issue during 2019 → fixed (the ASU was equipped with a resistor to fix a threshold of the sk2 not needed by SK2a)
- Some issues appeared during the 2020 gluing of the first FEV:
  - Different glue (different viscosity)
  - Connectors were in place  $\rightarrow$  need of readaptation of the aspiration plate
  - New software for the robot → needed some tuning
  - Intrinsic difficulty of gluing wafers on a board with a wafer.

Result:

- Wafers slightly missaligned → the one near the connectors is 100-200um outside → need extra care for the connectivity.
- One wafer with only 90% of cells connected.
- The gluing of wafers in the second FEV12 was perfect (learning curve!)
- Both are operative (nice cosmics seen in all wafers)







## COB :-(

2 COBs with only on 500 um wafer each + 1 COB with only chips.

All equipped with Skiroc 2a.

- Very bad news!!
- Encapsulation with Globtopby Swiss company Hybrid lead to deformation of the COBs
- Most likely due to mechanical stress during curing of Globtop
  - At 140 C for 6 hours !!
- Boards are operational but unreasonable/impossible to glue more wafers
- Boards are still useful for technical tests
- ► Have to study "cold" Encapsulation after beam test





# Adaptation of the "old modules" to the compact DAQCALGO

- 10 short slabs based on FEV10/11 were produces
  - 7 of them tested in 2017
  - 6 of them operational in 2018
- Short slab description:
  - FEV +
  - + 16 CHIPs (all Skiroc 2)
  - + 4 wafers (all 320 um)
  - + SMBv4 (adaptor card) connected with thermically soldered kapton connectors
  - + a long HV kapton (glued to the wafer)
  - All embedded in a carbon frame

- Process of adaptation (phase 1):
  - Disconnect the SMBv4
  - Clean the pads + add new Gradcon connectors
  - Unglue the HV kapton.



# Adaptation of the "old modules" to the compact DAQCADG

- Process of adaptation (phase 2):
  - Solder Gradconn/Antelect female connectors
  - Reconnect the HV kapton (short sheet designed for the compact DAQ) \*\*
  - Mount them in a new carbon frame adapted to the compact DAQ mechanical structure (see later)  $\rightarrow$  easy to dismount







\*\* Currently only in 5 slabs, the rest of the kaptons are still making 5<sup>th</sup> March 2020 | McGill University | CALICE Meeting



#### **Result of the process**



			DESY 2017		CERN 2018		2020	
	type	SLAB	Readiness	calibrated cells	Readiness	calibrated cells	Readiness	calibrated cells
1	FEV11	13		0%		0%		
2	FEV11	14		0%		0%		
3	FEV10	15		0%		0%		
4	FEV11	16		92%		?		
5	FEV11	17		93%		95%	travelling Japan – France	
6	FEV11	18		94%		?		
7	FEV11	19		93%		93%		
8	FEV11	20		94%		96%		
9	FEV11	21		54%		0%		
10	FEV11	22		84%		87%		
11	FEV10	23		0%		0%		

More details in the back-up slides

- ▶ 5 slabs recovered during the adaptation to the new compact DAQ.
  - Including the slab23 which was never connected to any adapter card.
- 2 slabs (16 and 18) have shown a reduction on the number of calibrated cells during 2018... is it the wafer partially disconnected from the ASU? (to be investigated)
- ▶ 11 FEV10/11 slabs in total  $\rightarrow$  All with 4 wafers of 320um

## FEV 13 integration with th SLBoard system

- ► An Interface card has been designed and produced.
- FW and software modifications needed (different routing of signals)
  - The realisation of these modifications before the beam test depends on the availability of engineers (busy with several a bit more urgent matters!)





#### **Design of the mechanical support**



Irène Joliot-Curie

ALICO

#### **Design of the mechanical support**







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#### **Design of the mechanical support: patch pannel**



Being cabled at the IJCLab (since 4<sup>th</sup> March)

5<sup>th</sup> March 2020 | McGill University | CALICE Meeting

#### **Mechanics: realisation**

- ▶ Up to 15 slabs with 2.1 mm tungsten.
  - + space for two more tungsten plates at the end/beginning.
- Patch pannel in the top.
- Support for the Core Module.
- ► Fan at the end for cooling of the electronics.
- Easy acces to the connectors











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## Commissioning

- Tools for debugging and commissioning:
- Automatic threshold scans performed with the DAQ
  - channel per channel or for several/all of them at the same time.
- Internal Calibration DAC integrated in the SLBoard
  - Allow for Hold scans and linearity checks
- Online monitoring tools
  - Charge (for all chips/channels/sca → easy masking procedure!)
  - BCID → coincidences searches
- Human readable configuration files

) Channels Hit Rate Scan Vs Threshold				-	- 🗆 ×
Star: Force Stop:	Min Common Threshold 400 600 200	Max Common Threshold 500600700 300	Nb of steps : ∰ 10 ⇒ 16 dac / Number of Cycles/ Step ∯ 5 Per	Save result in Save r	IFIIe Iodulo: 2 V at once
	CORE side Left SLAB 2 @2	ALL ASUs 🔹 ALL ASIC	All Channels	Display Color M	laps Panel:
72-					1
65- 00- 55- 50- 45- 1 45- 1 9- 45- 1 9- 9- 1 9- 9- 1 9- 9- 1 9- 1 9- 1 9		Or (pre-com	iline scurves Old plot missioning,	s no HV)	Skiroc 0 Skiroc 1 Skiroc 2 Skiroc 3
9 30- 25- 20-					Skiroc 4 Skiroc 5 Skiroc 6 Skiroc 7 Skiroc 8 Skiroc 9
15- 10- 5-					Skiroc 10 Skiroc 11 Skiroc 12 Skiroc 13 Skiroc 14
0-1- 180 185 190 195 200	205 210 215 220 225 230 235 240	0 245 250 255 260 265 270 : Threshold	275 280 285 290 295 300 305 310	o alis azo azis ado adis ado	Skiroc 15

#### **Commissioning: linearity**









- Semiautomatic procedure to calibrate sca 0-3 for all channels of all 15 SLABS
  - Low gain and high gain
- Possibility to compare pedestal with fit method with pedestal obtained with "hit bit = 0"

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#### **Commissioning: linearity**





Semiautomatic procedure to calibrate the hold of all chips





#### **TB2020 at DESY TB24 (last week of March)**

- 14-15 slabs integrated in the compact DAQ system.
- 4-6 FEV13 equipped with the legacy DAQ system at the back as a catch tailer
  - 4 FEV13 tested in 2018-19
  - 2 more in production



- **Program:** 
  - DAQ tests
  - MIP calibration of all modules → for future tests
  - Electromgnetic showers at different energies

#### ► A possible calorimeter layout

Layer number	Abs type bef.	mm	X0	X0 cumul.	Sh. Max /E	SLAB	REM :			
1	0	0	0	0.0		COB (¼×500)				
2	1	2.1	0.6	0.6		FEV11/10 (320)				
3	1	2.1	0.6	1.2		FEV13 (650)	Early : Alignment			
4	1	2.1	0.6	1.8		FEV11/10 (320)				
5	1	2.1	0.6	2.4		FEV11/10 (320)				
6	1	2.1	0.6	3.0		FEV12 (500)				
7	1	2.1	0.6	3.6	1.001	FEV11/10 (320)				
8	1	2.1	0.6	4.2	I Gev	FEV11/10 (320)				
9	1	2.1	0.6	4.8	3 COV	FEV12 (500)	500 µm @ core of shower			
10	1	2.1	0.6	5.4	3 Gev	FEV11/10 (320)				
11	1	2.1	0.6	6.0	6 GeV	FEV11/10 (320)				
12	1	2.1	0.6	6.6		FEV11/10 (320)				
13	1	2.1	0.6	7.2		FEV11/10 (320)				
14	1	2.1	0.6	7.8		FEV11/10 (320)				
15	2	4.2	1.2	9.0		FEV11/10 (320)				
16	2	4.2	1.2	10.2		FEV13 (320)	Comparison FEV11/13			
17	2	4.2	1.2	11.4		FEV13 (650)				
18	2	4.2	1.2	12.6		FEV13 (500)				
19	2	4.2	1.2	13.8		FEV13 (650)				
20	2	4.2	1.2	15.0		FEV13 (500)				
21	2	4.2	1.2	16.2		FEV13 (650)				
Тур	Type thickne 2.1 mm 0.6 X0									



#### **Common beam test**



- ▶ The AHCAL has beam time just the week before in the same beam area.
- Tests of common DAQ are foreseen (from the 19<sup>th</sup> March)
- The CCC shares the clock and the start acq between both systems.
  - We will have a fixed time offset, to be determined during data taking
- Modifications in both systems are needed to accept/distribute busy signals  $\rightarrow$  Ongoing activity (DESY/Prage/IJCLab)
- The EUDAQ implementation has been studied: it is feasible but will be postponed to after the beam test.



#### Summary



- ► We still have a couple of weeks of frenetic activities and then...
- In let the fun begin !



#### **Back-up**







#### FEV10/11 status

#### Historic (<2020)

- Slab 13 had problem with the adapter card (glue was spilled in it, affecting to the conductivity)
- Slab 14: Problem in the ASU (broken connexion between configuration lines)
- Slab 15: mistery! (it was operative during the first phase of the 2017 commissionig and then stopped... SMBv issue?)
- Slab 16 and 18 → we observed that some areas cannot be calibrated... deconnexion between wafer and ASU?
- Slab 21: unknown.
- Slab 23: it was never equipped with adapter card.

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9 FEV11	21		54%		0%		
10 FEV11	22		84%		87%		
11 FEV10	23		0%		0%		

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#### **SLAB 14: recovered for data taking**

- Slab not tested at DESY 2017 due to a problem of the Signal/Slow Control Return lines that blocked the readout.
- First slab used to test the "disassembly procedure" (November 2019)
- Satisfactory DAQ tests done by bypassing 4 chips.
- Status: slab fully recovered and commissioned → similar performance than the other FEV11s had during 2017



