SiW-ECAL: Retriggers

Yu Kato

The University of Tokyo

Special thanks to Vincent
for suddenly accepting speaker!

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katou@icepp.s.u-tokyo.ac.jp

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SiW-ECAL technological prototypes

Vincent Boudry, LCWS2019 Sendai

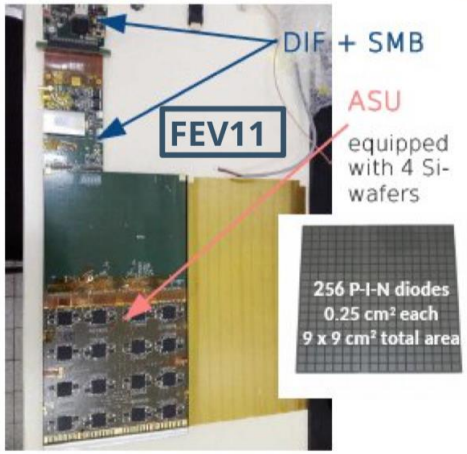
ASU: 12+ years of R&D

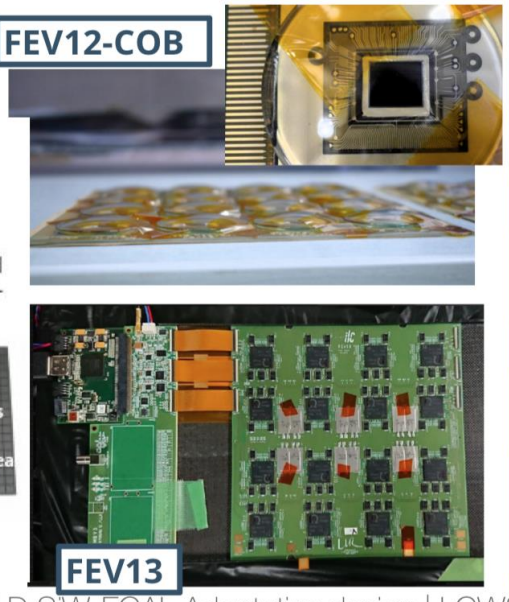
Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints

3 versions working

- with S/N_{Trig} ≥ ~12 (for 320µm)



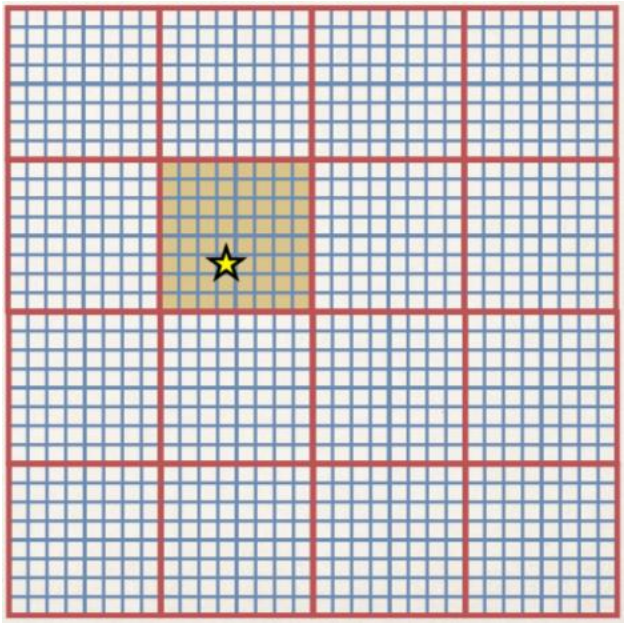


Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	Slab:FEV11	10 units, 320µm	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	10 SLAB: 5 FEV11 320µm 5 FEV13 650*µm Compact stack	SK2 & SK2a (⊃timing)	Improved S/N (1/64 masked ch.) Timing...
1st COB	2019	FEV12-COB	1 wafer, 500µm	S/N ~ 22

Vincent.Boudry@in2p3.fr ILD SiW-ECAL Adaptative design | LCWS

Data acquisition mechanism of SiW-ECAL

- **Geometrical structure**
  - Si pixel: 5.5 × 5.5 mm^2
  - 32 × 32 = 1024 ch / slab
  - 16 ASICs / slab
  - 4 Si wafers / slab



- **Readout information**
  - Bunch Crossing ID (**BCID**)
    f = 5 MHz, Δt = 0.2 μs
  - Hit bit
    - self-triggered by each channel
  - Analogue output (Any two of the three)
    - Charge [1]High/[2]Low gain, [3]Timing

- **Readout mechanism**
  - independently on each ASIC

1. Some tracks are triggered within one BCID interval (0.2 μs)
2. Analog outputs from all channels are stored in memory cells (15 SCAs)
3. After the acquisition phase, all stored data is read out

Studies for retriggers

- Setup
  - We used following data in this talk.
  - The data used for evaluation was obtained in TB2019 @ DESY.
  - All the results are based on FEV13 so far.

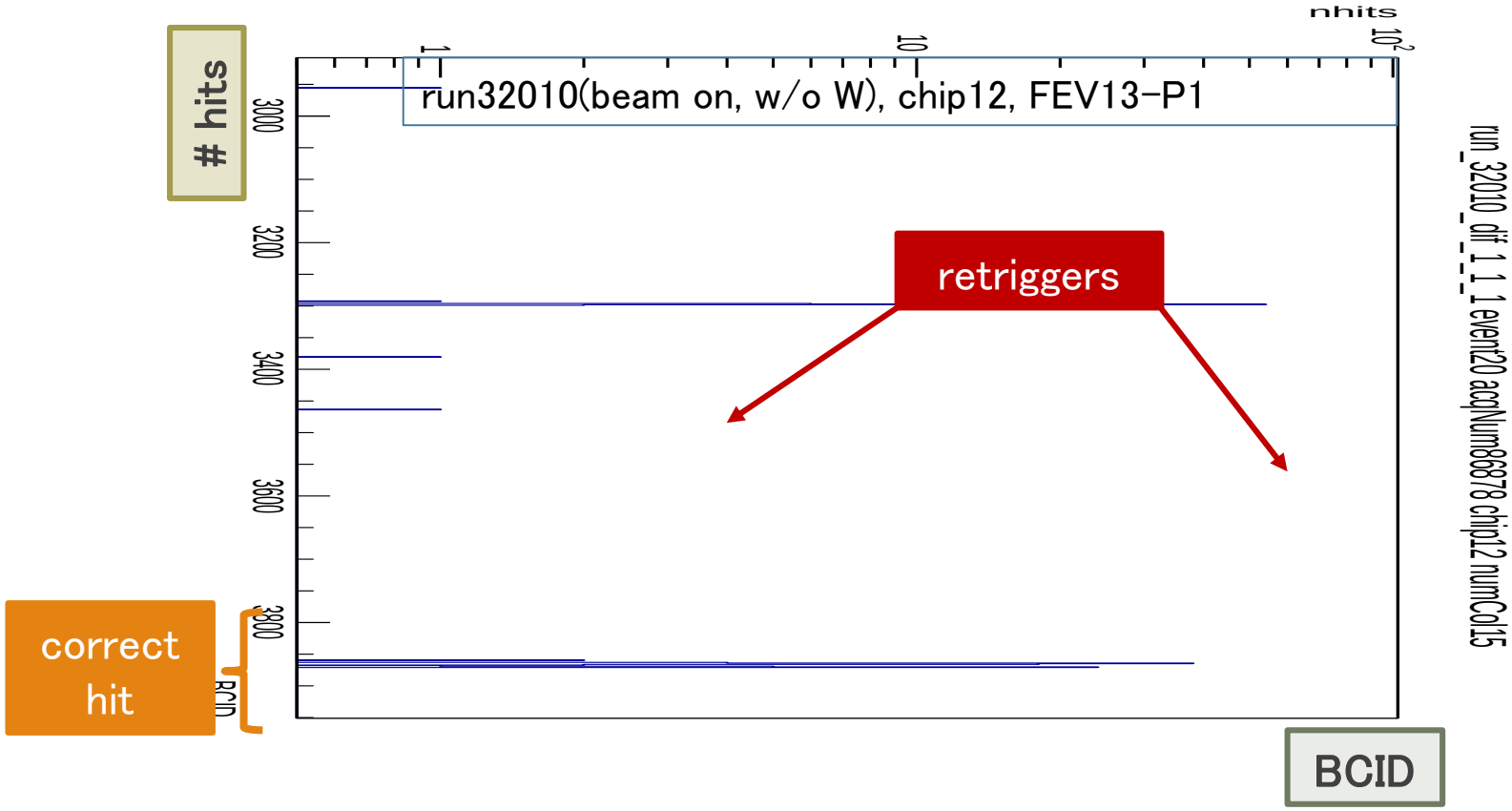
run	beam	Output mode	W absorber
32004 – 32010	On (e− 3 GeV)	ADC	None
32012	OFF	ADC	None
32015	On	TDC	None

ADC mode: Charge High(×10) & Low(×1)
TDC mode: Timing & Charge High

What is Retriggers?

- many fake hits just after correct hit(s)
- consecutive BCIDs

➢ **Memory cells are occupied by retriggers and may fail to store normal events**



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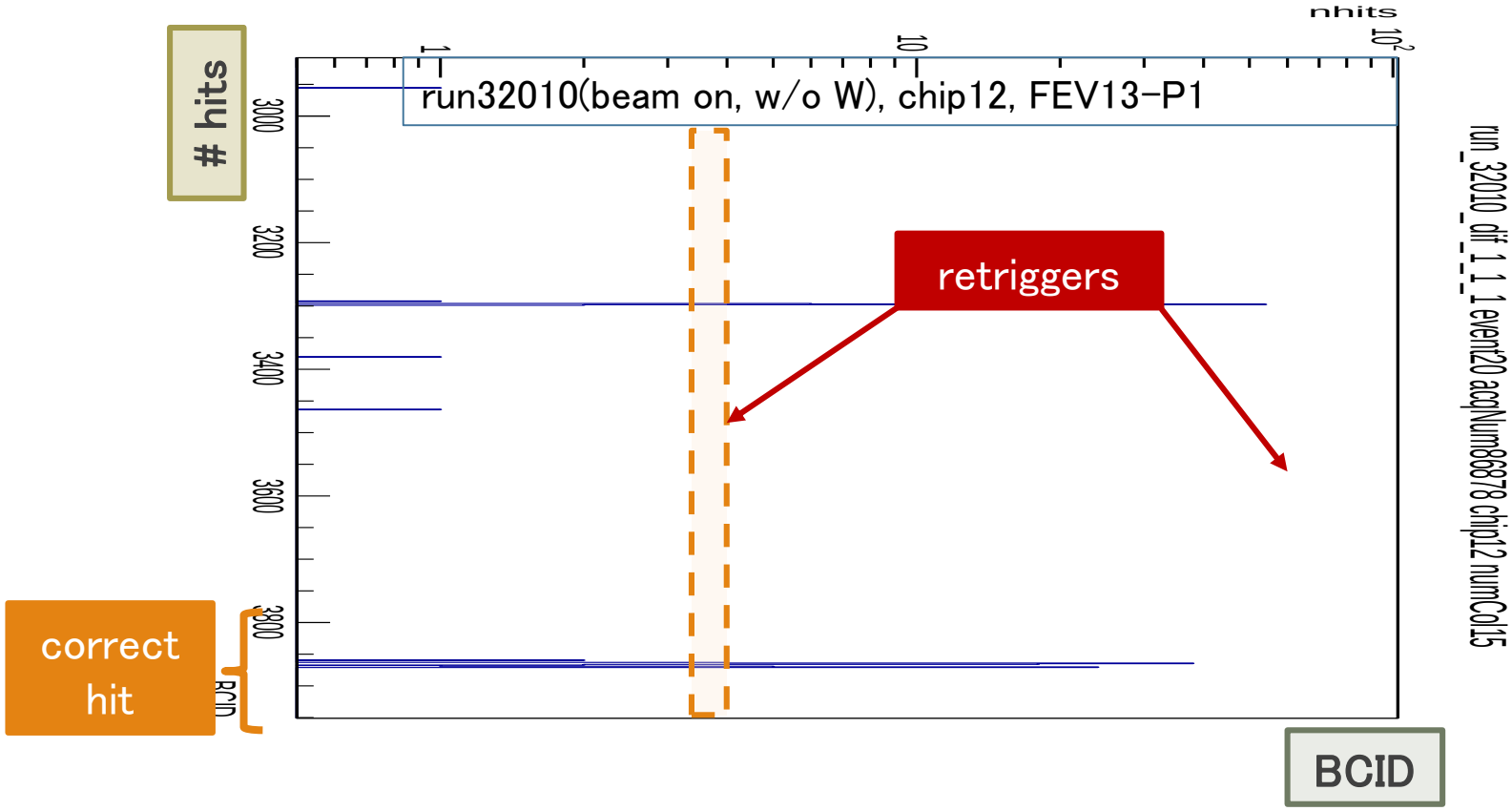

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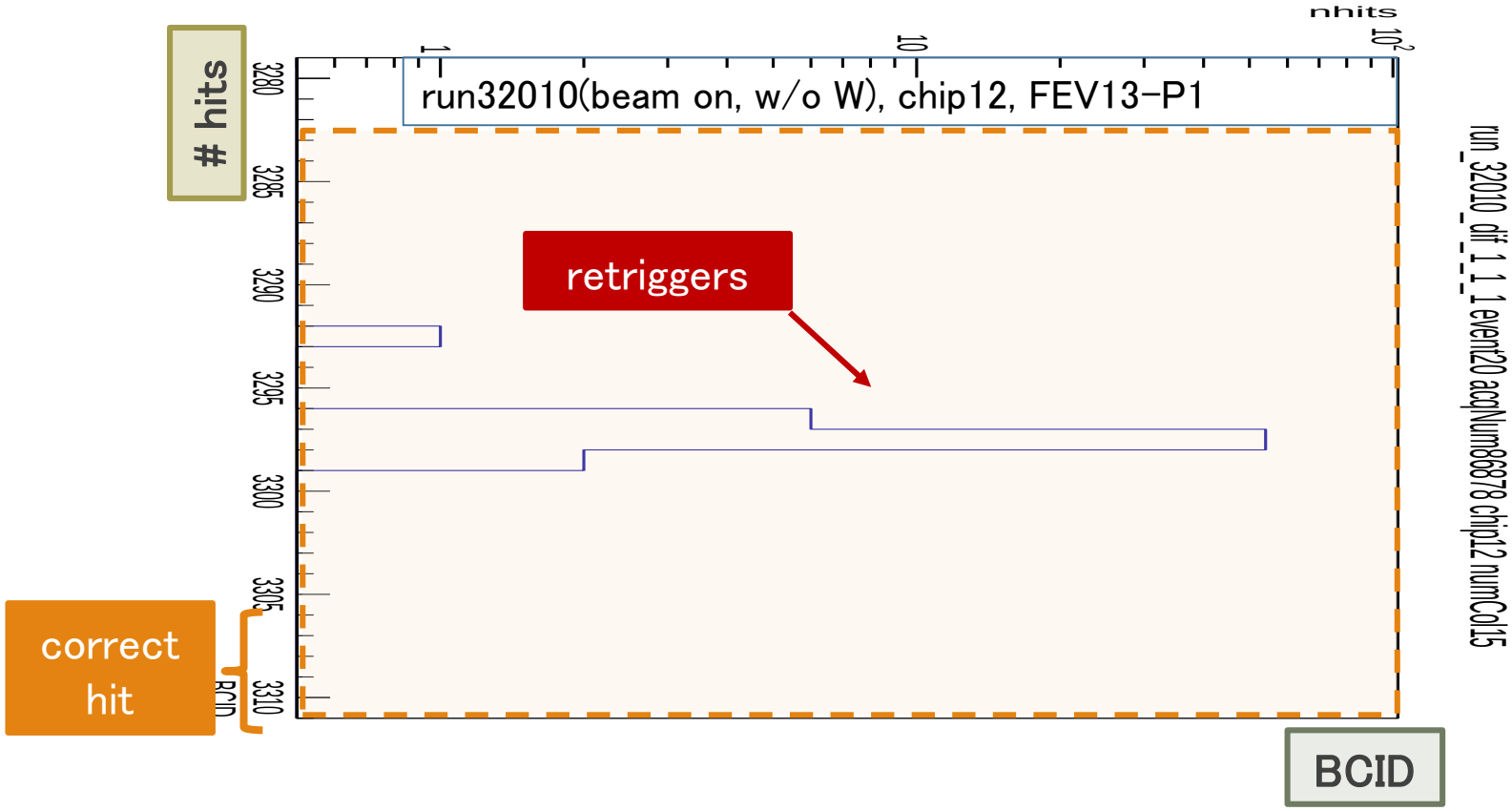
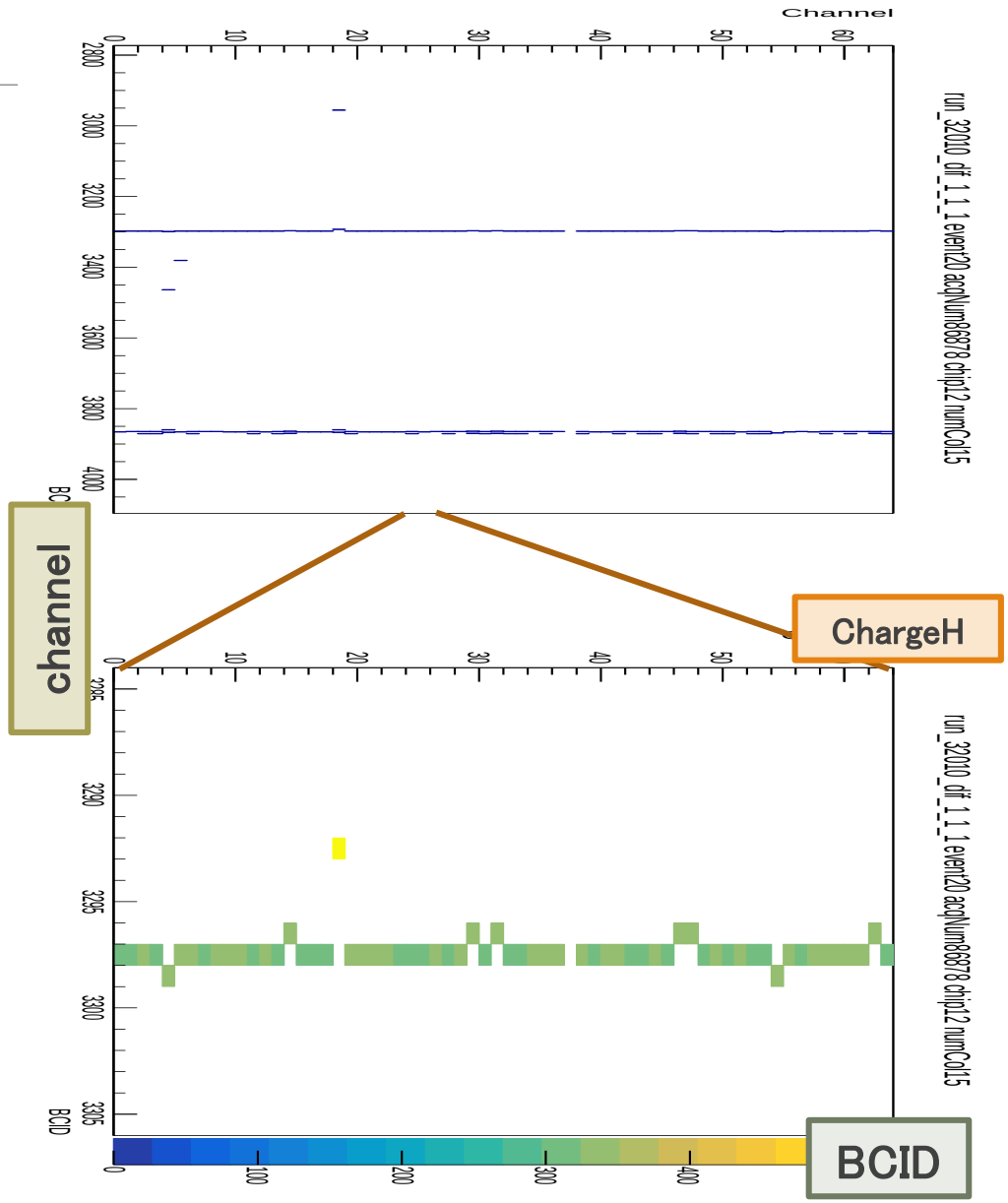


run32010(beam on, w/o W), chip12, FEV13-P1

Retriggers: Structure

Triggered channels vs BCID

- The retriggers looks “line”.
  - All channels are triggered once each without duplication in a group of retriggers.
    - except masked channel
    - sometimes one or two channels do not triggered
- Many consecutive hits occur after 4 – 6 BCIDs from the hit that looks normal.
  - The previous single hit might cause retrigger(?)
- We found similar events in the other data.

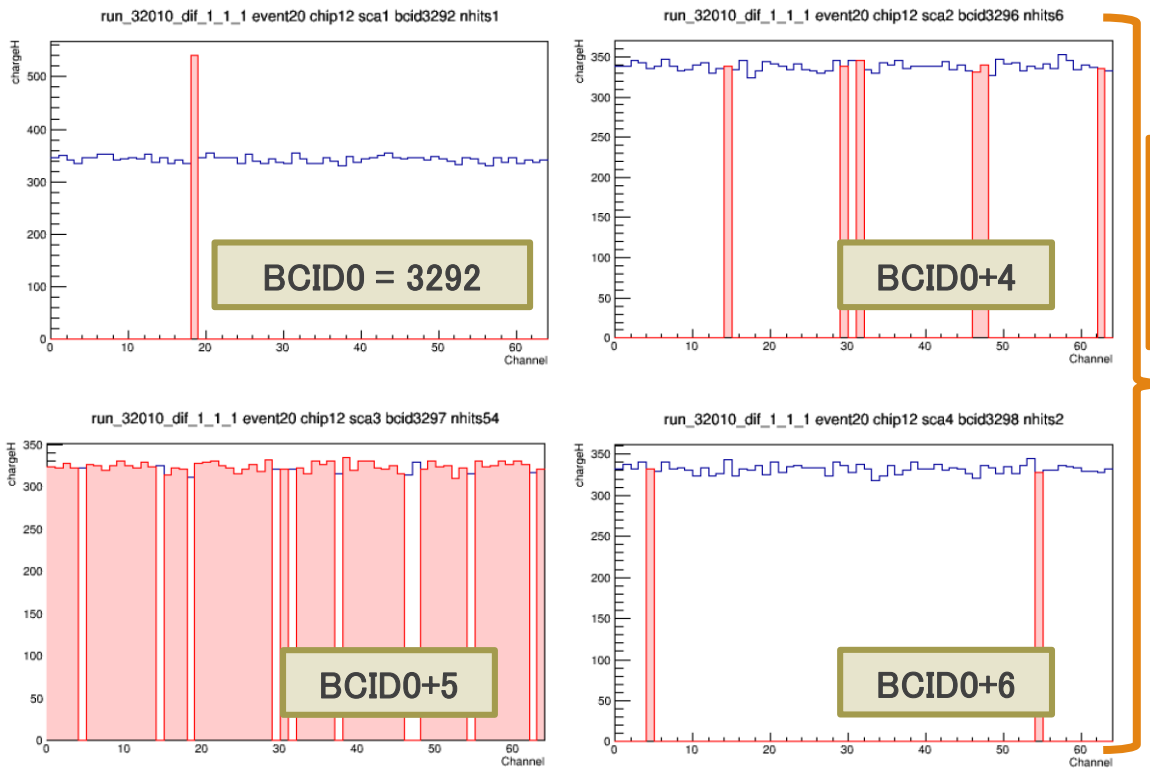


Retriggers: Structure

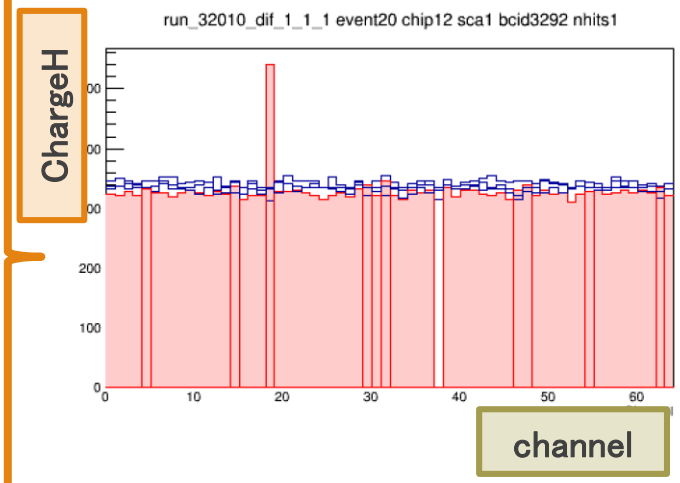
Trigger & Charge

run32010(beam on, w/o W), chip12, FEV13-P1

- Even the channels which charge is around pedestal level are triggered.
  - Fast shaper (trigger line) is presumed to be affected by retriggers.



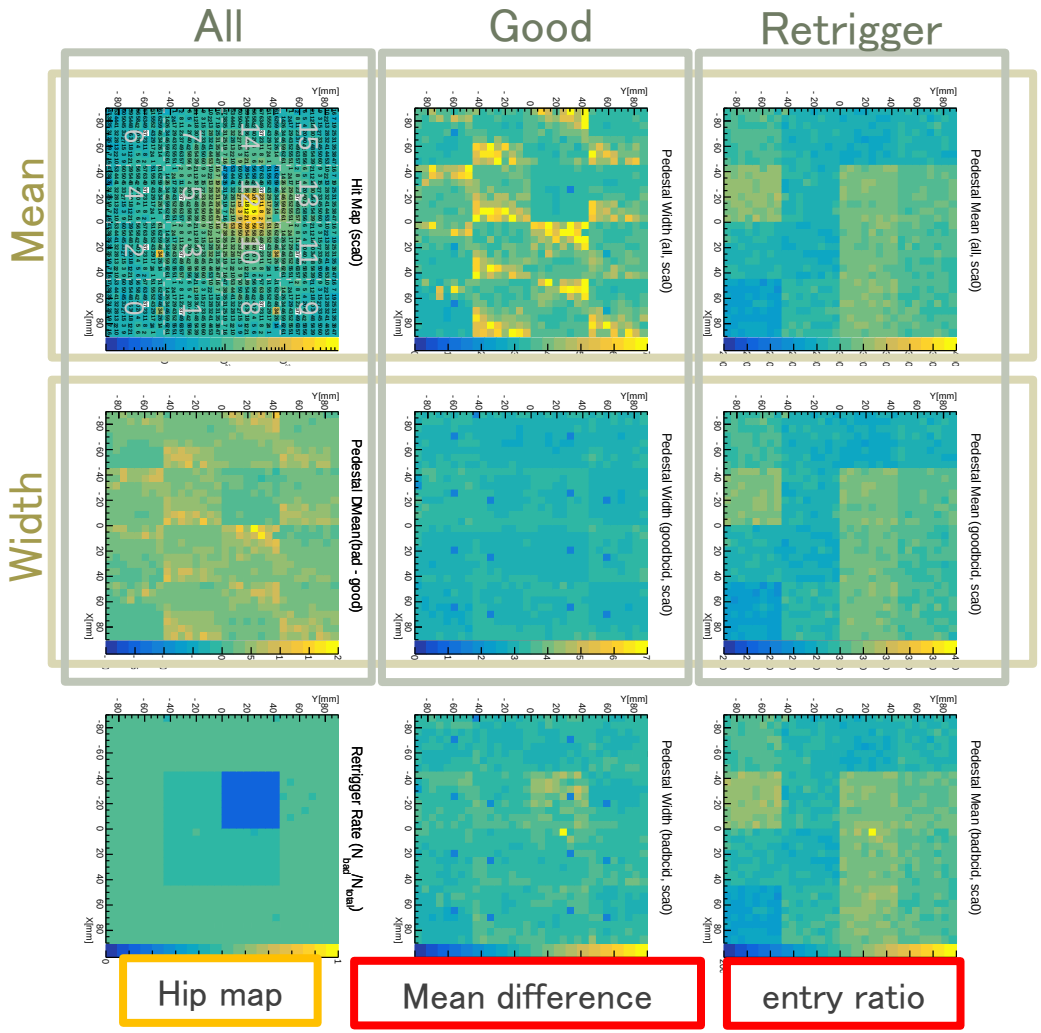
triggered

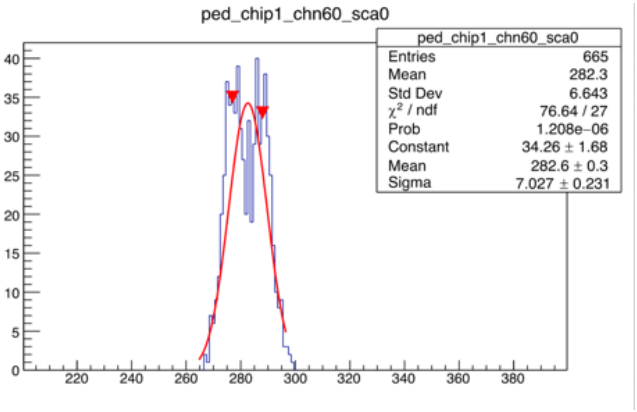


#37: masked channel

Retriggers: Double Pedestal

- Pedestal map (run 32004–32010, FEV13-P1, SCA-0)





Double pedestal
by retrigger

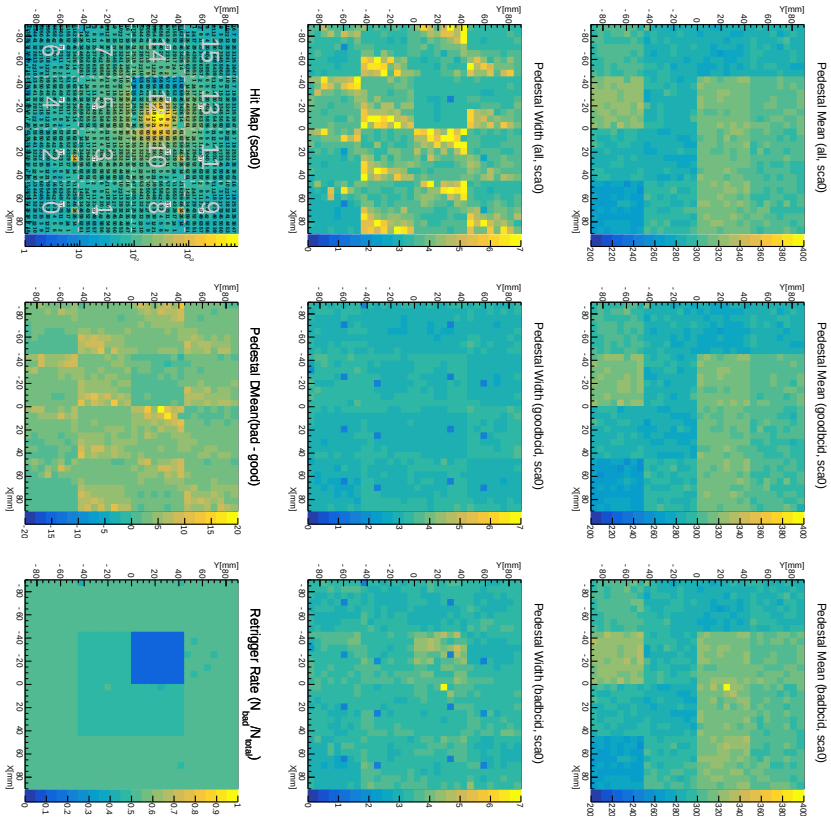
Double pedestal depends on channel position in ASIC.

Retriggers: Double Pedestal

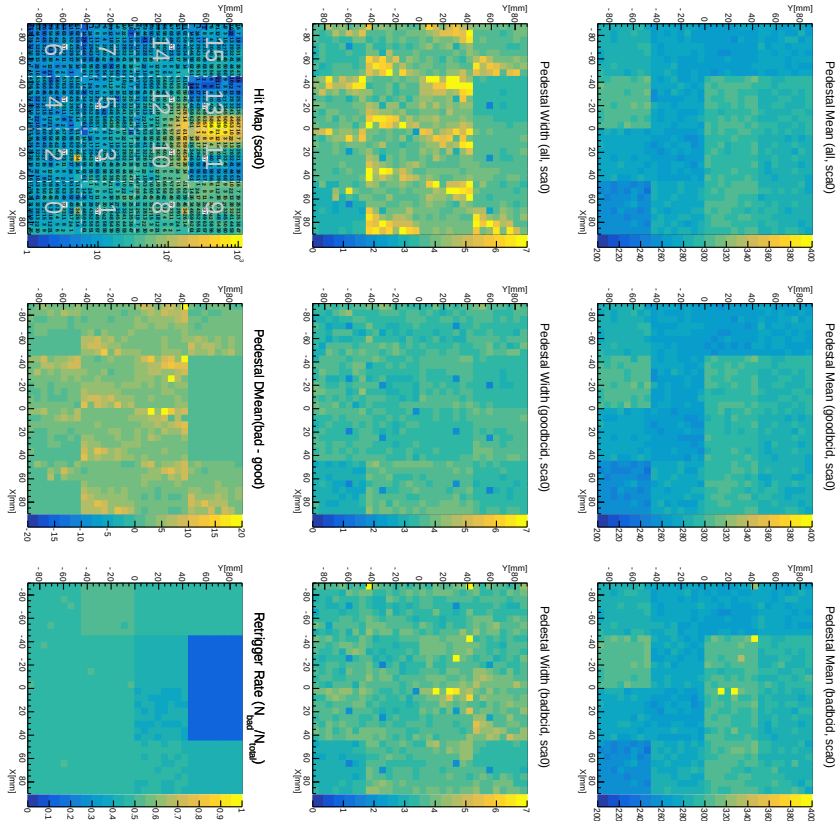
- Comparison of pedestal map between ADC/TDC mode.
  - Both pedestals are for SCA-0 and used High gain charge.
  - There are almost no difference.
  - Double pedestals are successfully removed.

ADC mode: Charge High(×10) & Low(×1)
TDC mode: Timing & Charge High

ADC mode (run32004-32010)

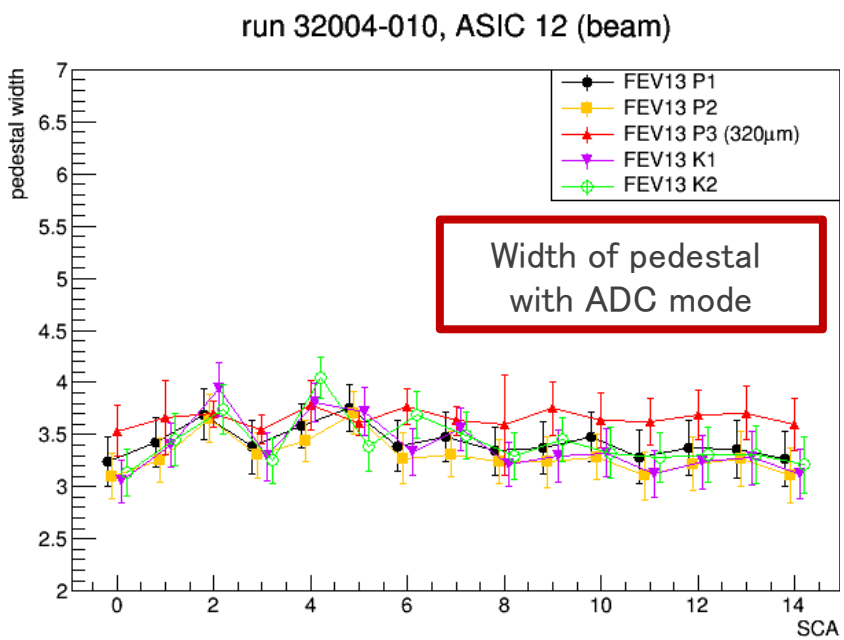


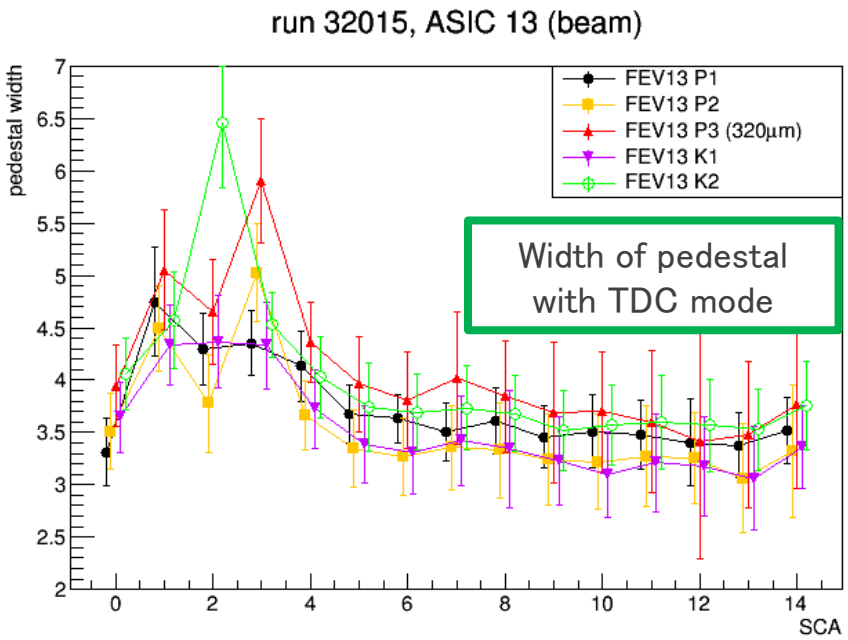
TDC mode (run32015)



SCA dependence on pedestal width: ADC/TDC mode

- We found the difference of pedestals at beam spot between ADC/TDC mode.
- TDC mode is worse around SCA-2.
- Even after retrigger removal, we still cannot remove them well.





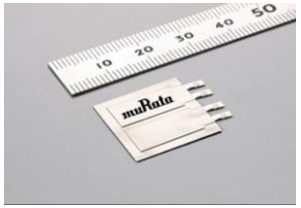
Summary

- Retriggers are still troublesome problem for SiW-ECAL prototype.
  - In single retrigger unit, all the channel except masked is triggered once each without duplication.
  - Basically retriggers appear after 4 – 6 BCIDs from single hit that looks normal.
- Double pedestal
  - depends on channel position in ASIC.
  - are successfully removed in SCA-0 by BCID selection.
  - has less difference in SCA-0 between ADC/TDC mode.
    - Even after retrigger removal, the pedestal width of TDC mode is worse (~ 4.5) around SCA-2.
  - Retrigger may affect not only fast shaper but also slow shaper.

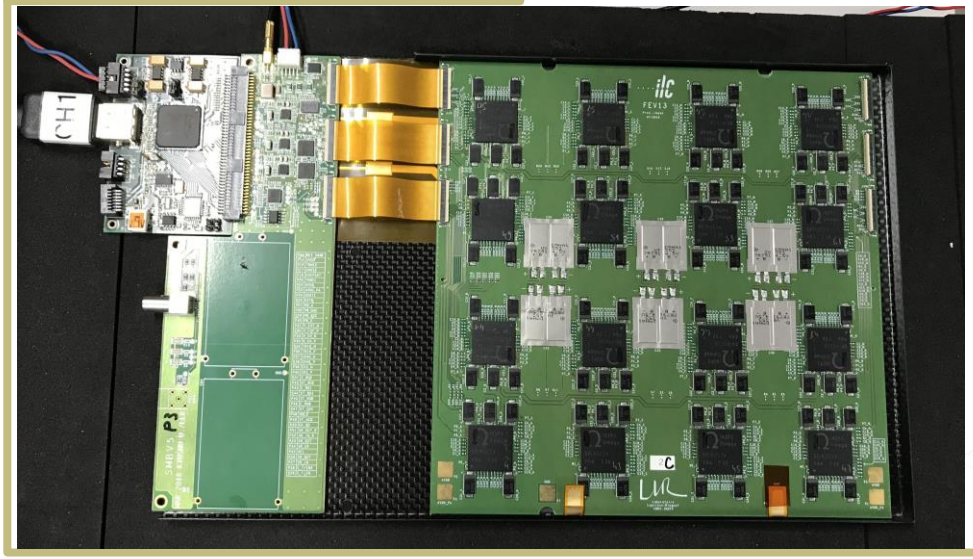
additional

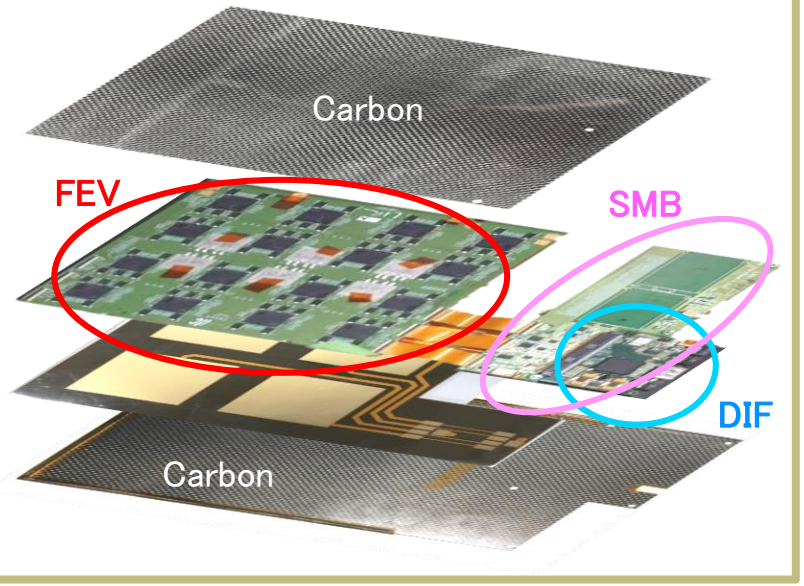
Major changes in FEV11→13

- ASIC: SKIROC2 → 2A
  - individual threshold control
  - improvement on TDC resolution
- Separation of power layers
  - power supply for analogue and digital
  - improvement on noise level
- Capacitor for Power Pulsing
  - 0.4 mm thickness, 40 mF x 6
- Carbon fiber frame/cover
- Smaller SMB footprint



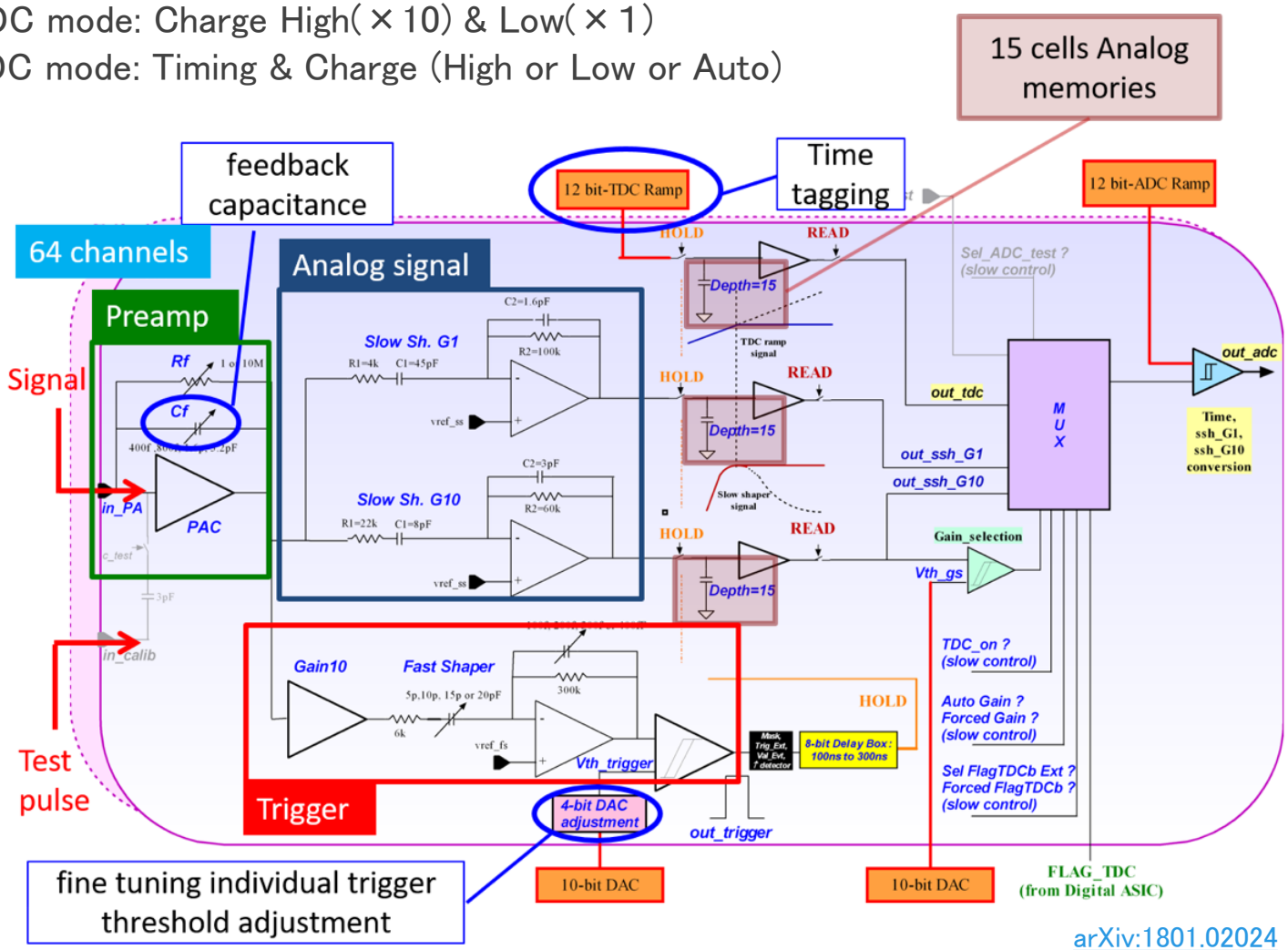
FEV13





Analogue core: SKIROC2A

- Outputs
  - ADC mode: Charge High(×10) & Low(×1)
  - TDC mode: Timing & Charge (High or Low or Auto)



arXiv:1801.02024

Known issues & facts about retrigger

1. Not observed in skiroc testboards
2. Double pedestal
   - discussed later
3. Deterioration in FEV13
4. Effect by CHIPSAT signal

Retriggers

- What is retriggers?
  - many fake hits after correct hit(s)
  - consecutive BCID

run32012(beam off) FEV13-K2

```
~/SiW-ECAL/tmp — -bash ...   ~ — katou@bepp02:~ — ssh ◂ ssh bepp   ~ — yu@cw14:~/work/JER_v02-0
*****************************************************************************************
==> 60 selected entries
(Long64_t) 60
root [27] fev10->Scan("event:acqNumber:chipid:nColumns:bcid:nhits","bcid!=-999&&chipid==8&&nColumns==15")
*****************************************************************************************
*    Row    * Instance *     event * acqNumber *    chipid *  nColumns *      bcid *     nhits *
*****************************************************************************************
*       18 *       120 *        19 *    116368 *         8 *        15 *      3381 *         1 *
*       18 *       121 *        19 *    116368 *         8 *        15 *      3385 *         8 *
*       18 *       122 *        19 *    116368 *         8 *        15 *      3386 *        48 *
*       18 *       123 *        19 *    116368 *         8 *        15 *      3387 *         4 *
*       18 *       124 *        19 *    116368 *         8 *        15 *      3388 *         1 *
*       18 *       125 *        19 *    116368 *         8 *        15 *      3389 *         2 *
*       18 *       126 *        19 *    116368 *         8 *        15 *      3392 *        37 *
*       18 *       127 *        19 *    116368 *         8 *        15 *      3393 *        21 *
*       18 *       128 *        19 *    116368 *         8 *        15 *      3395 *         3 *
*       18 *       129 *        19 *    116368 *         8 *        15 *      3396 *         1 *
*       18 *       130 *        19 *    116368 *         8 *        15 *      3397 *         2 *
*       18 *       131 *        19 *    116368 *         8 *        15 *      3399 *        26 *
*       18 *       132 *        19 *    116368 *         8 *        15 *      3400 *        28 *
*       18 *       133 *        19 *    116368 *         8 *        15 *      3401 *         3 *
*       18 *       134 *        19 *    116368 *         8 *        15 *      3403 *         2 *
Type <CR> to continue or q to quit ==>
*       71 *       120 *        72 *    117199 *         8 *        15 *      2006 *         1 *
*       71 *       121 *        72 *    117199 *         8 *        15 *      2010 *         8 *
*       71 *       122 *        72 *    117199 *         8 *        15 *      2011 *        47 *
*       71 *       123 *        72 *    117199 *         8 *        15 *      2012 *         4 *
*       71 *       124 *        72 *    117199 *         8 *        15 *      2013 *         2 *
*       71 *       125 *        72 *    117199 *         8 *        15 *      2014 *         1 *
*       71 *       126 *        72 *    117199 *         8 *        15 *      2017 *        39 *
*       71 *       127 *        72 *    117199 *         8 *        15 *      2018 *        18 *
*       71 *       128 *        72 *    117199 *         8 *        15 *      2020 *         3 *
*       71 *       129 *        72 *    117199 *         8 *        15 *      2021 *         1 *
*       71 *       130 *        72 *    117199 *         8 *        15 *      2022 *         2 *
*       71 *       131 *        72 *    117199 *         8 *        15 *      2024 *        27 *
*       71 *       132 *        72 *    117199 *         8 *        15 *      2025 *        25 *
*       71 *       133 *        72 *    117199 *         8 *        15 *      2026 *         2 *
*       71 *       134 *        72 *    117199 *         8 *        15 *      2028 *         3 *
```

Retriggers

- channel combination
  - Almost all the channel is triggered in single retrigger unit.
  - It's difficult to distinguish some retriggers to divide into unit.

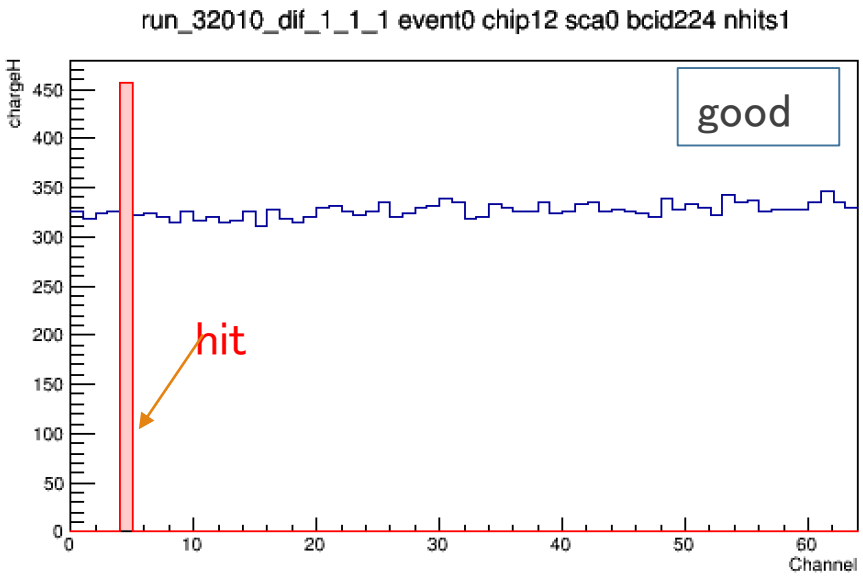
```
root [6] fev10->Scan("event:acqNumber:chipid:nColumns:bcid:badbcid:nhits","bcid!=-999&&chipid==12&&event==21")
*****************************************************************************************************************
*    Row   * Instance *     event * acqNumber *    chipid *  nColumns *      bcid *   badbcid *     nhits *
*****************************************************************************************************************
*       20 *      180 *        21 *     86878 *        12 *        15 *      2955 *         0 *         1 *
*       20 *      181 *        21 *     86878 *        12 *        15 *      3292 *         3 *         1 *
*       20 *      182 *        21 *     86878 *        12 *        15 *      3296 *         3 *         6 *
*       20 *      183 *        21 *     86878 *        12 *        15 *      3297 *         3 *        54 *
*       20 *      184 *        21 *     86878 *        12 *        15 *      3298 *         3 *         2 *
*       20 *      185 *        21 *     86878 *        12 *        15 *      3380 *         0 *         1 *
*       20 *      186 *        21 *     86878 *        12 *        15 *      3463 *         0 *         1 *
*       20 *      187 *        21 *     86878 *        12 *        15 *      3859 *         3 *         2 *
*       20 *      188 *        21 *     86878 *        12 *        15 *      3863 *         3 *         4 *
*       20 *      189 *        21 *     86878 *        12 *        15 *      3864 *         3 *        38 *
*       20 *      190 *        21 *     86878 *        12 *        15 *      3865 *         3 *        18 *
*       20 *      191 *        21 *     86878 *        12 *        15 *      3866 *         3 *         2 *
*       20 *      192 *        21 *     86878 *        12 *        15 *      3868 *         3 *         1 *
*       20 *      193 *        21 *     86878 *        12 *        15 *      3869 *         3 *         5 *
*       20 *      194 *        21 *     86878 *        12 *        15 *      3870 *         3 *        24 *
*****************************************************************************************************************
```

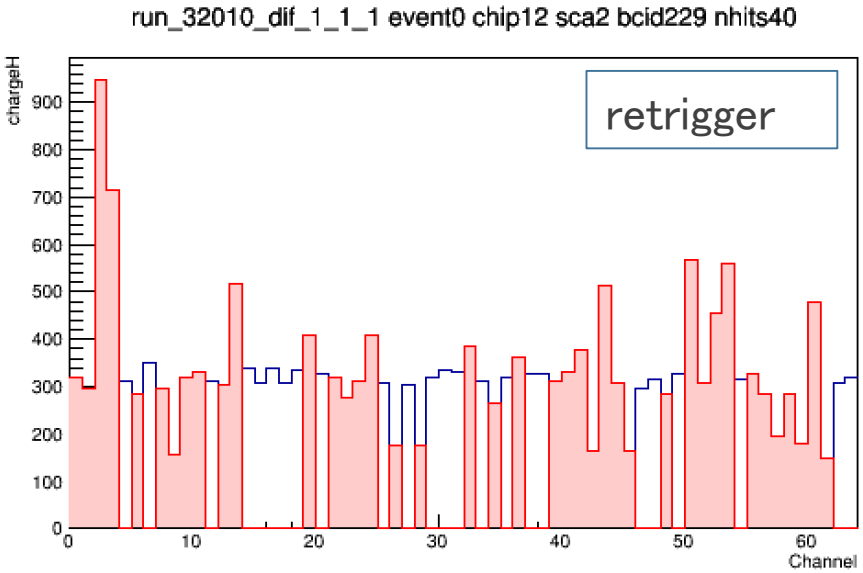
run32010(beam on) FEV13-P1

Retriggers

- trigger vs charge
  - Which shaper has problems that cause retriggers?
  - The charges and hits are compared between good/retrigger events.
  - Even the channel which charge is lower than pedestal is triggered.

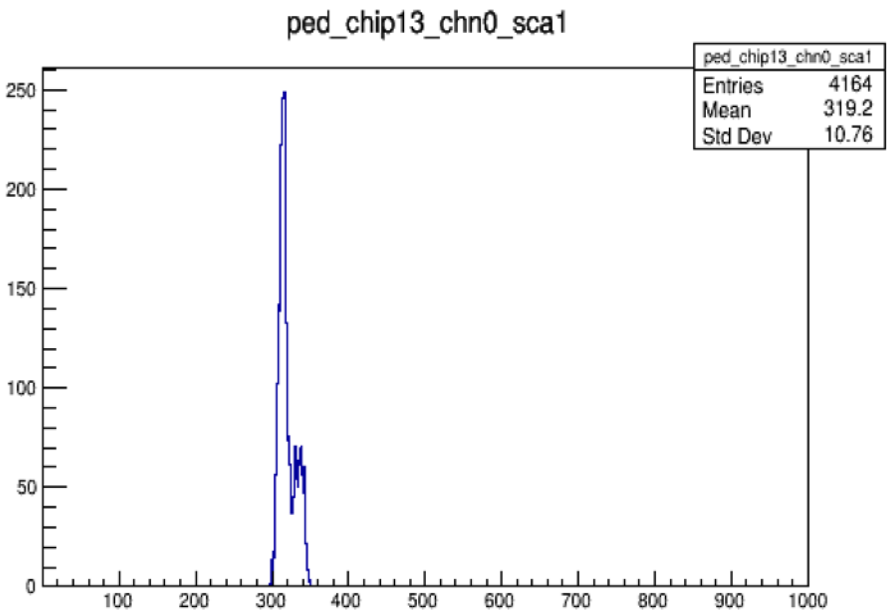
➢ Fast shaper has some problems in retrigger?

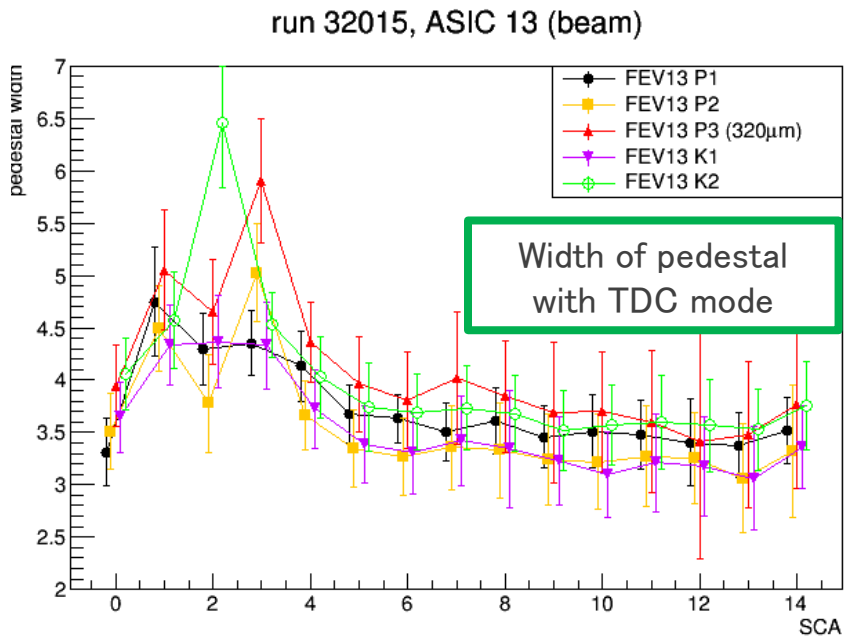




Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In TDC mode, SCA~2 is worse.

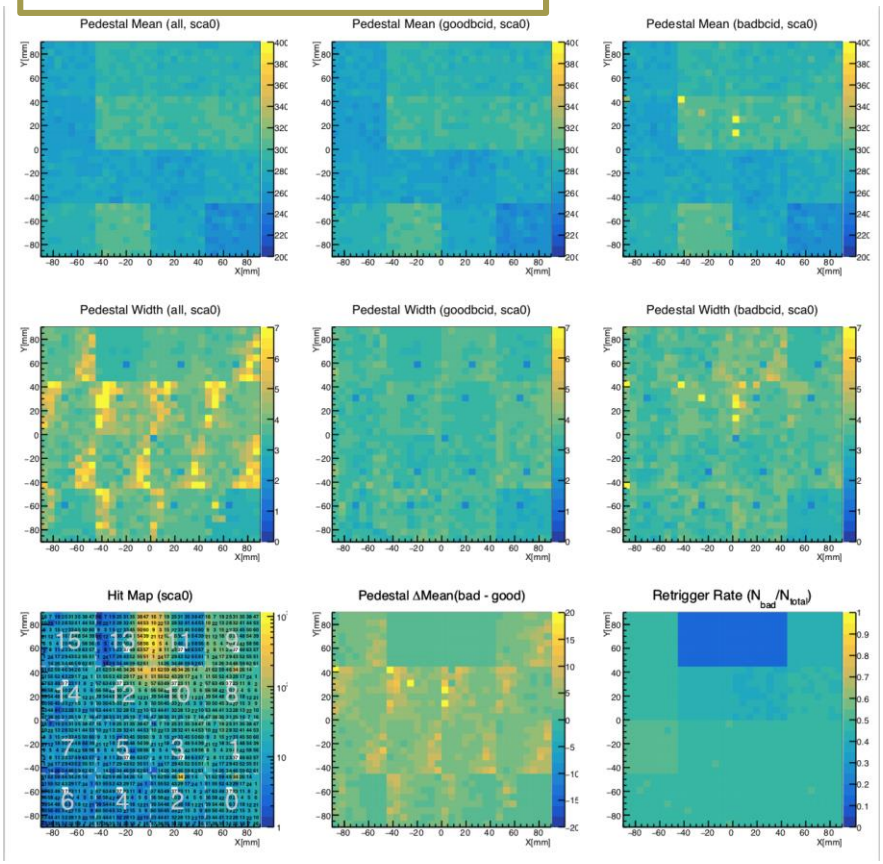




- There are double pedestal even after bcid selection in TDC mode.
- The criteria for identification of double pedestal is not optimized.

Retriggers

SCA 0
TDC mode (run32015)



SCA 1
TDC mode (run32015)