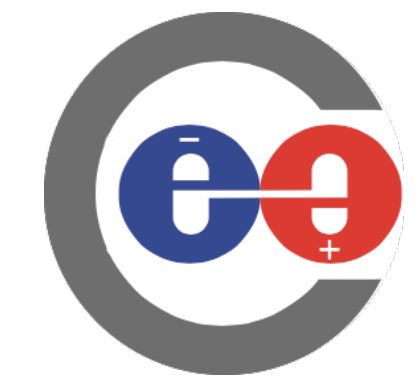# Simulation studies of material and scintillator non-uniformities

CALICE Collaboration Meeting - Montreal
5.3.2020

Lorenz Emberger

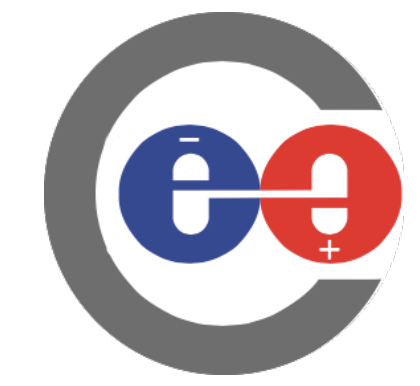Showing Work from Malinda DeSilva

MAX-PLANCK-INSTITUT
FÜR PHYSIK

Overview

Geant4 study to investigate the effects of non-uniformities in the calorimeter:

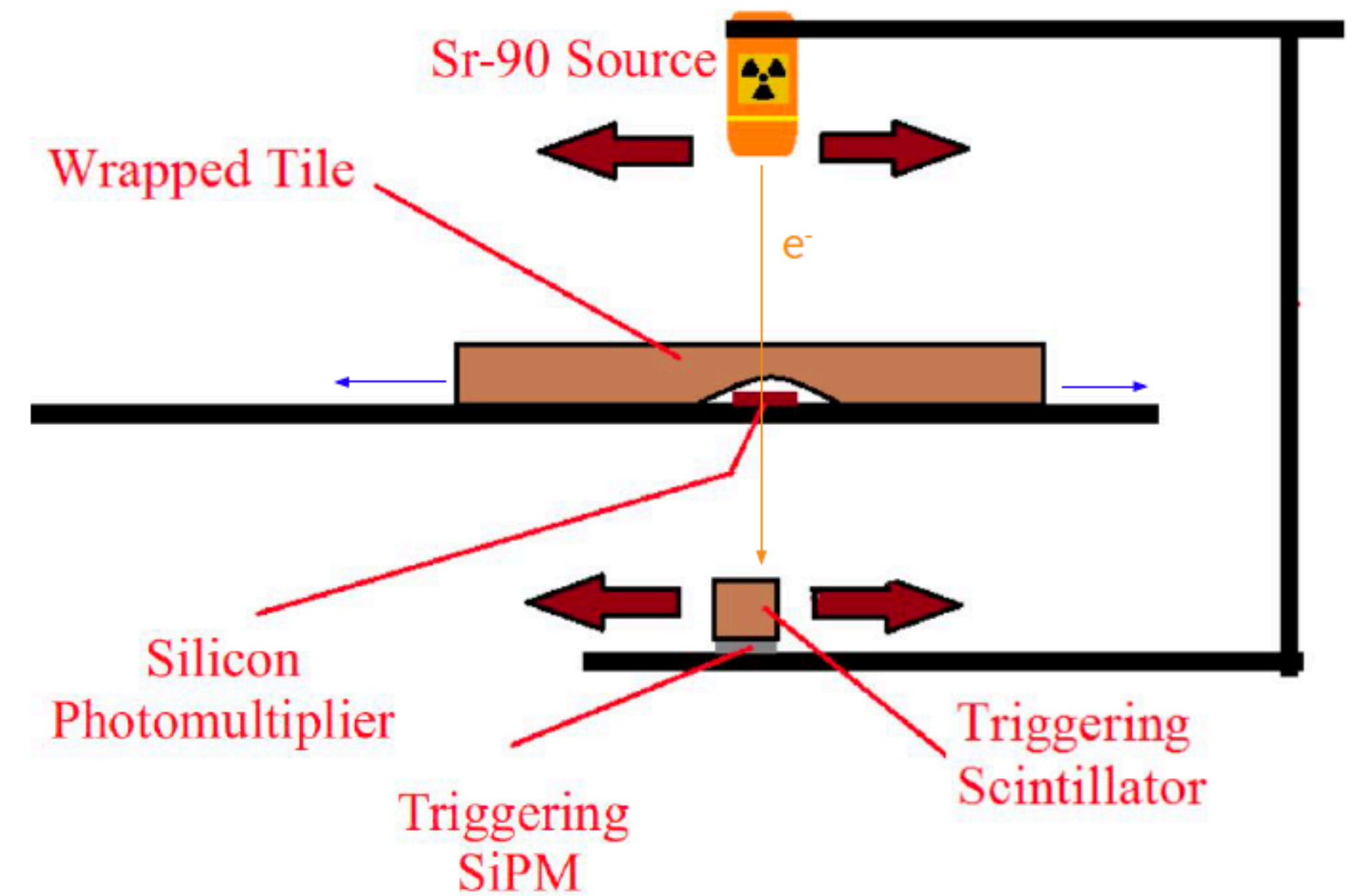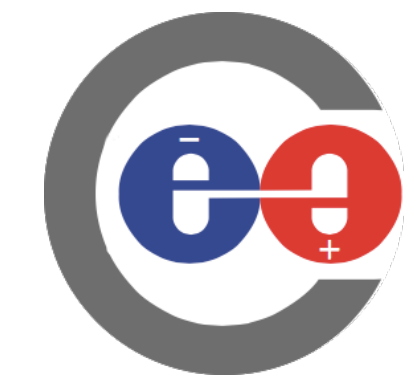• Misalignment of tiles wrt to SiPM

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Geant4 study to investigate the effects of non-uniformities in the calorimeter:

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Geant4 study to investigate the effects of non-uniformities in the calorimeter:
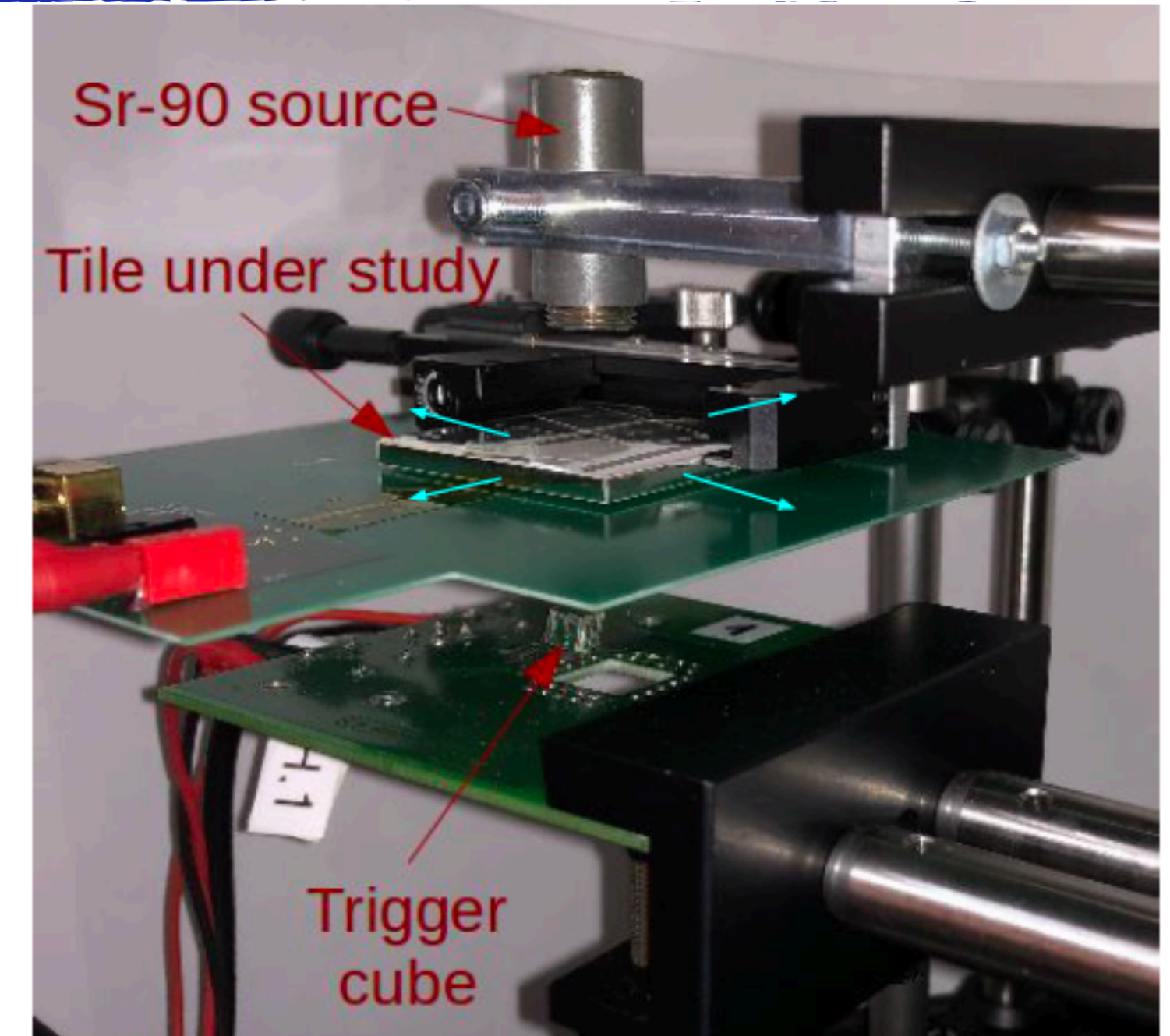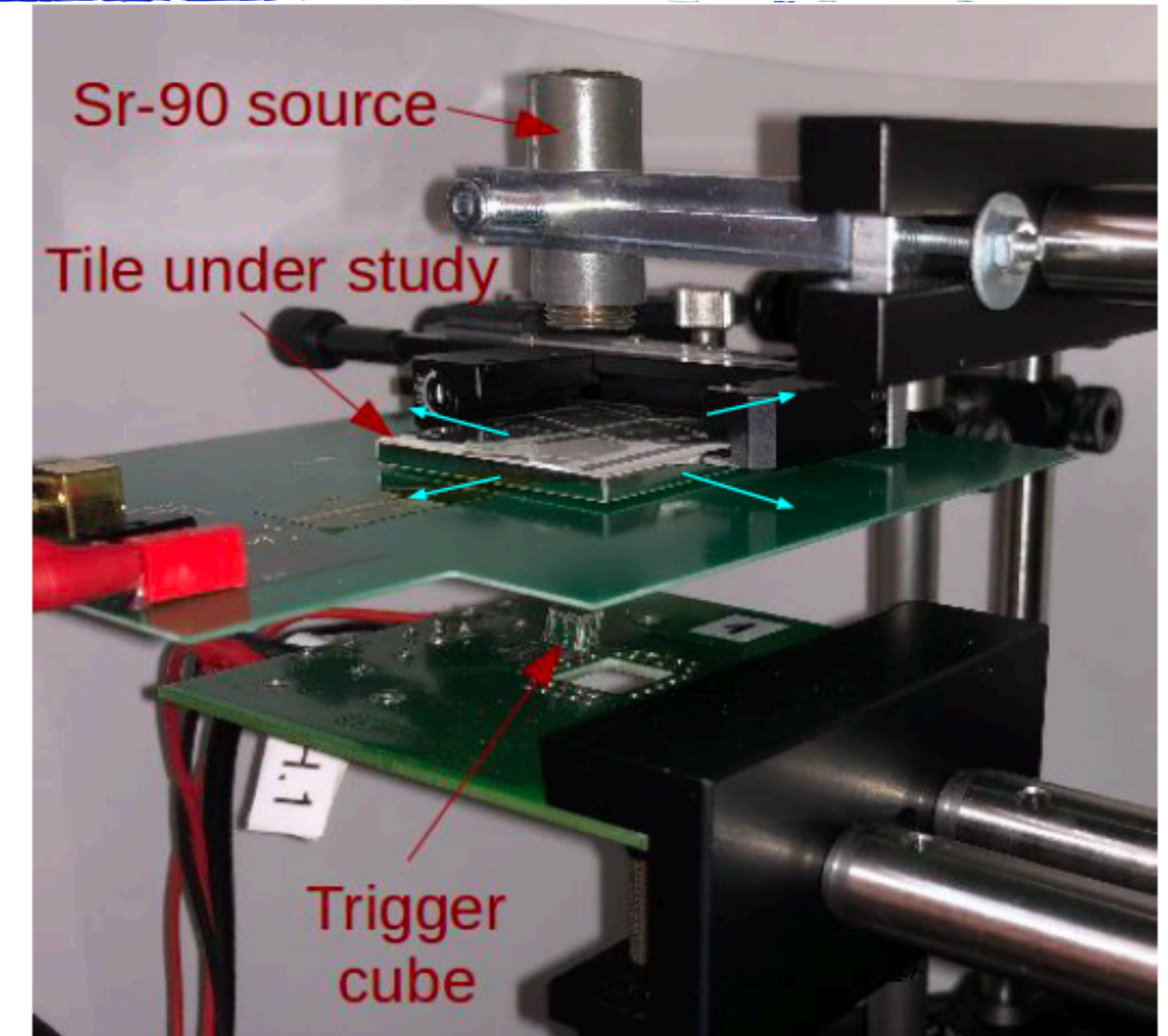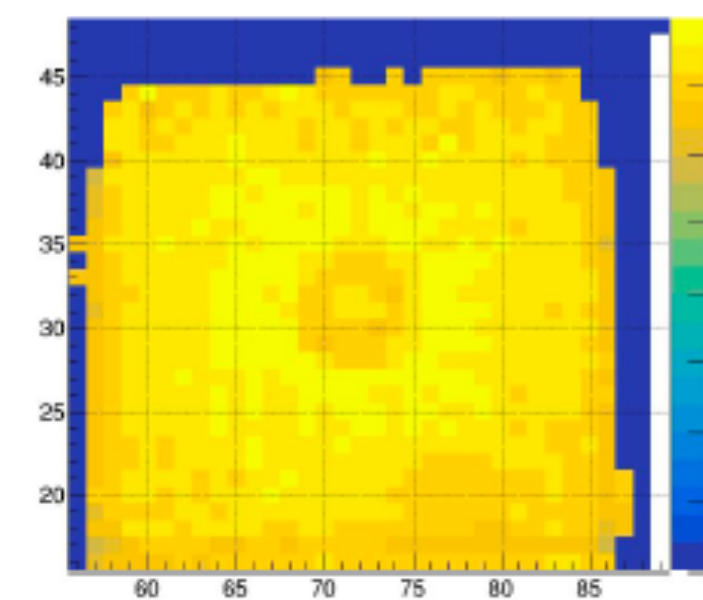
- Misalignment of tiles wrt to SiPM

- Presence of ASICs

- Presence of gaps between tiles

Overview

Geant4 study to investigate the effects of non-uniformities in the calorimeter:

- Misalignment of tiles wrt to SiPM

- Presence of ASICs
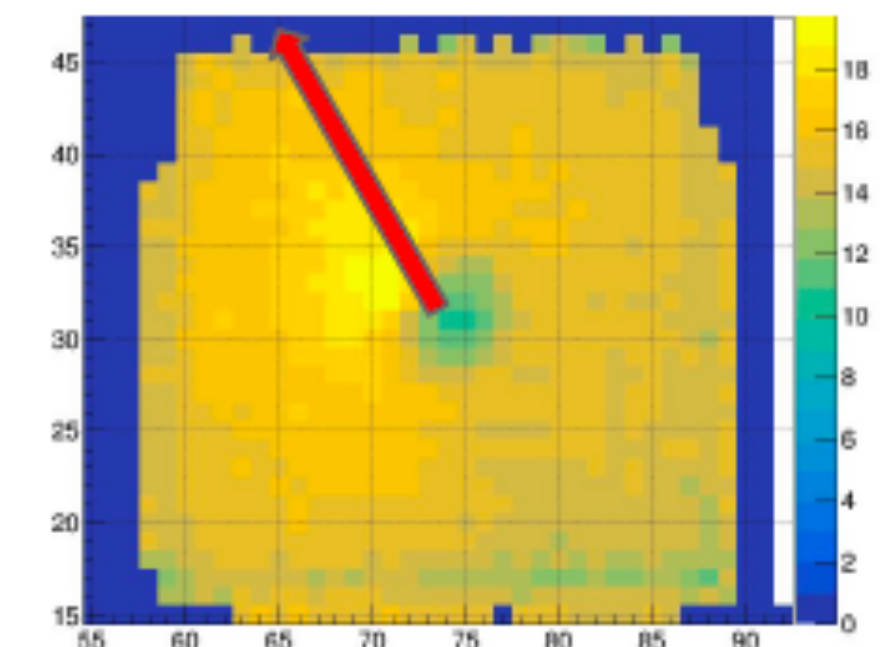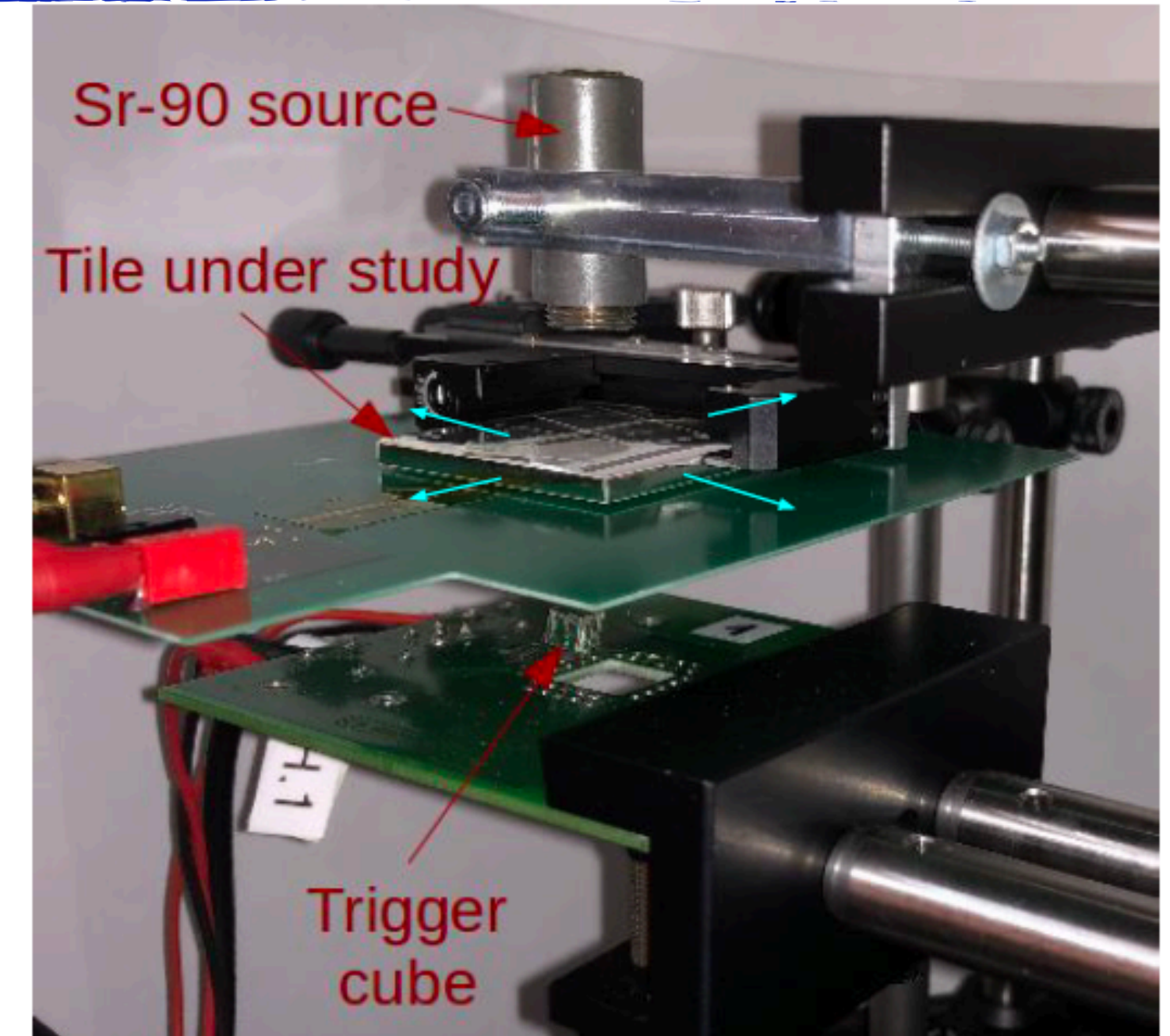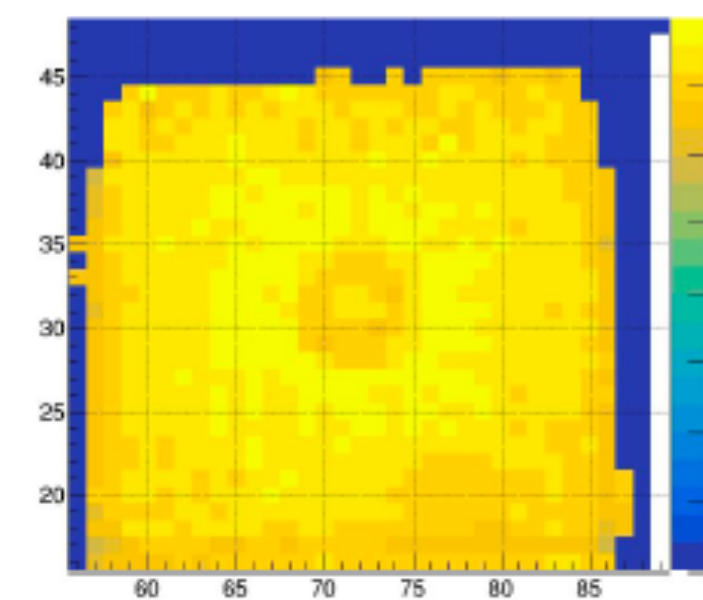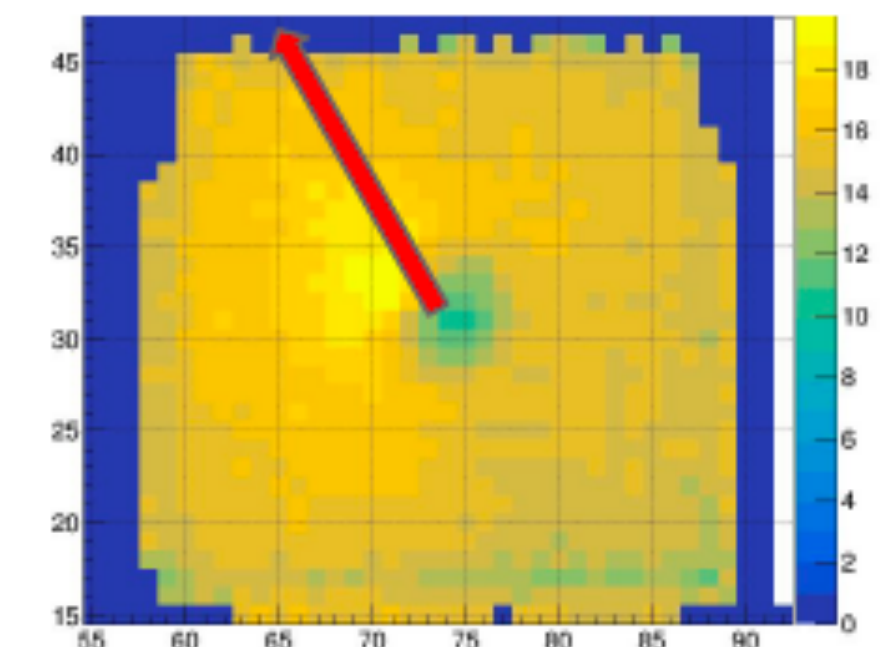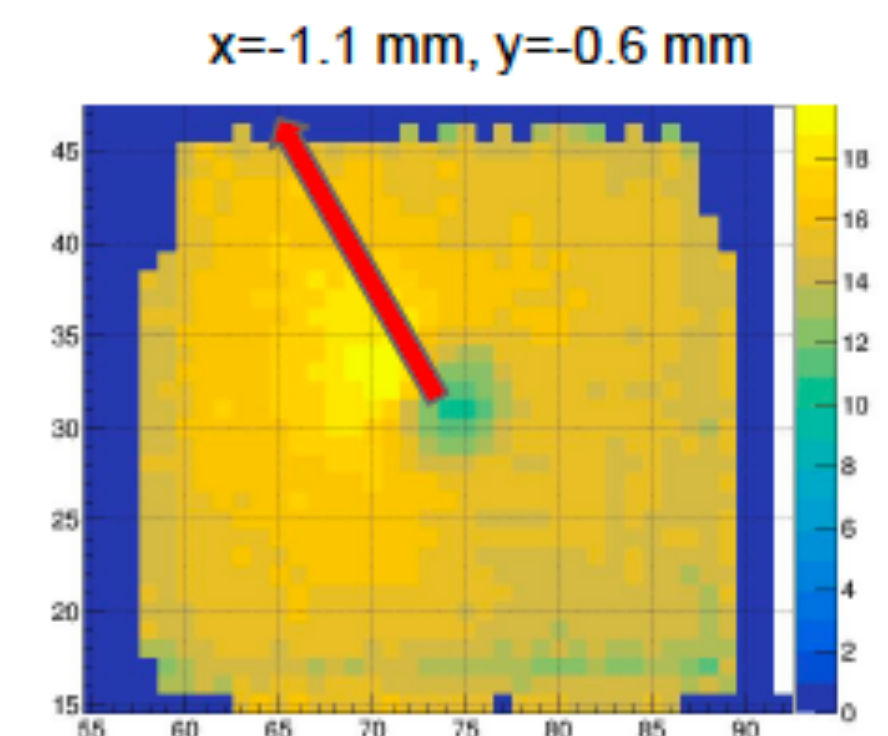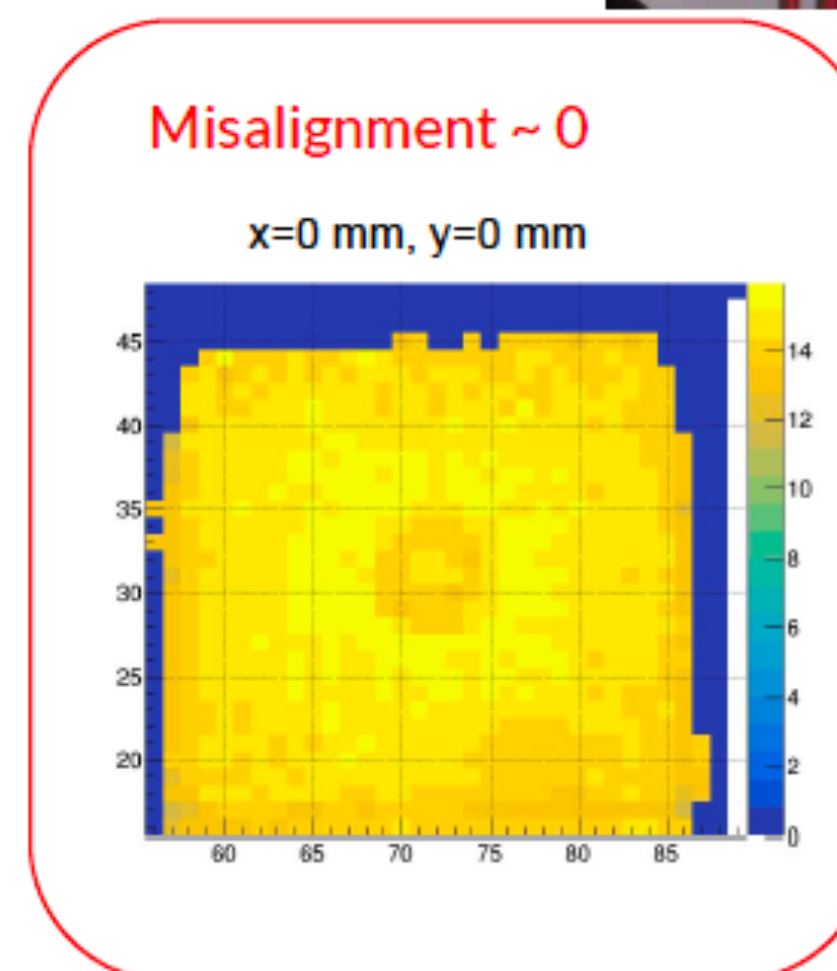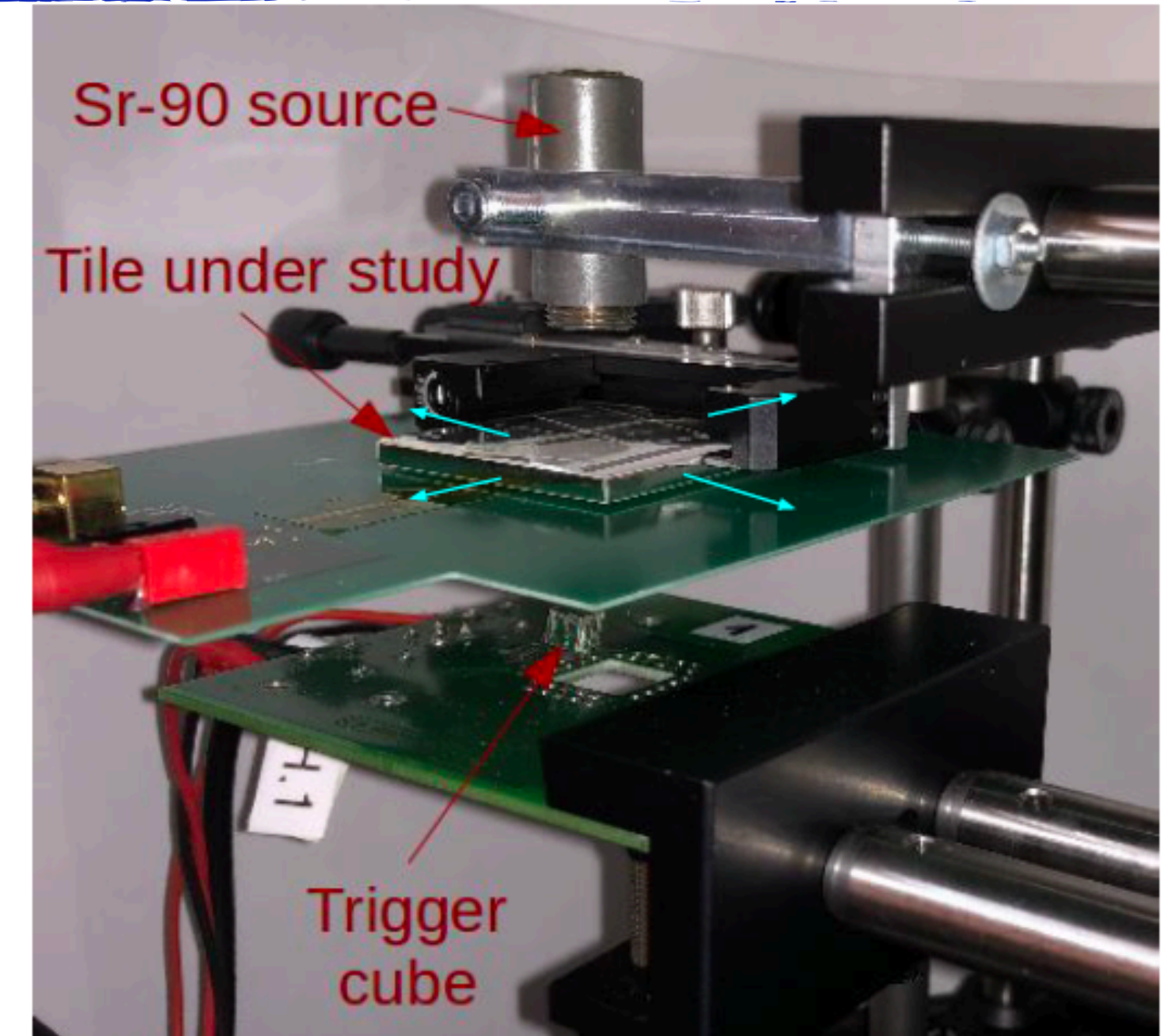
- Presence of gaps between tiles

Quantify the influence of individual kinds of non-uniformities and combinations:
- Energy range of 50MeV - 1.5GeV with copper absorber
- Energy range of 5GeV - 80GeV with tungsten absorber
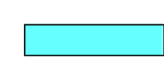
ECAL Setup in Geant4
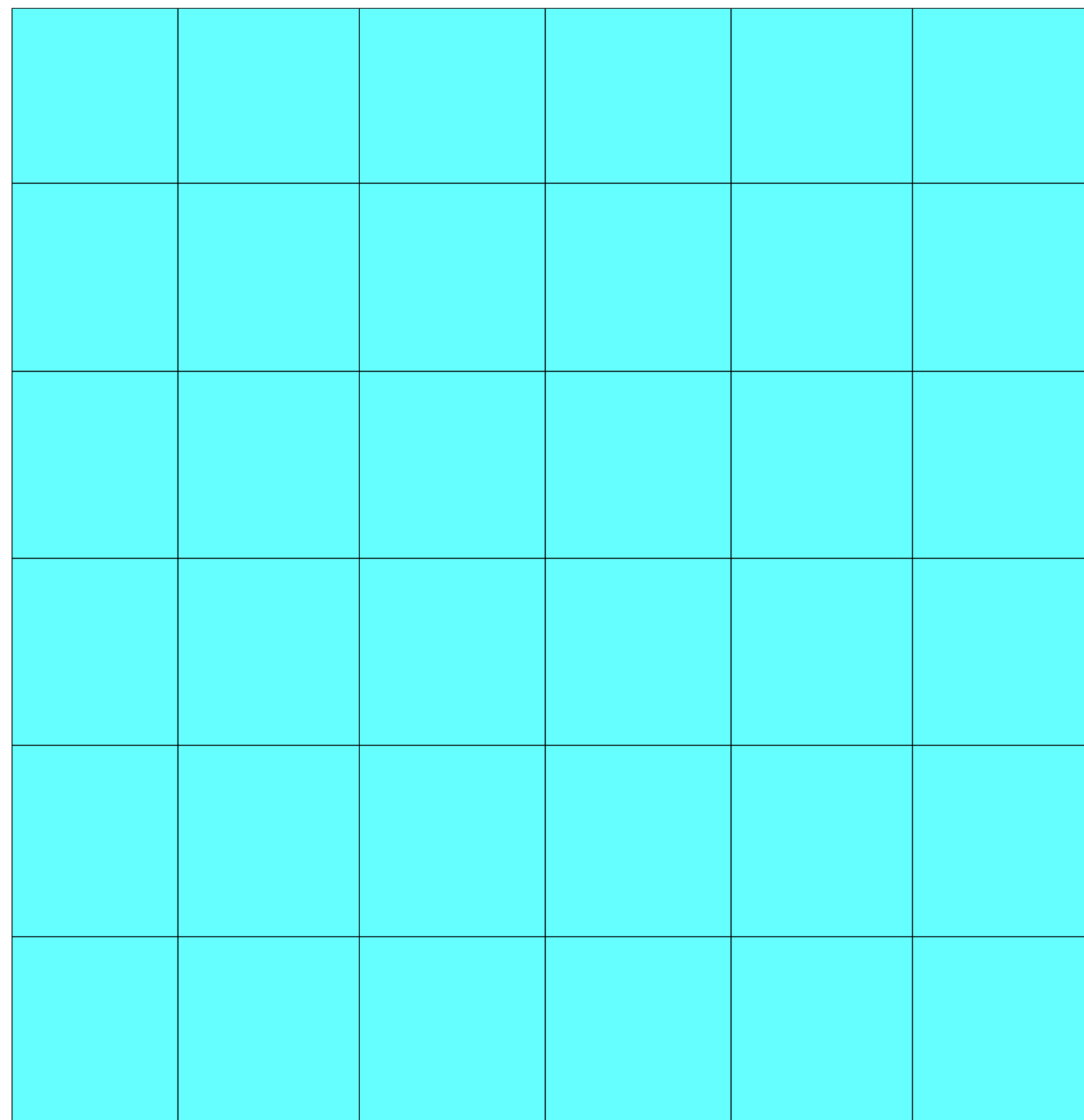
Front View

Side View

Scintillator Tiles

Copper Absorber

PCB layer

Basic simulation study without support structures

300 alternating layers of:
- 2 mm thick copper absorber
- 120 polystyrene scintillators of size 30x30x5 mm3
- 0.7 mm thick PCB layer

20,000 photons simulated covering the 4 central tiles uniformly

Including:
- Poissonian photon statistics
- Range cut: 0.05 mm
- Energy cut: 0.3 MeV

Baseline setup $\implies$ implement non uniformities step by step
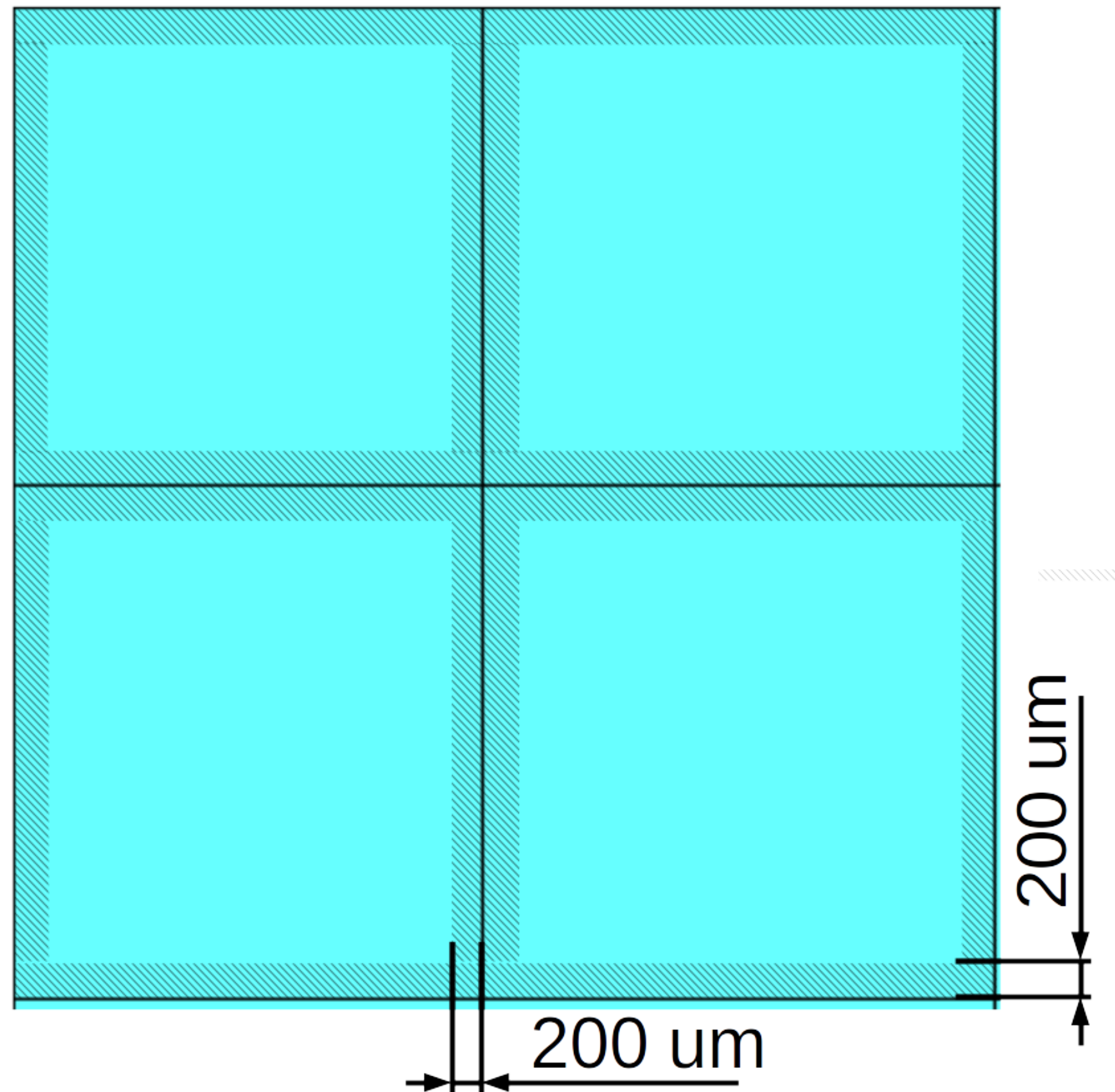
Implementation of Gaps

- Gaps caused by manufacturing, wrapping and placement accuracy

- Gaps implemented by setting the energy deposition in the outer area of the tile to zero.

- NOTE: Particles still traverse scintillator material

Implementation of ASICs
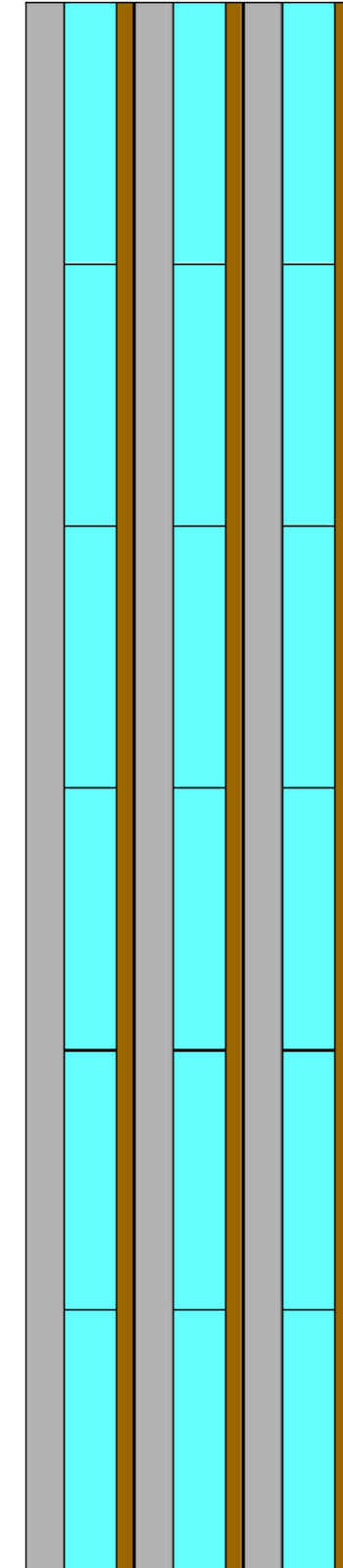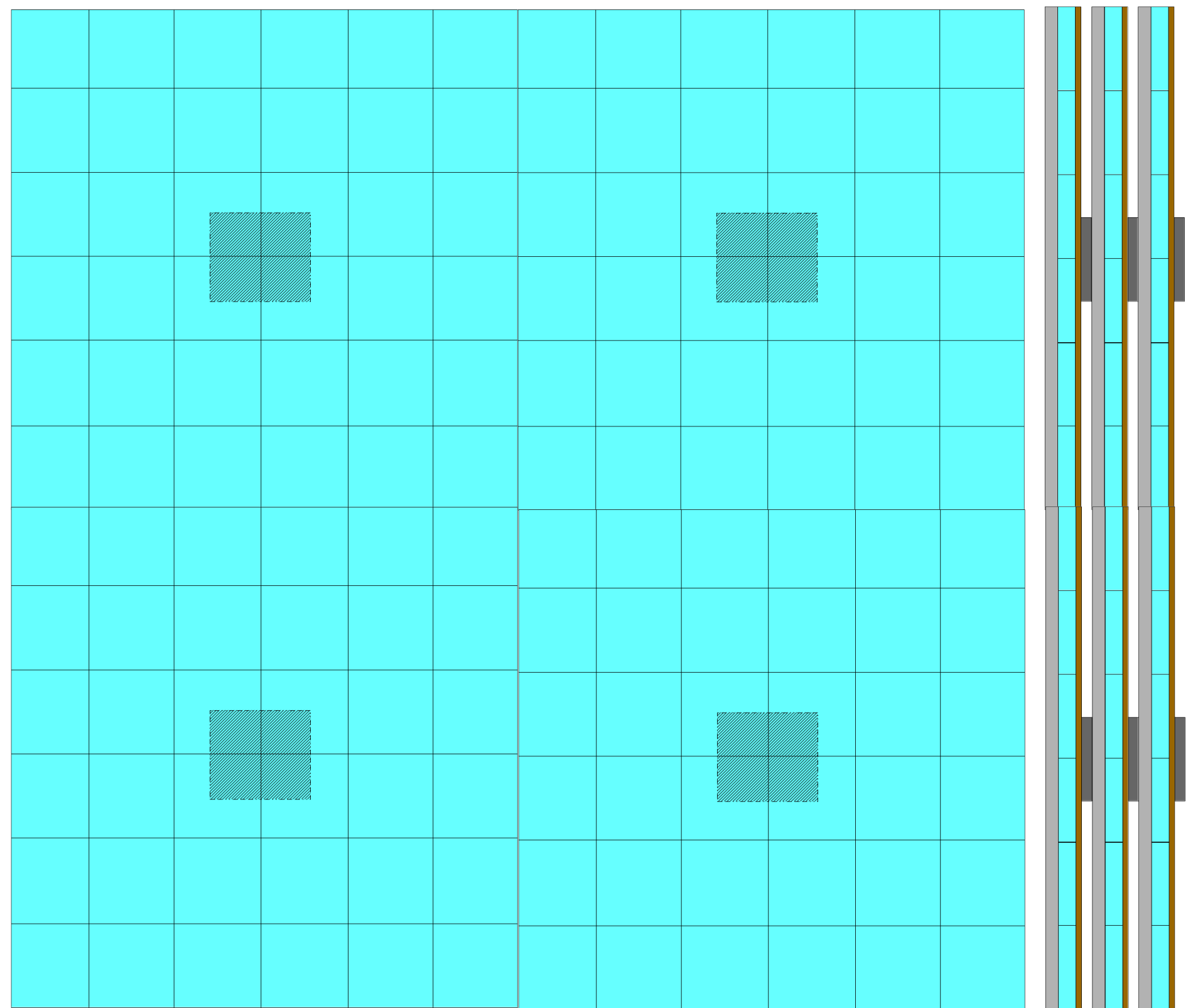

Front View   Side View
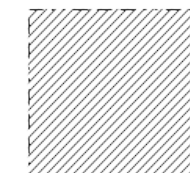
- Scintillator Tiles
- Copper Absorber
- PCB layer
- ASIC

ASIC placement with respect to the Tiles

- 300 alternating layers of:
  - 2 mm thick copper absorber.
  - Polystyrene scintillators of size 30x30x5 mm^3.
  - 0.7 mm thick PCB layer.
  - 2 mm thick Si ASIC of 30x30 mm^2 area.

- ASICS are implemented as Si plates

- ASICs are placed 18 cm (center-to-center) apart.

Implementation of Misalignment

Front View   Side View
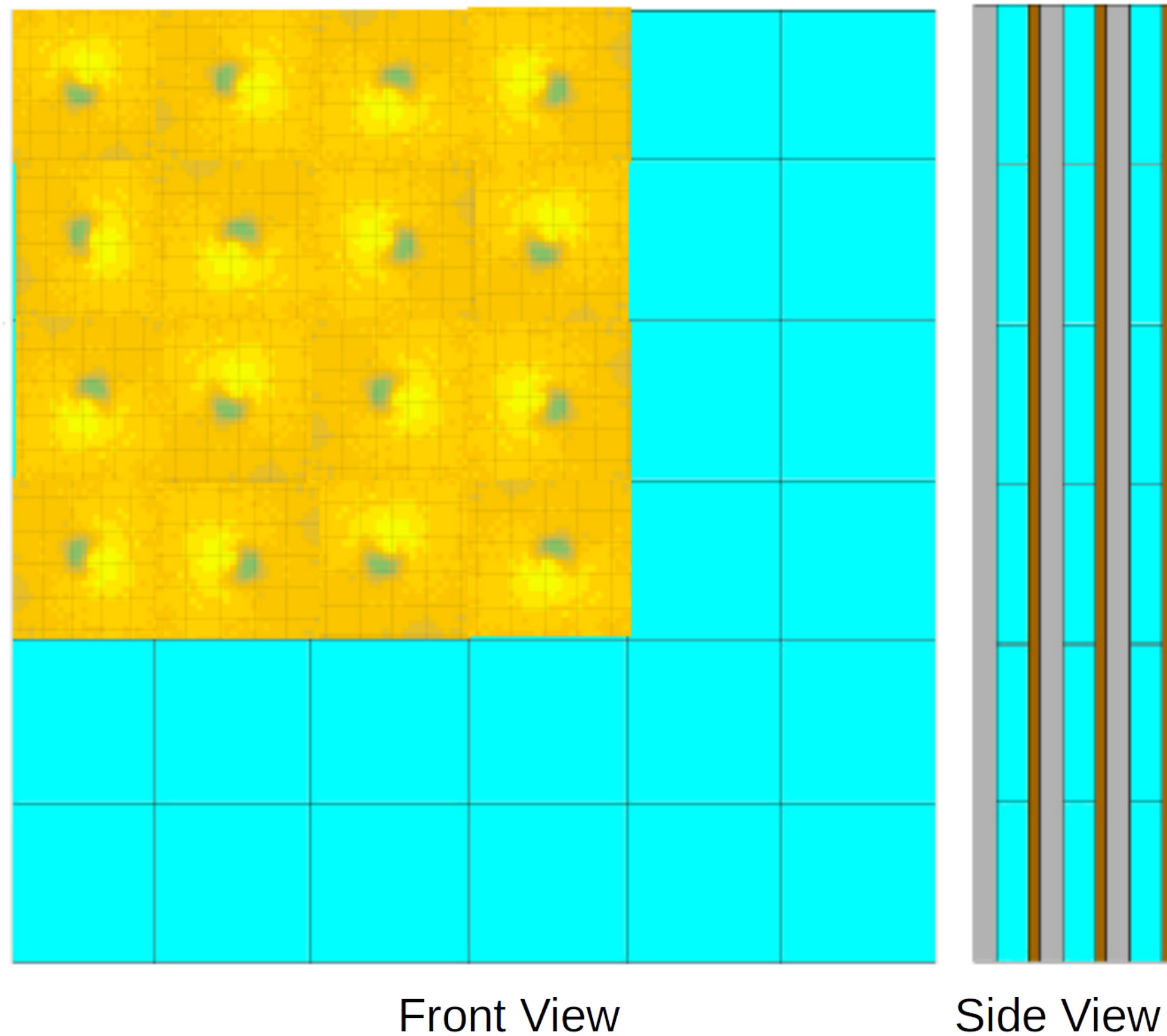
Scintillator Tiles
Copper Absorber
PCB layer

- 300 alternating layers of:
  - 2 mm thick copper absorber
  - Polystyrene scintillators of size 30x30x5 mm³
  - 0.7 mm thick PCB layer
 - 2 mm thick Si ASIC of 30x30x2 mm² area

- Every tile is mapped to a randomly rotated light yield scan of a tile

- After execution of a step in Geant4, scale the energy deposition according to the measured light yield

Study impact of single sources of non uniformity and combinations

Performance with Cu Absorber

- Baseline: Uniform Tile:
  - A perfectly uniform tile with no positional light yield dependence
  - Light yield throughout the tile is 15 p.e.

Comparison of individual sources of non uniformity
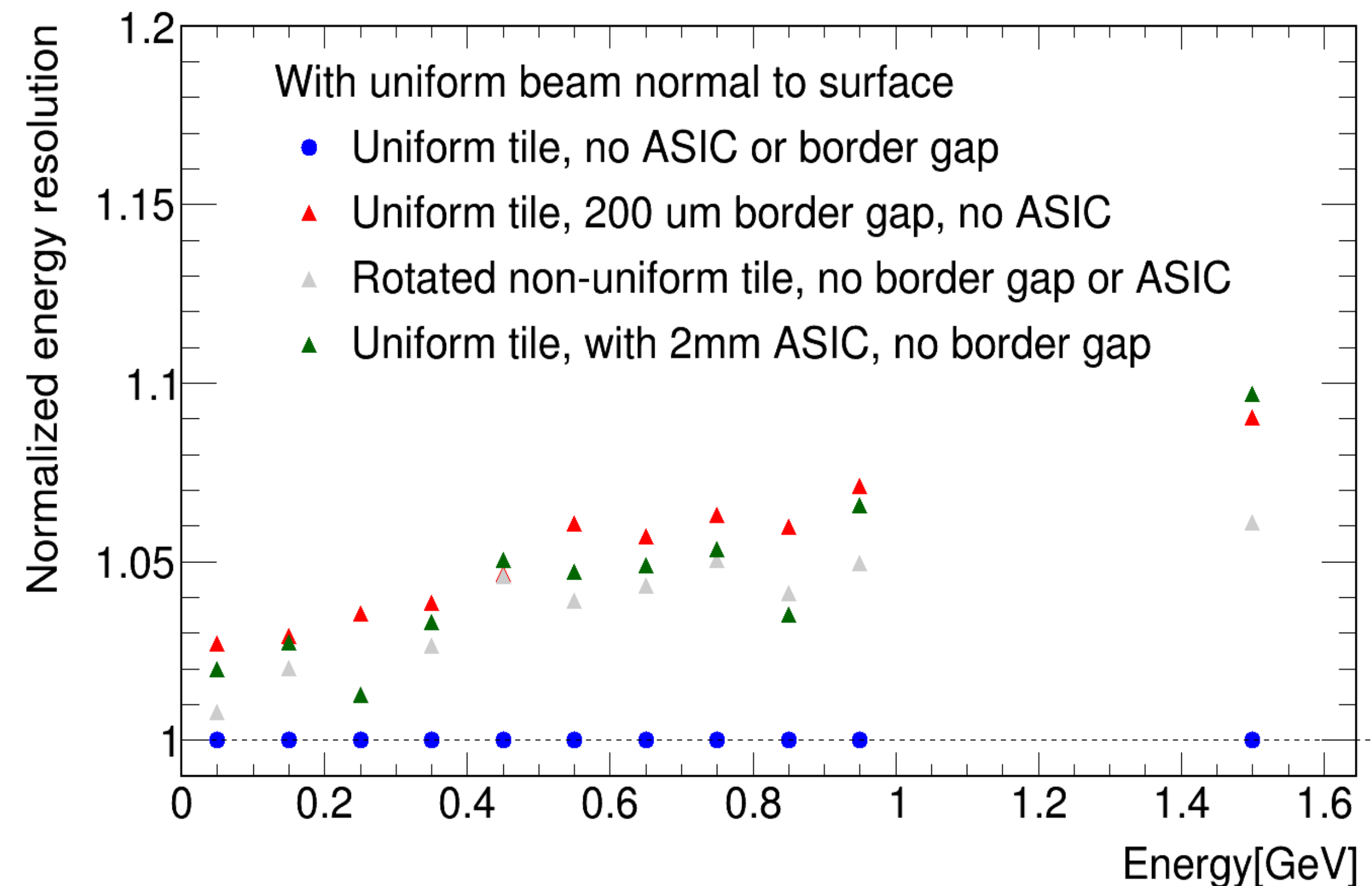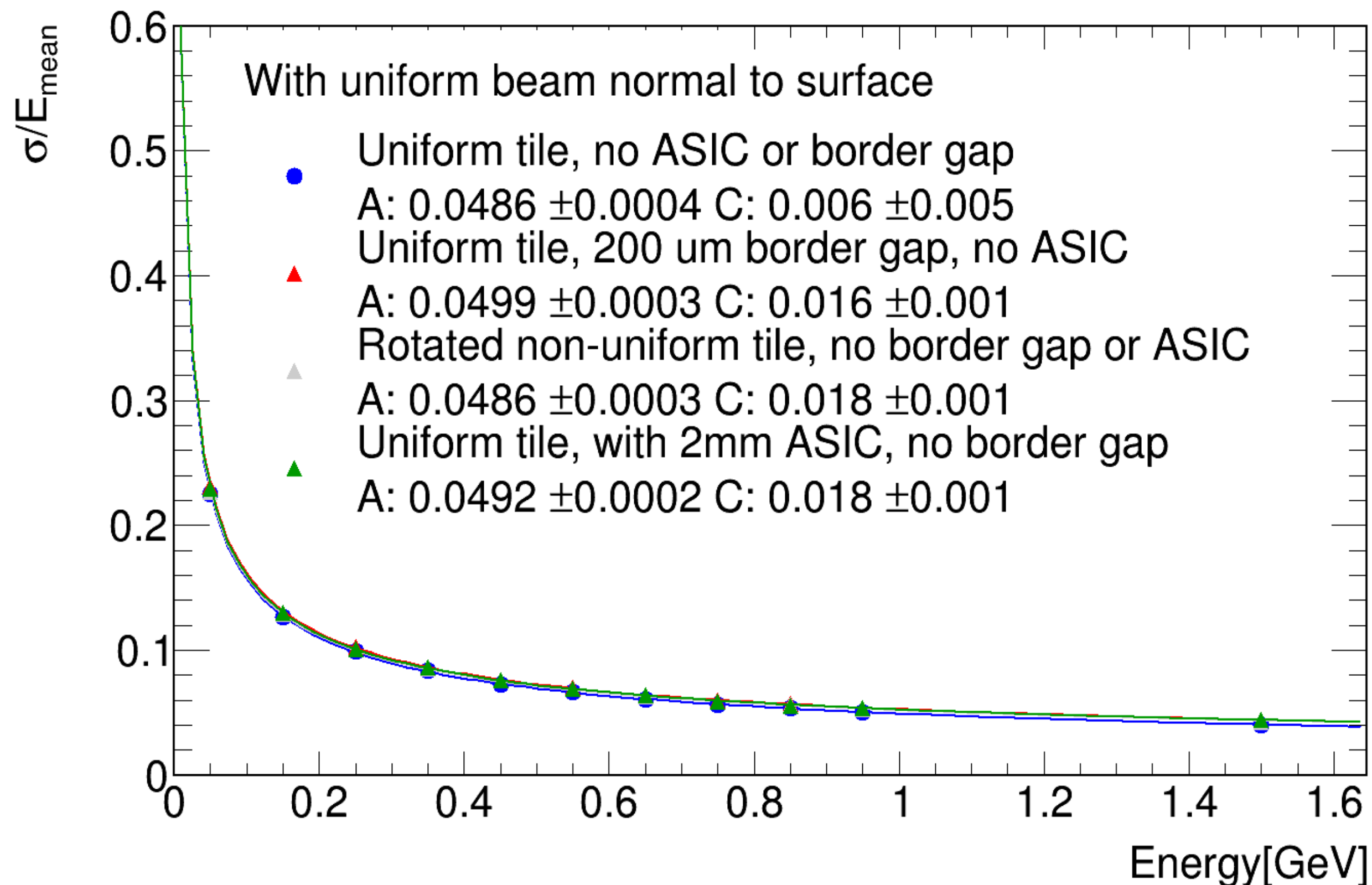
Performance with Cu Absorber

- Baseline: Uniform Tile:
  - A perfectly uniform tile with no positional light yield dependence.
  - Light yield throughout the tile is 15 p.e.

Look at combinations of non uniformities

ECAL with Tungsten Absorber

Front View   Side View

Scintillator Tiles

Tungsten Absorber   ASIC placement with respect to the Tiles

PCB layer

ASIC

Energy range: 5 GeV to 80 GeV

300 alternating layers of:
- 2 mm thick tungsten absorber
- 120 polystyrene scintillators of size 30x30x2 mm^3
- 0.7 mm thick PCB layer
- 1mm or 2mm thick Si ASIC of 30x30 mm^2 area

2,000 photons simulated covering the 4 central tiles uniformly

Including:
- Poissonian photon statistics
- Range cut: 1 mm
- Energy cut: 0.3 MeV

Performance with W Absorber

- Baseline: Uniform Tile:
  - A perfectly uniform tile with no positional light yield dependence
  - Light yield throughout the tile is 15 p.e.

- Comparison of individual factors affecting the resolution
  - Non-uniformity (caused by misalignment)
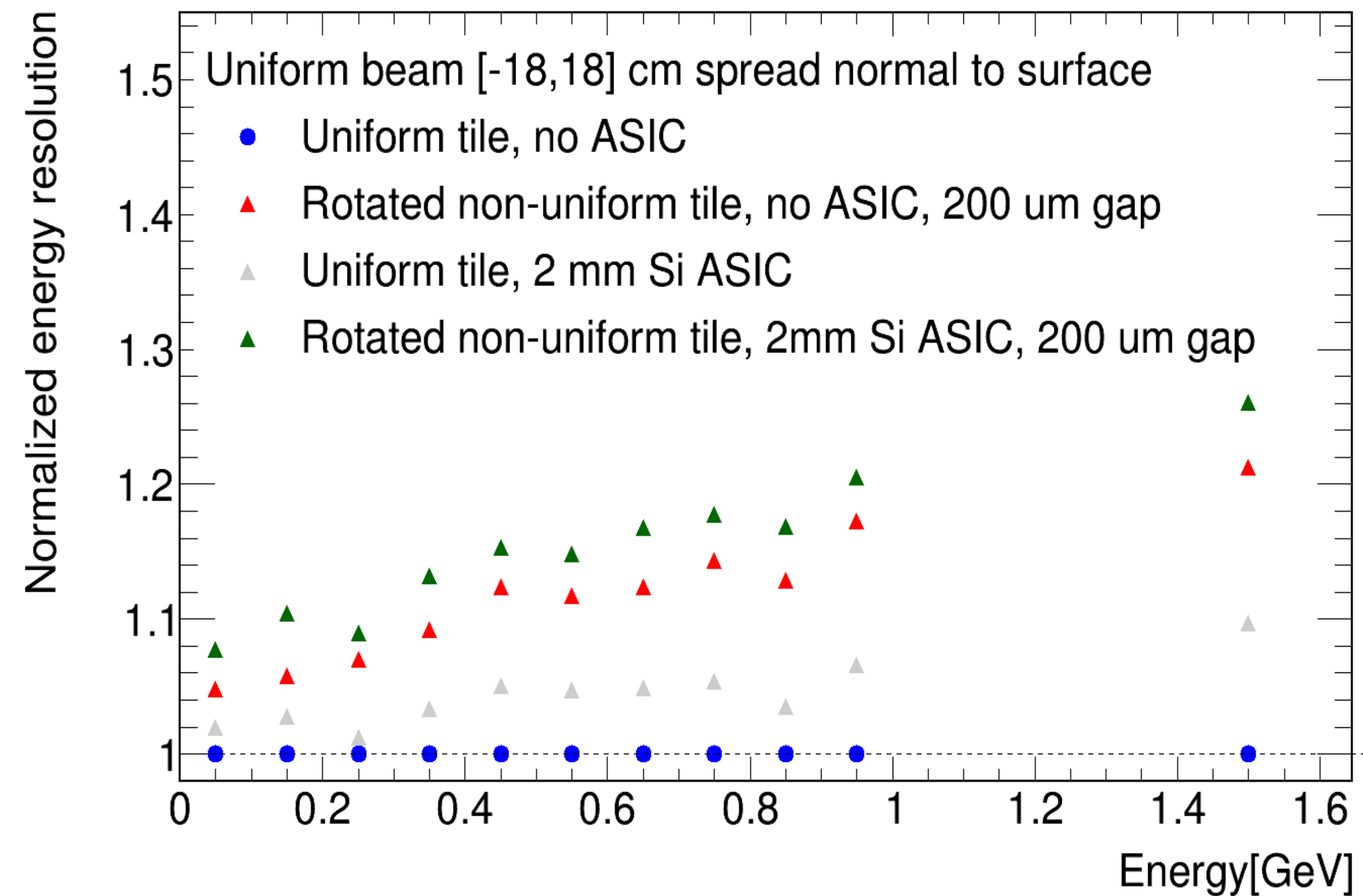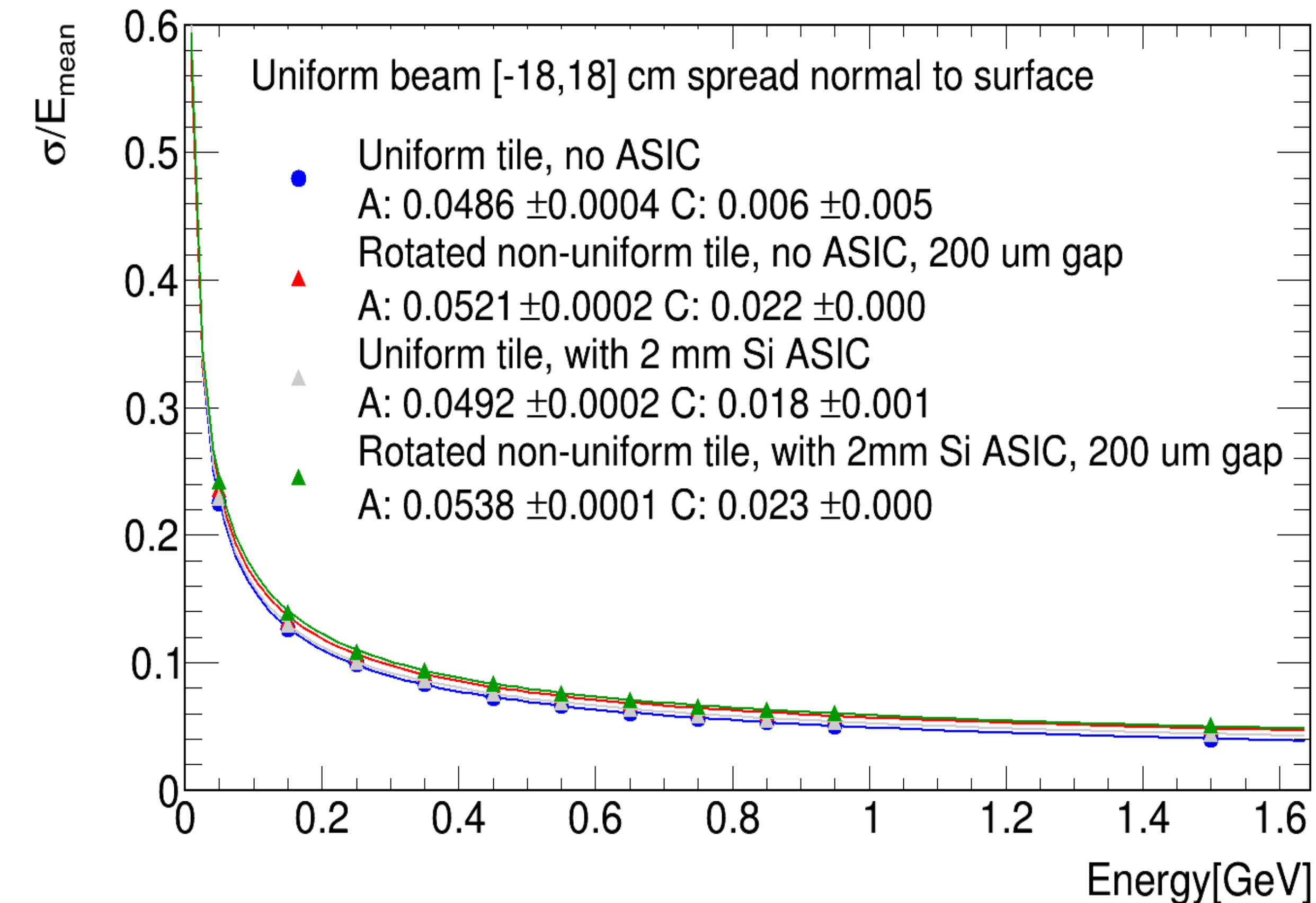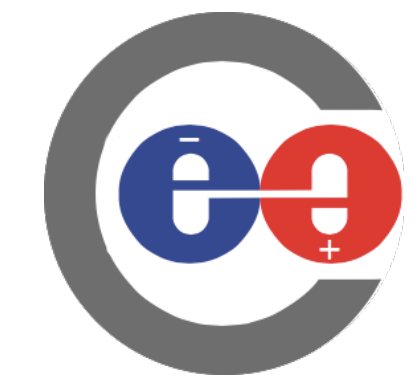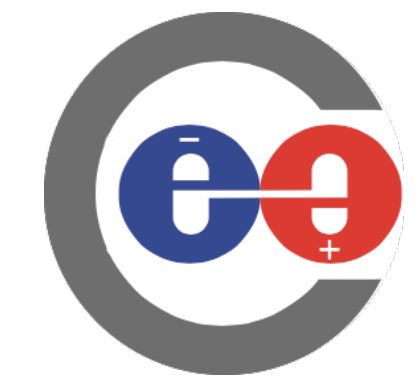 - 200 um border gap
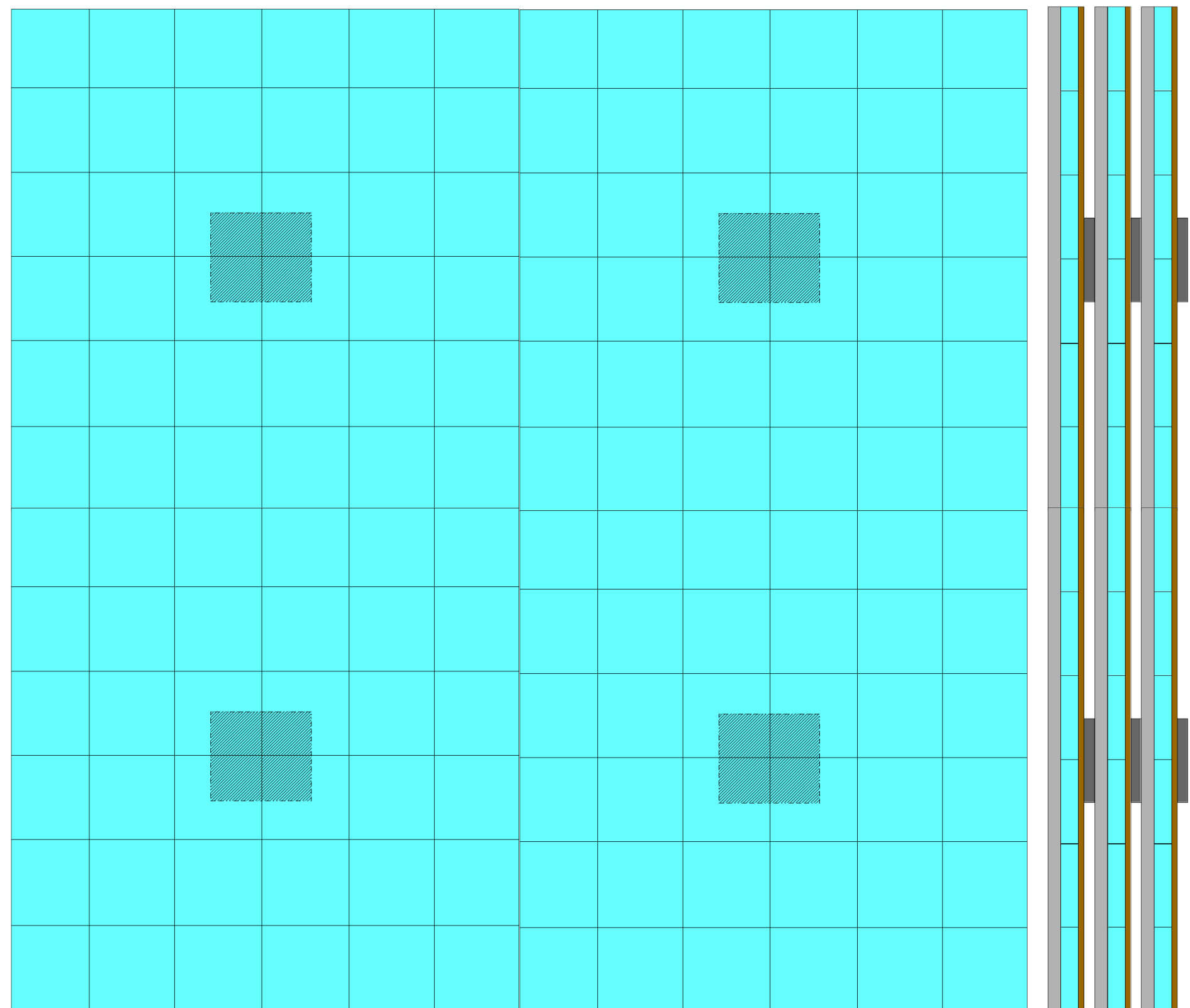 - 2 mm thick ASIC
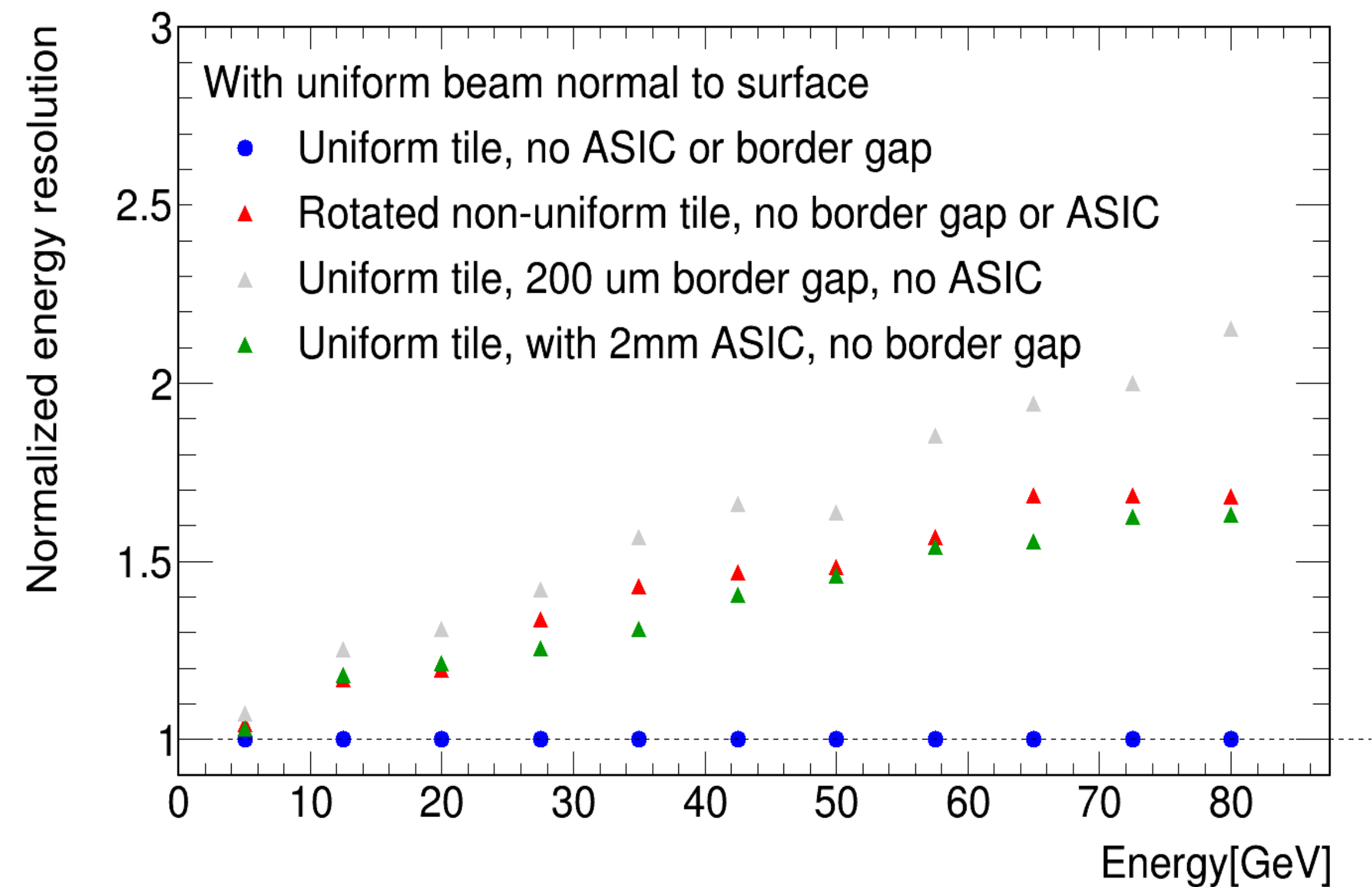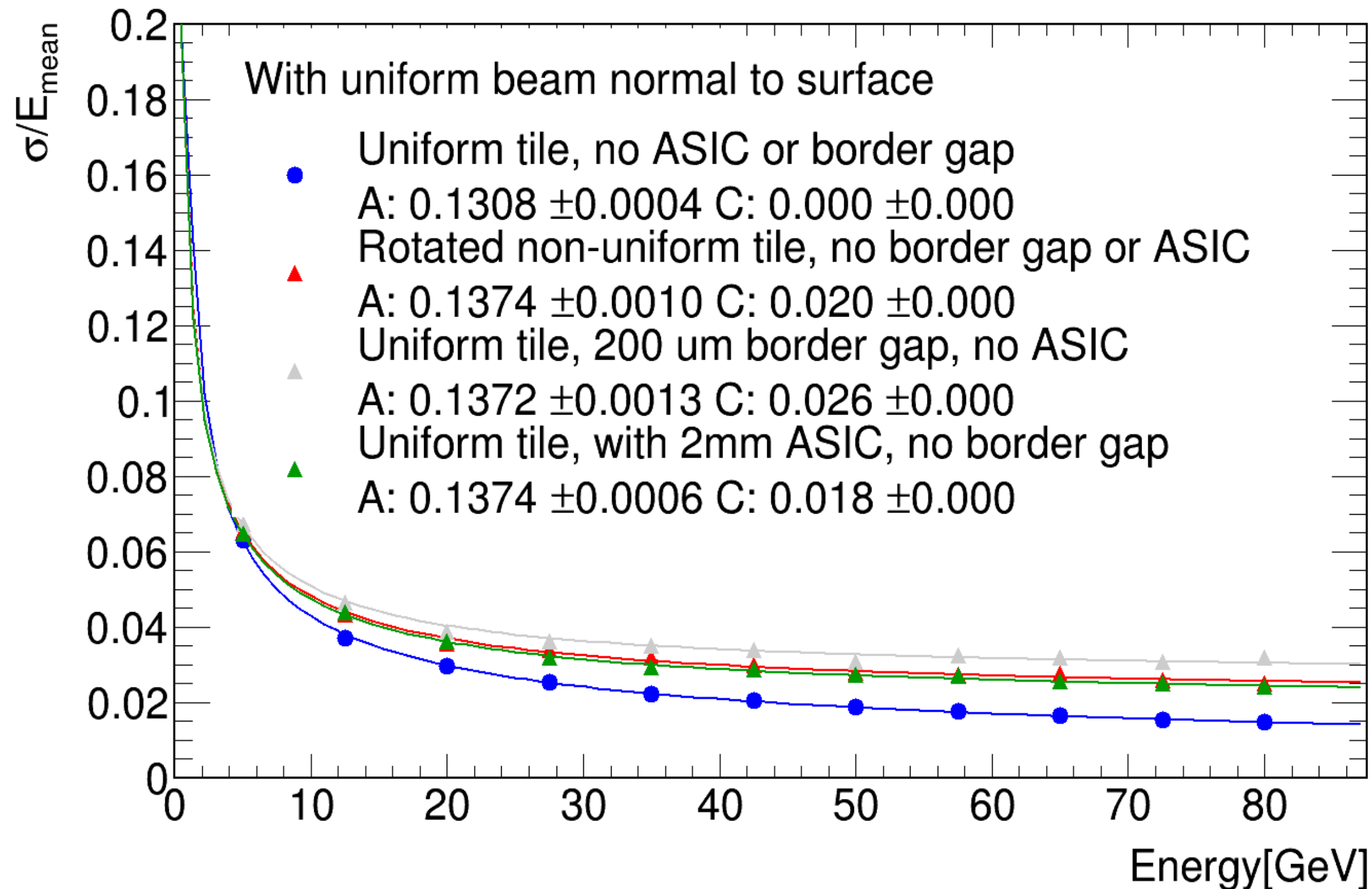
Performance with W Absorber

- Baseline: Uniform Tile:
  - A perfectly uniform tile with no positional light yield dependence
  - Light yield throughout the tile is 15 p.e.

- Comparison of the scenarios with the worst energy resolution
  - ASIC size -> 1 mm and 2 mm
  - Alignment -> best aligned and worst aligned
  - Border gaps -> 100 um and 200 um

With uniform beam normal to surface

- Uniform tile, no ASIC, no border gap
  A: 0.1308 ±0.0004 C: 0.000 ±0.000

- Rotated least misaligned tile, with 1mm ASIC, 100um border gap
  A: 0.1257 ±0.0017 C: 0.037 ±0.000

- Rotated most misaligned tile, with 2mm ASIC, 200um border gap
  A: 0.1420 ±0.0030 C: 0.043 ±0.000

With uniform beam normal to surface

- Uniform tile, no ASIC, no border gap
- Rotated least misaligned tile, with 1mm ASIC, 100um border gap
- Rotated most misaligned tile, with 2mm ASIC, 200um border gap

Conclusion

Copper Absorber

Non uniformities in low energy (50MeV - 1.5GeV) applications (DUNE,…) deteriorate the energy resolution:

- ~ 6% from misalignment wrt to SiPM
- ~ 8% from 2mm silicon ASIC
- ~ 9% from 200 um gap between tiles
- ~ 25% combined

Tungsten Absorber

Non uniformities in high energy (5GeV- 80GeV) applications (collider detectors,…) deteriorate the energy resolution:

- ~ 70% from misalignment wrt to SiPM
- ~ 60% from 2mm silicon ASIC
- ~ 110% from 200 um gap between tiles
- ~ up to 300% combined
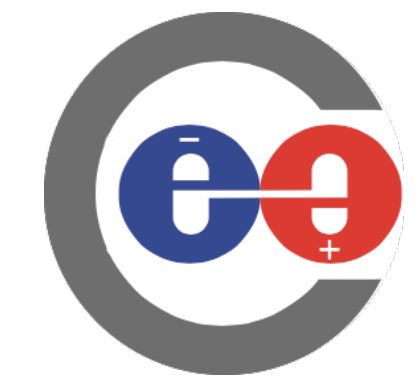- Major impact on constant term: 0 for a uniform calorimeter, 4.3% including all studied non uniformities
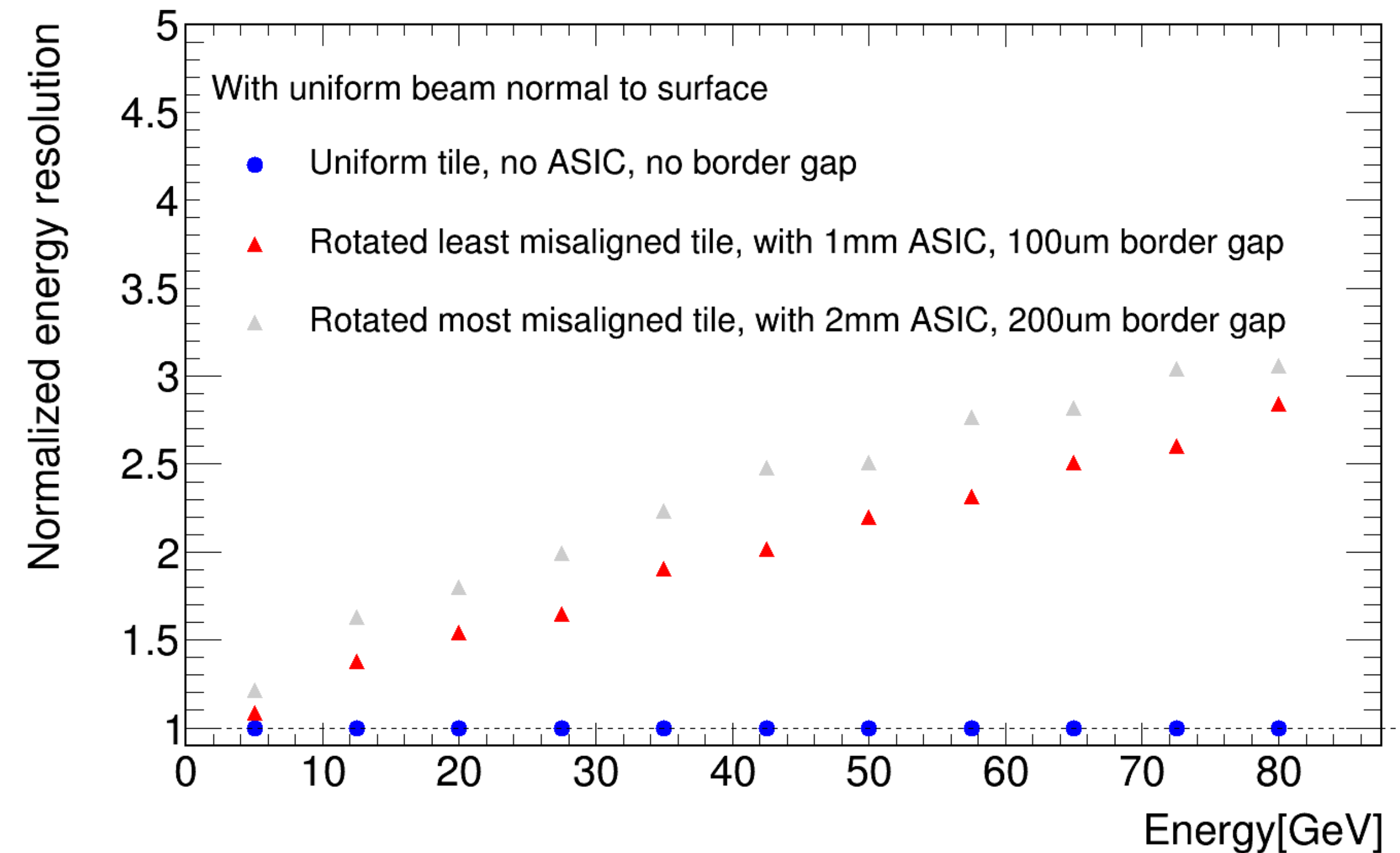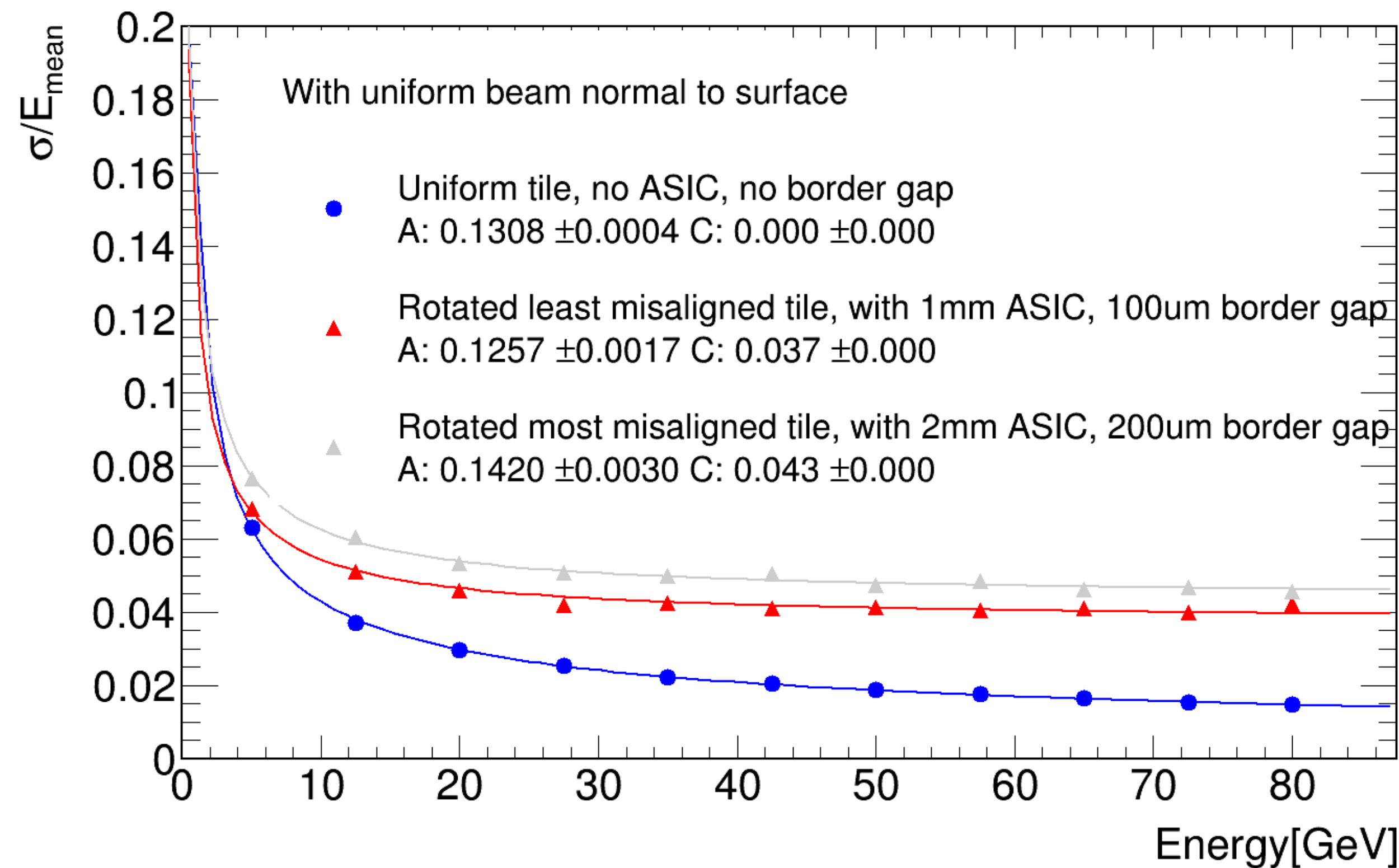
- Baseline: Uniform Tile:
    - A perfectly uniform tile with no positional light yield dependence
    - Light yield throughout the tile is 15 p.e.

- Comparison of border gaps
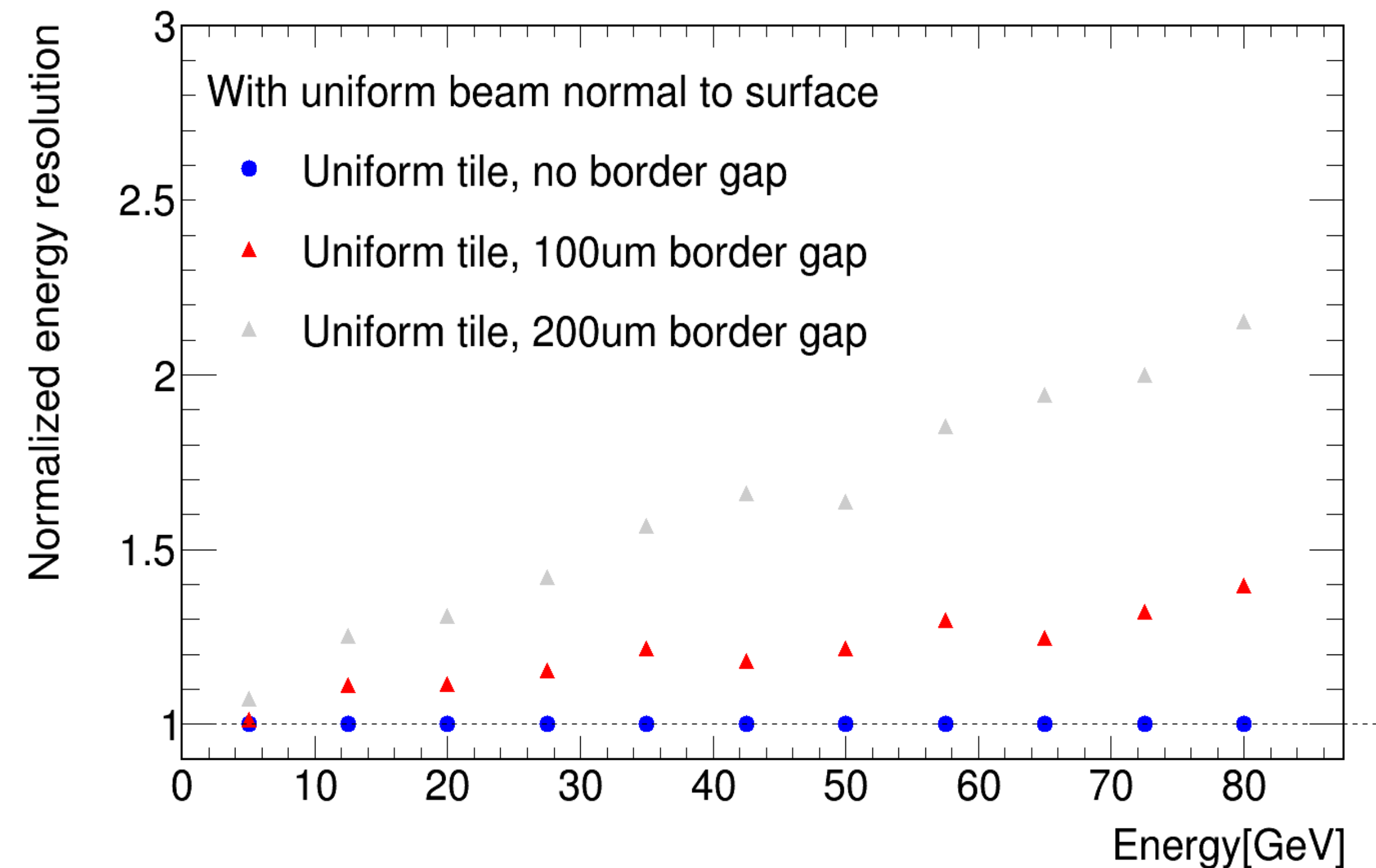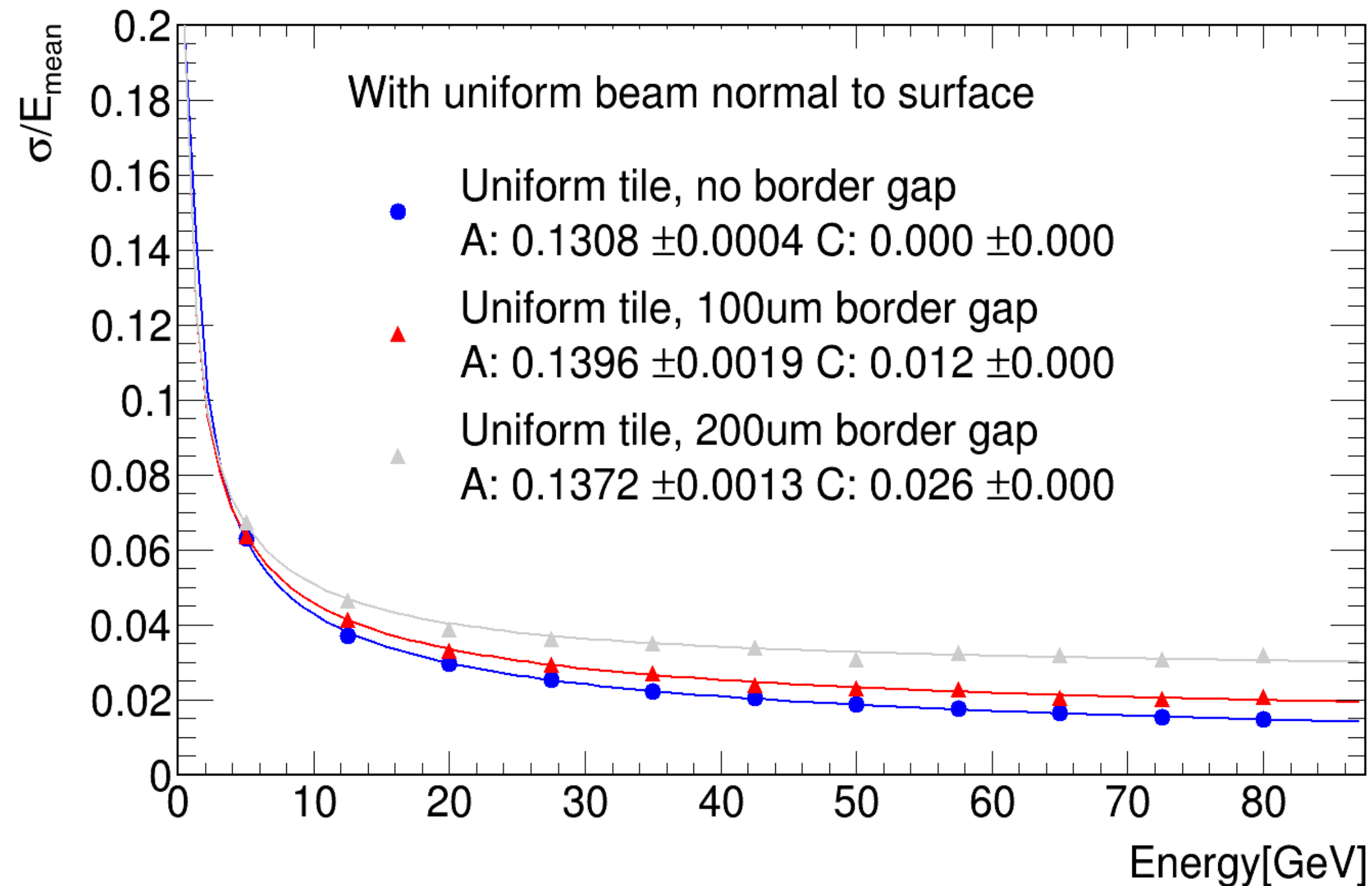
With uniform beam normal to surface

Uniform tile, no border gap
A: 0.1308 ±0.0004 C: 0.000 ±0.000

Uniform tile, 100um border gap
A: 0.1396 ±0.0019 C: 0.012 ±0.000

Uniform tile, 200um border gap
A: 0.1372 ±0.0013 C: 0.026 ±0.000

With uniform beam normal to surface

Uniform tile, no border gap

Uniform tile, 100um border gap
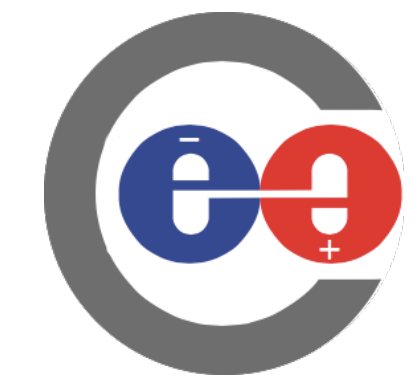
Uniform tile, 200um border gap

Performance with W Absorber

- Baseline: Uniform Tile:
  - A perfectly uniform tile with no positional light yield dependence
  - Light yield throughout the tile is 15 p.e.

- Comparison of ASICs of different sizes

With uniform beam [-6,6] cm normal to surface

Uniform tile, no ASIC
A: 0.1308 ±0.0004 C: 0.000 ±0.000

Uniform tile, with 1mm ASIC
A: 0.1340 ±0.0013 C: 0.013 ±0.000

Uniform tile, with 2mm ASIC
A: 0.1374 ±0.0006 C: 0.018 ±0.000

With uniform beam normal to surface, no border gap

Uniform tile, no ASIC

Uniform tile, with 1mm ASIC

Uniform tile, with 2mm ASIC