SiW Ecal Compact Digital Readout Electronics

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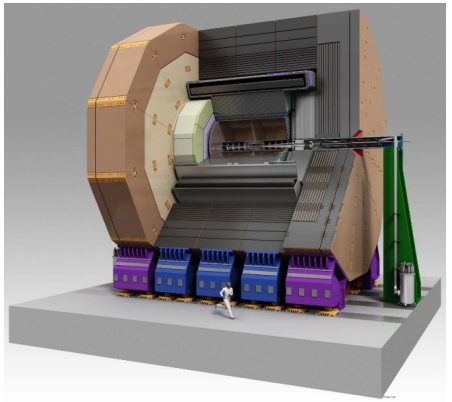
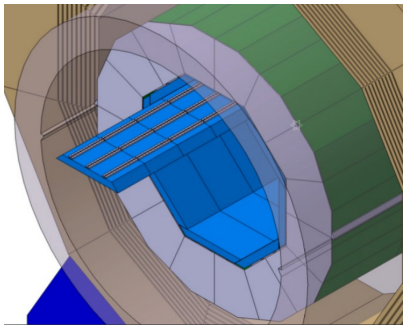
Introduction

- Description/ status of the new SiW Ecal compact digital electronics
  - SL-Board + Kapton interface
  - CORE module : Control and Readout
- Implementation in last test beam : June 24th – July 7th 2019
- Preparation for next test beam
- Future plans





Reminder: Constraints on Readout Electronics

Spatial constraints for the Active Sensor Units (ASUs)

- Very limited space **between layers (depending on the total number of layers)**.

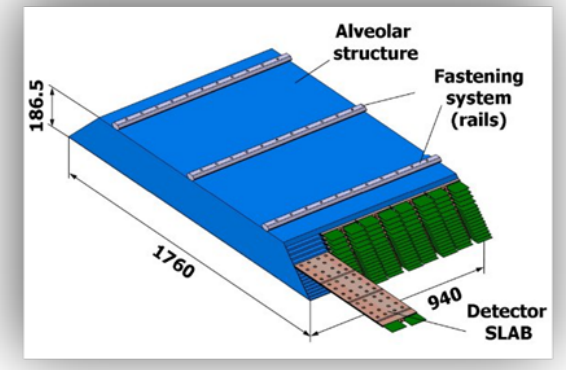
➢ Two protoype versions have been realized with different SKIROC packaging and thickness:

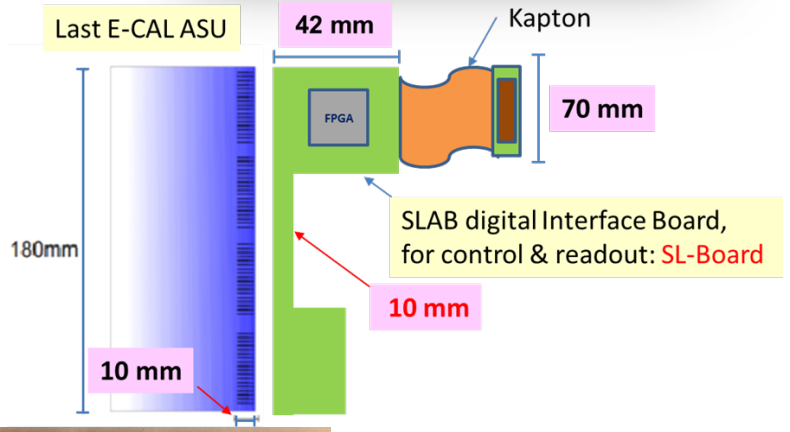
✓ BGA option : PCB + components*(1,2 mm)* + connectors = **~ 3,2 mm**

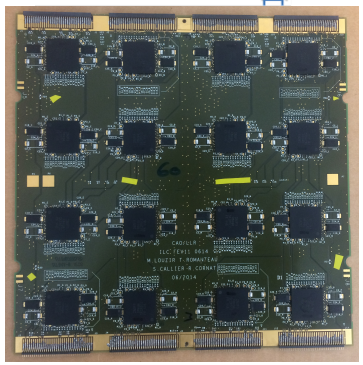
✓ COB (Chip On Board) option : PCB and ASICs **= 1,2 mm** + connectors = **~2,3 mm**

Constraints for the Slab Interface Board (SL-Board)

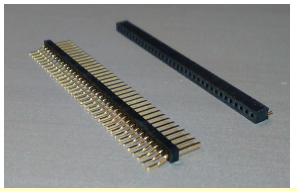
- The SI-board will be installed between ECAL and HCAL, separated by only 67 mm
- L-shape because of the cooling system
- Maximum Height : **6 to 12 mm depending on the location**
- **Control & Readout electronics at the extremity of the Slab**
- Signal Integrity over a Slab : up to 15 interconnected ASUs
- Very low Power consumption (~ 150 mA/ Slab) : needs to run in **power pulsing mode**





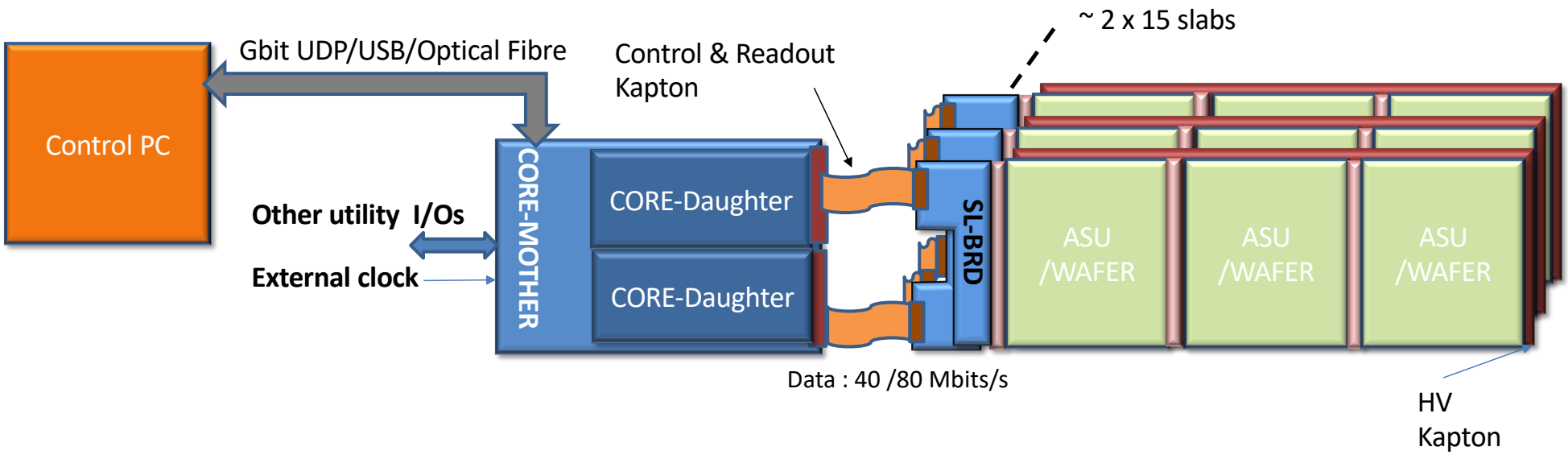


ASU: FEV 11, with Skiroc BGA option, and the gradconn connectors



Gradconn connectors (1,5 mm high)

Global Architecture Scheme



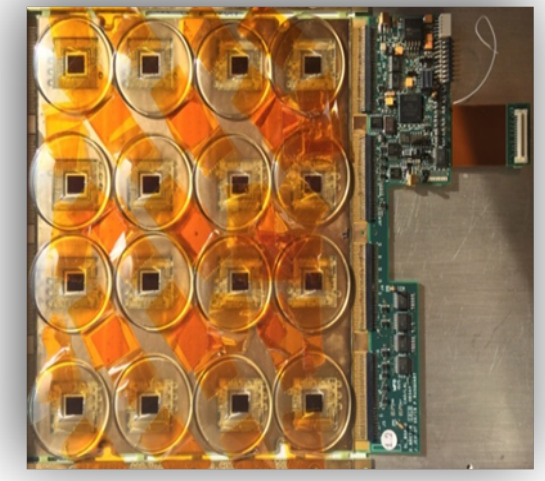
CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab

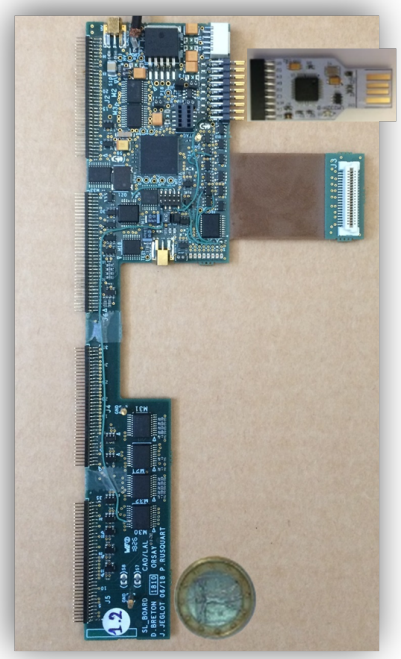
External clock and Utility I/Os : possibility to be synchronised with other systems!

The SL-Board

The **SL-Board** is the sole interface for the **~10,000 channels of a slab :**

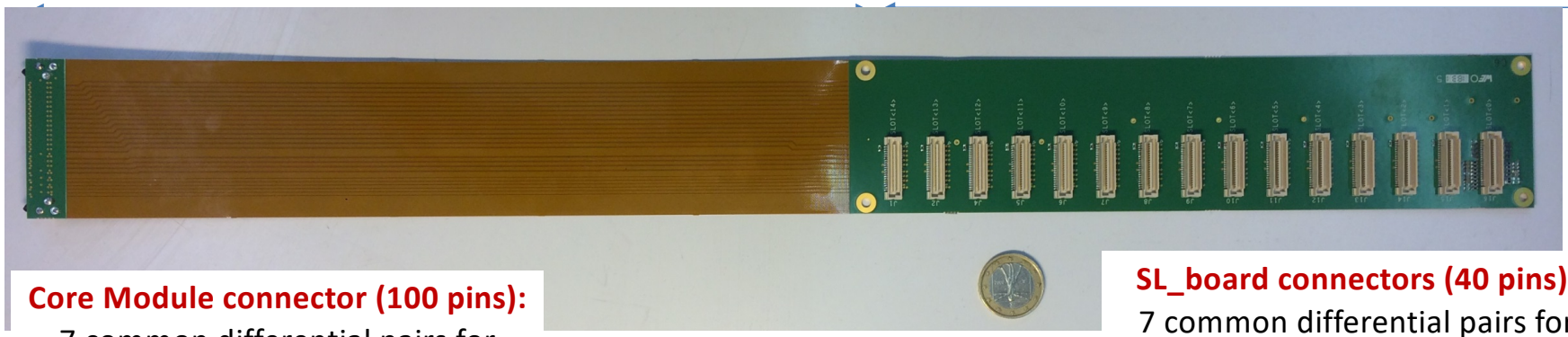
- It delivers the **regulated power supplies,** including **High Voltage**, **controls** the SKIROC ASICs, and **perfoms the full data readout**.
- It is connected to the CORE-Kapton via an internal **kapton layer** and a 40-pin connector.
- It is based on a **MAX10 from ALTERA**, which is a mix of CPLD and FPGA.
- It includes an ADC which will be used to monitor the pulsed power supply.
- Very size **limited:** 18 cm in width, 10 to 42 mm in length.
- Its **own power** consumption is **< 1W**
- It can also be an **autonomous system** with direct computer access for testing and characterization purposes (using the **FTDI USB module**).





The SL Board Core-Link (Core-kapton)

CORE side — Flexible kapton — Total length ~40 cm — Slab side (~22cm, rigid, pitch of 15mm)



Core Module connector (100 pins):
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

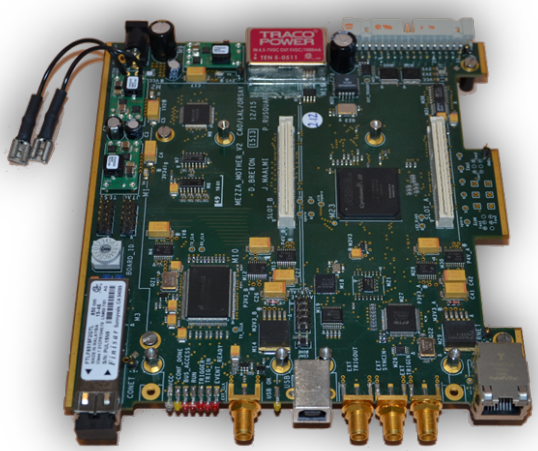
SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

- The **CORE kapton** measures 40 cm. It is the **interface** between the CORE Daughter and the SL-Board. It permits driving and reading out **up to 15 slabs**.
- It transmits all the **clocks and fast signals**, and houses the control and readout links.
- It handles the **synchronisation** of the **15 slabs**.
- The Kapton Interface makes use of **asynchronous serial transmissions** in order to greatly simplify the synchronization of the numerous control and data links.
- The speed of the slow control and the individual readout links is : **40 Mbits/s**
- Reminder : readout link of the ASUs **: 2 x 5 MBits/s**

The CORE Module

The CORE Mother:

- The **Control and Readout Motherboard** have been developed for housing up to 2 **Mezzanines**: it permits separating the **acquisition** part from the specific front end part.
- **External** input and output signals permit **synchronising** or interfacing the module with other systems.
- The CORE mother sends common clocks and fast signals to the Core Daughters to keep the **system synchronised**
- The control and readout is possible through **USB(2.0)**, Ethernet (secured UDP) over copper **or Optical link**
- The CORE module **power consumption** is **5 W**

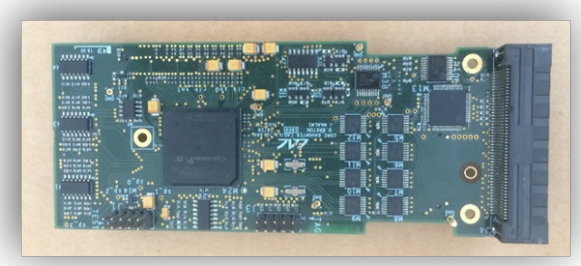


The CORE mother

The CORE module

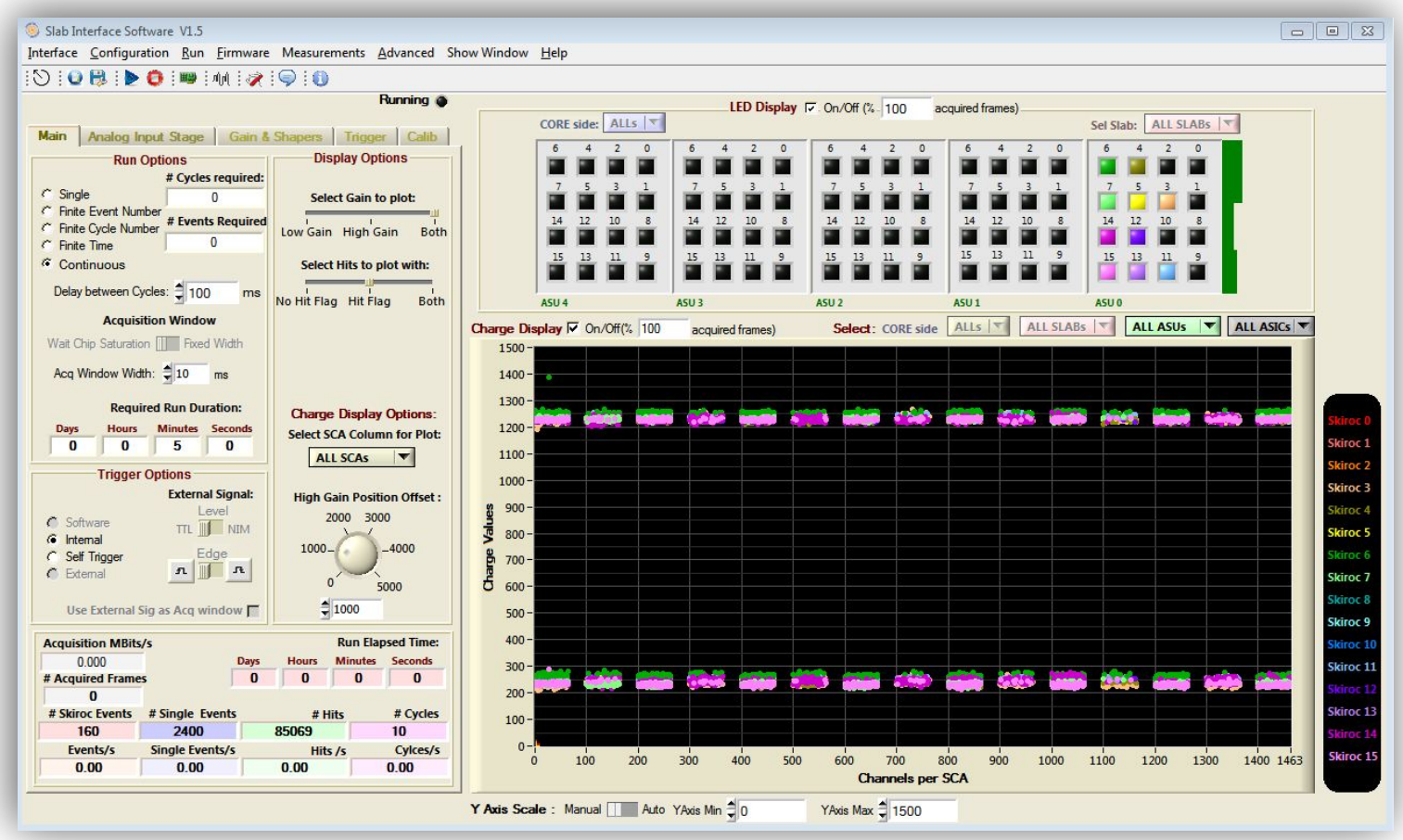
The CORE Daughter:

- The **CORE Daughter** is based on a Cyclone IV FPGA. It is the interface between the CORE motherboard and the Kapton which permits driving and reading out **up to 15 slabs**.
- It buffers all the clocks and fast signals, and deals with the control and readout links through the Kapton Interface.
- It houses the second level of **event buffers** (derandomizers).
- Ctrl & Readout link between CORE Daughter and CORE Mother **: 60 MBytes/s** if USB**, and 125 Mbytes/s** if UDP**.**



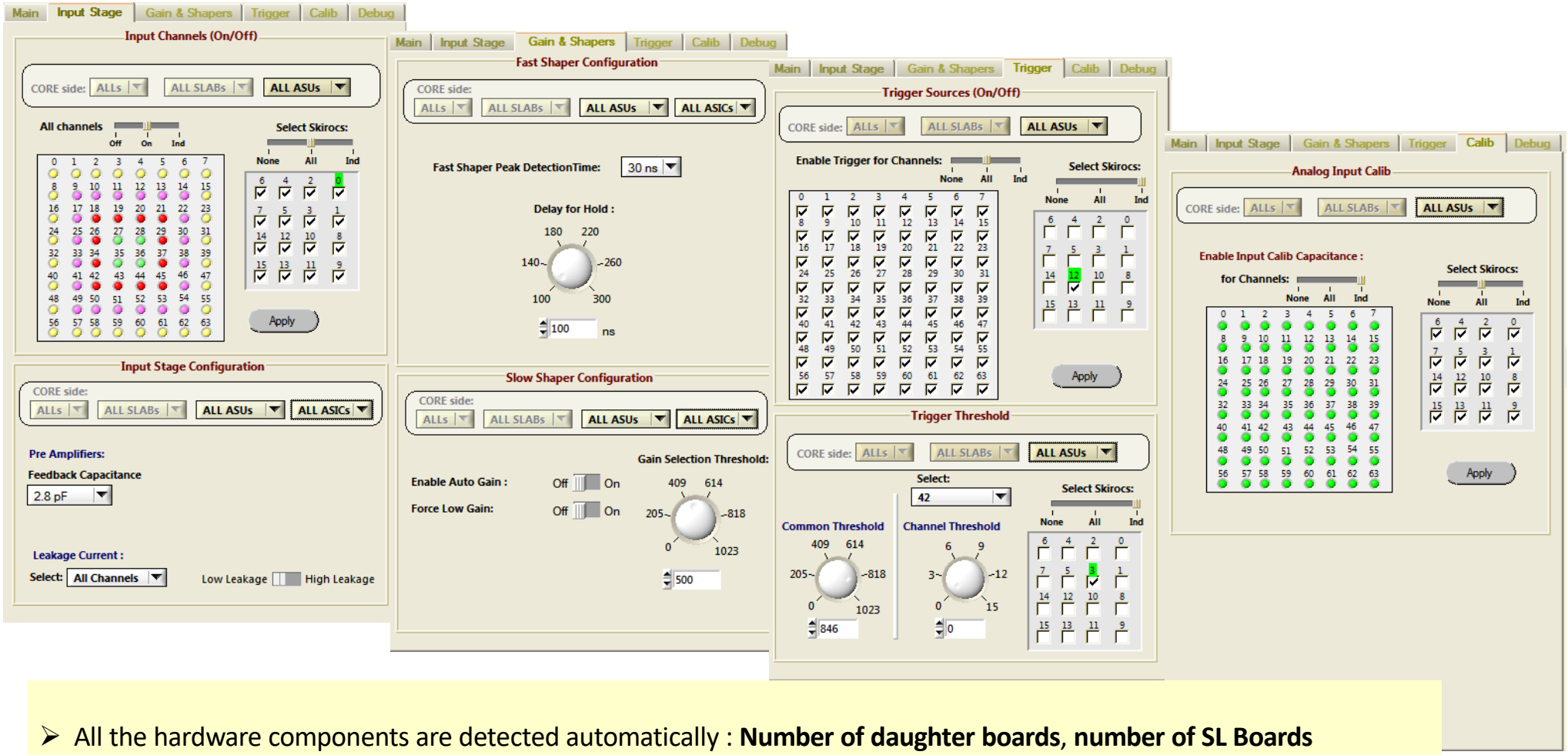
The CORE daughter

Acquisition Software



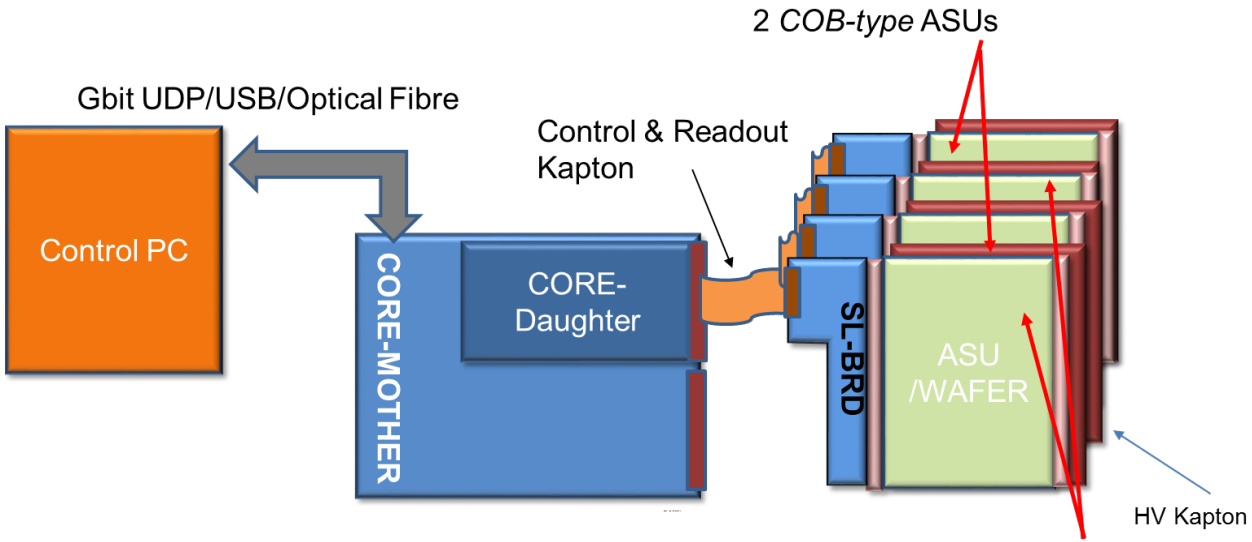
- The Software can handle the communication through FTDI connector **or** through **CORE Module**.
- It handles the **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**
- Advanced measurements can be performed Online such as threshold scans…
- The C-functions that handles the communication (readout and configuration) can be used as a a library with any other program that handles C-langage.

Slow Control



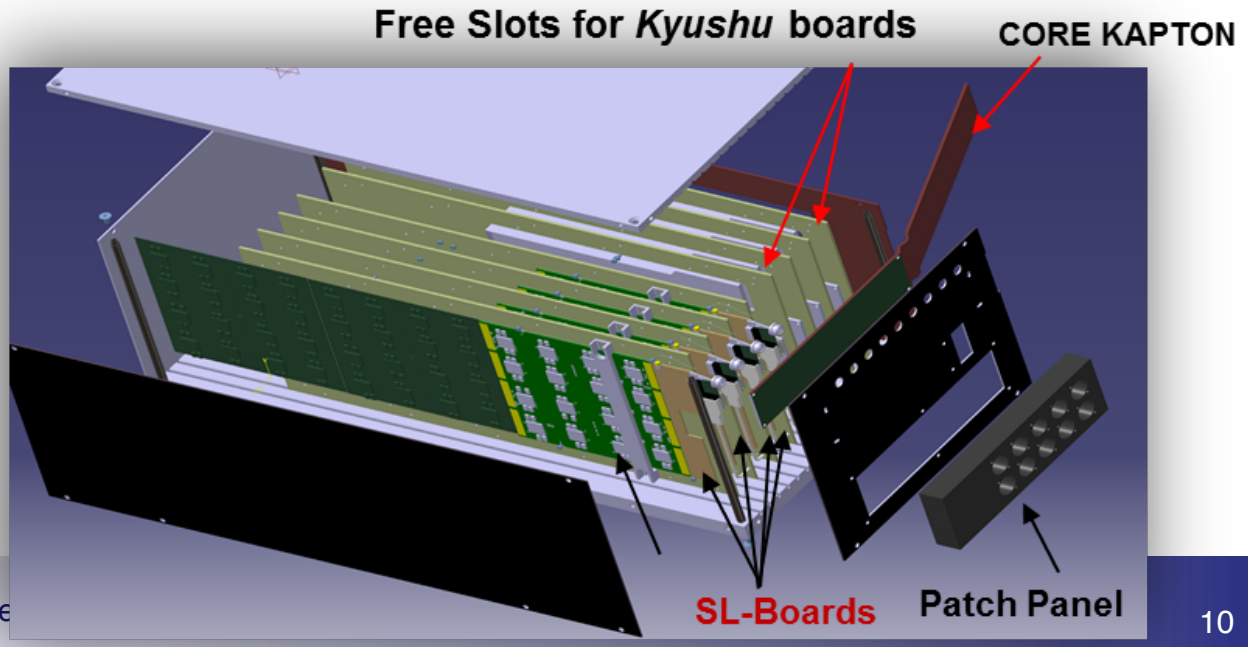
- All the hardware components are detected automatically : **Number of daughter boards**, **number of SL Boards** connected to each daughter board, and also the **number of ASUs** on each slab using **slow control readout**.
- **Slow Control**:
  - All necessary slow control **parameters** can be programmed through the Software
  - Slow control configuration is checked by writing twice the same values to the SKIROC shift regiser and reading back the pushed value on the SROUT signal.
- Control and data Readout with **direct connection** to the SL Board via FTDI module or through the **CORE module**.

Implementation in the last test beam (July 2019)



CORE *Module/Mother/Daughter* : Control and Readout
SL-BOARD : Interface board to Slab

- **Cycles** and **acquisition windows** are programmable and generated by the CORE Module.
- All ASUs run **synchronously**.
- Possibility to check **buffer overflow**



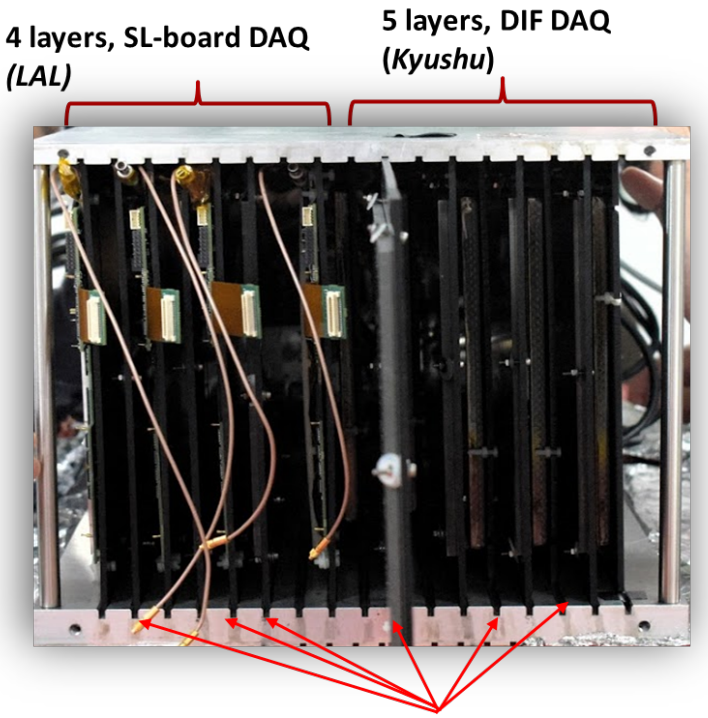
Test beam at DESY: June 24th to July 7th

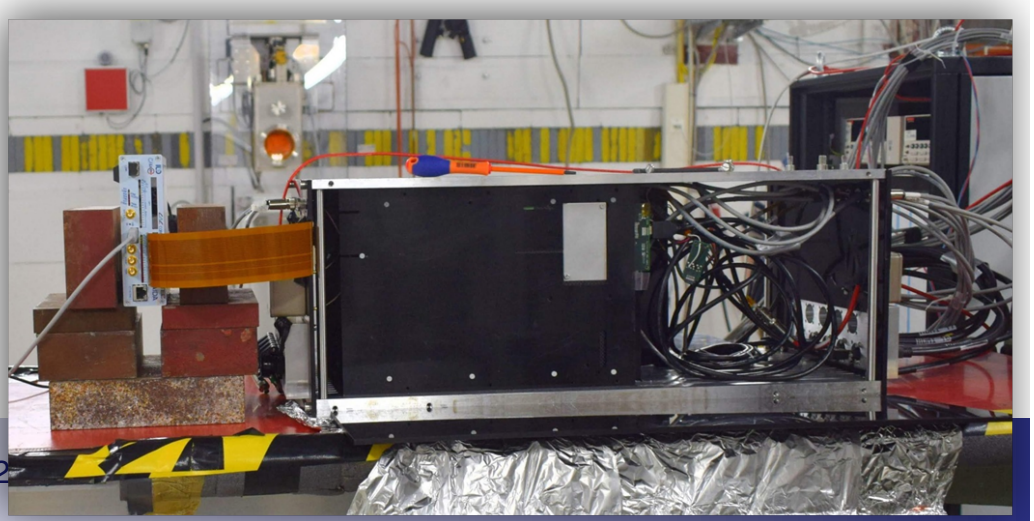
- Number of Layers in the prototype box: **4 Layers** running with SL-Board DAQ, and **5 Layers** with DIF DAQ.
- 4 Layers readout with the SL-Board/Core Module DAQ :
  - 2 ASUs (***COB option***) with **500um Si wafers**
  - 2 ASUs (***FEV12***, *BGA option*) with **500um Si wafers glued at LPNHE**
- 5 Layers (Kyushu) readout with the DIF DAQ (SMBv5):
  - 4 ASUs (FEV13) equipped with **650 um Si Wafers**
  - 1 ASU (FEV13) with **320um Si Wafer**.
- The **Front End** ASICs used are **SKIROC** version **2a**.

- **Two weeks** of testbeam.

- First **individual runs**, then **common runs** of the 9 Layers using a **common external signal as Start/Stop** of the acquisition window of the Front End ASICs.

- Tunsgten plates added during the second week between the 9 Layers.



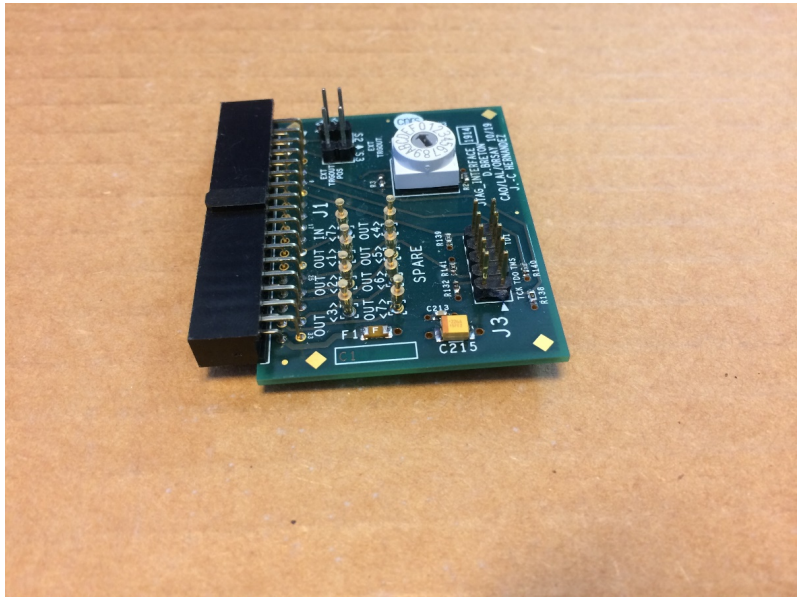


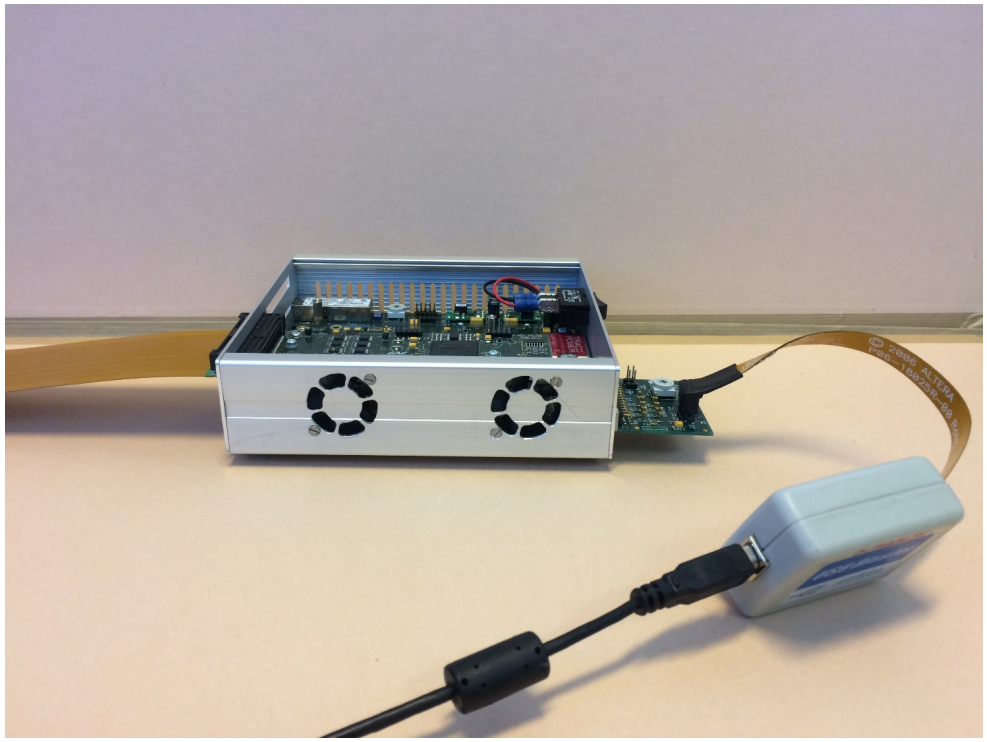
What we learnt from the test beam

- **Firmware :**
  - Some errors in the events were due to the « Enable_Trigger » during the acquisition phase. (Thanks S.Callier for the tip)
  - **Need to program the firmware of the SL Board without opening the box:**
    - **JTAG adaptor board** designed in order to **program** the SL Boards firmware through the CORE Module via the CORE Kapton.
- **Software:**
  - Improvements for test beam: saving/loading settings to/from ASCII files
  - Online Charge histograming and pedestal measurements
- **Hardware**
  - SL Board V2 → see next slides
  - A prolem with a Resistor that should have been removed on the FEV12. (added an offset in the Threshold..)
- **Mechanics:**
  - Improvement of the prototype box: modification of the front panel for giving a better access to all connectors of the SL Boards.
  - Better fixation for the ASUs
- **Preparation of the next test beam (March 2020 ?):**
  - More layers: Goal to reach 15 Layers
  - More calibrations and commissionning before test beam (tests with muons, calibrating noisy channels..)
  - **Full synchronisation with an external system:** same clock and anquisition window

Programming Firmware through CORE module: The JTAG Interface Board

- We designed this board in order to program the SL Boards Firmware through the CORE Module via the Core Kapton.
- We can program **all the SL Boards at once** (encoder wheel add = 0xF) or one by one.





Going from SL_Board V1 to V2

Experience from beam test permitted **upgrading the design** of the SL_Board:

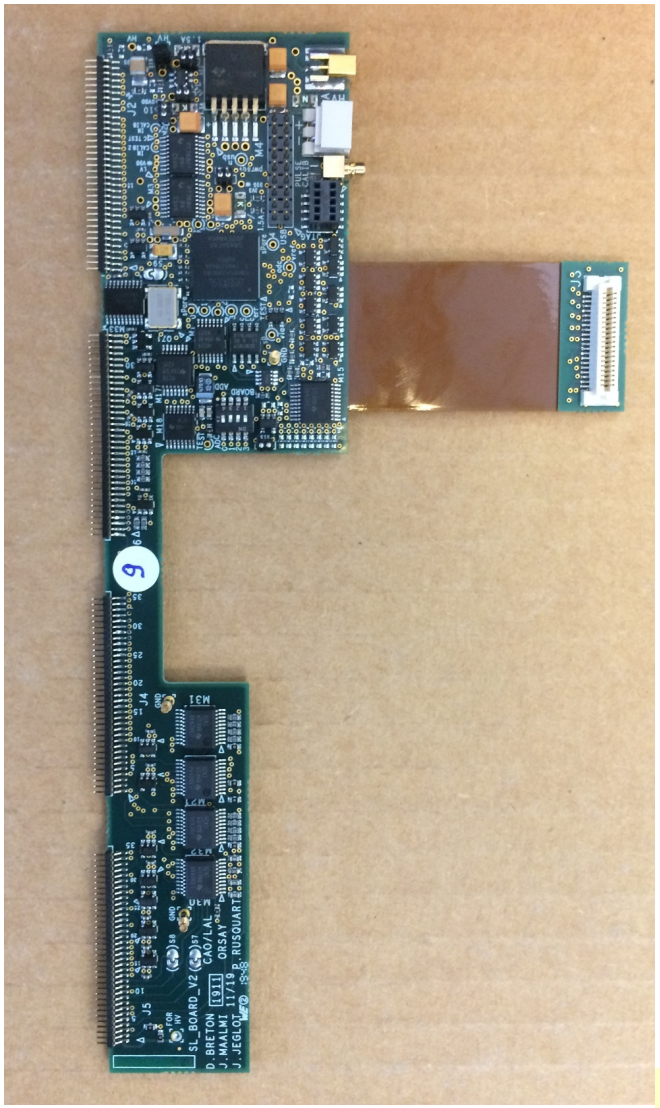
- All useless circuitry has been removed and the rest optimized
- Kapton length has been raised from **40** to **48 mm** (this will **ease the plugging to the kapton**)
- The main input plugs are moved next to the kapton (HV and calibration pulse in MMCX)
- The connector for the FTDI USB module is changed and moved => takes less space, easier to handle
- A more robust LV connector has been mounted which permits using thicker wires (we had a large voltage drop with the old ones)
- A **switch** has been added to encode the **slot number**

- We added:
  - a **DAC for SKIROC ADC calibration**
  - a **flash EEPROM** for permanent information storage: Serial Number

- The FPGA can produce **pulses** for **autonomous functional calibration of both gains**

- The **HV will be made available on the SL_Board** to ASU connectors (both sides)

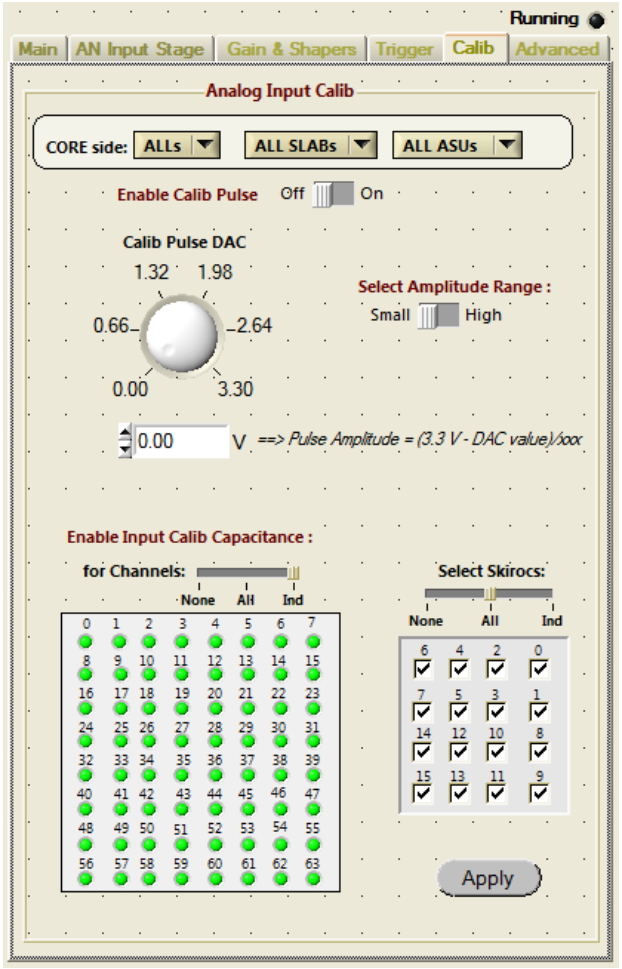
SL Board V2



- 20 boards have produced and equiped.
- Almost all the functionalities have tested and validated:
  - Communication through FTDI and CORE KAPTON
  - Firmware programmation trhough CORE KAPTON.
  - Calibration pulses (see next slide)
- Still need to be tested:
  - FLASH eeprom
  - Power pulsing mode using the current limiter.

15 SL Boards already tested and successfully validated !

Calibration Pulses

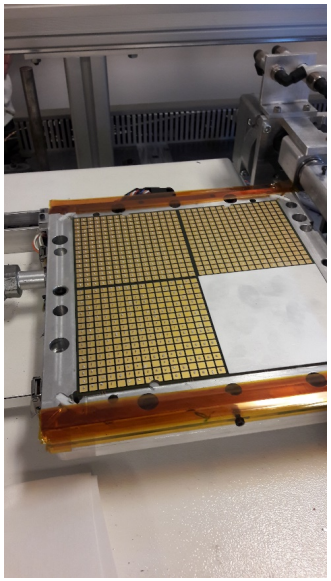


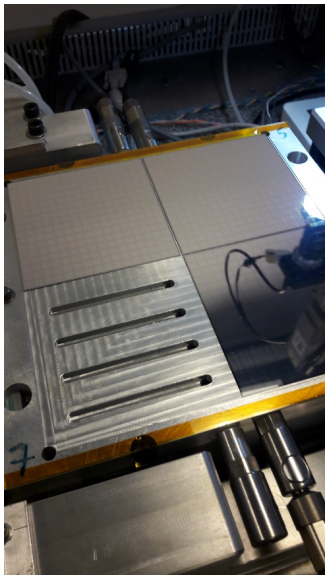
- We have two ranges of amplitudes: in order to test High and Low Gain.
- Thanks to the DAC on the SL Board, we can send Pulses with Amplitude from ~few mV to ~150 mV.
- The FPGA can generate equidistant pulses with known distance:
  - Permits testings the synchronization between multiple layers
  - we can study the Re-triggers…

➔ Thanks to this feature we can adjust the Common Threshold/ ASIC and the individual thresholds for each channel to trigger on ~0.5 p.e

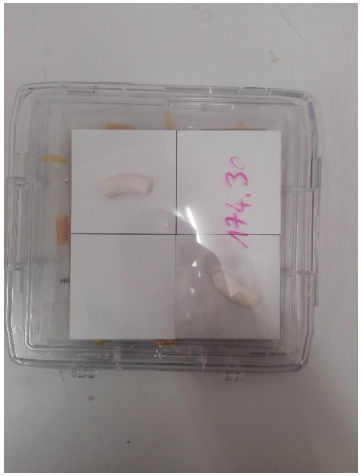
Towards 15 layers …

- We are gathering the highest possible amount of ASUs for the next test beam :
  - 8 FEV11 and 1 FEV10 from LLR
  - 1 FEV10 from LPNHE
  - 1 FEV13 and 1 FEV11 from Japan
  - 2 FEV12 and xx FEV11_COB from LAL: 2 equipped with wafers and other 6 not equipped…
- We completed the wafer gluing on the FEV12s that were equipped with single wafer.
- Probleam of planarity of the FEV11_COB after the resin deposition on the ASICs: need to think better the procedure…





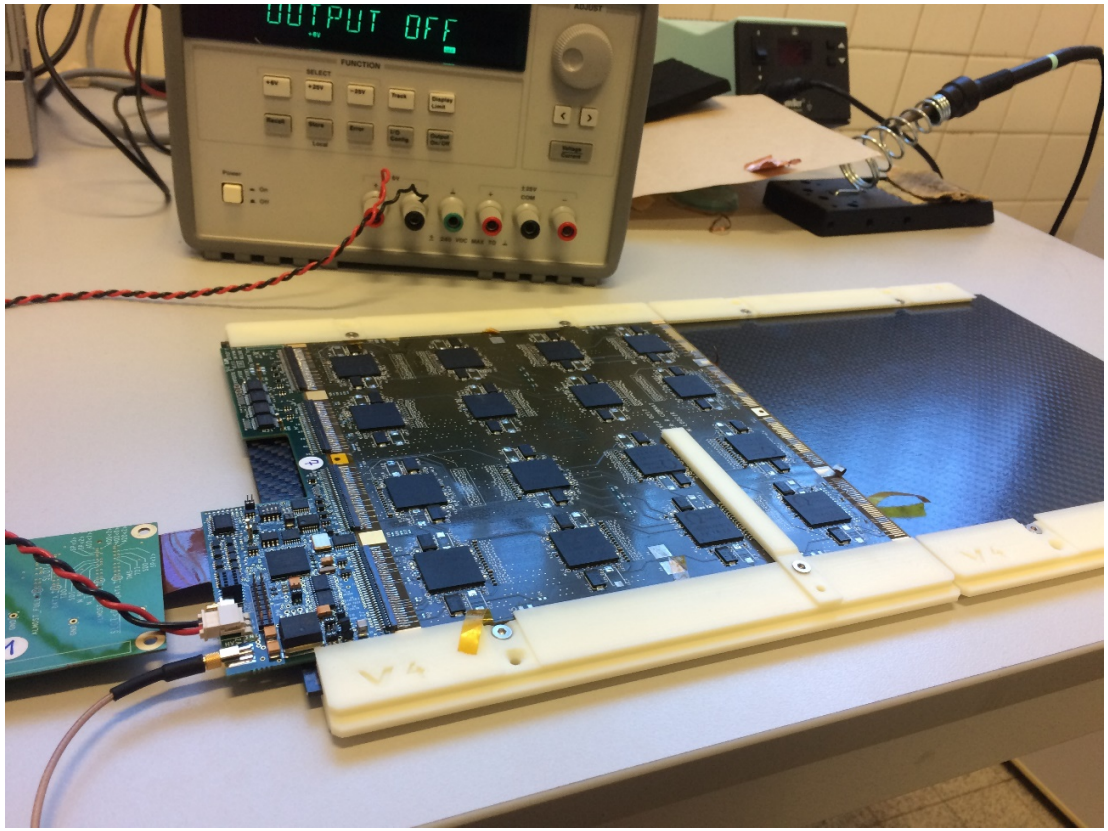
Gluing of Wafers at LPNHE



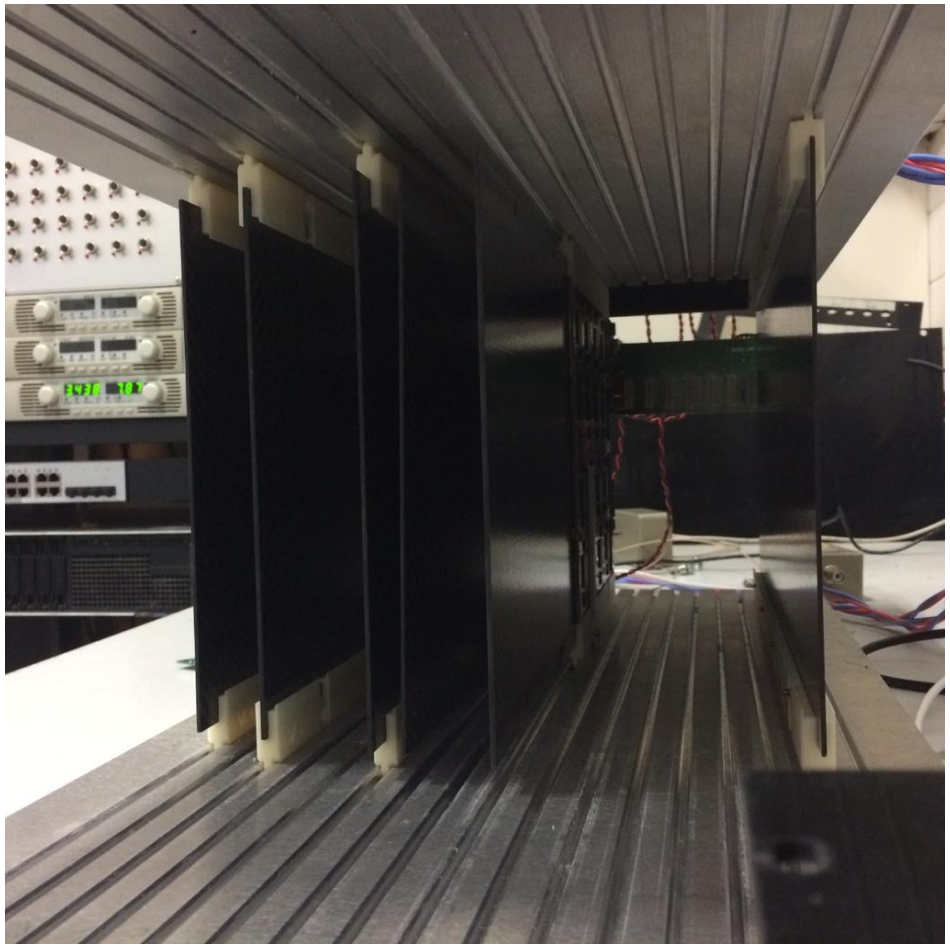
FEV12 with 4 Wafers.

Improved Integration (1) (for testbeam in March 2020)

The SL_Board V2 is coupled to the FEV which holds the wafer on its bottom side. They are then pushed together into the **plastic slides** screwed on the new **carbon frame**. The **tungsten plate** will be fixed on the back of the carbon frame.

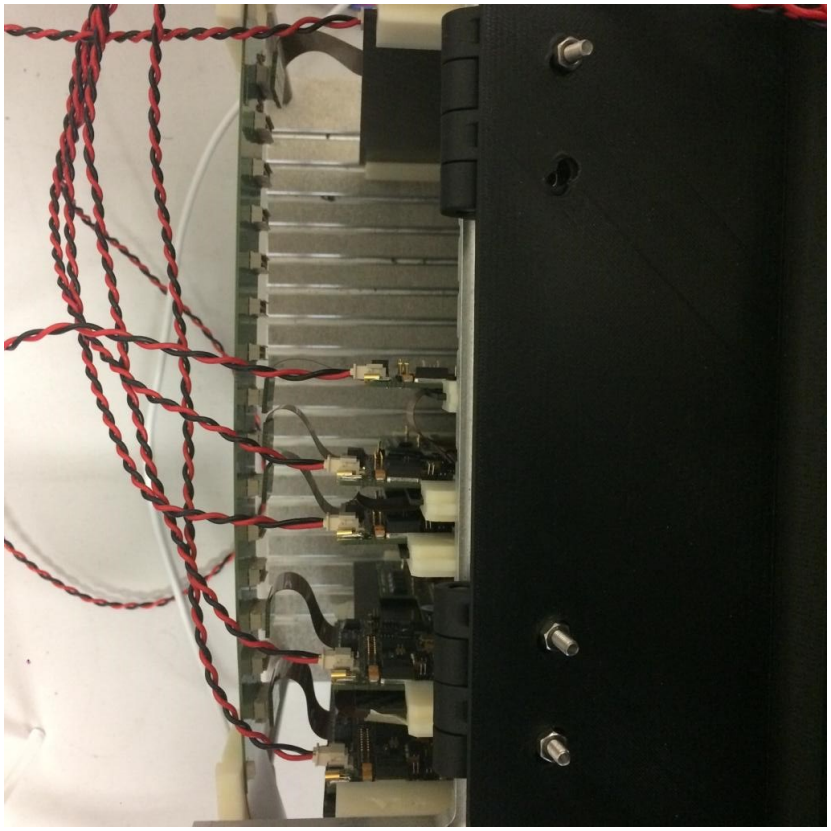


The full slab is then pushed into the rails of the metallic box, which can house **up to 15 slabs**.

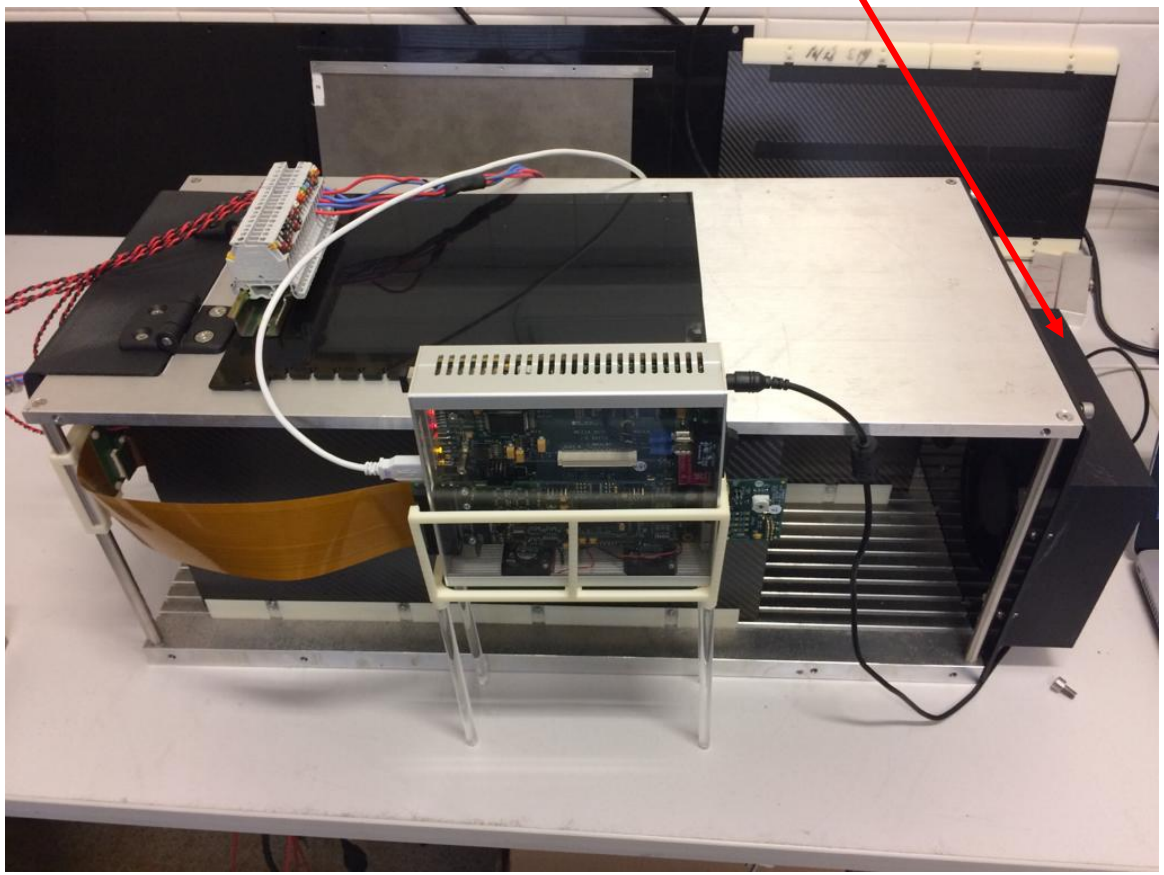


Improved Integration (2) (for testbeam in March 2020)

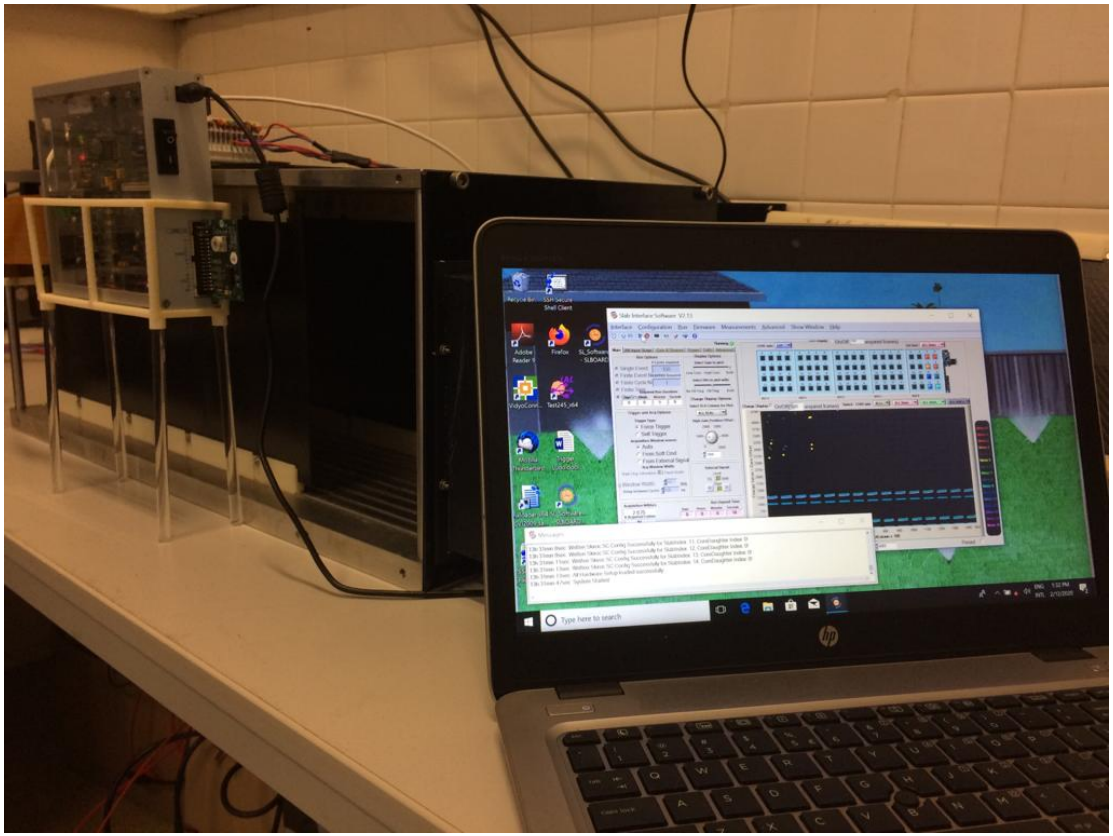
Once the slabs are inserted, the Kapton then the power supplies are connected (LV and HV). Total LV current will be of the order of **24A** with **no power pulsing**, producing **~90W** .



A **dedicated support** has been designed for carrying **the CORE module** to which the CORE_Kapton is connected. Electronics inside the box **is cooled down by two fans**.



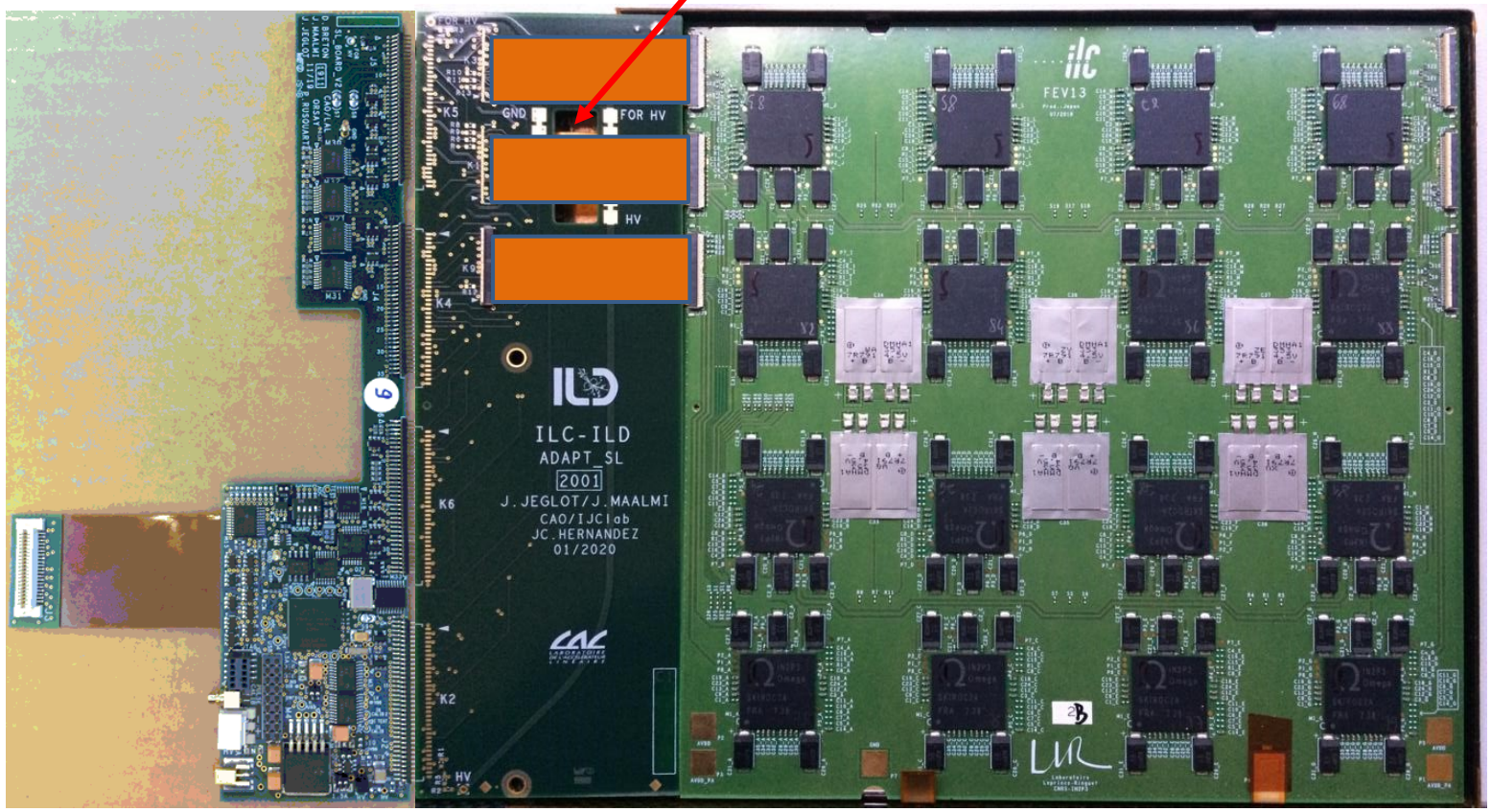
Starting integration tests

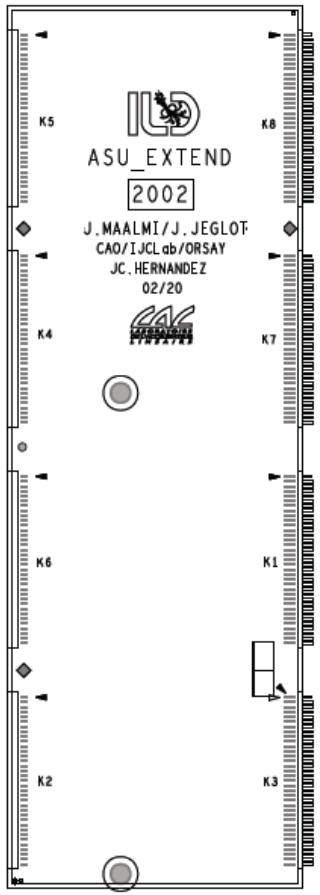


- Started **intensive runs** with multiple layers :
  - In order to validate the acquisition firmware and Software (even without HV)
- We will start soon calibrating noisy channels, and run commissioning runs with muons.
- Software and firmware improvements in continuous progress.

Interfacing SL_Board to FEV13:
design of the SL-ADAPT board

The new **SL-ADAPT interface** board permits the **control** and **readout** of a **FEV13** by a SL_Board. A **hole below the 3 kapton** cables permits connecting the high voltage for the wafers.





ASU_EXTEND Board

➔ To align all the FEVs11/12 with the FEV13

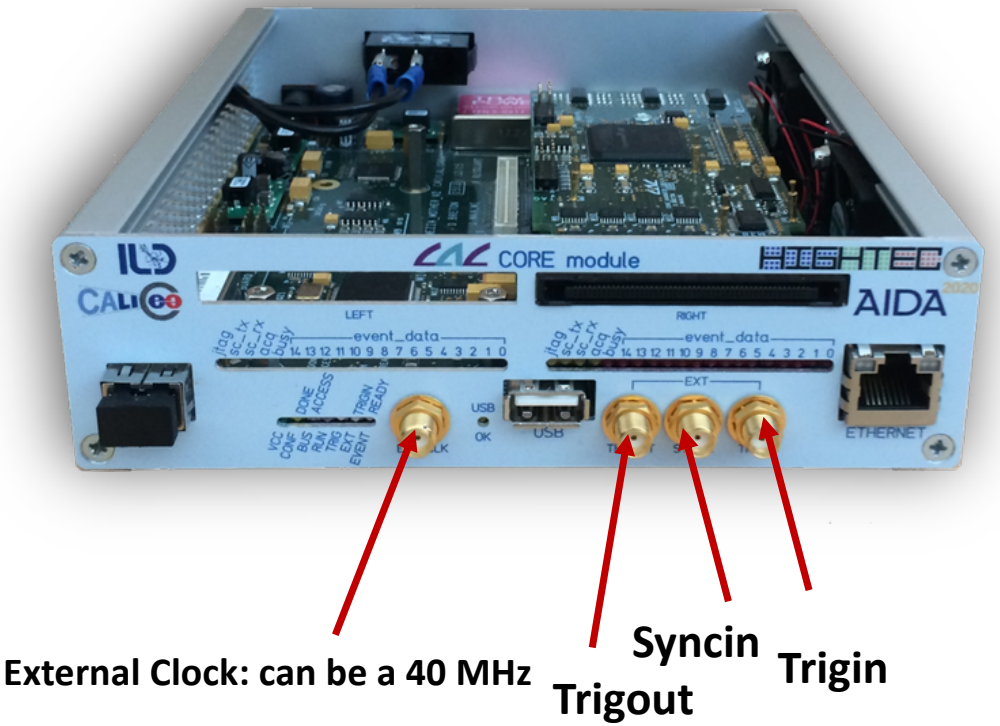
Synchronising with an external system

- We can use a « first level » Synchronisation :
  - **Same Acquisition window:**
    - This is what we did in the last test beam to synchronise with the ASUs from japan.
    - A **CycleID** is added to each event with its **Timestamp** : permits to check the syncronisation.
    - Problem: there is an offset between the two systems that changes at each power on and the clocks of the two systems will drift with time.

- **Full synchronisation:**
  - Constraint: We need the same « 5MHz » clock and same **Sync** signal (to reset all the timestamps)

  - Accepted input clock: between 15MHz and 40MHz : **can not be the 5MHz clock.**
    - can be the **40 MHz clock** ➔ the 5 MHz clock is derived from the 40 MHz.
    - We need a Sync signal to have the same 5MHz clock phase otherwise: fixed offset at each power on.

  - Use **External AcqWindow : do we need to handle a « busy » ?**



Recent Posters/Presentations

- Poster presented at **Twepp 2019** (September 2019- Spain, **J.Jeglot**)

  Title : « New compact readout electronics for SiW Ecal »

- Poster presented at IEEE 2019 , (Oct Manchester)

Title : **« Testing Highly Integrated Components for theTechnological Prototype of the CALICE SiW-ECAL »** ➔ Proceeding Paper submitted

- Talks at CHEF 2019 (November 2019, Fukuoka/Japan)
  - Title : **« Calice SiW Ecal- Development and performance of a highly compact digital readout system »** (R.Poeschl) ➔ proceeding paper to JINST in submission.
  - Title : « **CALICE SiW ECAL - Development and first beam test results of detection elements using Chip-on-Board Technology »** (A.Irles)

Future Plans for readout electronics

Firmware/Software

- Continuous progress on Firmware and Software to add new features
  - Interfacing to FEV13
  - Firmware: Temperature monitoring/ Analog Voltage monitoring ..
  - Software: Online sending data to Network : common DAQ? C-Library …

Power/Pulsing and long SLAB:

- We can test power pulsing with one ASU with the current hardware.
- For a long SLAB: we will need a new design of the ASUs with distributed low value capacitors on the FEV and individual regulators. (cf. backup slide)

Conclusion

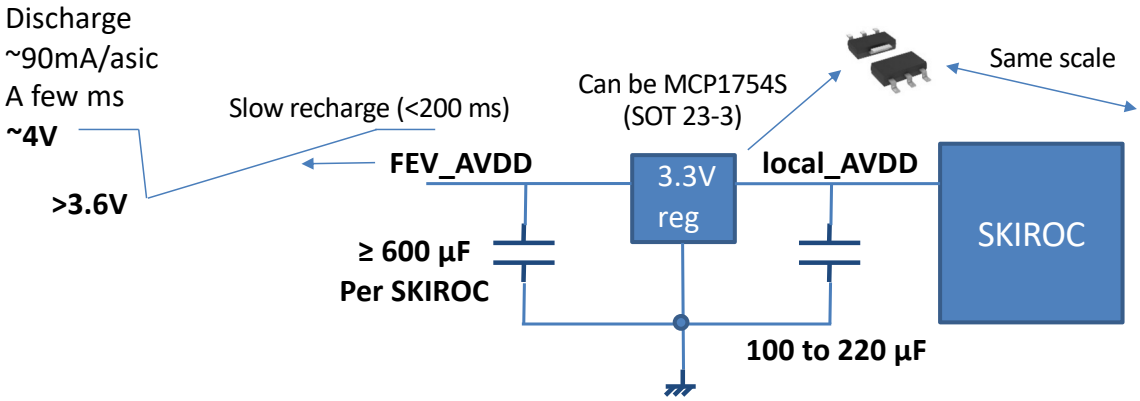
- The new compact digital electronics for the control & readout of the SiW ecal is functional
  - It worked very nicely during the test beam last June with 4 layers ➔ will soon be tested with more layers.
- A lot of experience learned from this test beam: improvements are being realized for the next one in March (mechanics, electronics and software).
- We improved the design of the SL-Board (V2 received mid-december) : 15 over 20 produced boards are already in use.
- We recently developed the SL_ADAPT board in order to interface the existing FEV13 boards with the SL-Board readout.
- Next Test beam in March: with 15 Layers.
- We still have to work on the power pulsing mode: need a new version of the FEVs
- The CORE module can handle up to 30-Layers (using the two CORE Daughters but we need to develop a new SL-Board with inverted shape).

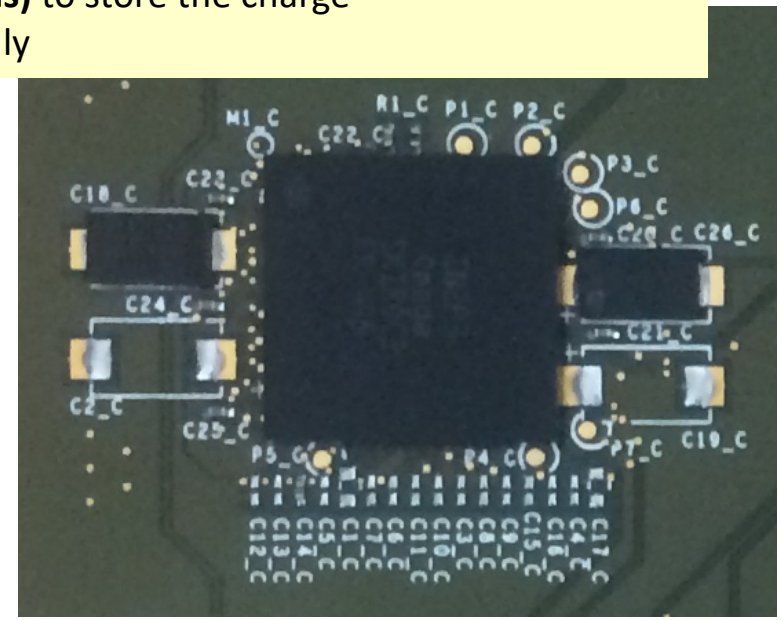
Backup Slides

Working on the power pulsing

Two remarks:
1) High-value flat capacitors actually have a poor **ESR** (**order of Ohms**) => not adapted to high currents
2) It is better that **the AVDD of the SKIROC chips does not vary** during the power pulsing

⇒ two actions:
1) Put **enough lower-value capacitors** with very **good ESR (~ tens of mOhms)** to store the charge
2) AND add an **individual regulator** for producing each SKIROC's AVDD locally





Example of Discharge/Recharge Cycle for one SKIROC block:
- Current of 90 mA during 2.5 ms in 600 µF => ΔV ~ 0.4V
- Total FEV capacitance ~ 15 000 µF
- Reload current can be as low as 15 mA/ASU

There are already 4 slots for decoupling capacitors around the SKIROC chips. More can be added if required (space is available).

There is **no more effect of the variations of AVDD on the SKIROC chips**
The only constraint is to **keep AVDD > 3.6 V.**
The higher the capacitance, the lower the variations => look for the optimum (~1000 µF ?)…