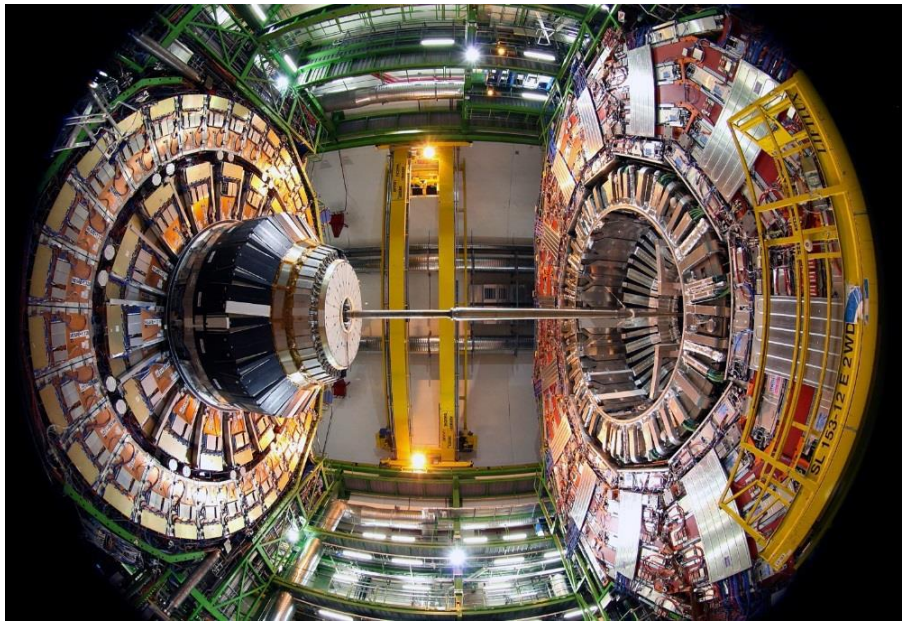
HGCROC-V2 summary of results

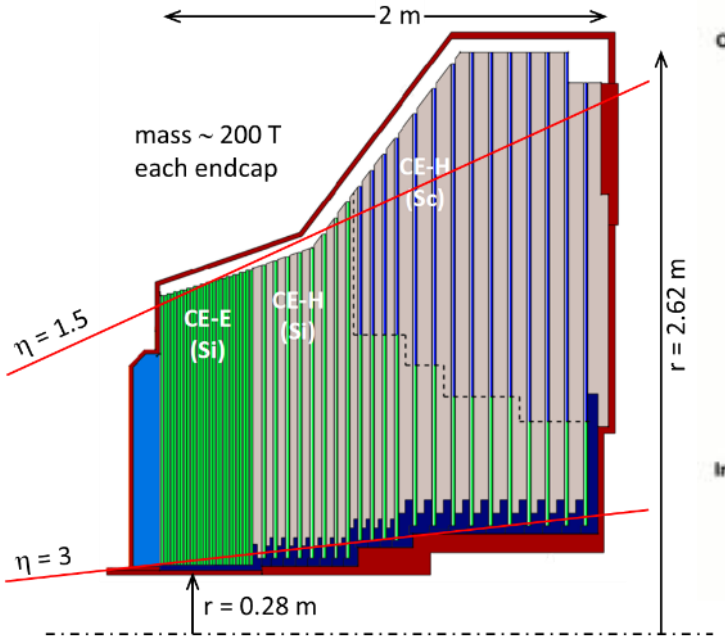
B. Akgun, G. Bombardi, J. Borg, F. Bouyjou, E. Delagnes, F. Dulucq, M. El Berni, P. Everaerts, S. Extier, M. Firlej, T. Fiutowski, F. Guilloux, M. Idzik, C. de La Taille, A. Lobanov, A. Marchioro, J. Moron, L. Raux, K. Swientek, D. Thienpont, T. Vergine

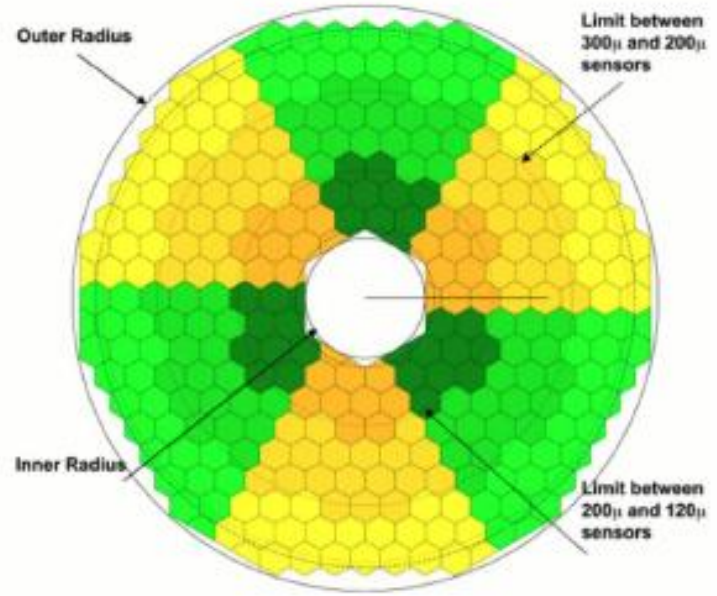
28 January 2020

Organization for Micro-Electronics desiGn and Applications

HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade

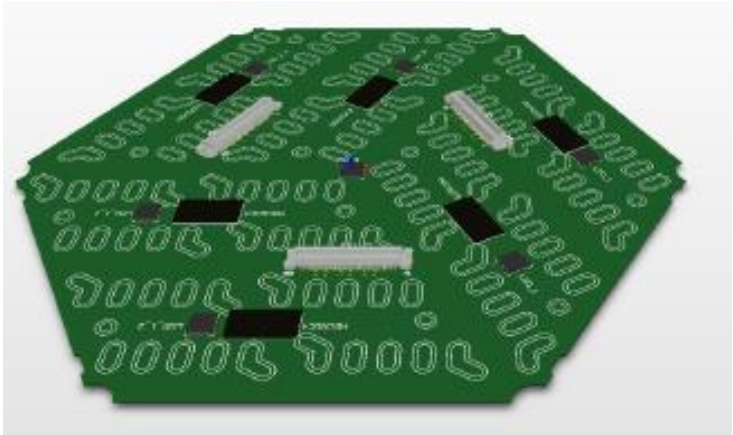


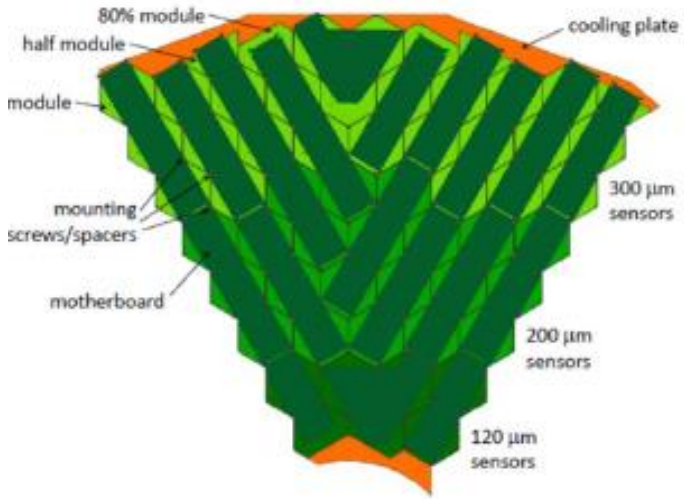




New Endcap Calorimeters

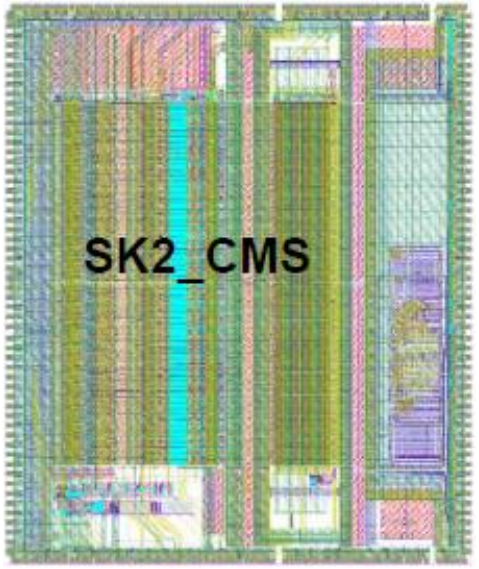
- Rad. Tolerant
- High Granularity: increased transverse and longitudinal segmentation, needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger and to identify the associated vertex and particles
- Precise timing capability: further mitigation of pileup effects

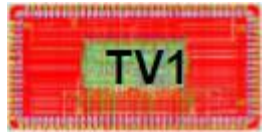


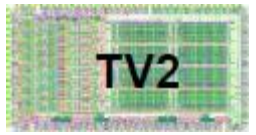


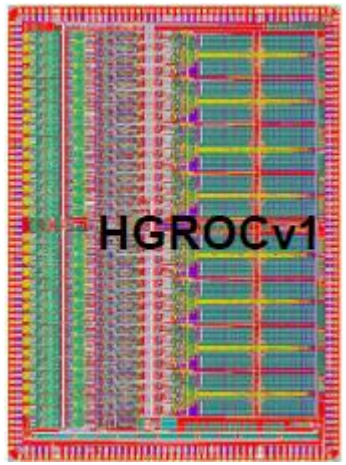
Development history

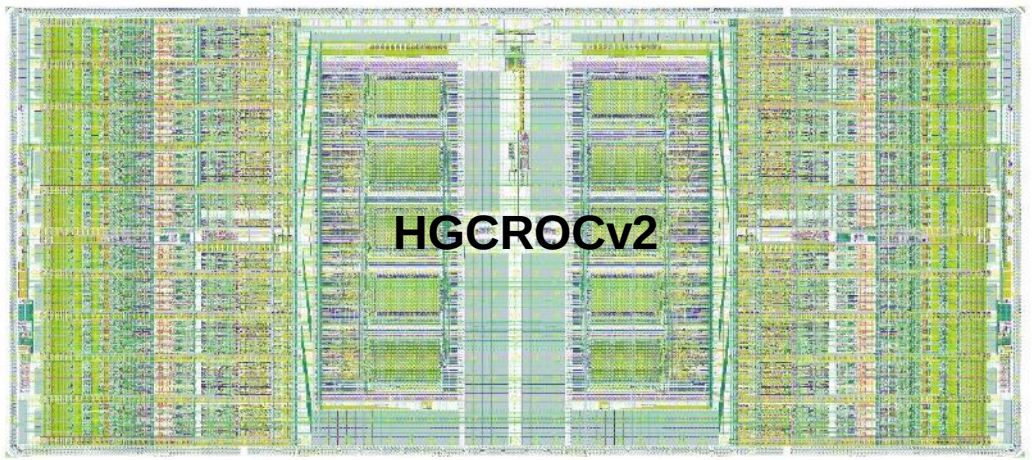
- Jan 16: SKIROC2_CMS [TWEPP 2016]
  - SiGe 350 nm 7x9 mm²
  - Dedicated to test beam and analog architecture (TOT)
- May 16: 1st test vehicle TV1
  - CMOS 130 nm 2x1 mm²
  - Dedicated to preamplifier studies
- Dec 16: 2nd test vehicle TV2 [TWEPP 2017]
  - CMOS 130 nm 4x2 mm²
  - Dedicated to technical proposal analog channel study
- July 17: HGCROCv1 [TWEPP 2018]
  - CMOS 130 nm 5x7 mm²
  - All analog and mixed blocks; large part of digital blocks
- Feb 19: HGCROCv2 (this talk)
  - CMOS 130 nm 15x6 mm²
  - Silicon and SiPM versions (for both 2 and 2A)
  - Final size, packaging and I/Os











HGCROCv2 overview

Overall chip divided in two symmetrical parts

- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

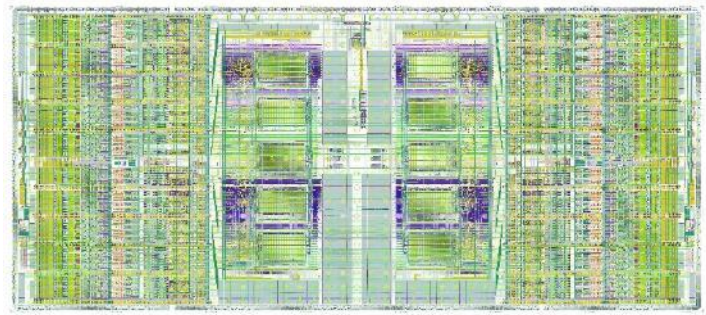
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links

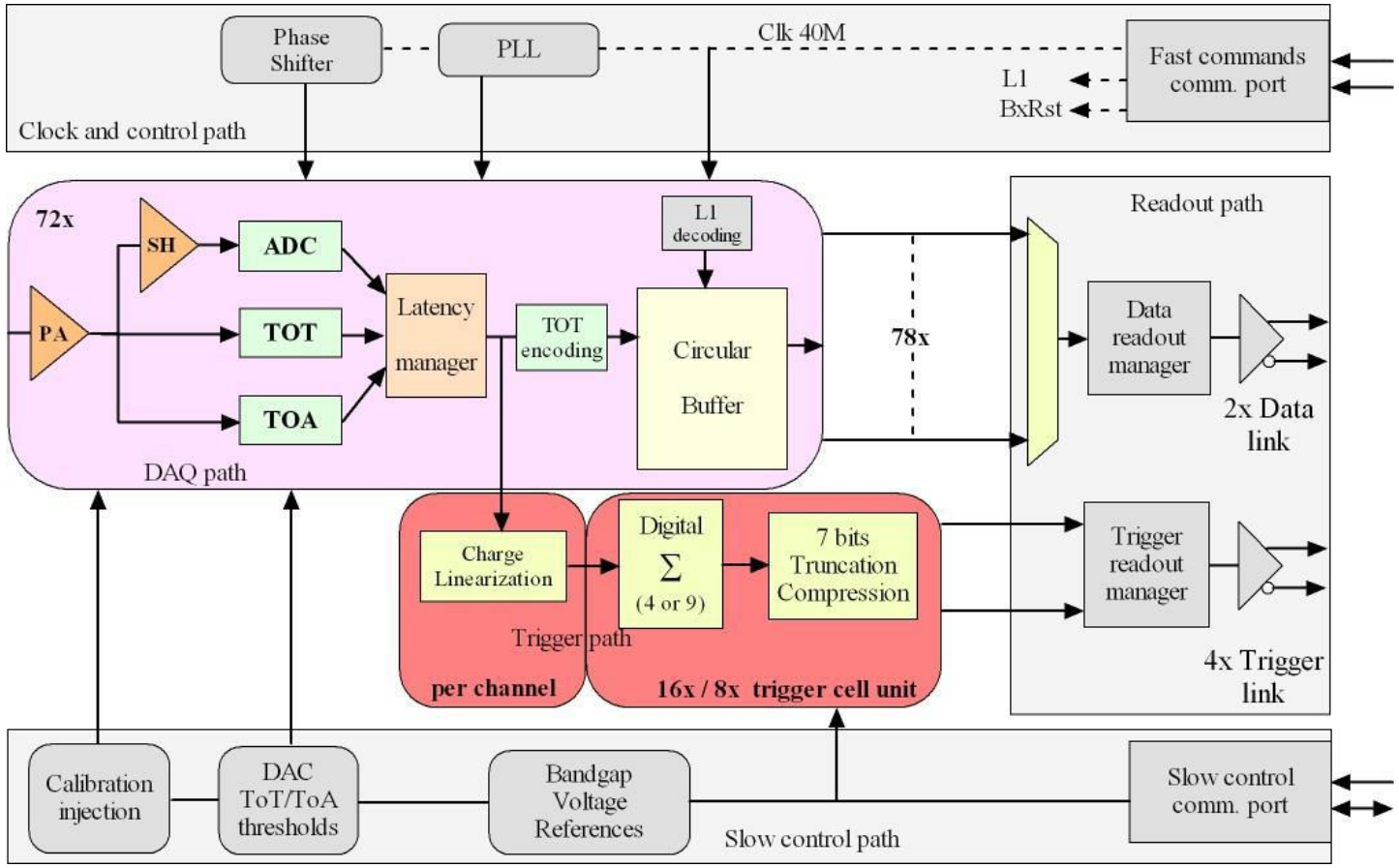
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

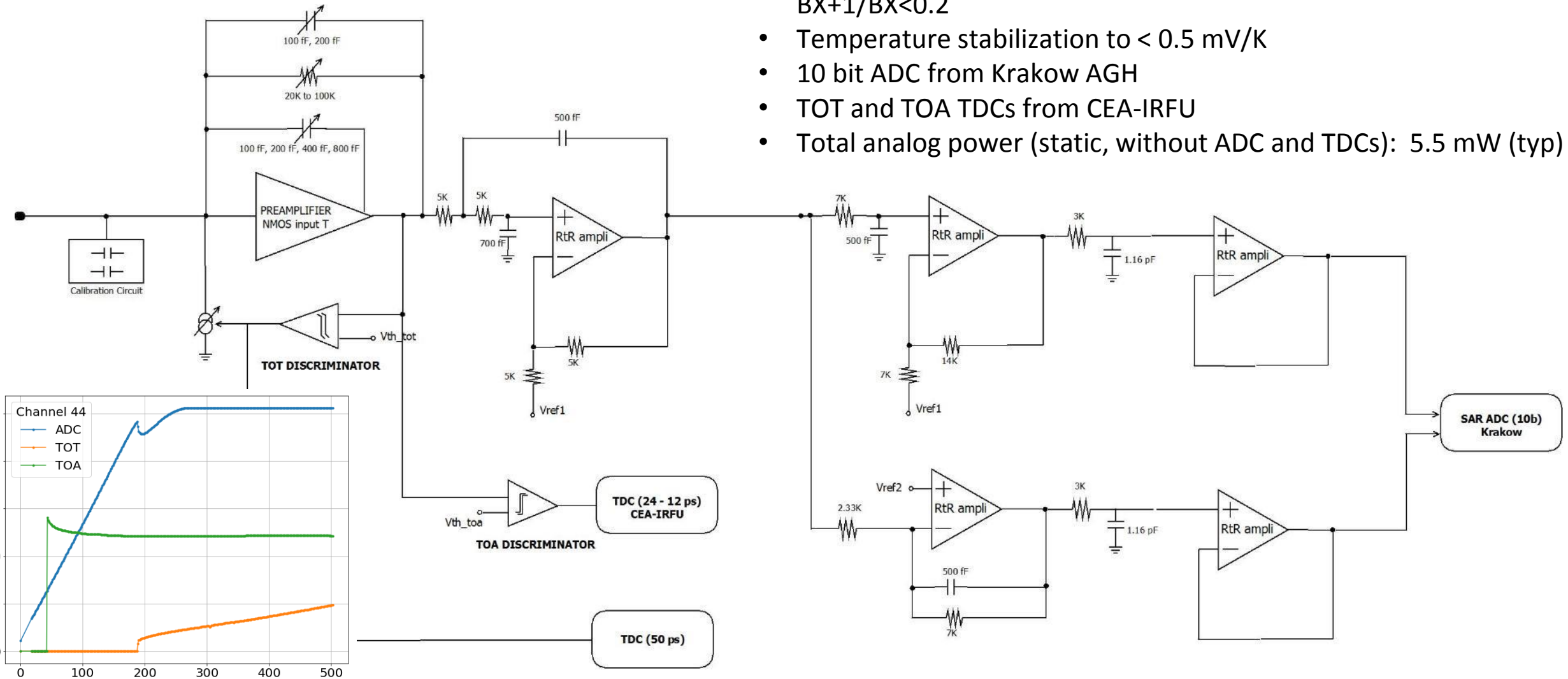




Analog Channel Overview

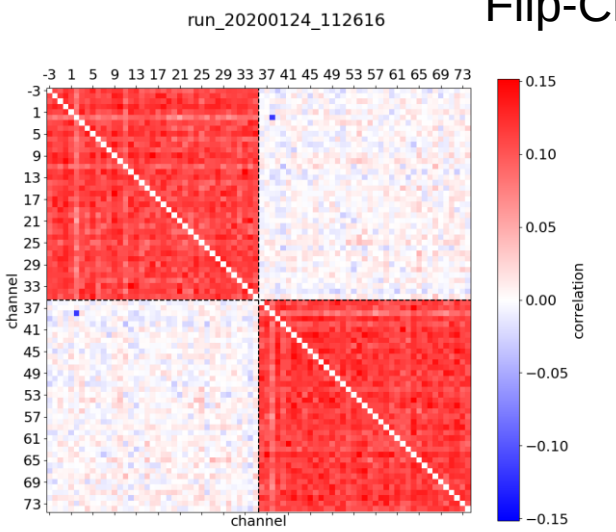
- New calibration pulser, 0.5pF and 8 pF calibration cap.
- Preamp : adjustable gains for 80, 160 and 320 fC ranges
- Tunable TOT over 5 bits

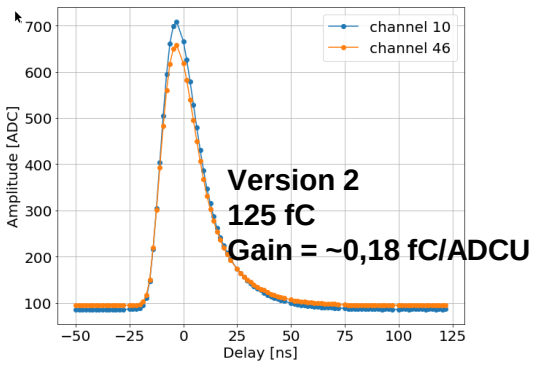
- Compensation for the leakage current, 10 µA max. (not shown in the figure)
- Sallen Key shaper RC4, tp<25 ns, tunable (~20%) with 2 bits, BX+1/BX<0.2
- Temperature stabilization to < 0.5 mV/K
- 10 bit ADC from Krakow AGH
- TOT and TOA TDCs from CEA-IRFU
- Total analog power (static, without ADC and TDCs): 5.5 mW (typ)

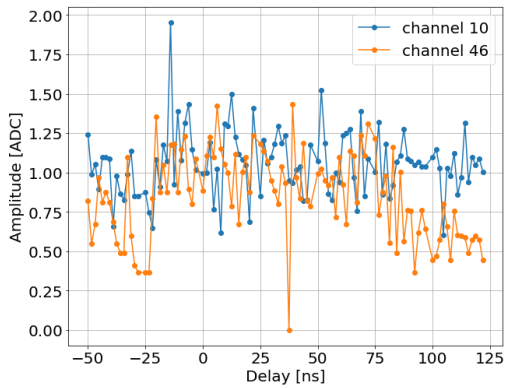


Pulse shape

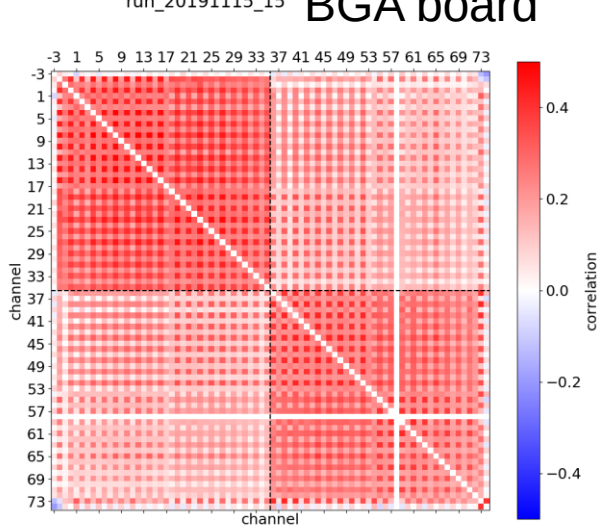
Flip-Chip board

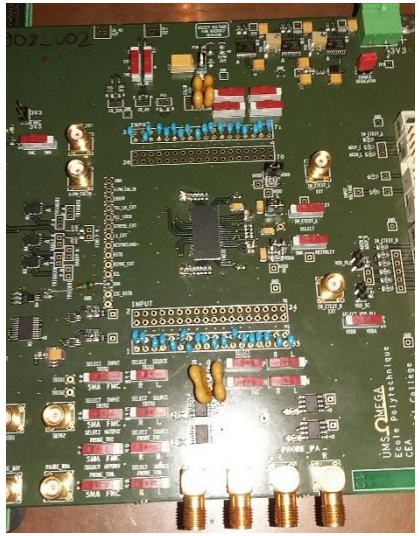


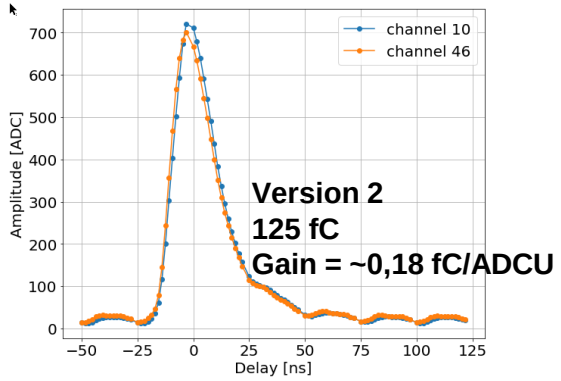


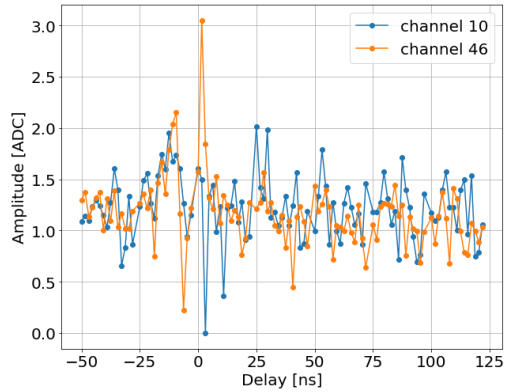


BGA board







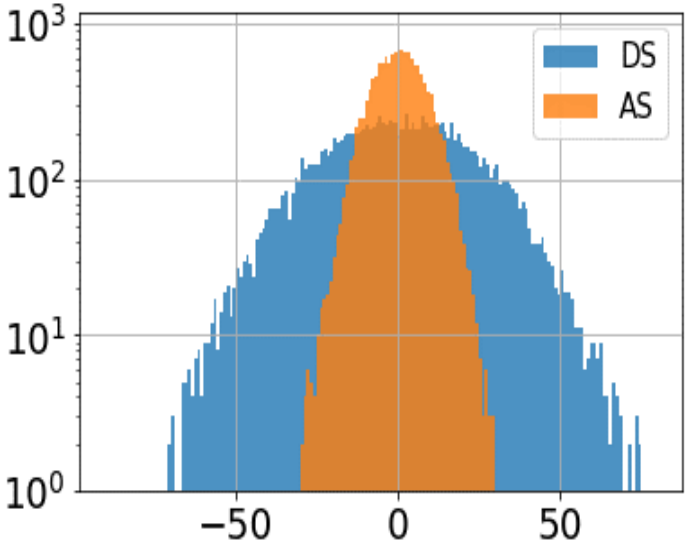


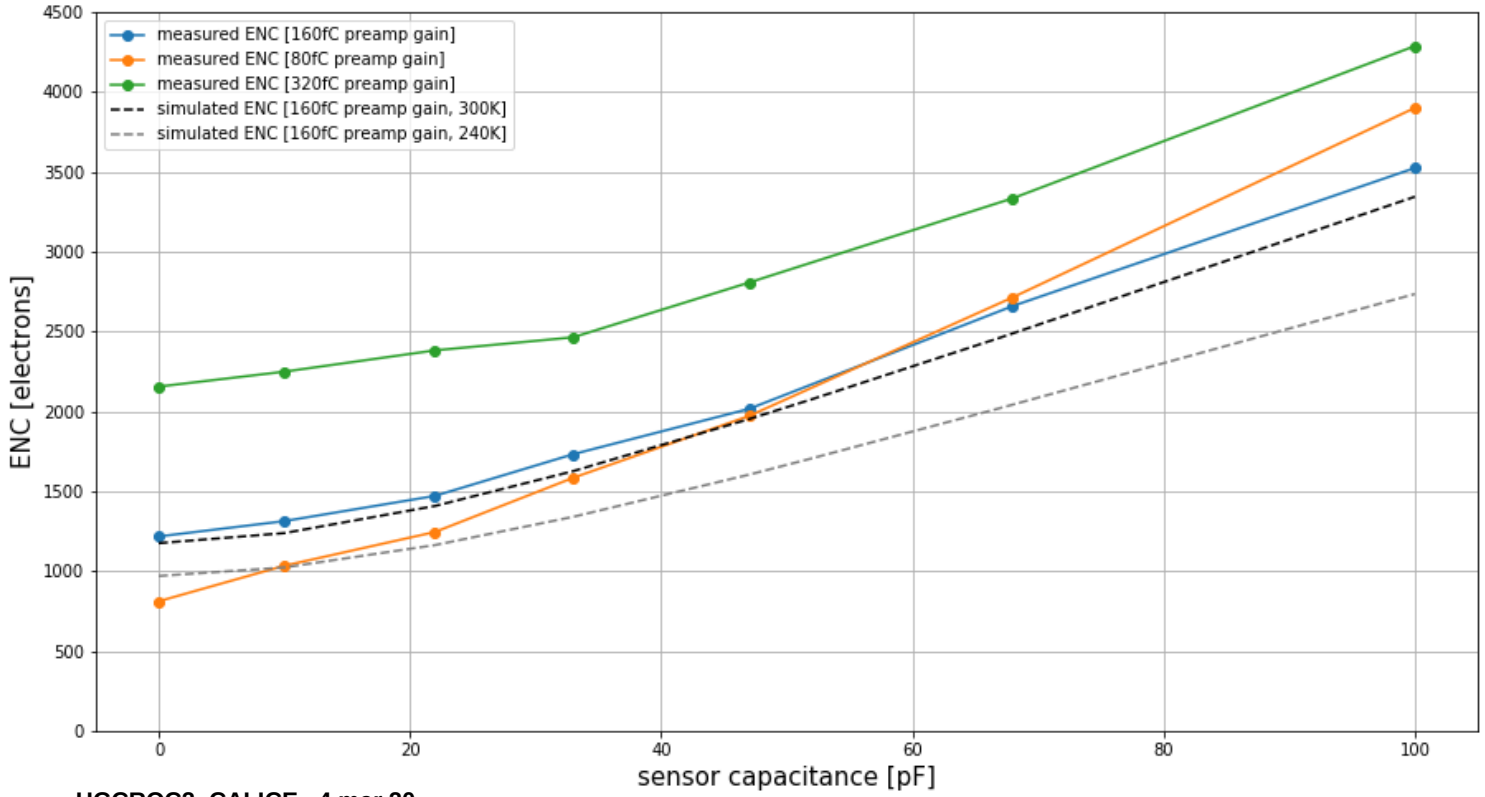
FlipChip
- No digital coupling on preamp inputs
- w/o sensor capacitance, noise = ~1 ADC (0,22 fC)

BGA
- Digital coupling on preamp inputs (20 ADC; 3,6 fC)
- w/o sensor capacitance, noise = ~1,25 ADC (0,27 fC)

noise

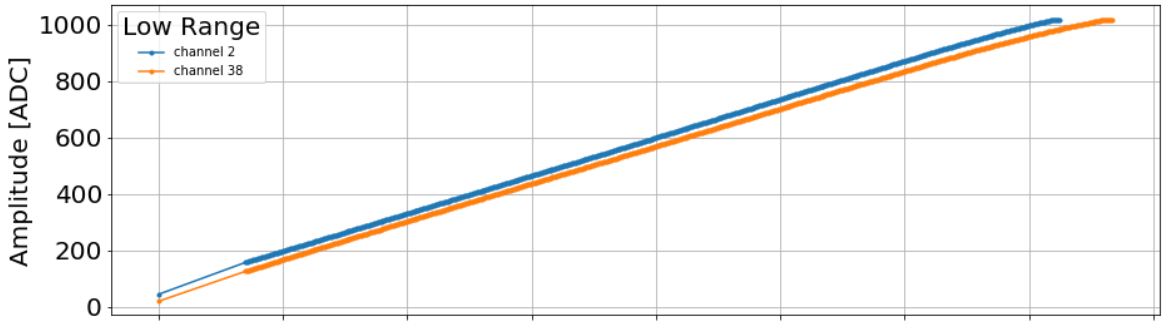
- 2000 electrons ENC at 47pF Cdet for “gain” 80 and 160 fC
- 2800 electrons ENC at 47pF Cdet for “gain” 320 fC
- Coherent noise extracted by comparing direct and alternate sums on n channels (n = 72): $DS = \sum ped[i]$; $AS = \sum(-1^i)ped[i]$
  - Incoherent noise $IN = rms(AS)/\sqrt{n}$
  - Coherent noise $\mathrm{CN} = \sqrt{var(DS) - var(AS)}/n$
  - Coherent noise fraction : CNF = CN / IN
  - **FlipChip, CNF = 5%. BGA, CNF = 10%**

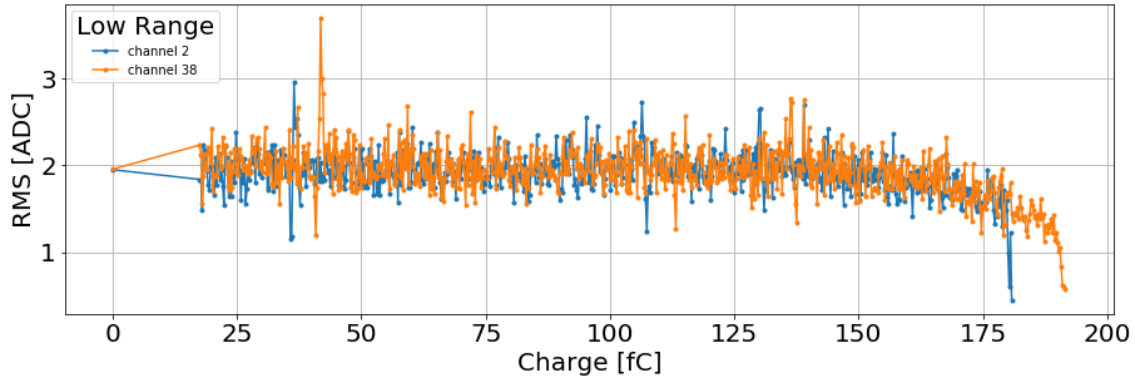


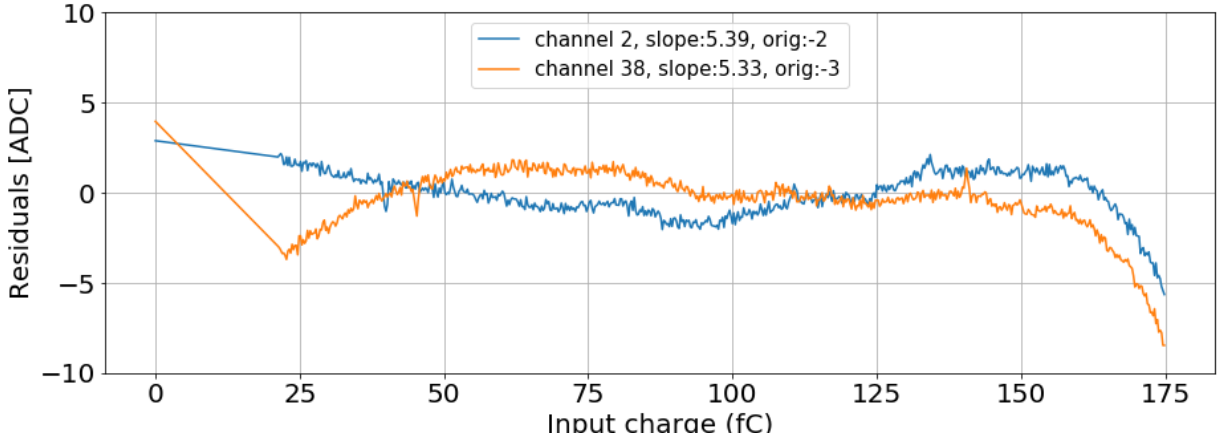


Charge ADC range: linearity, residuals

- Two 10b-DAC to globally set the pedestal to a wanted level
- 5b-DAC to reduce dispersion per channel
- Good linearity in-between +/- 1%
- Noise 1-2 ADC counts depending on Cd

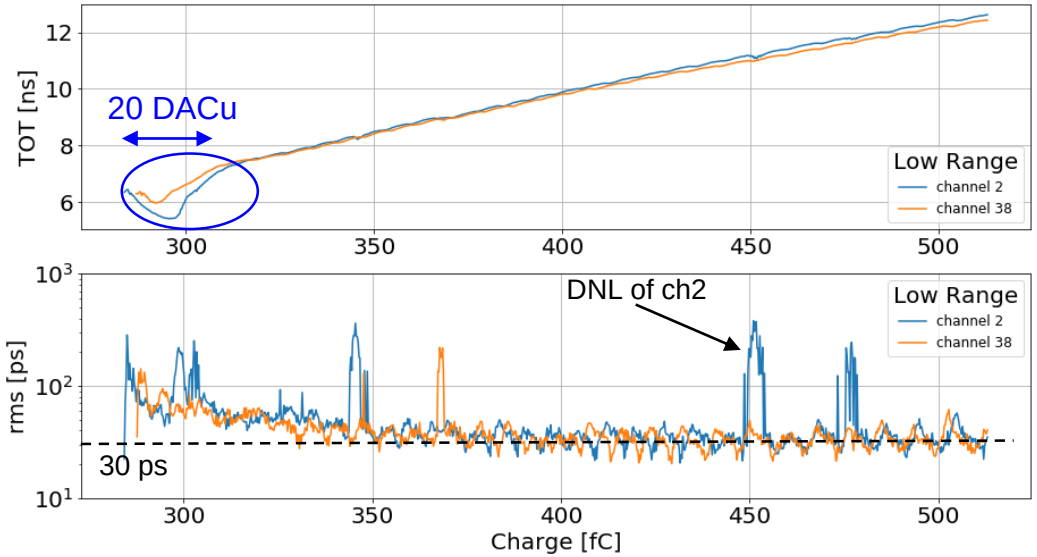


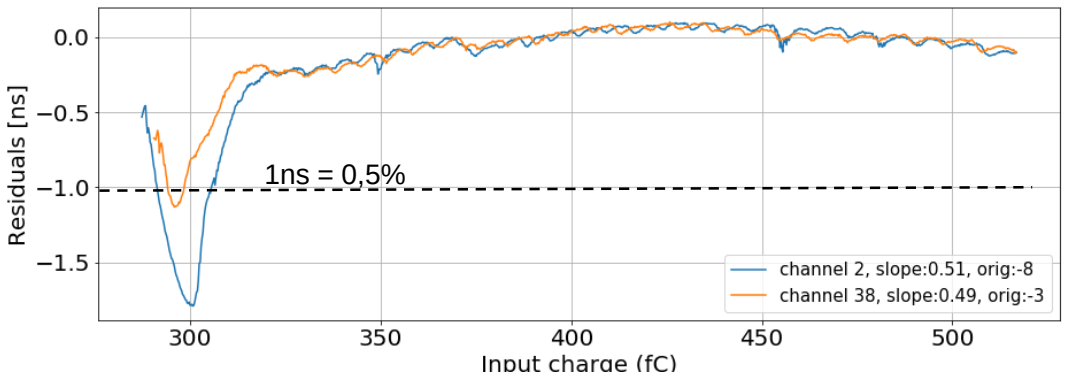




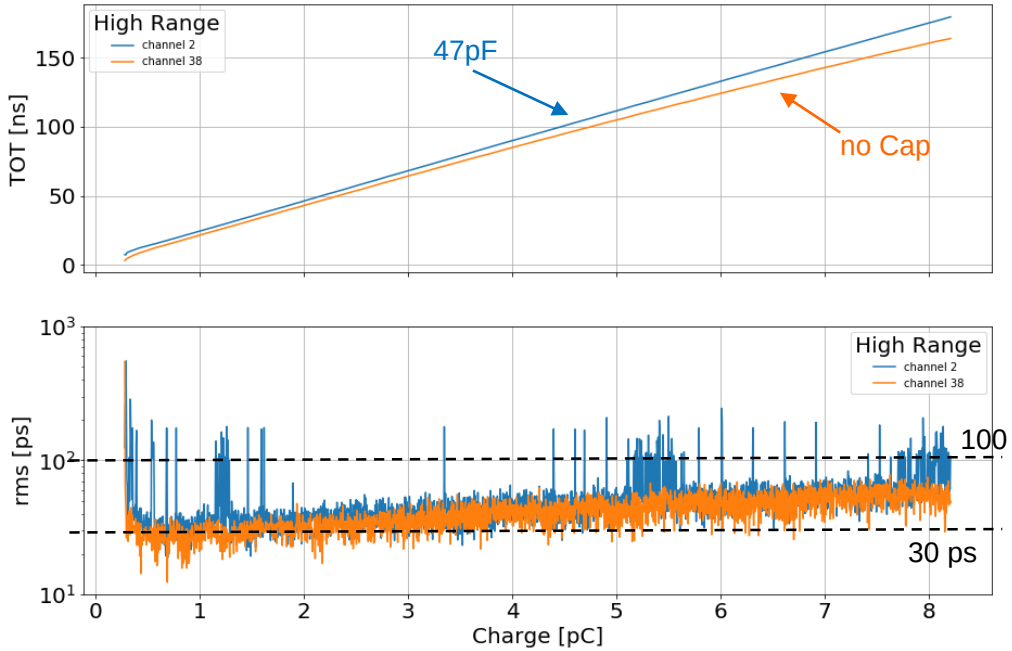
MasterTDC optimization applied but not ch-wise

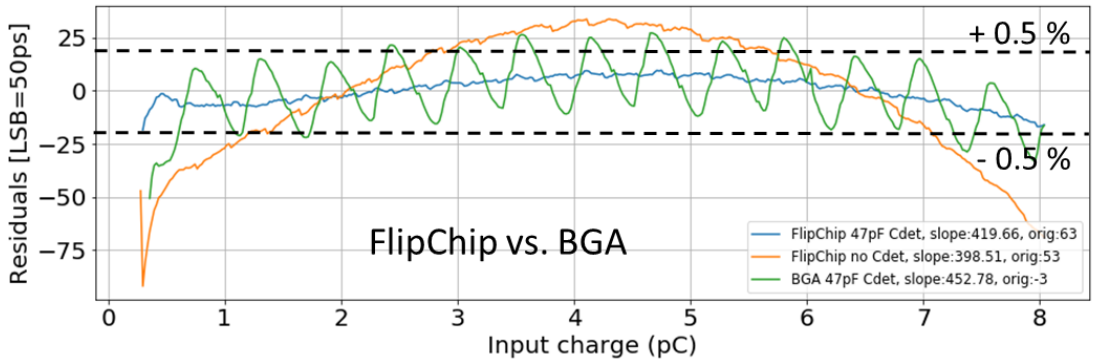
0.5 pF injection Cap.



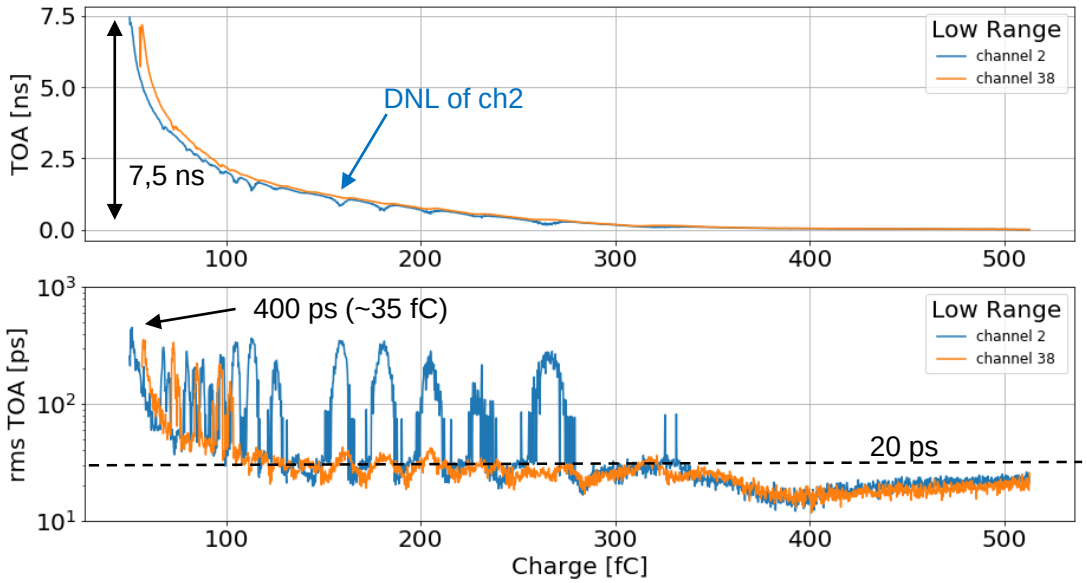


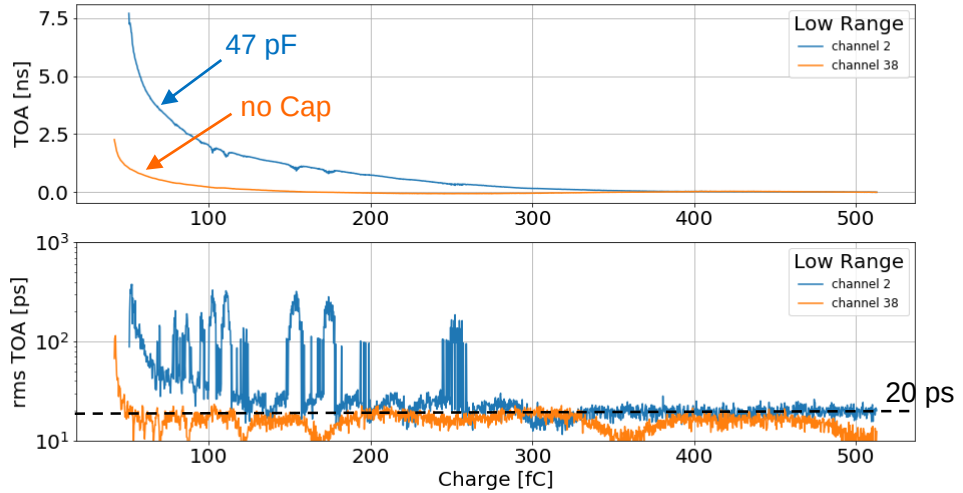
8 pF injection Cap.





0.5 pF injection Cap.





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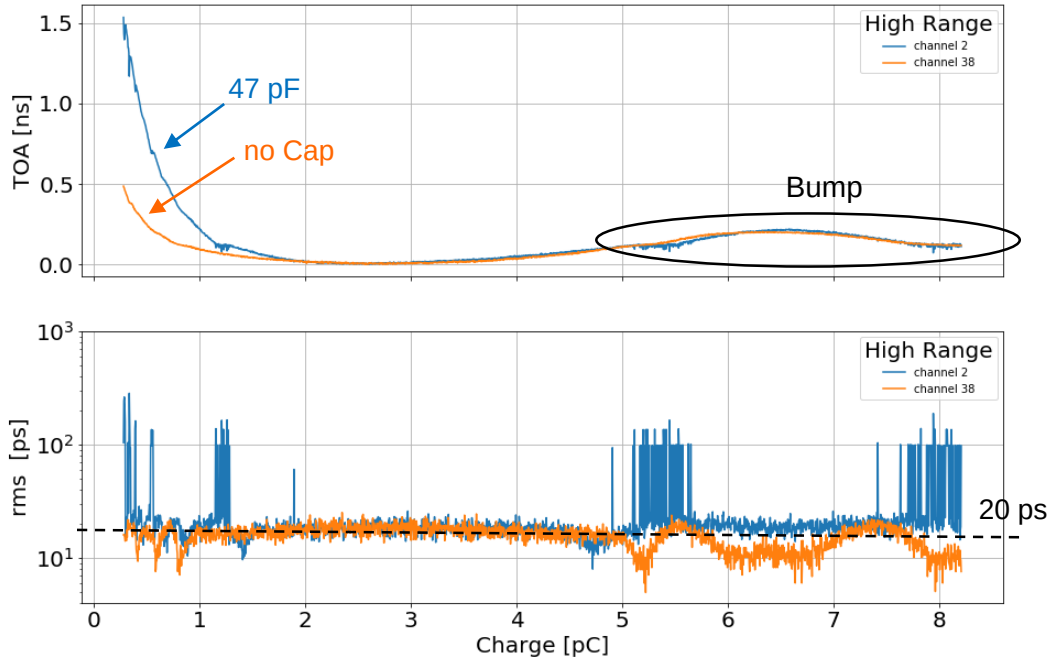


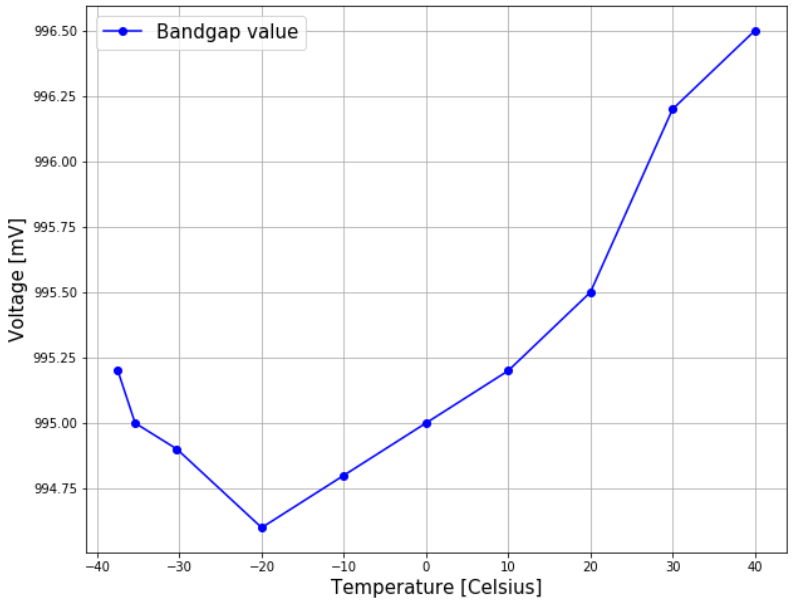
"Flip-Chip" board

Fine channel-wise adjustment has to be applied to further improve resolution performance

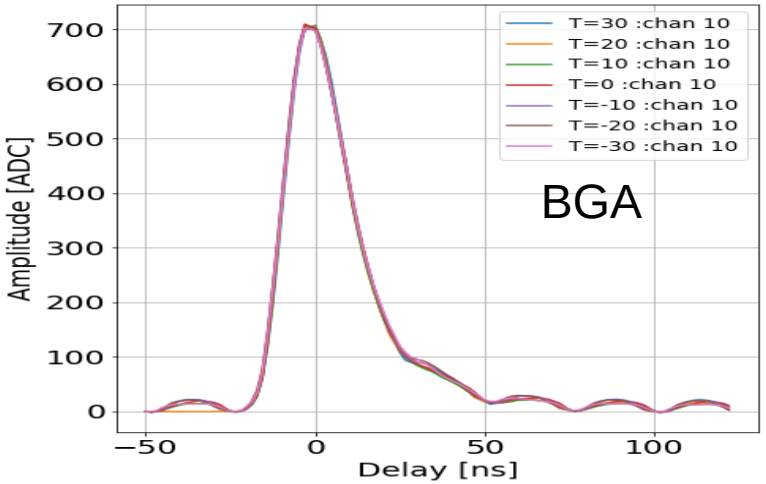
Bandgap and temperature measurements

- Bandgap value moves over 2mV between -40°C and +40°C, but lower shift around -20°C
  - ~ 6-8 mV increasing after 300 Mrad

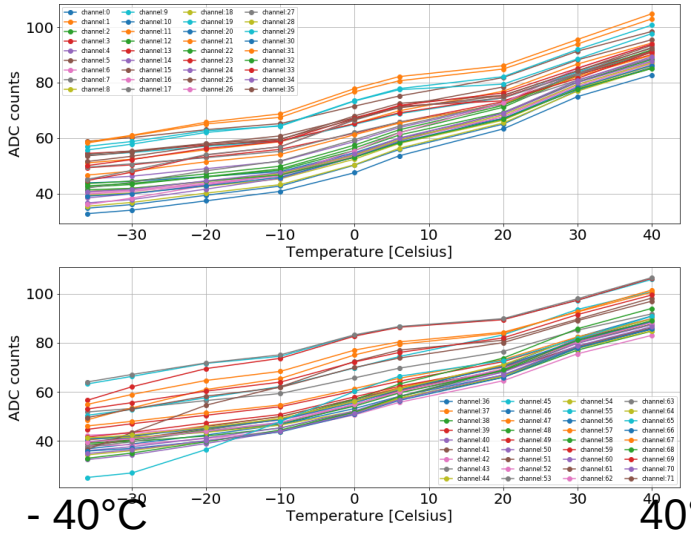
- Pedestals
  - 1 ADC/°C in room temperature
  - ~ 0,4 ADC/°C around -30°C



Gain as a function of the temperature



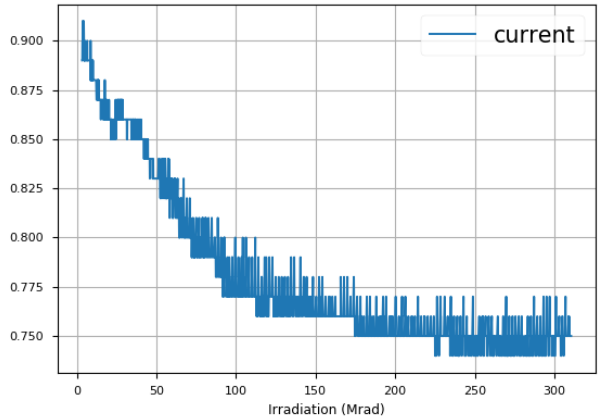
Pedestals value as a function of the temperature

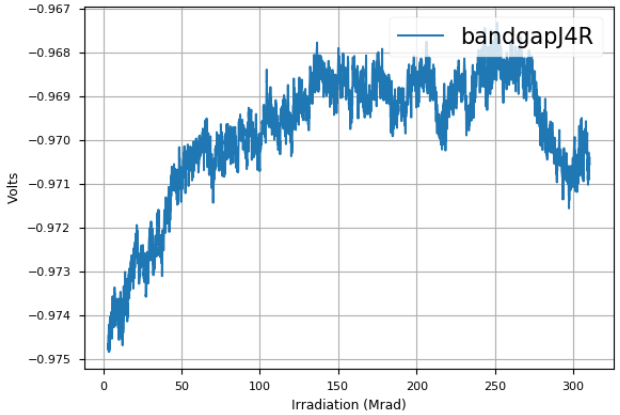


- 40°C 40°C

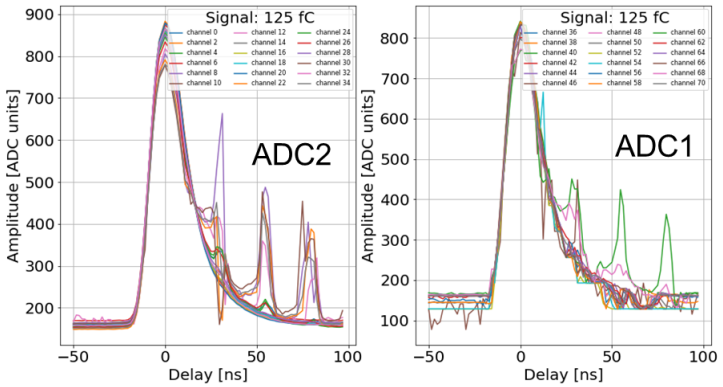
Irradiation testing: TID

- Analog probes
  - Consumption
    - All currents decrease, except that of PLL
  - Bias, reference, bandgap and pedestal
    - Vbo_discri to be improved
- ADC
  - Start to misbehave after 100Mrad
  - Recover correct operating after annealing
  - Redo at cold temperature
- TDC
  - Start to misbehave after 100Mrad
  - Still problems after annealing
  - Under study
- DRAM
  - No problem observed
  - Retention time to be checked
- PLL
  - VCO voltage shift
  - Survived 310Mrad

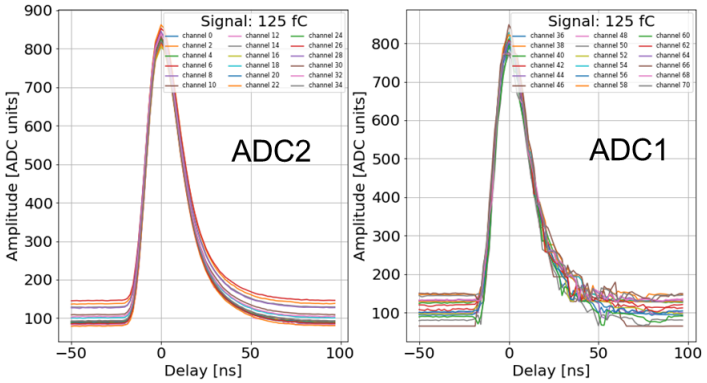




After 310 Mrad (in 5 days)



After 2 days annealing



Plans for CALICE

- AMS SiGe is discontinued => move to TSMC65/130n
- Adapt HGCROC to CALICE
  - Add power pulsing
  - Slow down shaper and ADC
  - Remove TOT
  - Remove trigger path
  - Remove timing branch ?
  - Anticipate < 5 mW/ch * 1% duty cycle = 50 uW/ch
  - More work needed to further optimize power consumption
- Could be prototyped in 2021 or 2022 depending on workload @Omega

backup

Power consumption

- ~ 10 mW per channel
- Too high current in vdd_adc right
  - Understood, comes from Vref_m
  - Vref_m will be connected to ground in V3

		chip1	chip2	
1	vdd_tdc_l	4	4	mA
2	vdd_buf_l	65	68	mA
3	vdd_adc_l	17	17	mA
4	vdd_sk_l	39	40	mA
5	vdd_dac_l	27	27	mA
6	vddd2_l	11	12	mA
7	vddd_l	22	23	mA
8	vdd_sc	0	0	mA
9	vddd1	38	41	mA
10	vddd_r	23	23	mA
11	vddd2_r	12	12	mA
12	vdd_pll	4	4	mA
13	vdd_tdc_r	4	4	mA
14	vdd_adc_r	68	73	mA
15	vdd_buf_r	66	64	mA
16	vdd_sk_r	39	43	mA
17	vdd_dac_r	27	28	mA
	TOTAL sans PA	466	483	mA
	TOTAL	650	650	mA
	vdd_pa	184	167	mA
	conso/ch	10	10	mW/ch

Irradiation testing: TID

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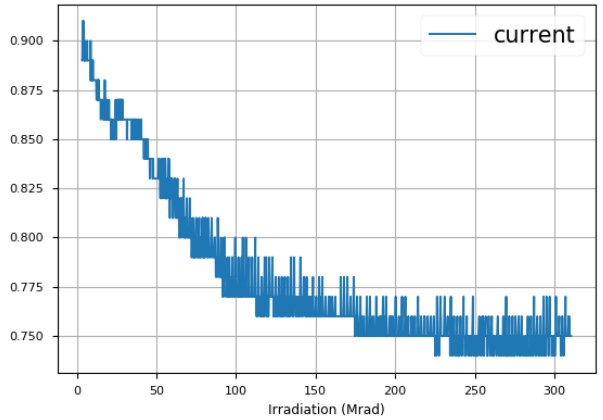
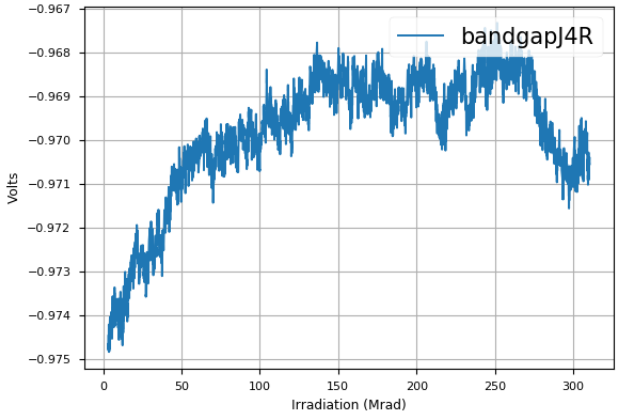
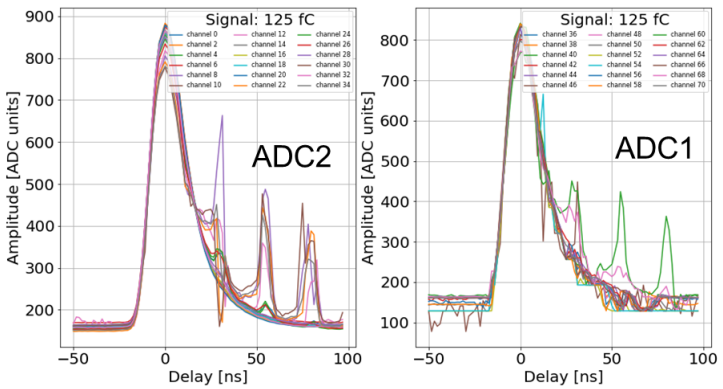




After 310 Mrad (in 5 days)



After 2 days annealing