Plans for 2020

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CALICE meeting
McGill U., 05/03/2020

A brief overview

ASU's

- FEV11/10 boards: 320 µm, SK2
  - DESY-2017, CERN -2018, DESY-2020-03: + 4!
    - $S/N_{ADC} \sim 20^{+}$; $S/N_{Trig} \sim 12^{-}$
- FEV13, 5 boards, 4×650µm + 1×320µm, SK2a
  - DESY-2018, (CERN-2018), DESY-2019:
    - Prelim: $S/N_{ADC} \sim 50$ for 650µm, small Δ Fr vs Jp PCBs
    - Prelim: $S/N_{ADC} \sim 21$ for 320µm
    - Prelim: But time dependance on ped. stability ?
- FEV12: ⟶ fully equipped: SK2a, 500µm
- FEV11-COB × 1/4th equipped, SK2a, 500µm
  - DESY-2019 ⇒ COB: promising results
    - Prelim: $S/N_{ADC} \sim 24^{+}$
    - no ch37 pbm
    - no PP

2020:

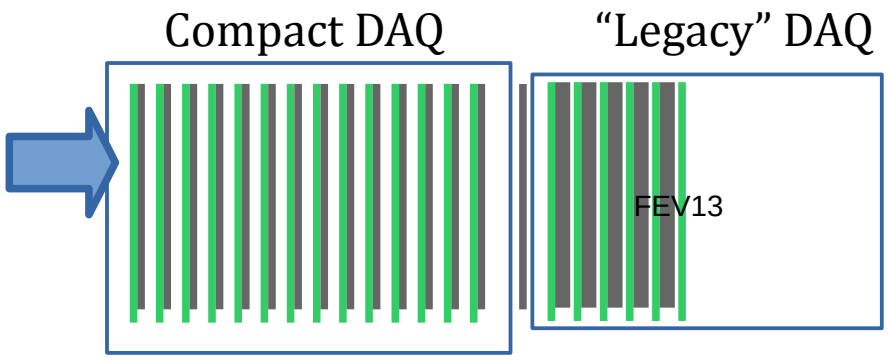
- Use of 2017 prod of 25 × 500µm wafers
  - 25 full wafers
    - 9 tested for FEV12+FEV-COB: **C2V similar to HPK measurements**
  - 132 baby wafers
- Production of 2 FEV-13 (500) in Kyushu (on-going)
  - PCB prod in France (~ identical PCB prod in Jp)
  - Mounting done in Jp **(back today)** ⟶ Gluing
    - Missing Murata flat capacitors ⟶ Big capacitors on SMB
  - 8×500µm wafers ⟶ 2 boards

    ⟶ 3 pts of comparison (320, 500, 650 µm)
  - ⟶ completion of 17 layers
    - 11 FEV11/10 + 2 FEV12 + 1 FEV 13 + 1 FEV-COB = 15 lay.
    - 4 FEV-13 (650+320)+ 2 FEV-13 (500) = 6 lay

Thanks to Taikan!

2nd stack for 15 X_0 ECAL

Combined structure



Low-E Calorimeter layer

+ "Core shower" = 4-5 X_0 of W in Front

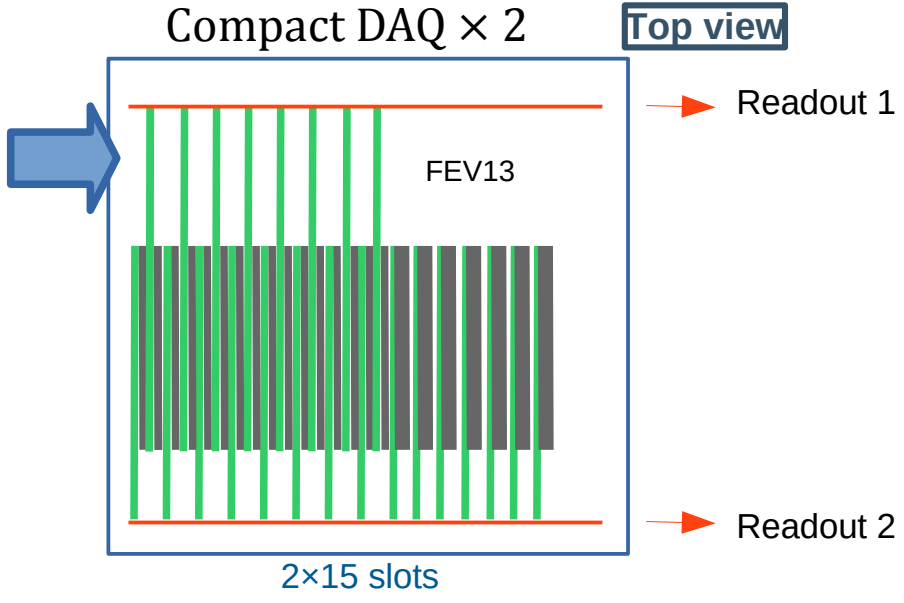
- ~ same response in all layers

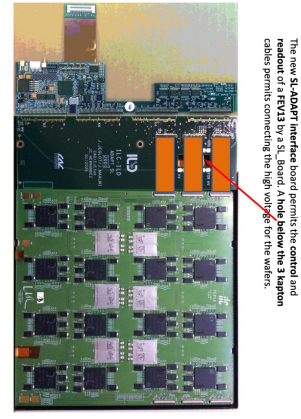
A possible calorimeter layout ?

- Mix perf ⊗ New / Tested ⊗ Shower profile

To be readout by 2×15 ladder in Nov ?

- ⇒ novel structure for compact layout





e-Long Slab

FEV12, 1/64th equipped

- Required HV decoupling
  ⇒ Noise prop between ASICs through wafer / HV ?
- Dependancy on positioning and ASIC seen (TBC)
  ⇒ opt. power scheme ?

Completion

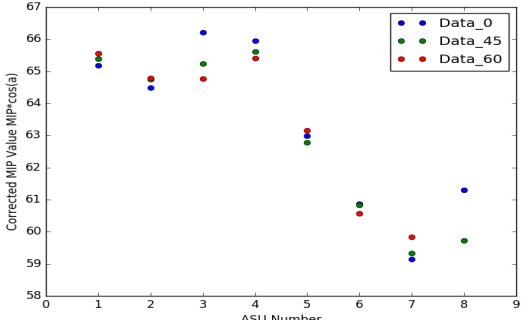
- + 15 baby wafers / ASU (= 120)
  - ×16 stat.
- X-check with source / Cosmics.

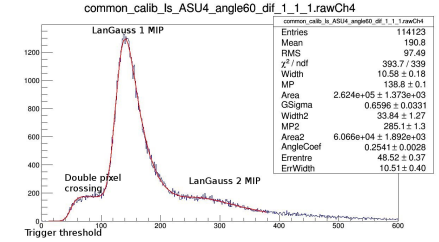
Switch to CompactDAQ

- Test various PS distrib/decoupl. solutions.

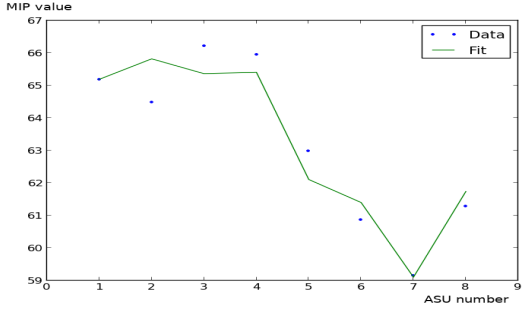
Results presented at CHEF:

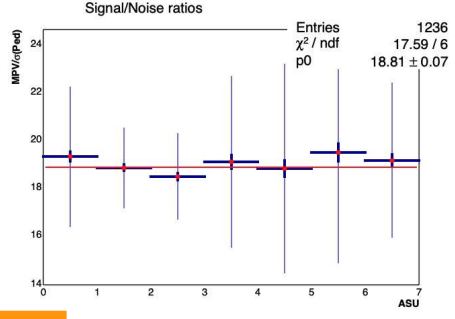
- Mip fitted, ≠θ vs positior





S/N ratio ~ const





Drop = 50% BandGap + Vdd drop

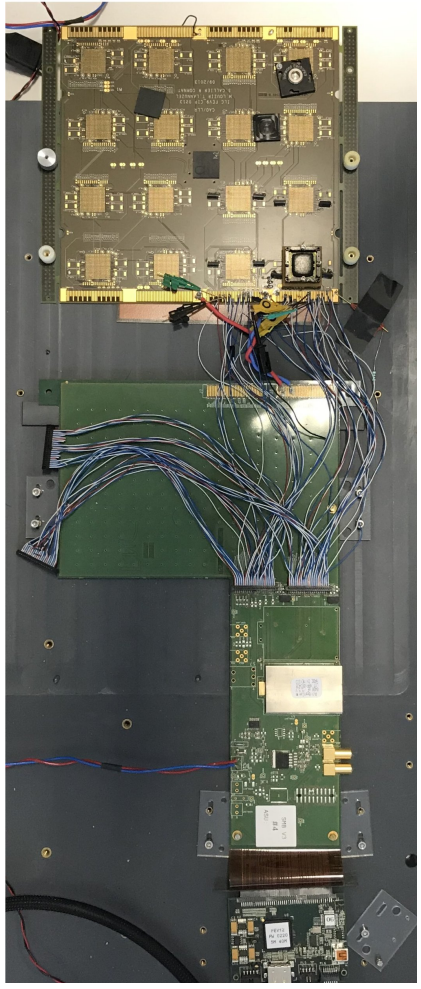
Chip Testing Bench

Pbm:

- Noisy ch37: not seen in COB…
  - → new packaging ?
- NovaPack stopped
- Retriggering by ChipSat
  - → better decoupling ?
  - only a pbm if noisy channels… but…
- Powering: stability (FEV13 ?), min. ON period, …

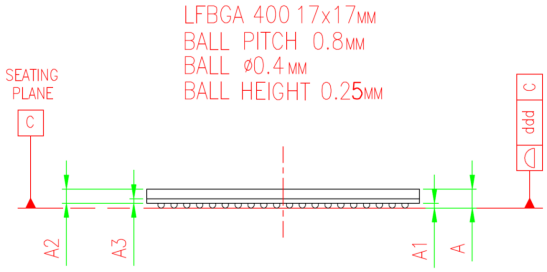
New Chip testing bench

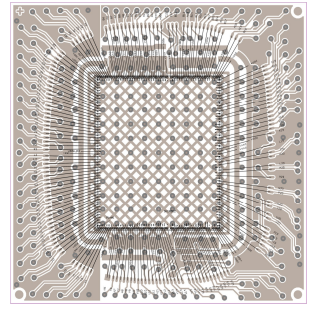
- Based on FEV13
- With baby wafers → Polarisation
  - → Calibration
    - Cosmics + Source

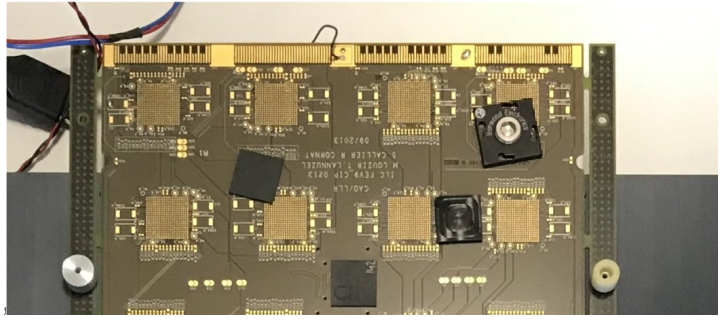


SK2a packaging

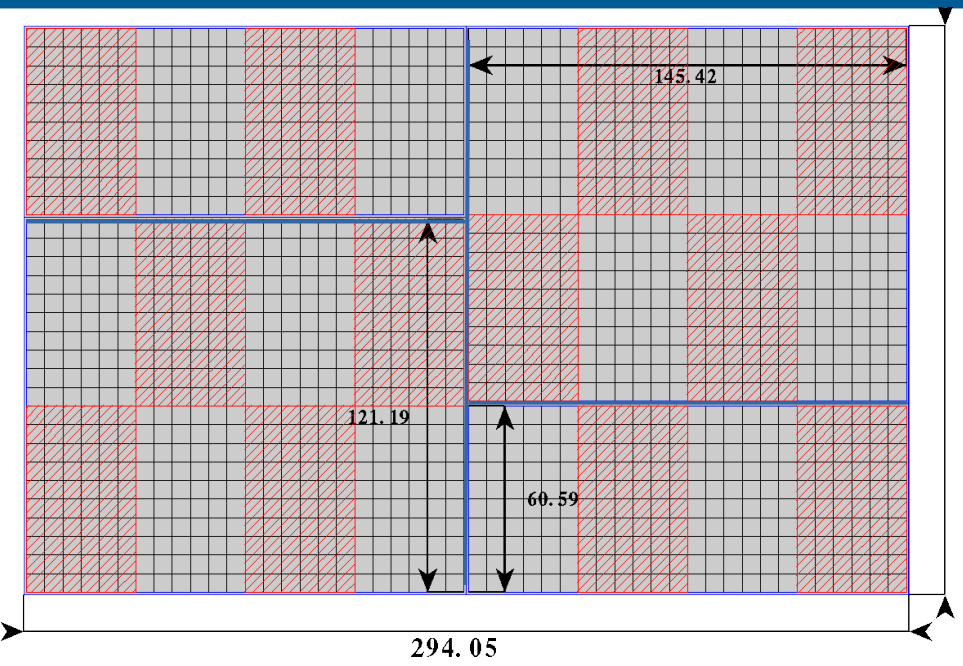
- Stop of NovaPack
- → APTASIC SA
  - CH-2017 Boudry (!)
  - sub-contacted to HYBRID SA
- Same layout as prev.
  - but Mini-PCB (≠ lidframe)
- 1 pre-prod received (10)
  - Being tested...







FEV-14: Prototype for ILD



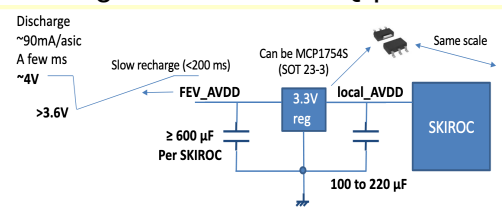
TDD:

- 24 ASICs of 60 ch. = 1440 ch
- Pads = ~ 6mm

Requirements:

- Test 24 ASICs, dim ~ TDD
  - Prototype compatible with 6" and 8" wafers
- Stitchable (→ EndCard or GradConn loops)
- Re-optimised routing
  - Reduced re-triggers (RamFull) / Data & Clock Integrity
- Reduced readout time → 2 partitions (*a la* FEV11)
- GradConn / style connectors (thin design) ?
  - Compatible Compact DAQ
- High-Lumi scheme compatible ? Power Pulsing @ 5 – 15 Hz
  - Thin capacitors ? Regulators ?
- HV distribution from the top
  - + Kapton on the side (between ASU's
  - → Independent ASU for testing
- Combined BGA / COB design ?

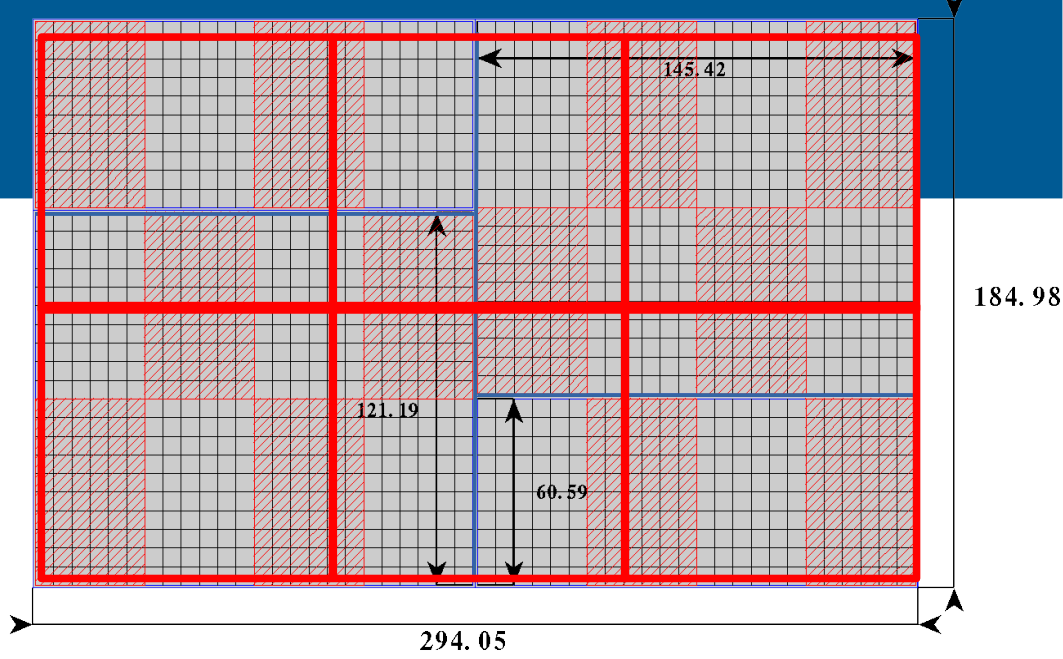
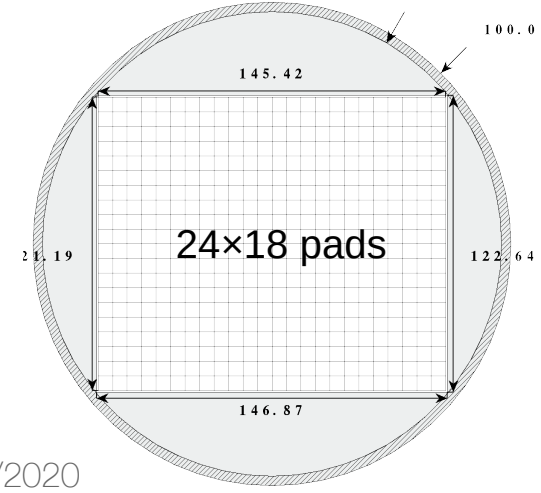
Regulator ? See DAQ pres.



FEV-14 Geometry

Prototype compatible with 6” and 8” wafers

- 6” wafers = 16×16 pad of 5.5 mm
- 8” wafers (TDD) = 24×18 (+12×18) pads of ~6 mm
  - y = 2×16 = 32 cells ≠ 27 = 1.5×18 cells
  - x = 3×16 = 48 cells ≠ 44 = 2×24 cells



- OK if square 8” wafers of 24×24 + 2×(12×24) 5.5 mm pads
  - y = 24+12
  - x = 2×24
  - ⟶ special prod. in June ?