

SDHCAL status

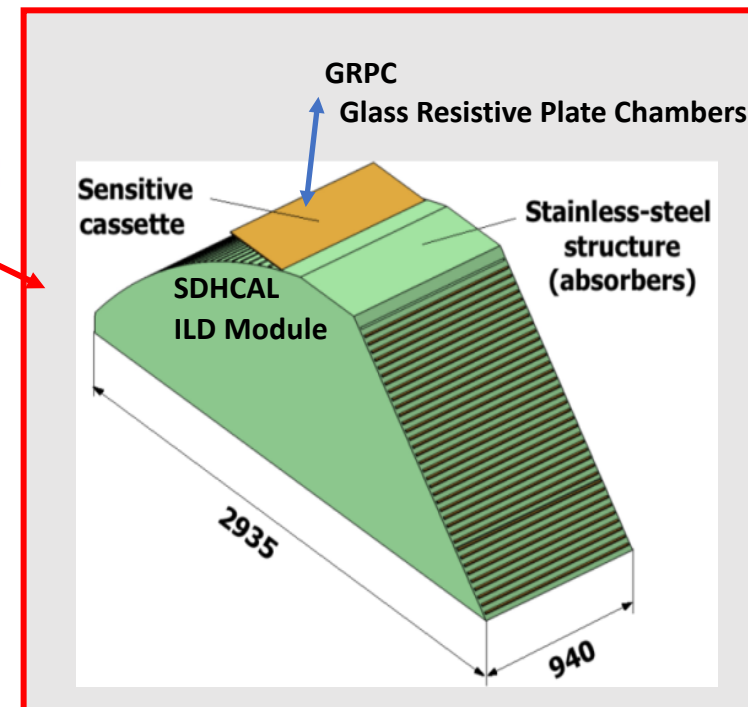
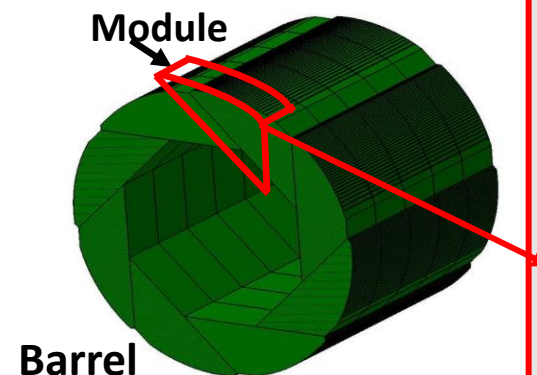
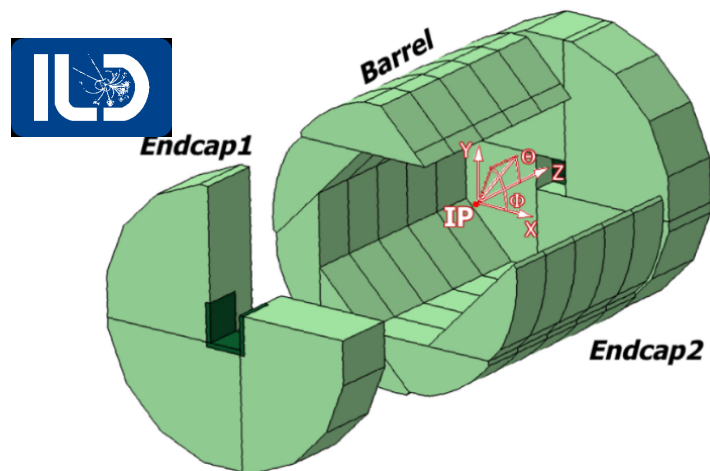
Mary-Cruz Fouz

On behalf of the SDHCAL group

CIEMAT

The new SDHCAL prototype

The new SDHCAL prototype



The $\sim 1\text{m}^3$ prototype built in the past was based of layers of plates absorbers of $\sim 1\text{m}^2$

To enlarge them to the maximum size ($\sim 3 \times 1\text{m}^2$) expected at ILD, implies new challenges for the detector, embedded electronics and mechanics

The goal

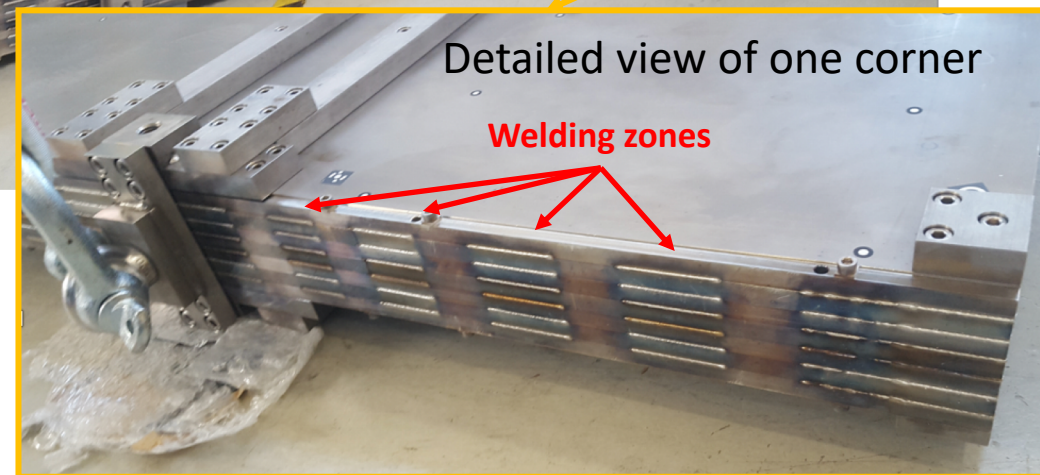
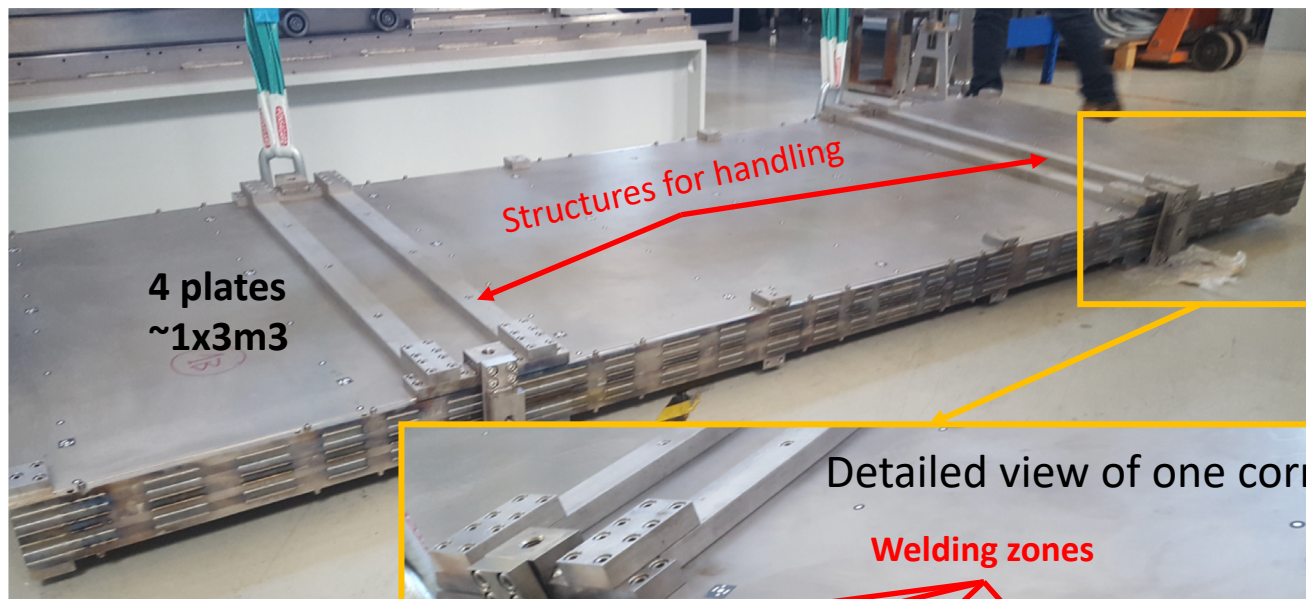
To build a ***new prototype with a mechanical structure of 4 plates of $\sim 1 \times 3\text{m}^2$*** (assembled with similar procedures to the final one) where inserting large ***RPCs equipped with a new improved electronics.***

Mechanical developments: Calorimeter absorber

Evaluation of the use of Electron Beam Welding for the assembly of the absorber mechanical structure



Introduction of the pre-assembled absorber structure inside the EBW machine at CERN

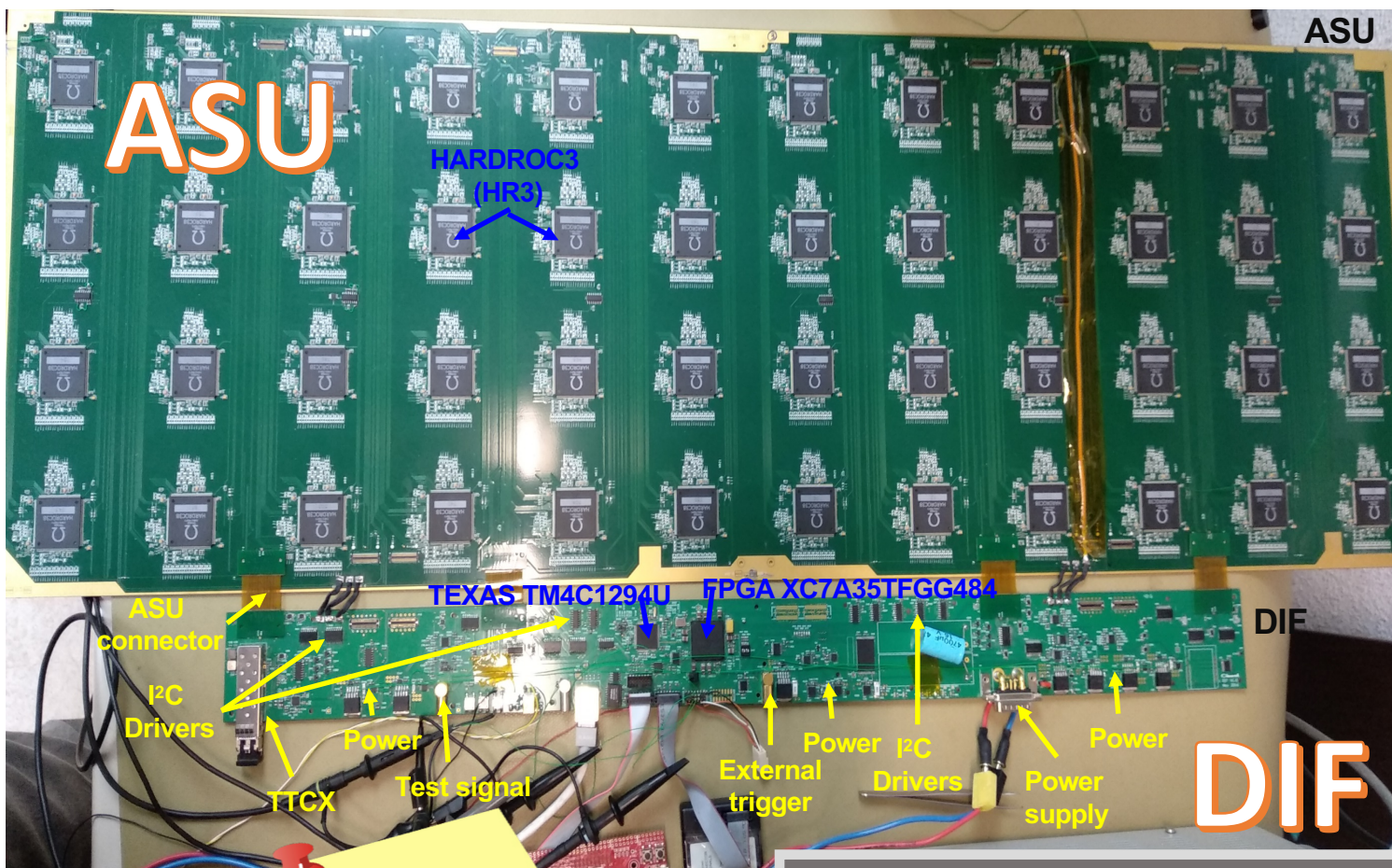


See MC Fouz's talk at the
CALICE Utrecht meeting

https://agenda.linearcollider.org/event/8109/contributions/43649/attachments/34441/53114/SDHCALMEchanics_EBW.pdf

DIF+ASU under tests

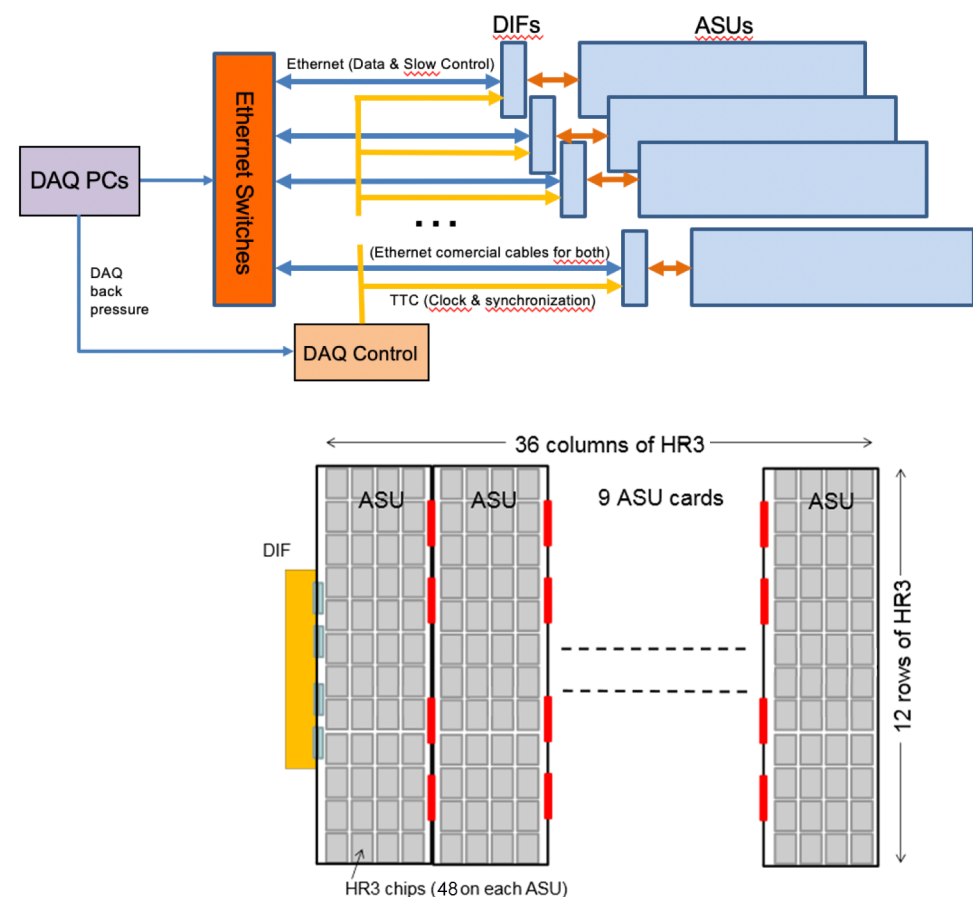
5



4 DIFs
Fully assembled
and operational

Some data acquisition & power pulsing tests still pending

Documentation is ongoing



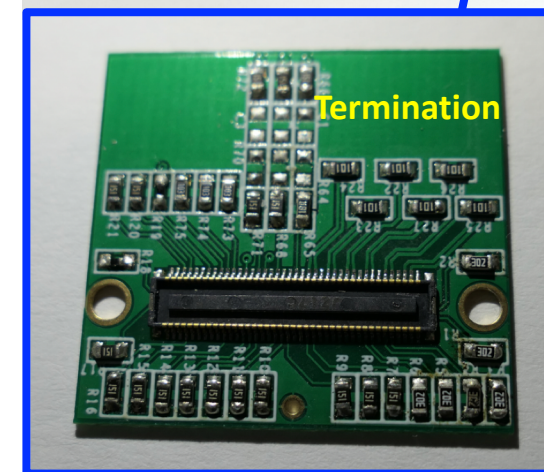
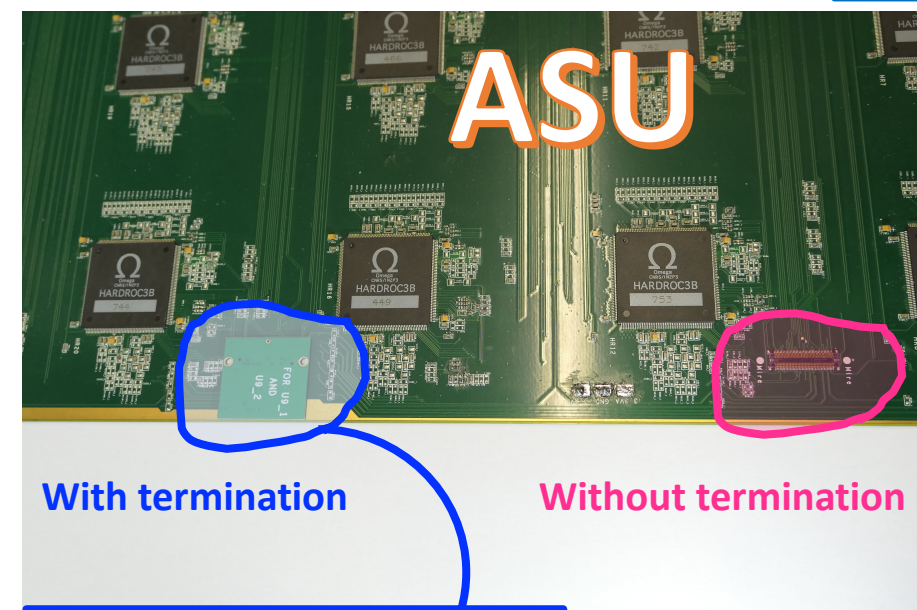
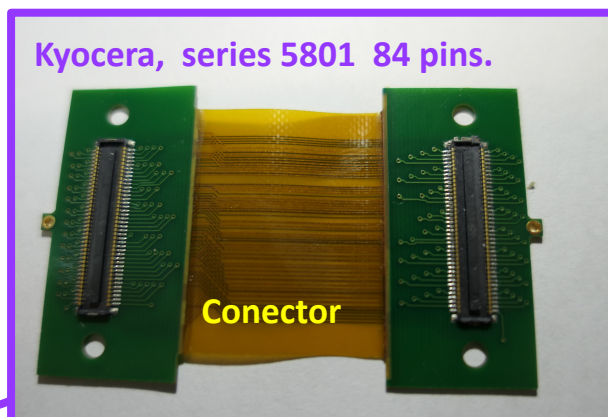
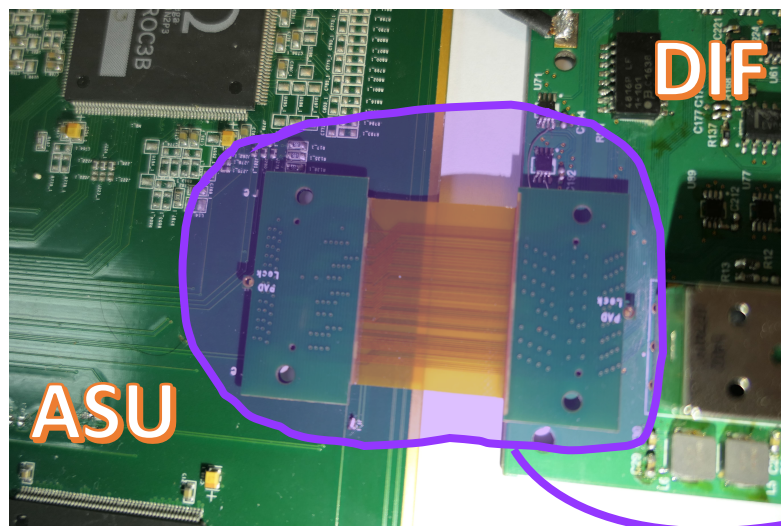
Future steps: **Integration with DAQ**

DIF+ASU tests

6

Main problems found

- It has been observed that the connectors of the boards for **ASU-DIF** and **ASU-ASU connections** are very **susceptible to bad contact** and it is **very difficult to verify** that the connection is correct. The **total consumption and operation of communication through the IC2 lines** provide some hints but not a final verification
- **Termination of certain signals** are **critical for proper operations of clock and communication with the IC2 lines**. **Once fixed, problems are solved**

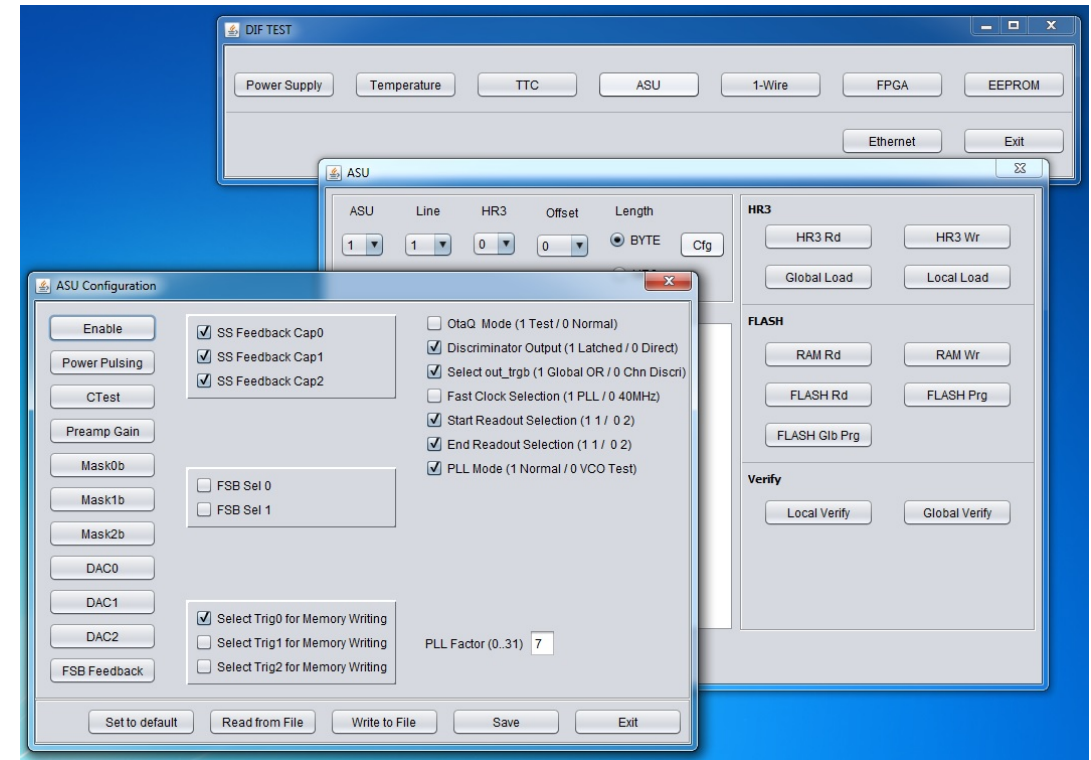


Java Application

7

➤ A Java application has been designed to test the different functionalities of the DIF and ASU boards.

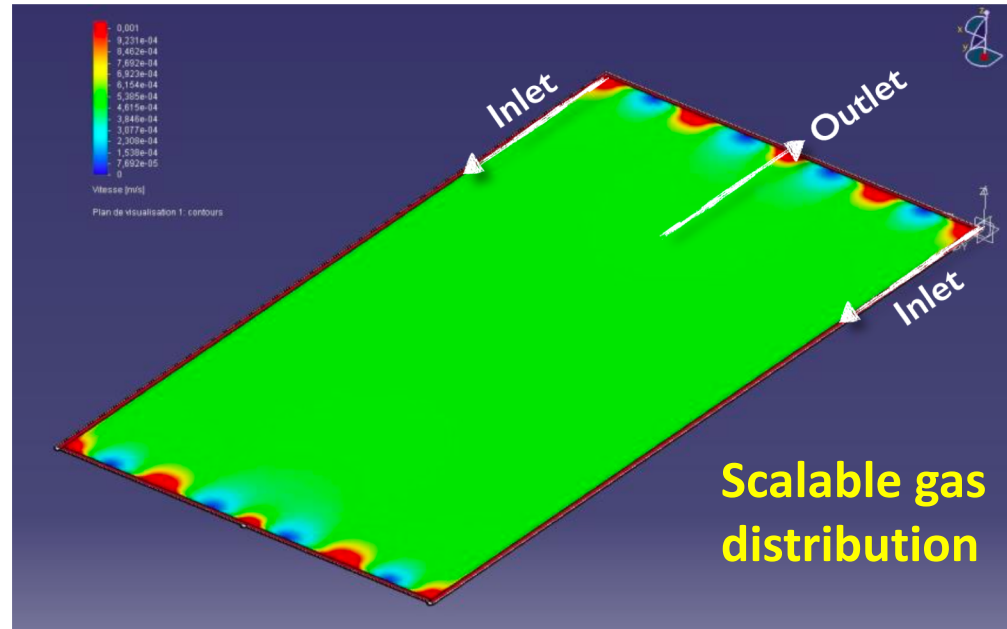
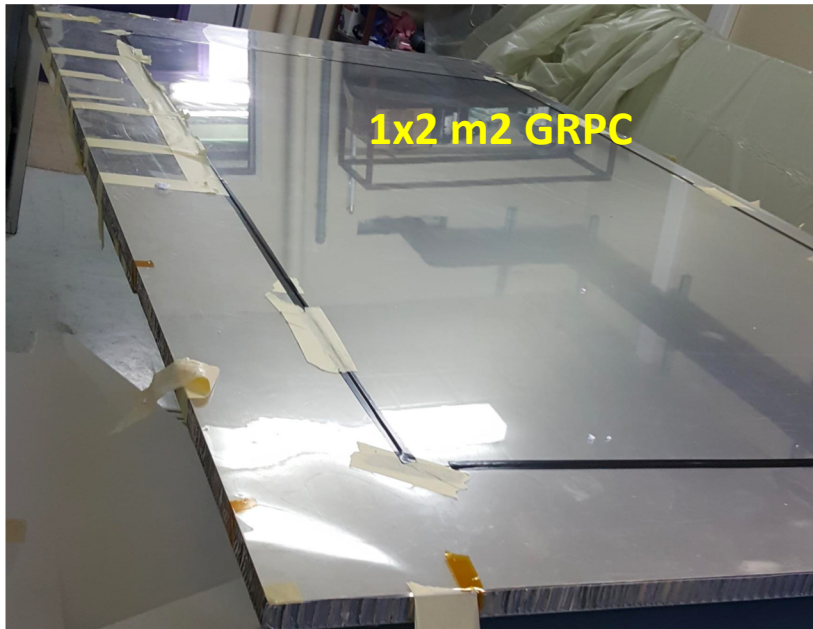
- The application communicates with DIF using the Ethernet link.
- The user can read and write the registers of the different ICs (power supply, temperature, TTC) and those implemented registers using the microcontroller and FPGA. On the other hand, it is possible to read and write the registers of the HARDROC and 1wire chips.



All the functionalities of both boards can be tested using this application

➤ Another Java application has been developed to allow the remote programming of the FPGA memory. Other allowed actions are: blank checking, erasing, etc.

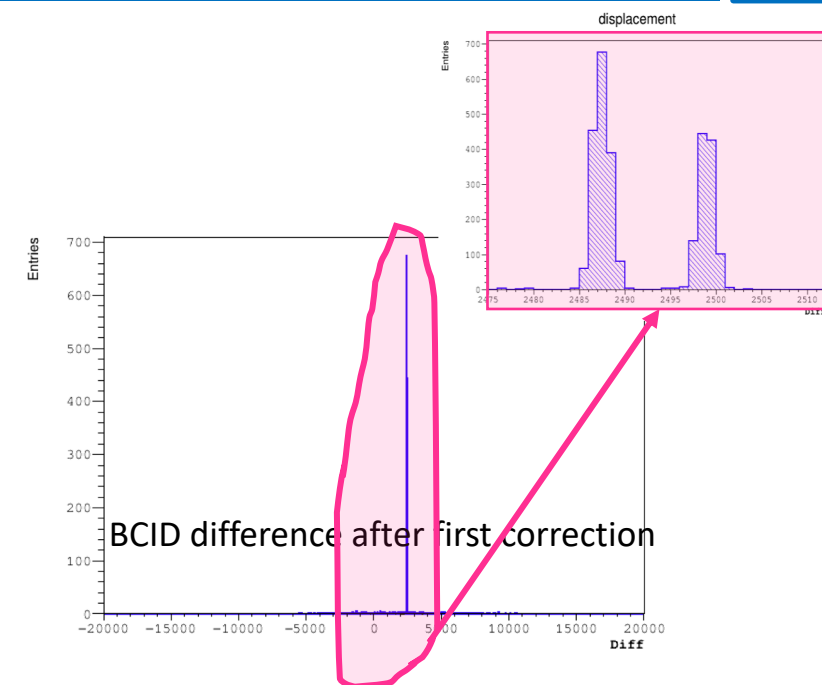
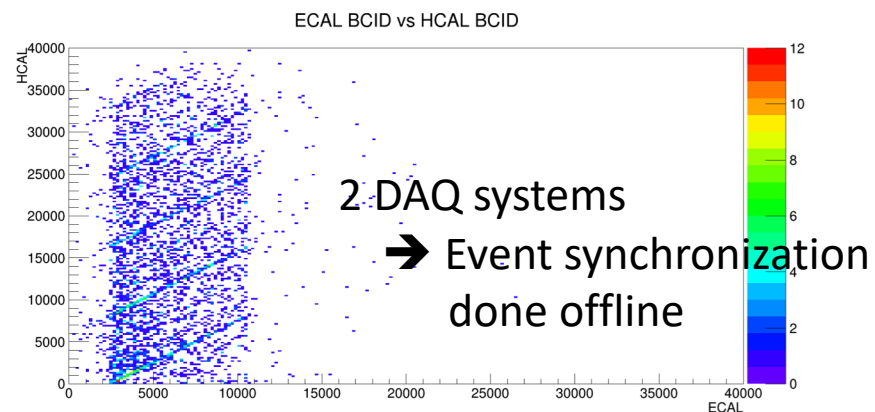
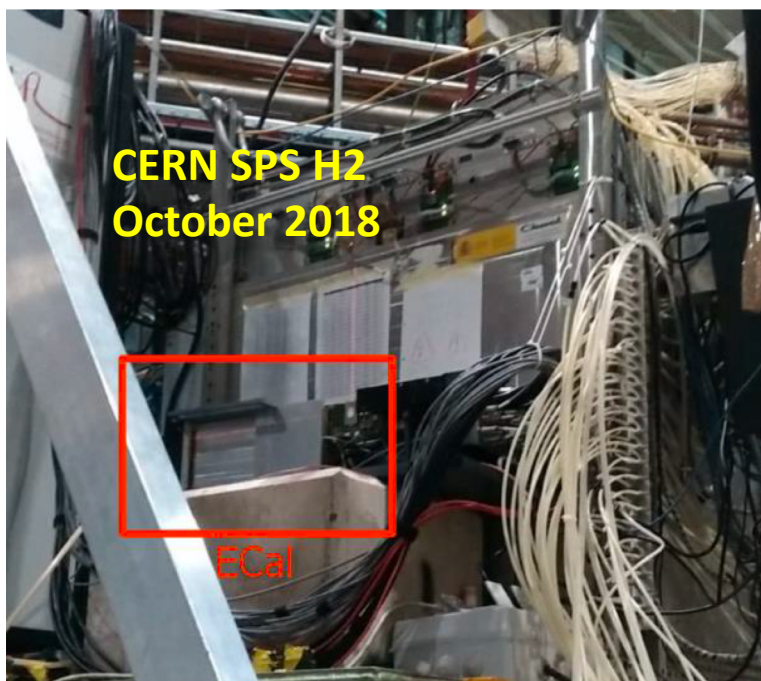
Large GRPC



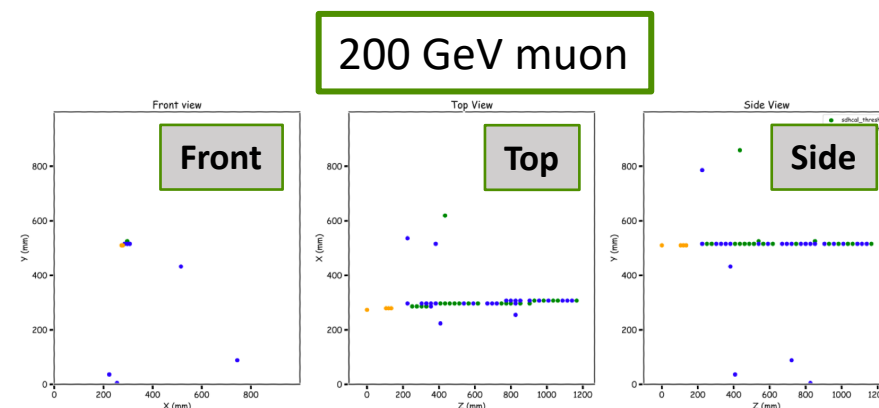
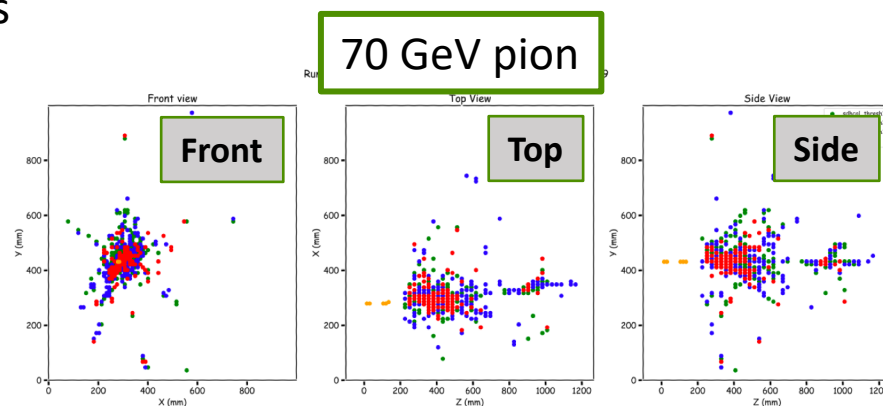
1m³ prototype - test beam data analysis

SiECAL + SDHCAL Common beam tests

10



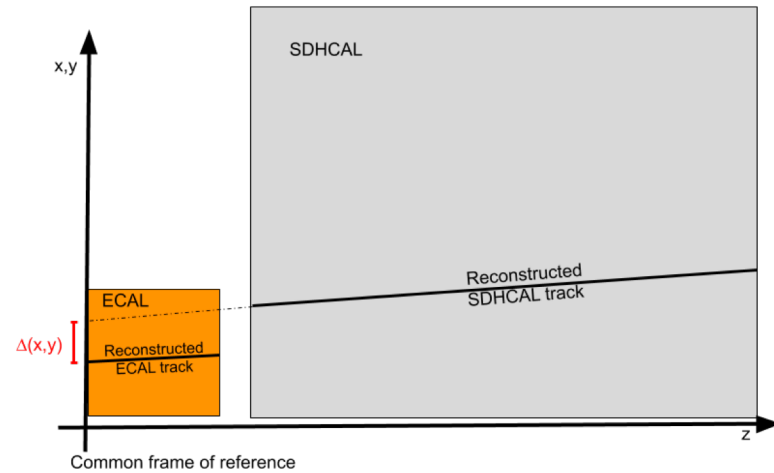
SiWECAL: 10 Layers
SDHCAL: 37 Layers



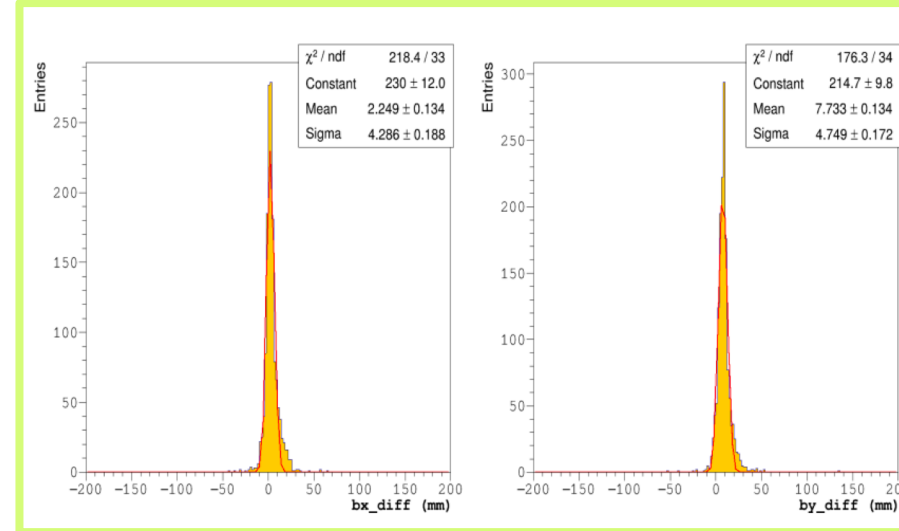
SiECAL + SDHCAL alignment

11

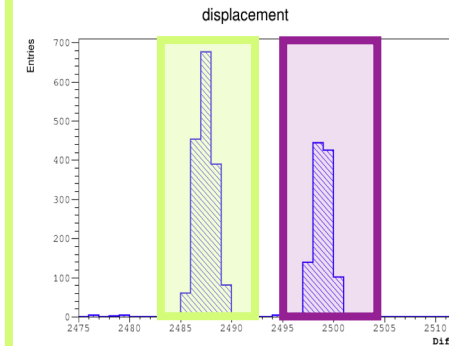
Alignment between both prototypes
Using tracks of muons



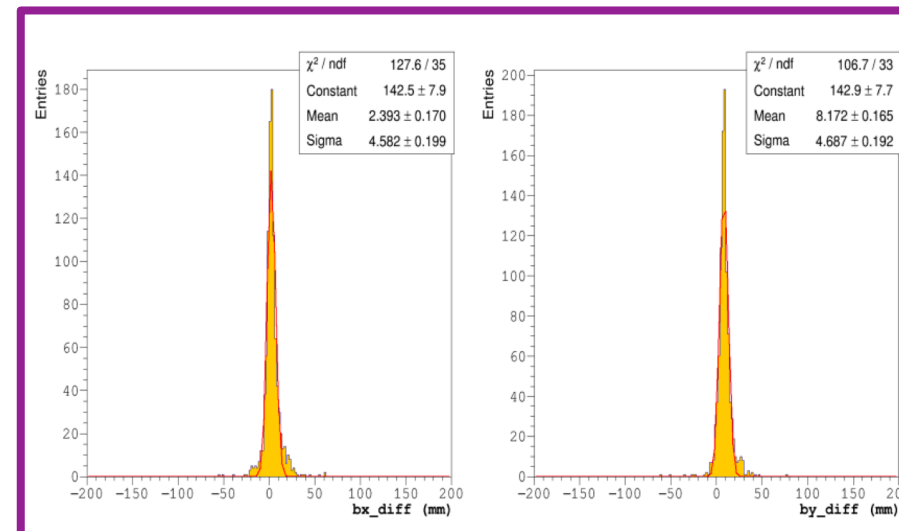
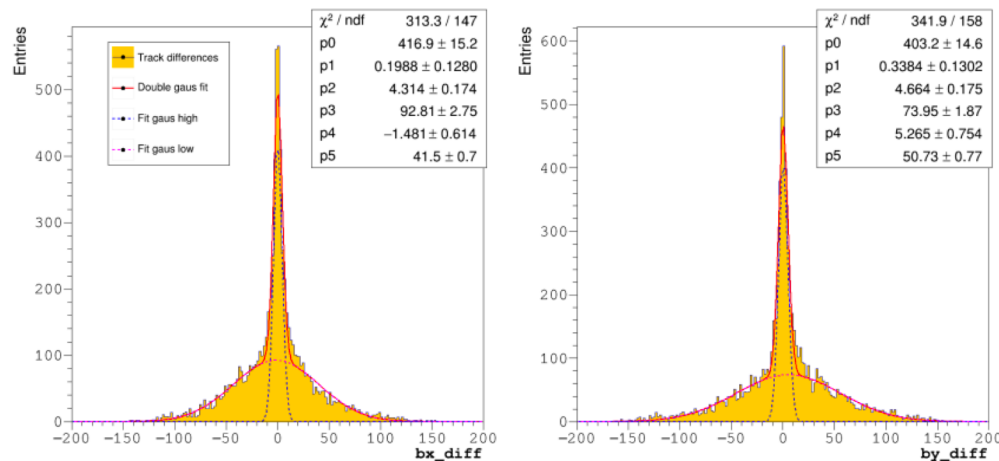
Difference of ECAL and SDHCAL track positions with
more restricting timing cut



Peak BCID difference
[2485,2489]



Difference of ECAL and SDHCAL track positions after alignment



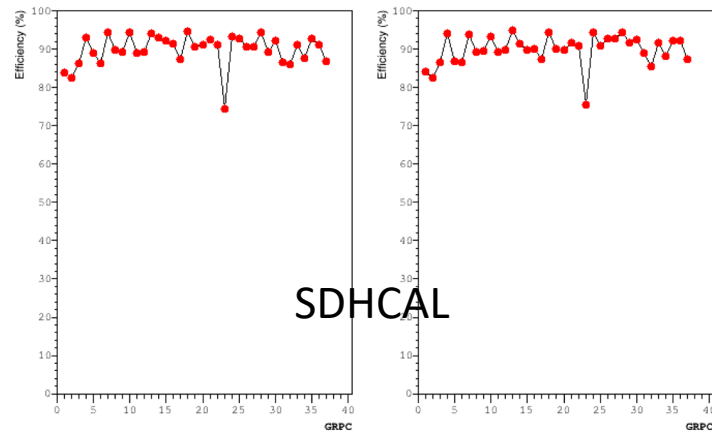
Peak BCID difference
[2496,2500]

Tails disappear

Something on Performance from last test beam

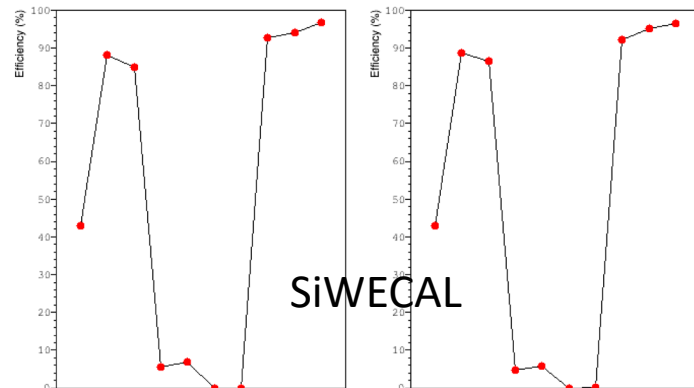
12

Efficiency computed using common muon tracks

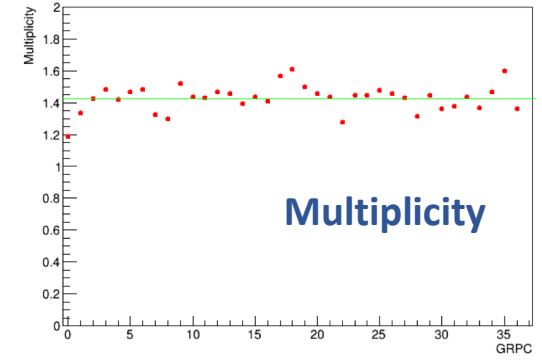
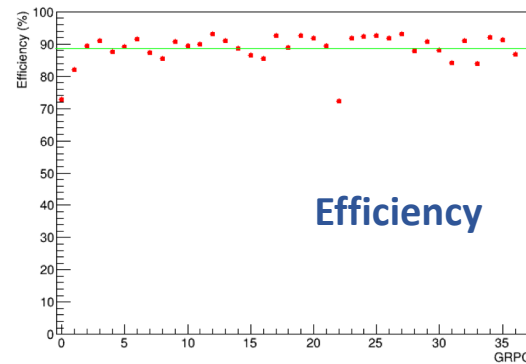


Peak BCID [2485, 2489]

Peak BCID [2496, 2500]



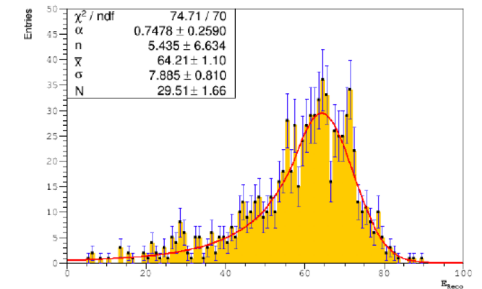
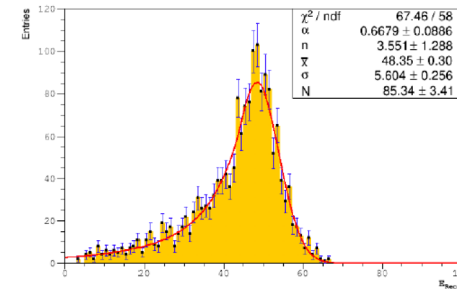
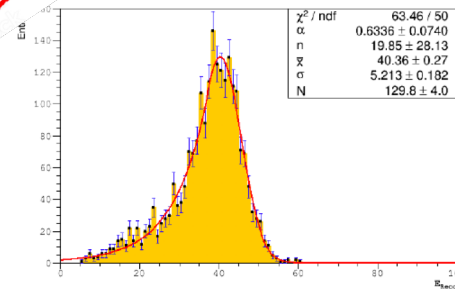
PRELIMINARY



40 GeV Pions

50 GeV Pions

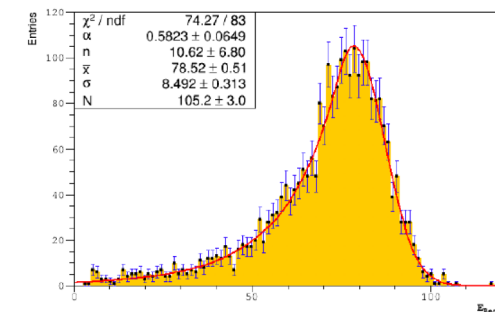
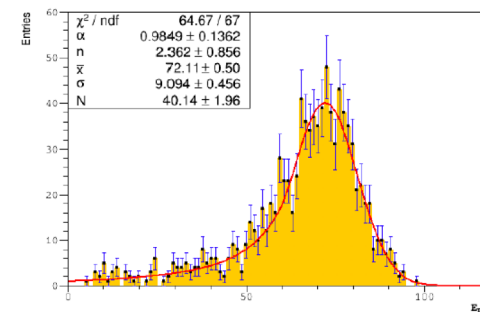
60 GeV Pions



Energy Reconstruction
Digital mode

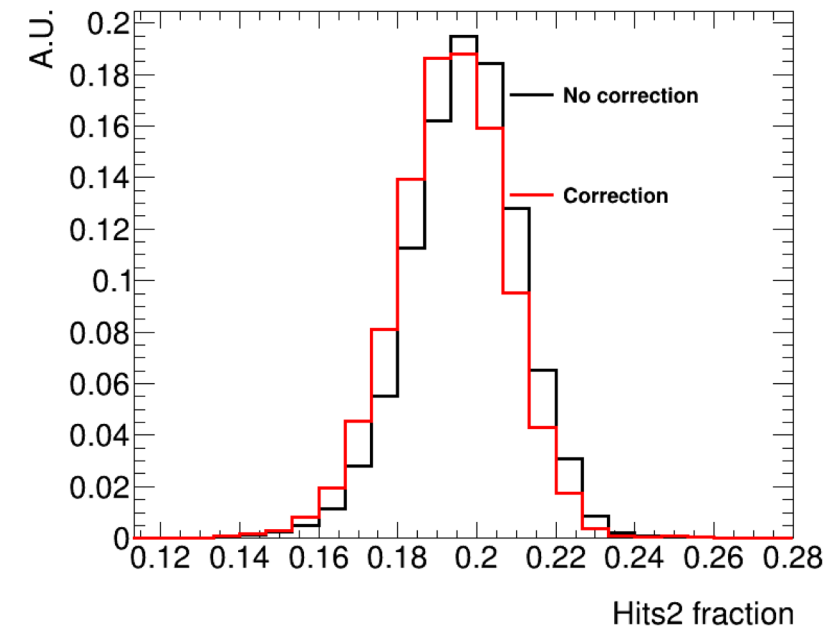
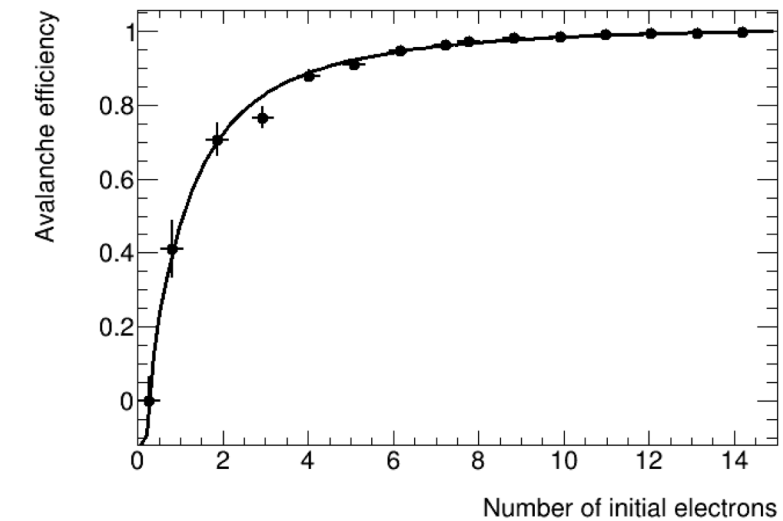
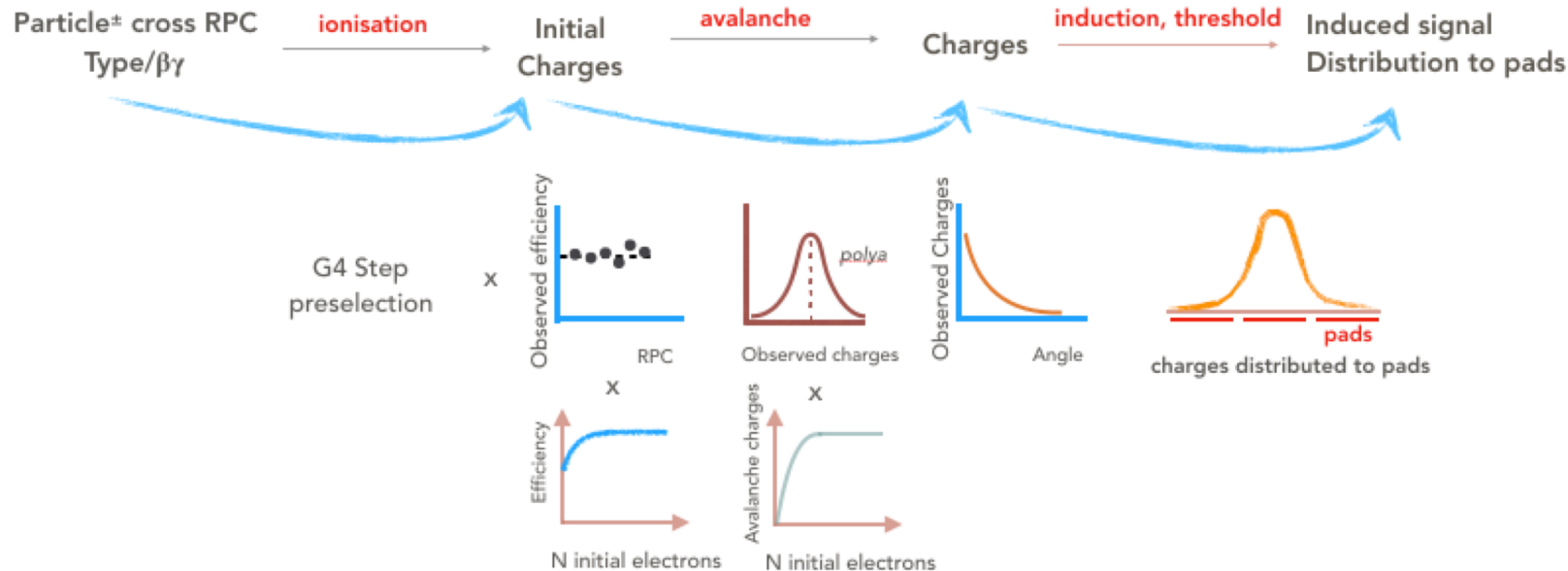
70 GeV Pions

80 GeV Pions



Simulations

RPC Digitization



- * Digitisation of RPC based high granular calorimeter is **challenging**:
- * Requires good modelling of both isolated and overlapping hits
- * Large number of (overlapping) effects
- * Digitiser model implemented and tested with SPHCAL prototype:
- * Reasonable description of electrons data and pions below 40 GeV despite its complexity
- * Several improvements identified, some already implemented
- * Modelling of the digitisation under study for **gas replacement**

Timing

SDHCAL – Nearby hadronic showers separation

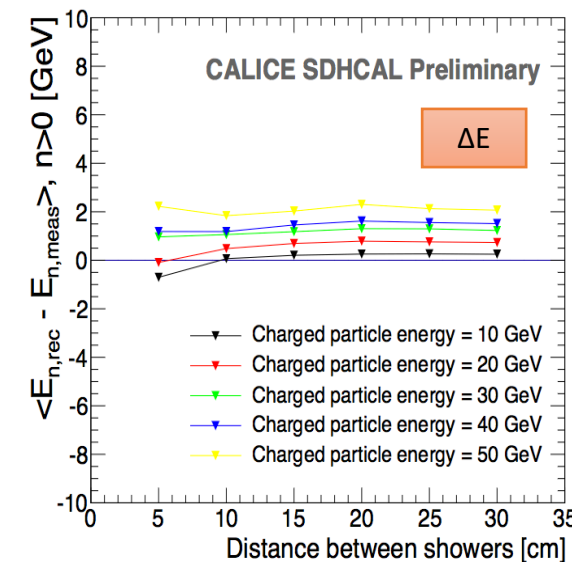
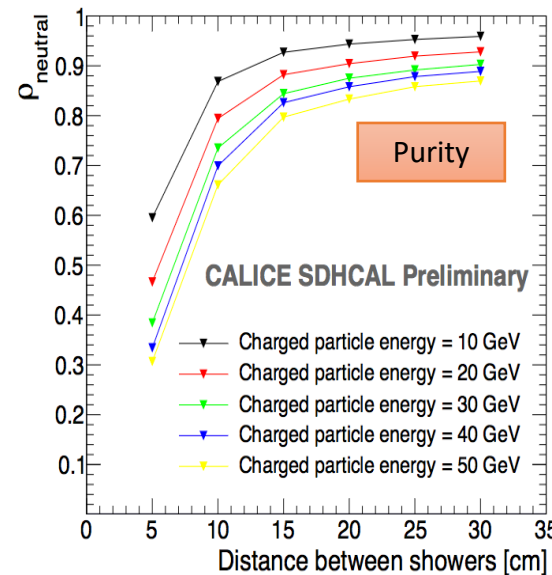
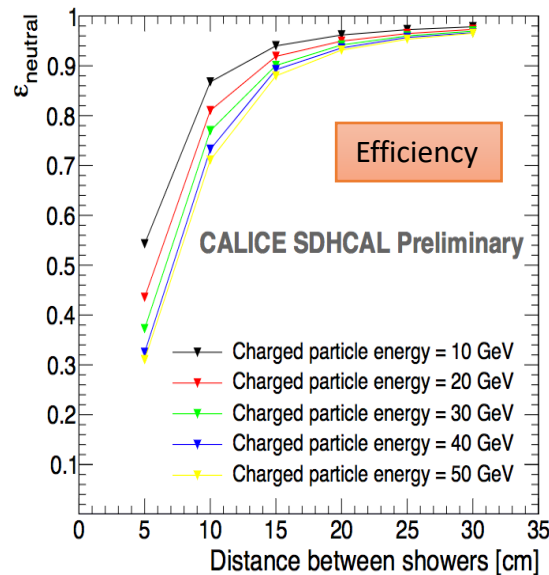
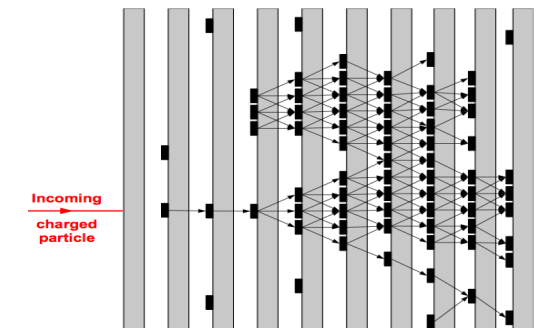
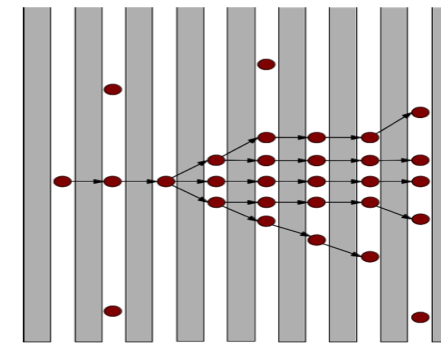
16

SDHCAL high granularity is good

It helps to optimize the connection of hits belonging to the same shower by using first the topology and then the energy information

ArborPFA algorithm:

It connect first hits and then their clusters using distance and orientation information then correct using tracker information (momentum)

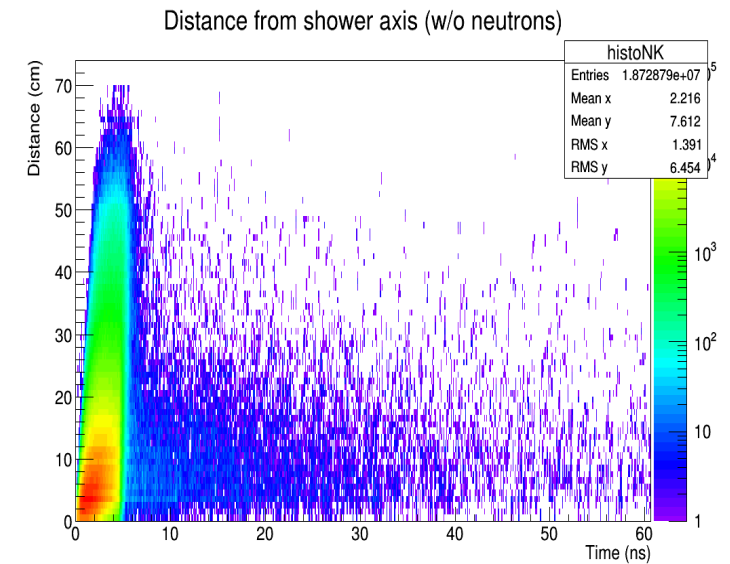
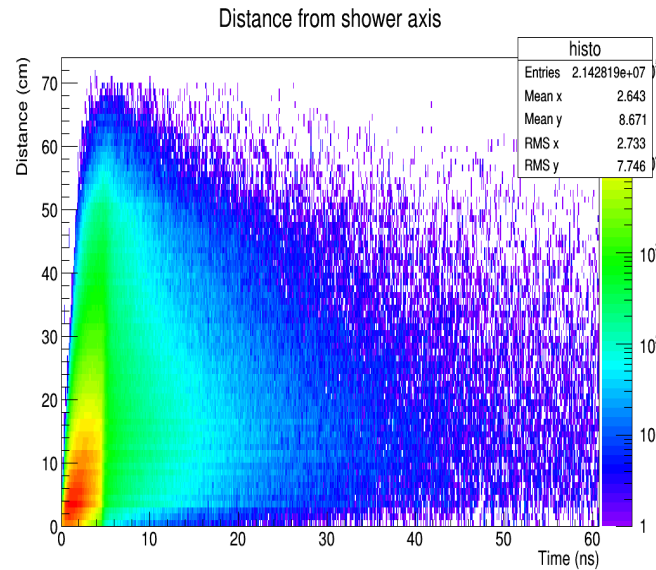
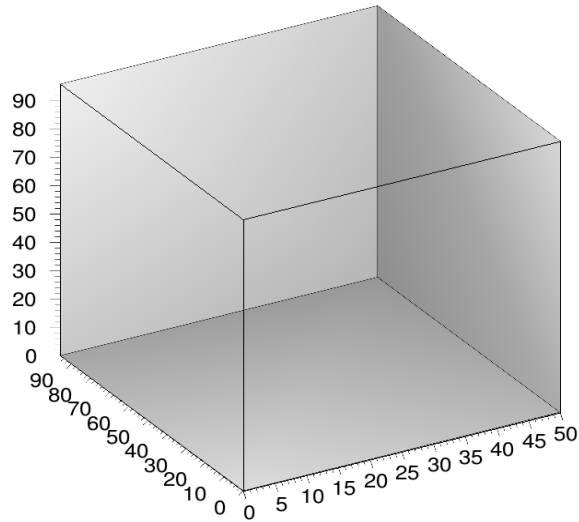


CALICE note CAN054

Using the 2012 CERN SPS H6 test beam data

Timing - neutrons

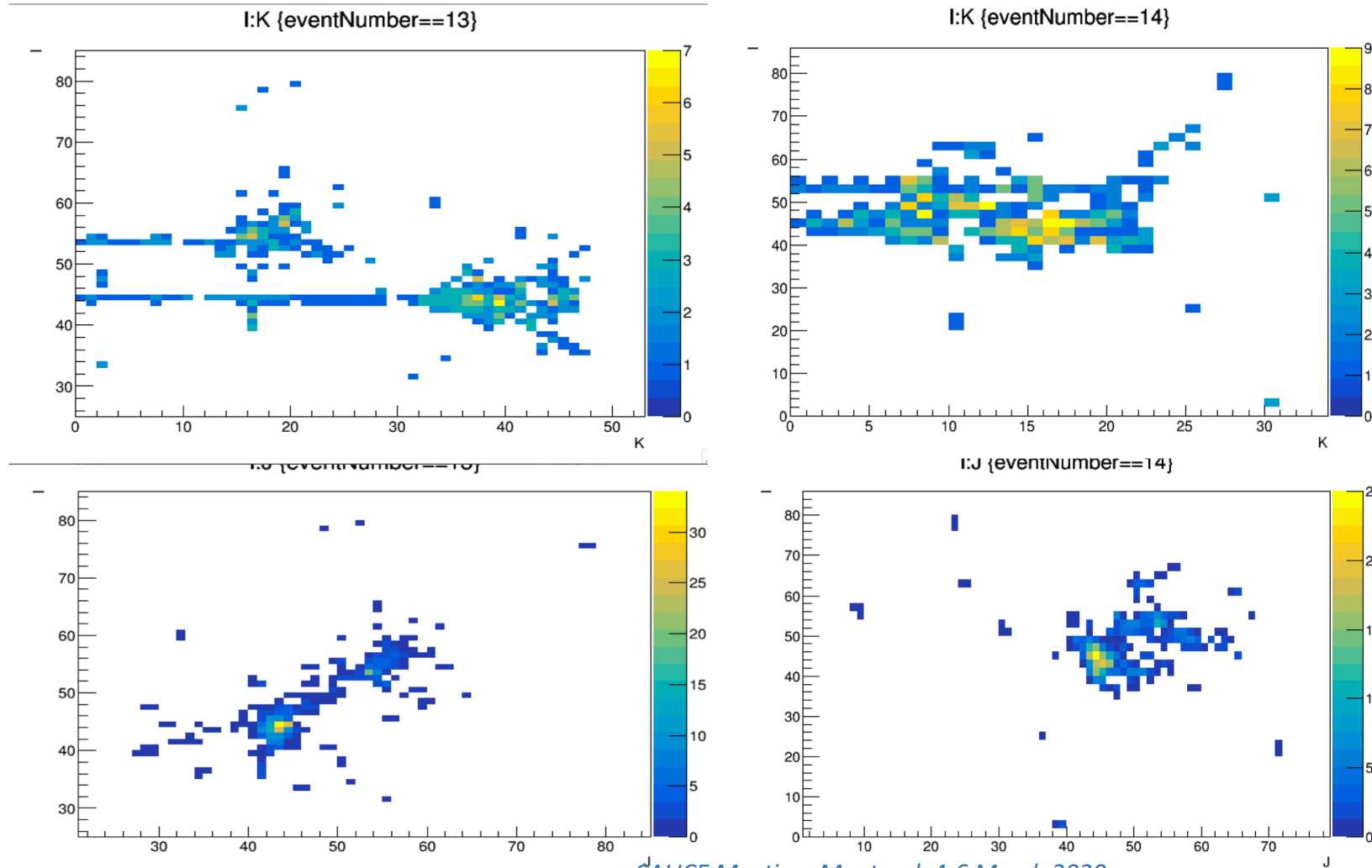
Timing could be an important factor to identify delayed neutrons and **better reconstruct their energy**



Timing – nearby showers separation

18

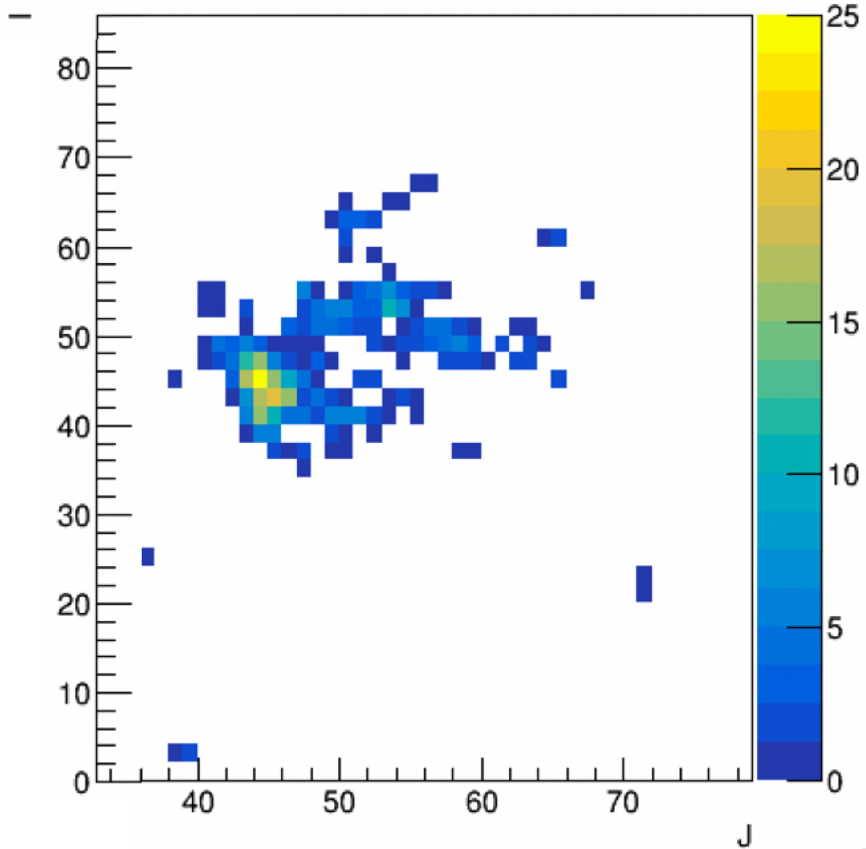
Time information can help to separate close by showers and reduce the confusion for a better PFA application.
Example: π -(20 GeV), K-(10 GeV) separated by 8 cm.



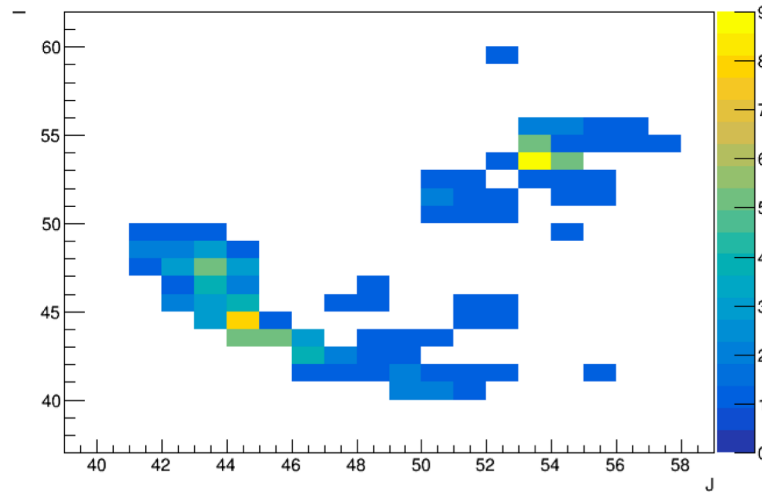
Timing – nearby showers separation (II)

If we have 1 ns resolution

I:J {eventNumber==14}

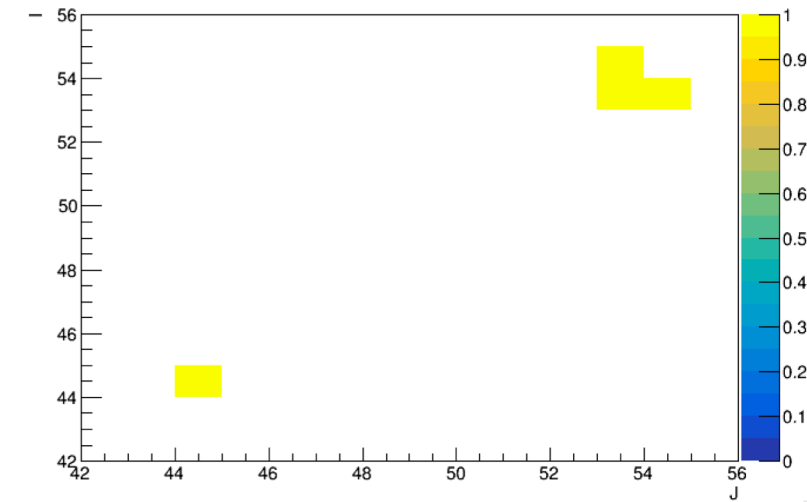


I:J {eventNumber==14&&time>6.7&&time<7.7}



If we have 100 ps resolution

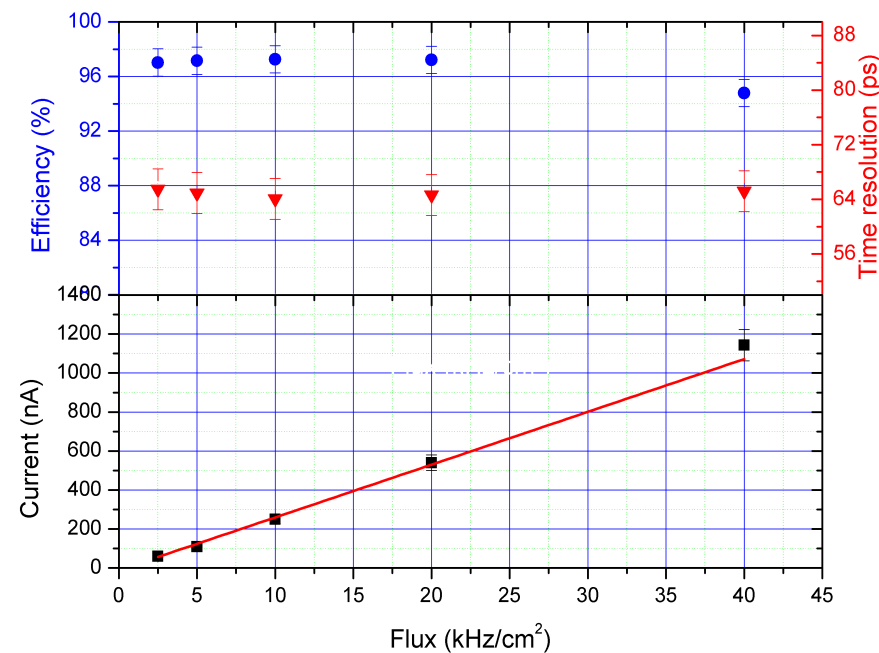
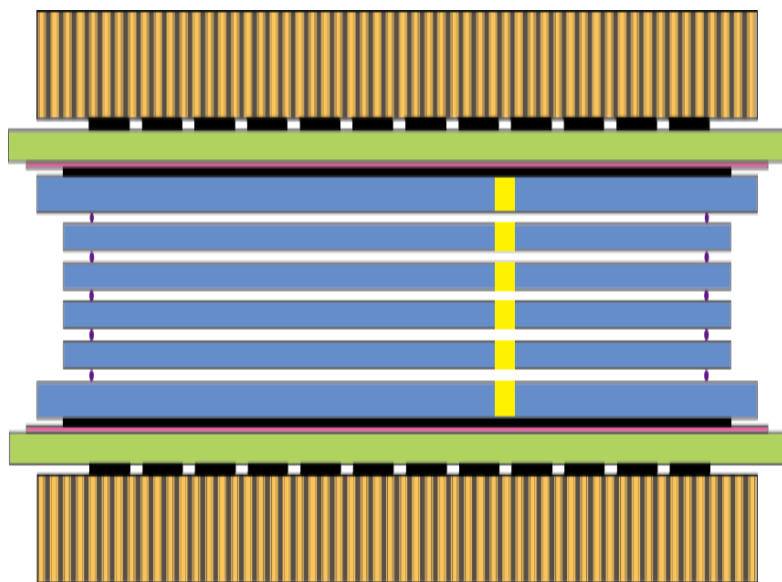
I:J {eventNumber==14&&time>6.7&&time<6.8}



Timing – How to achieve excellent time resolution?

- Multi-gap RPC are excellent fast timing detectors

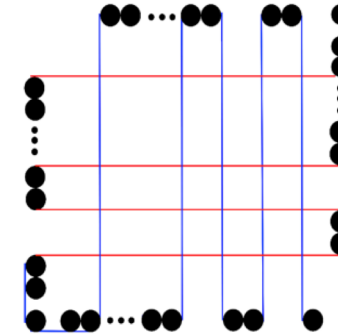
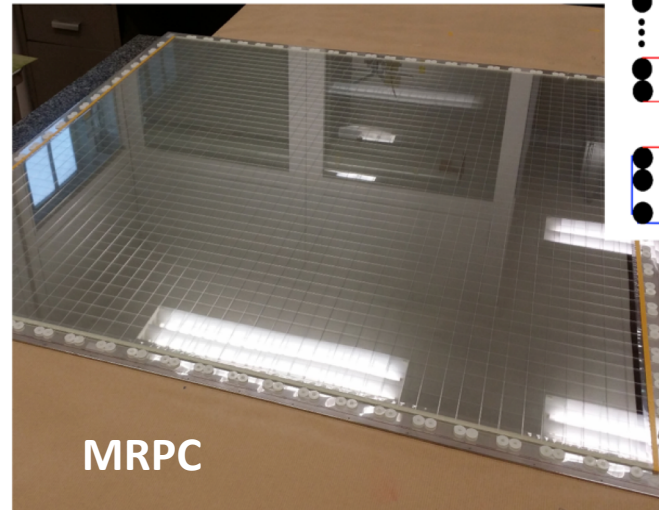
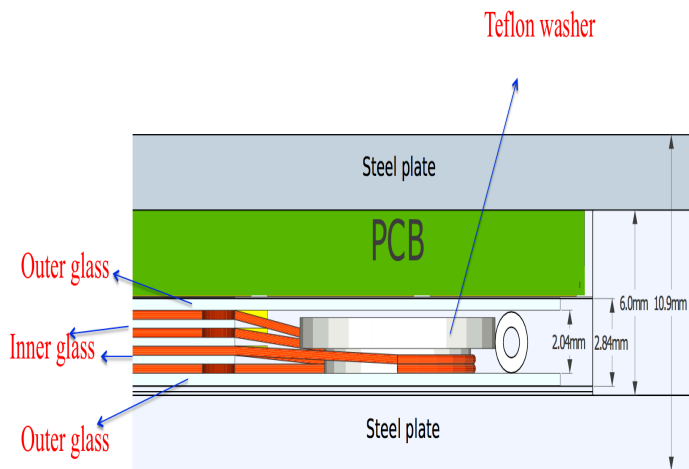
Time resolution of *better than 100 ps* was obtained with 5-gap RPC by Tsinghua group



Timing – How to achieve excellent time resolution?

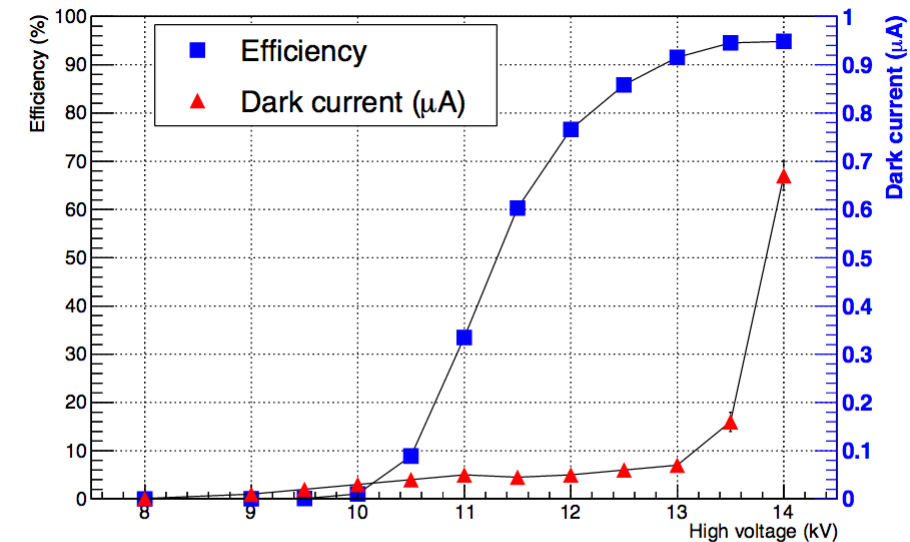
21

- Multi-gap RPC are excellent fast timing detectors



Schematic of the fishing lines configuration for odd and even layers

NIMA, volume 871,
November 2017,113-117



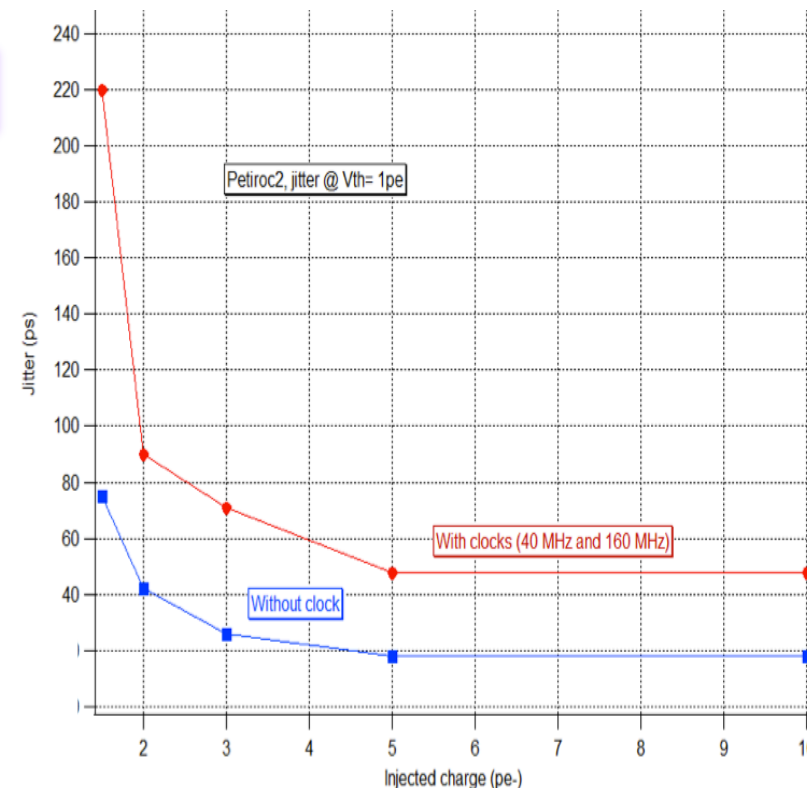
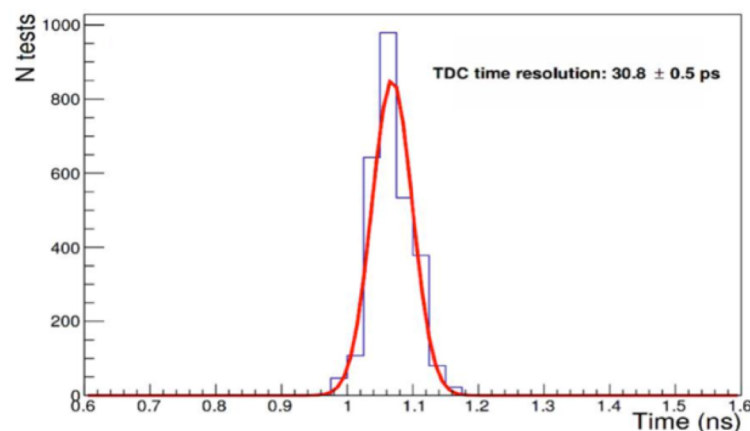
Threshold sets at 114 fC

Timing – How to achieve excellent time resolution?

❑ An ASIC with a fast preamplifier, precise discriminator and excellent TDC

→ **PETIROC 32-channel**, high bandwidth preamp (GBWP > 10 GHz), <3 mW/ch, dual time and charge measurement ($Q > 50$ fC).
jitter < 20 ps rms @ $Q > 0.3$ pC

→ TDC (delay-line, Vernier,..etc)



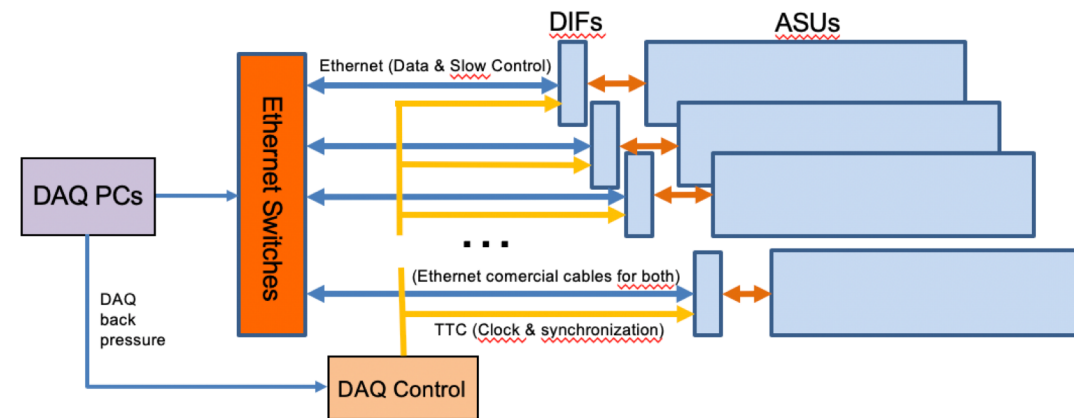
- Develop large MRPC (1 m x 1 m) with excellent time resolution
- Develop large pickup pads PCB hosting both the PETIROC with TDC in collaboration with the Chinese group of SJTU
 - Later use ToT if possible for “analog” readout.
- Develop DIF boards
- Build several detectors and several electronics board to equip them
- Develop a DAQ system allowing to read out both SDHCAL electronics (HR2) and the new ones that use PETIROC
- Replace some of the SDHCAL layers with the timing ones and check the G4 model validity for what concerns time information
- Replace all of the SDHCAL layers with timing ones (if funding)





SDHCAL DAQ architecture

A **central PC** collects data from all the **ASUs** (containing de **ASIC chips**) through an **Ethernet switch** acting in such a way as **data concentrator** and generates the required commands for **ASU** and **DIF** configuration generating at the same time **synchronization signal** required for a correct data acquisition process.



DIF architecture

- Only **one DIF per plane** (instead of three)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors
(vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**

