Analysis of SiW-ECAL technological prototype beam test with electron beam

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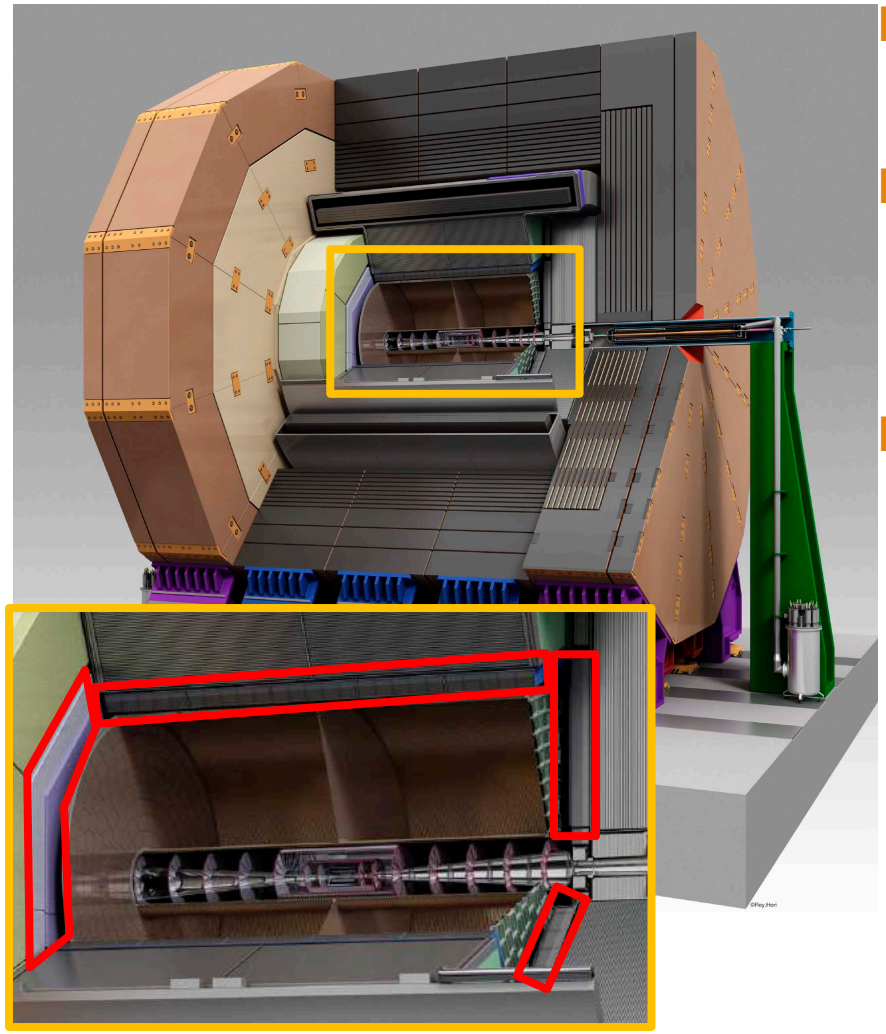
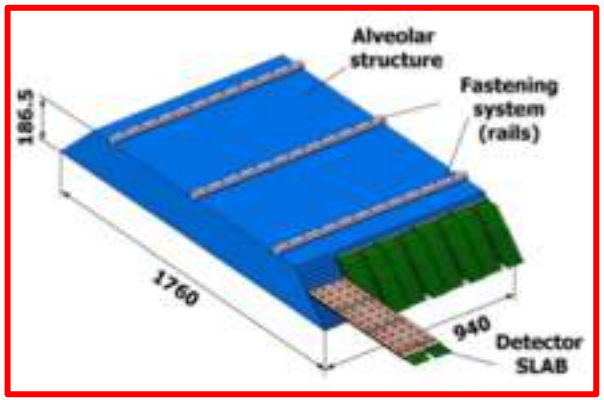
International Large Detector



- One of the detector concepts at the ILC
- Optimized for Particle Flow Algorithm
  - Reconstruct & identify all the particles
- Components
  - Vertex detector
  - Trackers
  - Calorimeters
    - ECAL
      - ScW-ECAL
      - **SiW-ECAL**
    - HCAL
  - Muon Yoke

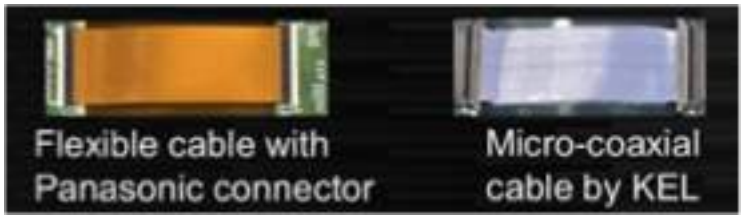
etc.



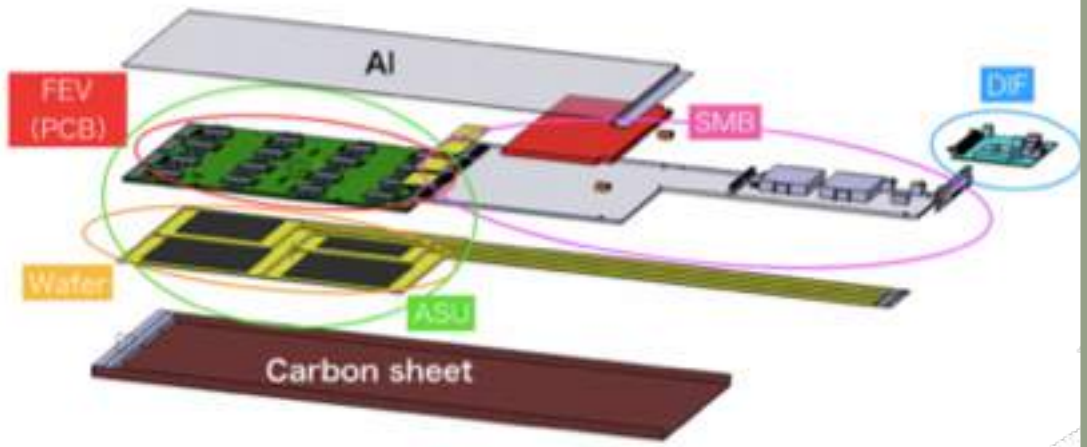
R&D of SiW-ECAL technological prototypes

Major changes in FEV11 → 13 and SMBv4 → v5

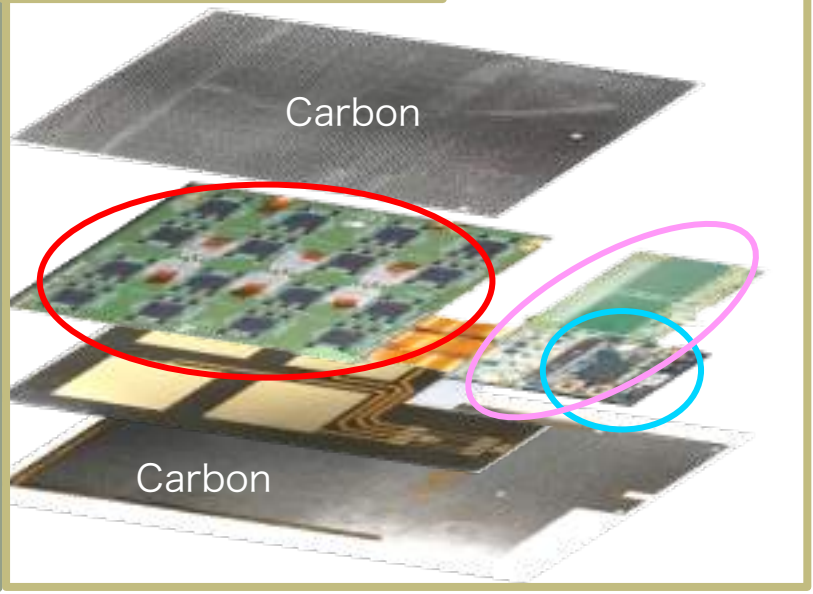
- ASIC: SKIROC2 → 2A
  - Individual threshold control
  - Improvements on TDC
- Smaller SMB footprint
- Connection by 0.4mm-pitch flex cables
  - Two candidates, footprint compatible



FEV11 & SMBv4

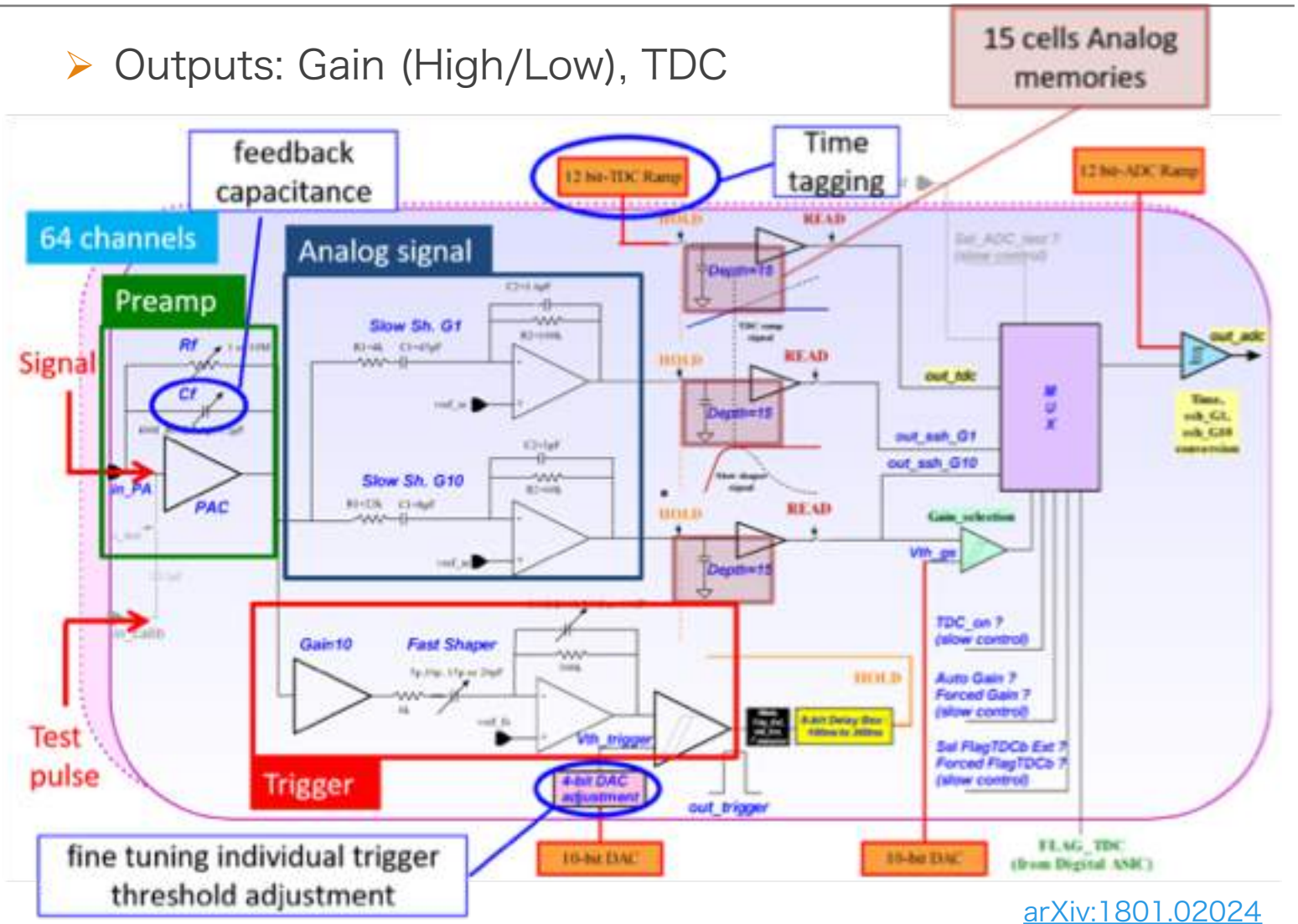


FEV13 & SMBv5



Analogue core: SKIROC2A

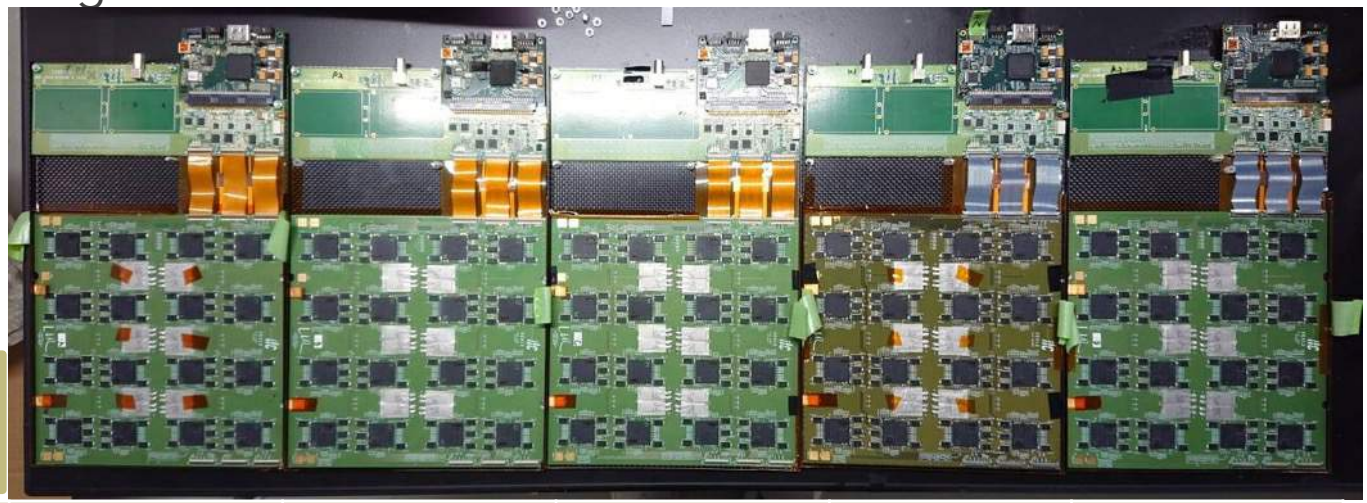
- Outputs: Gain (High/Low), TDC



arXiv:1801.02024

FEV13-Jp Status

- ASIC: SKIROC2A
- Si thickness: 320μm & **650μm** New!
  - 256 ch/sensor × 4 sensor/slab
- FEV-SMB Connection: Flexible cable or Micro-coaxial cable
- EM shielding: w/ Carbon frame and cover
- Power Pulsing

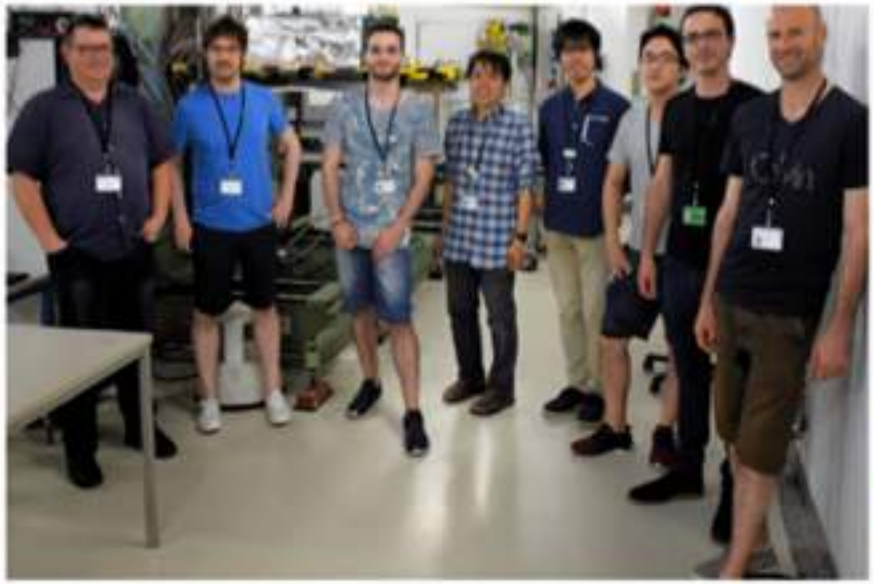


Total 5 slabs
in Kyushu U., Japan

slab ID	P1	P2	P3	K1	K2
Si thickness	650 μm	650 μm	320 μm	650 μm	650 μm
Assembly	in Kyushu U.	in Kyushu U.	in Kyushu U.	in LLR	in Kyushu U.

Beam Test 2019 @ DESY

- Beam time:
  - 24th June - 7th July at DESY test beam facility
  - e^- beam: 1 - 5 GeV
- Presence from:
- Support & Hardware from:



Beam Test 2019 @ DESY

- Beam time:
  - 24th June - 7th July at DESY test beam facility
  - e^- beam: 1 - 5 GeV
- Objectives:
  - Comparison of ASU based on BGA and based on Chip-On-Board (COB)
  - Test of new SL-Boards (SLB)
  - **Validation of FEV13-Jp** ← Target of this talk
- Programs:

MIP program (w/o Tungsten)

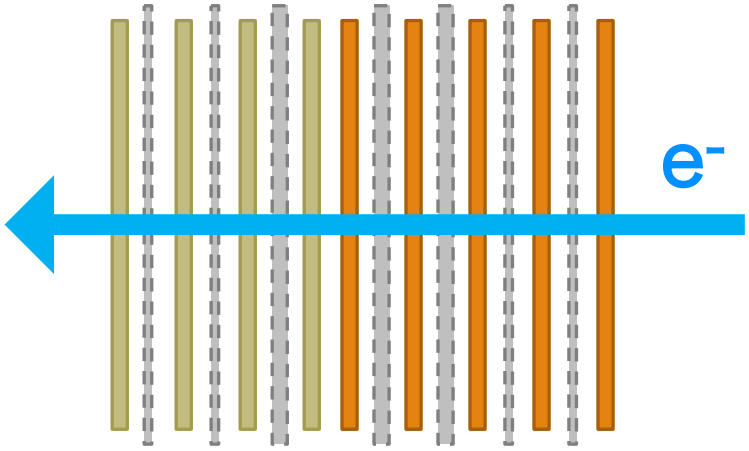
- **Position scan for MIP calibration**
- TDC test
- Angled beam: 25 deg.
- **Retriggering / double pedestal**

Shower program (w/ Tungsten)

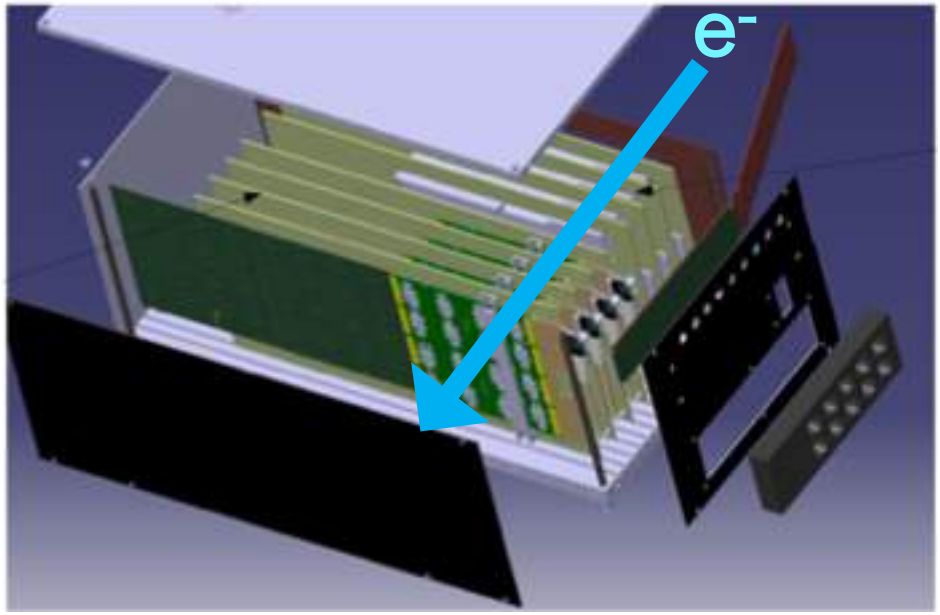
- **Energy measurement**
- Response from large signal
- TDC / auto gain
- Edge effect

Setup for Beam Test

- Devices: 2 types of readouts
  - DIF based slabs: FEV13-Jp × 5
  - SLB based slabs:
    - COB × 2
    - FEV12 × 2
- Absorber: Tungsten
  - X_0 = 3.5 mm, R_M = 9 mm, λ_0 = 96 mm



SLB slabs DIF slabs
Tungsten (2.1 mm / 4.2 mm)



Procedure for Energy Measurement

Single Slab Analysis

1. Trigger adjustment & Masking of noisy channels
2. Pedestal calibration

   16 chips × 64 channels × 15 memories
3. Gain calibration using MIP

   16 chips × 64 channels

Multi Slab Analysis [in progress]

1. Timing coincidence

   using bunch crossing ID (BCID): $\Delta t = 0.2\ \mu s$
2. Event Building

Trigger Adjustment

- Threshold scan is performed for estimation of S/N_{Trig} and trigger adjustment.

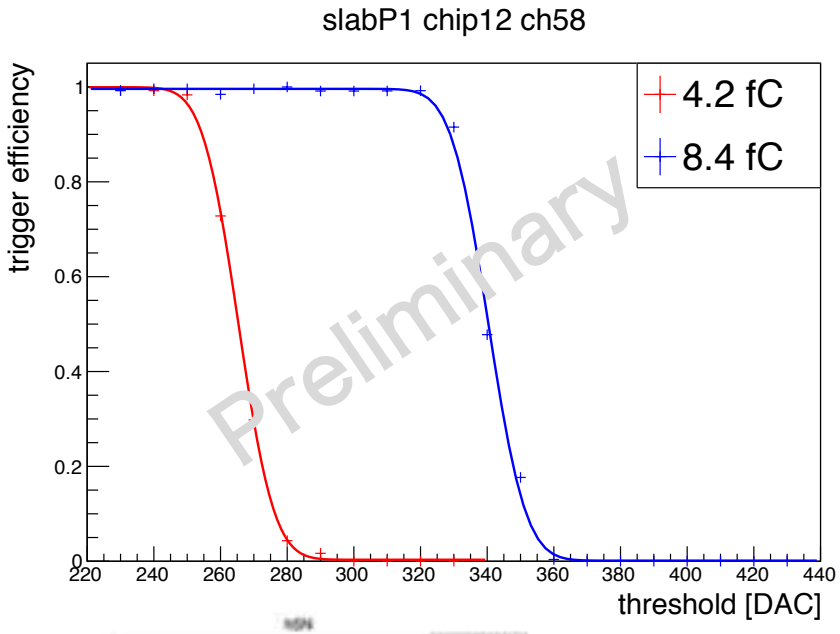
$$S/N_{Trig} \equiv \frac{\mu_{2\mathrm{MIP}} - \mu_{1\mathrm{MIP}}}{\sigma_{1\mathrm{MIP}}}$$

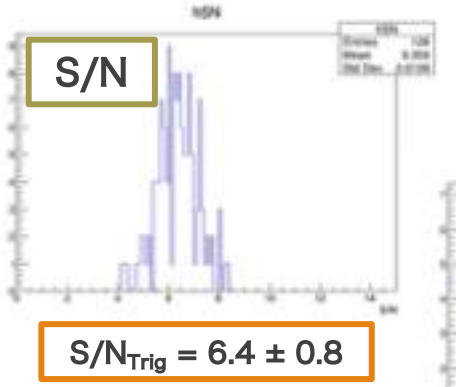
- Test pulse of {4.2, 8.4} fC is injected.
  - 4.2 fC: 1 MIP for 320 μm
- S-curve is fitted by Err-function.

$$f(x) = A \times Erfc(\frac{x-\mu}{\sqrt{2}\sigma}) + const.$$

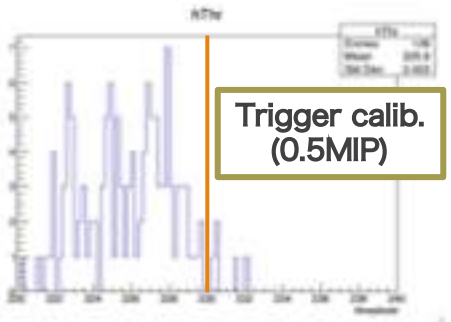
Injection [fC]	4.2	8.4
mean [DAC]	265.4	340.4
sigma [DAC]	12.0	12.5
S/N_{Trig}	6.4 ± 0.8	

- Trigger is set as 0.5 MIP of 320 μm slab: ~ 230 DAC.





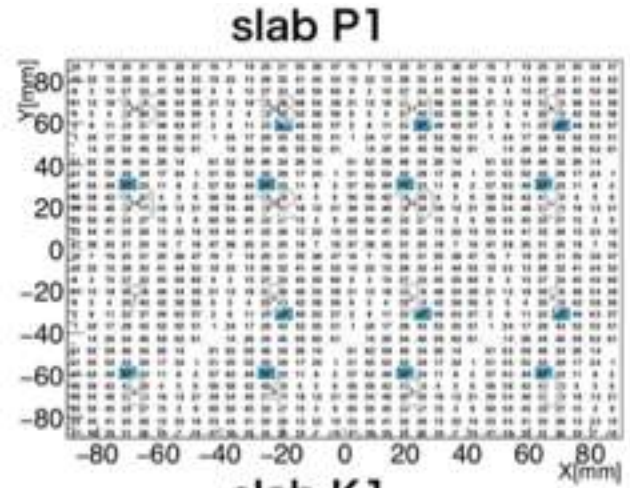
P1, all chips, ch 58-63

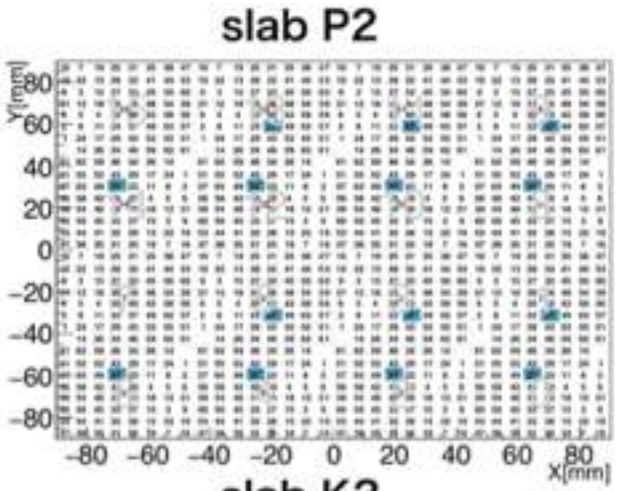


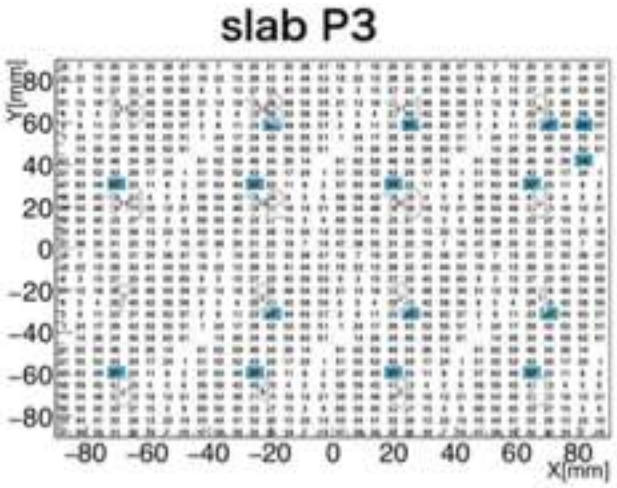
S/N_{Trig} is worse (previous: 11.6), under investigation.

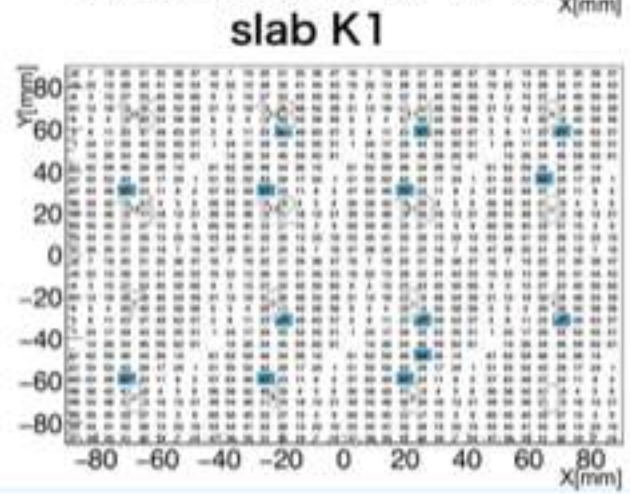
Masking of Noisy channels

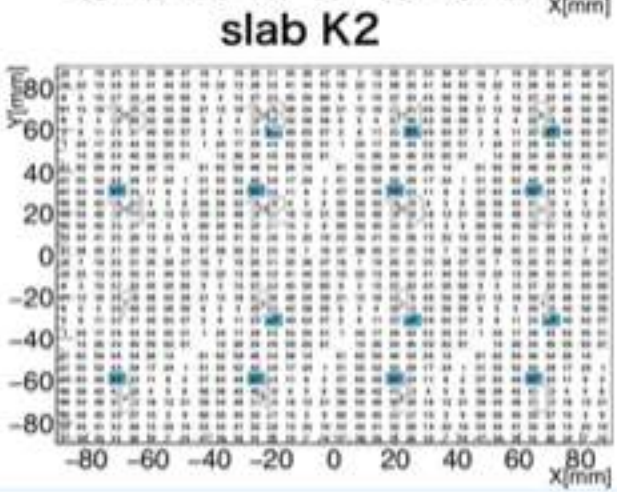
- A few channels are noisy after trigger adjustment and masked: 1 - 2 %.
- Individual threshold control was not used because it wasn‘t ready. → Next TB





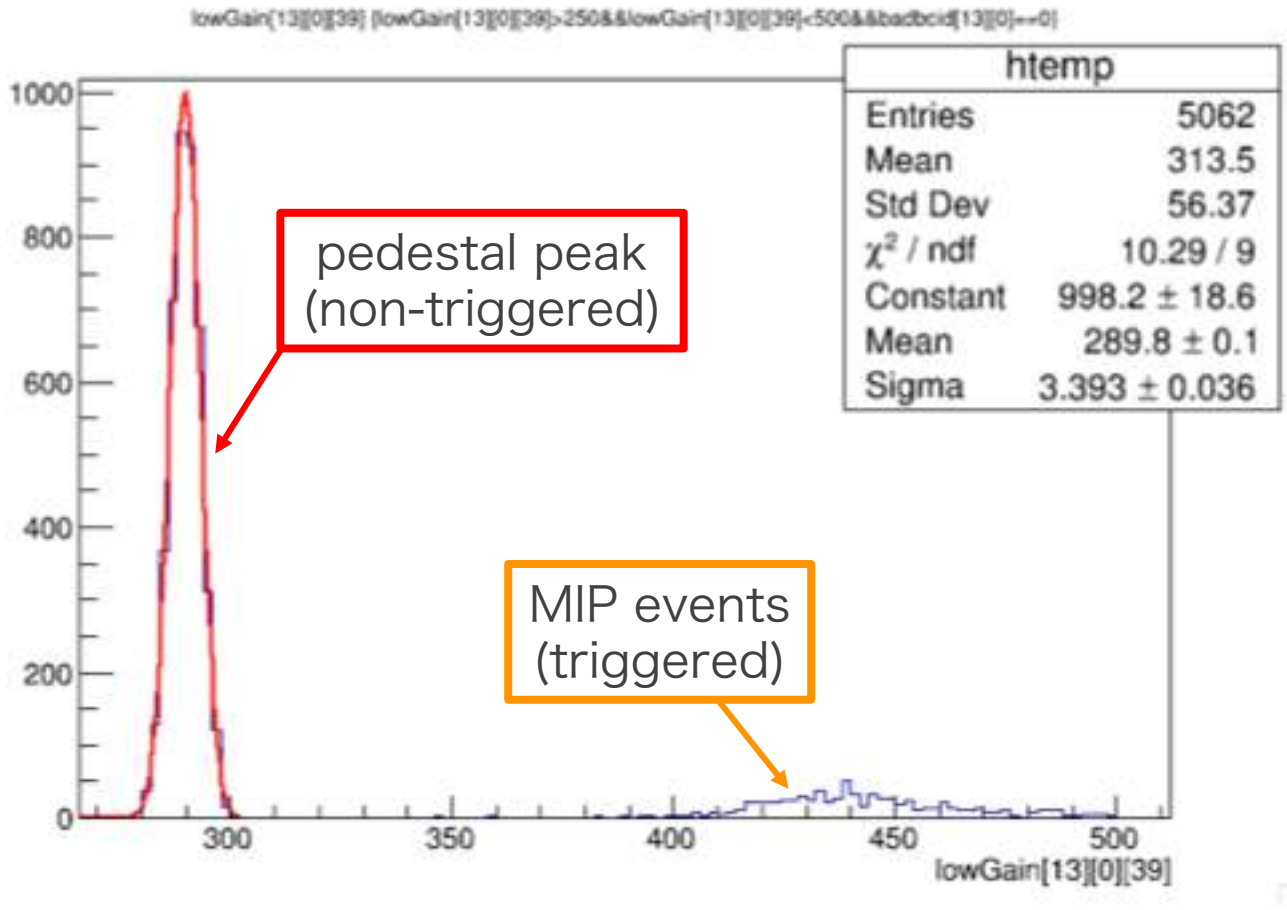






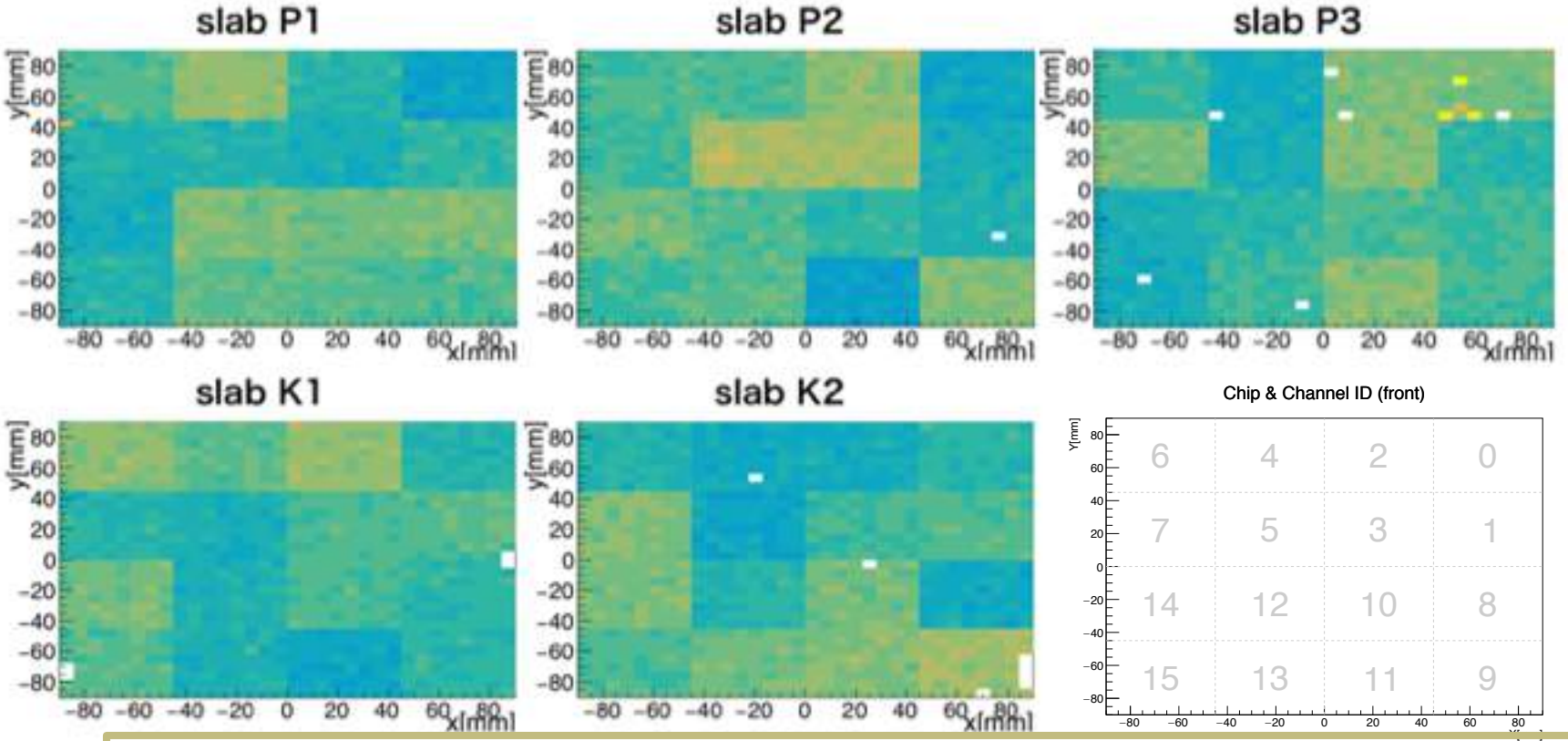
Pedestal Analysis

- Non-triggered ADC output (around ~300 [ADC])
- Fitted by Gaussian



Pedestal Uniformity: Mean

- Mean of Gaussian
- Result of 1st Memory (Memory-cell dependence is referred later.)

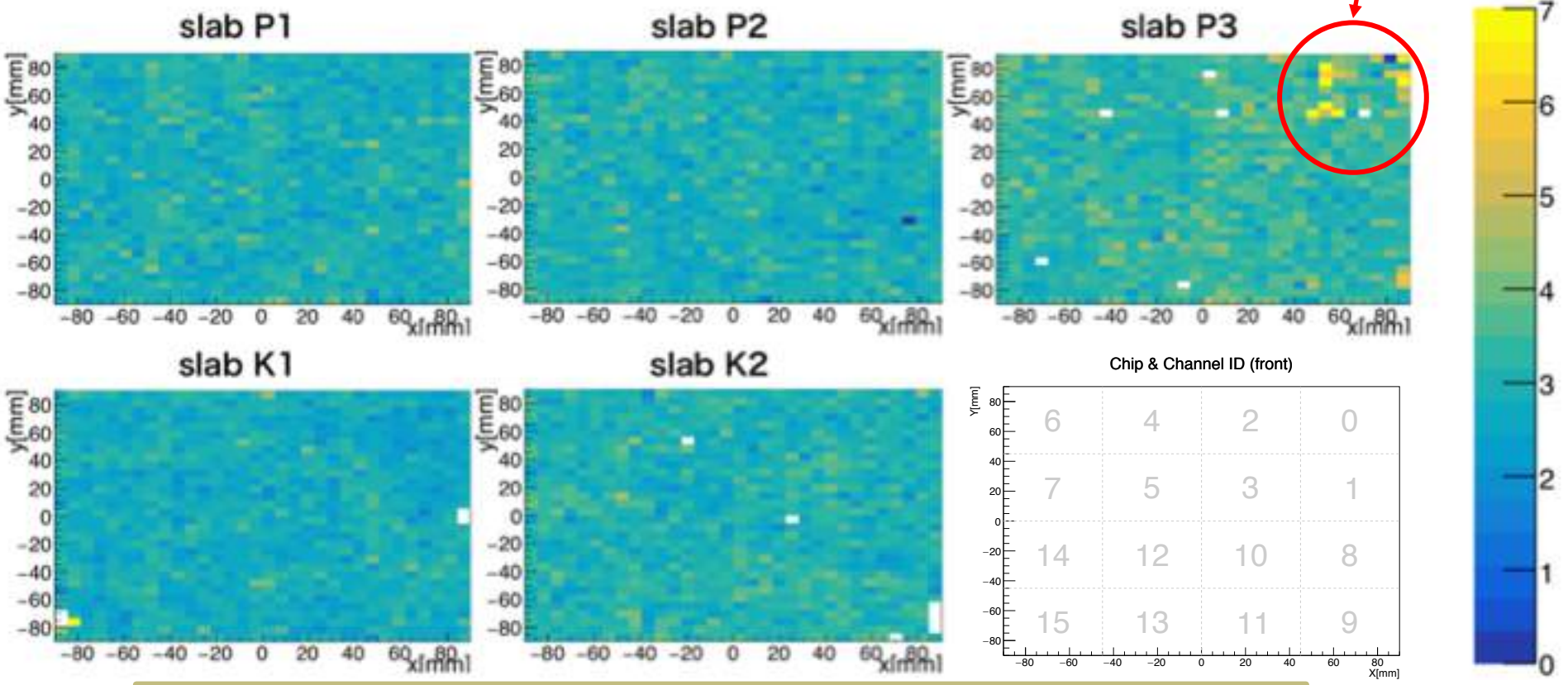


➢ Although there are differences between chips,
mean of pedestals looks generally uniform within the same chip.

Pedestal Uniformity: Width

- Sigma of Gaussian
- Result of 1st Memory (Memory-cell dependence is referred later.)

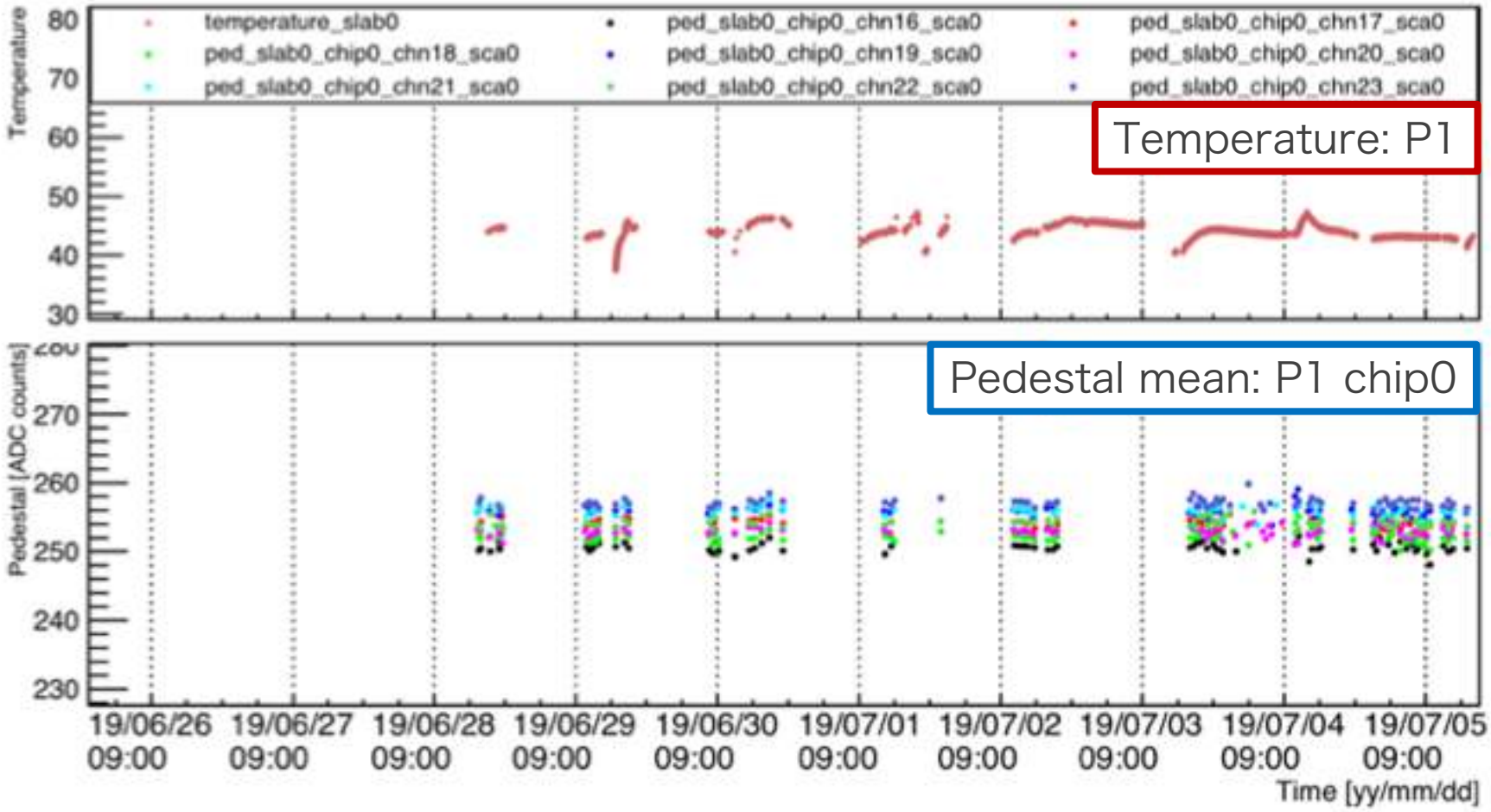
P3-chip0 looks strange.
This chip may be broken.



➢ Width of pedestal is almost uniform (3~4) throughout.

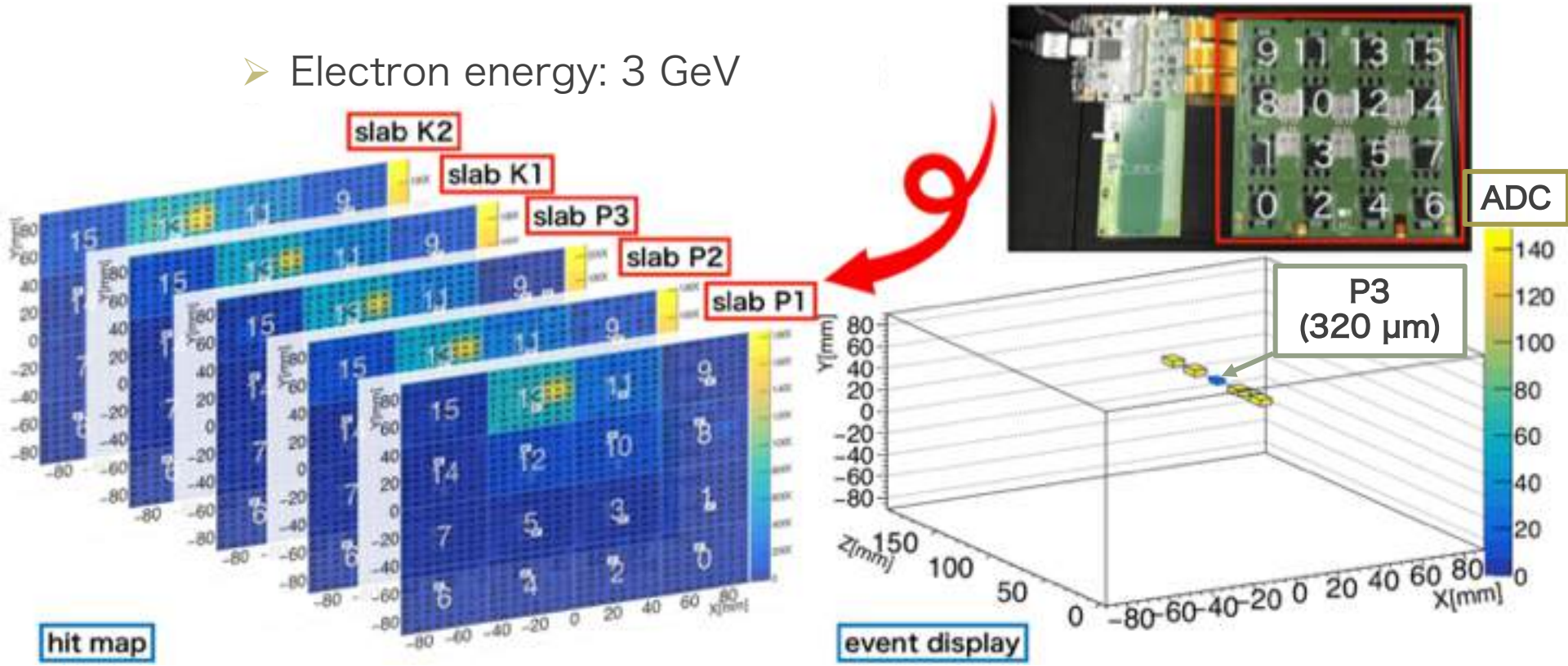
Pedestal Stability

- Pedestal stability is confirmed in this beam time.



MIP event

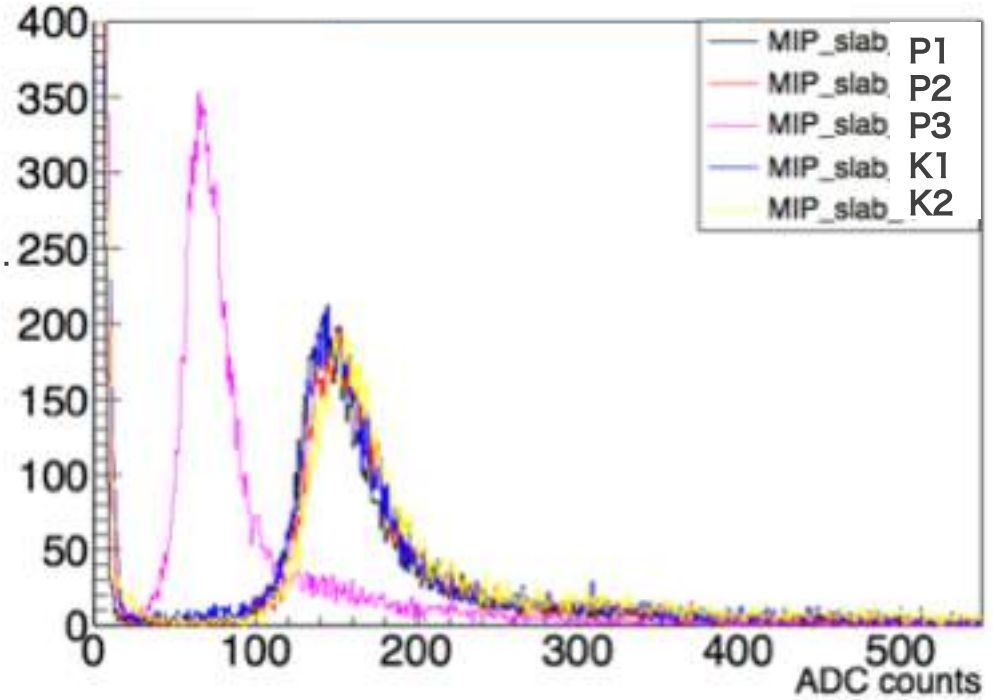
- MIP program is performed for mainly energy calibration of all the pixels.
- Hit map: Sum of the triggered events
- Event display: ADC output of single event after event building
  - Electron energy: 3 GeV



MIP spectrum

- Typical MIP spectrums of each slabs are shown.
- Pedestal is subtracted.
- Fitted by Lan-Gaus function.
  - Convolution of Landau × Gaussian
- MPV: Most Probable Value
- Definition of S/N_{ADC}:

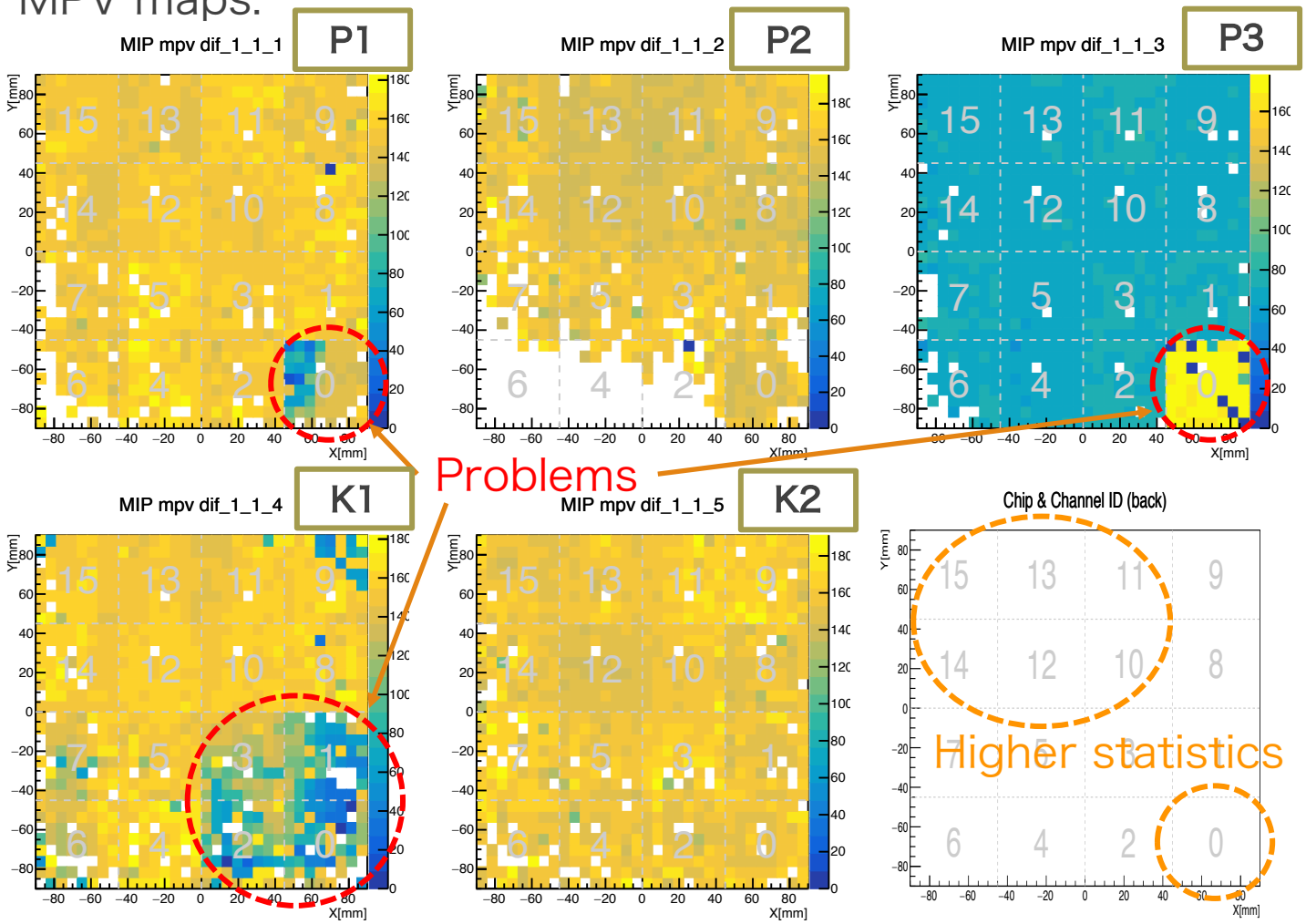
$$S/N_{ADC} \equiv \frac{MPV_{1\mathrm{MIP}}}{Width_{pedestal}}$$



slab	P1	P2	P3	K1	K2
thickness	650μm	650μm	320μm	650μm	650μm
MPV	146.5	144.9	71.3	141.4	146.1
Ped_width	3.0	3.0	3.3	2.8	3.1
S/N	49.0	48.9	21.7	50.2	47.5

MIP calibration: Summary

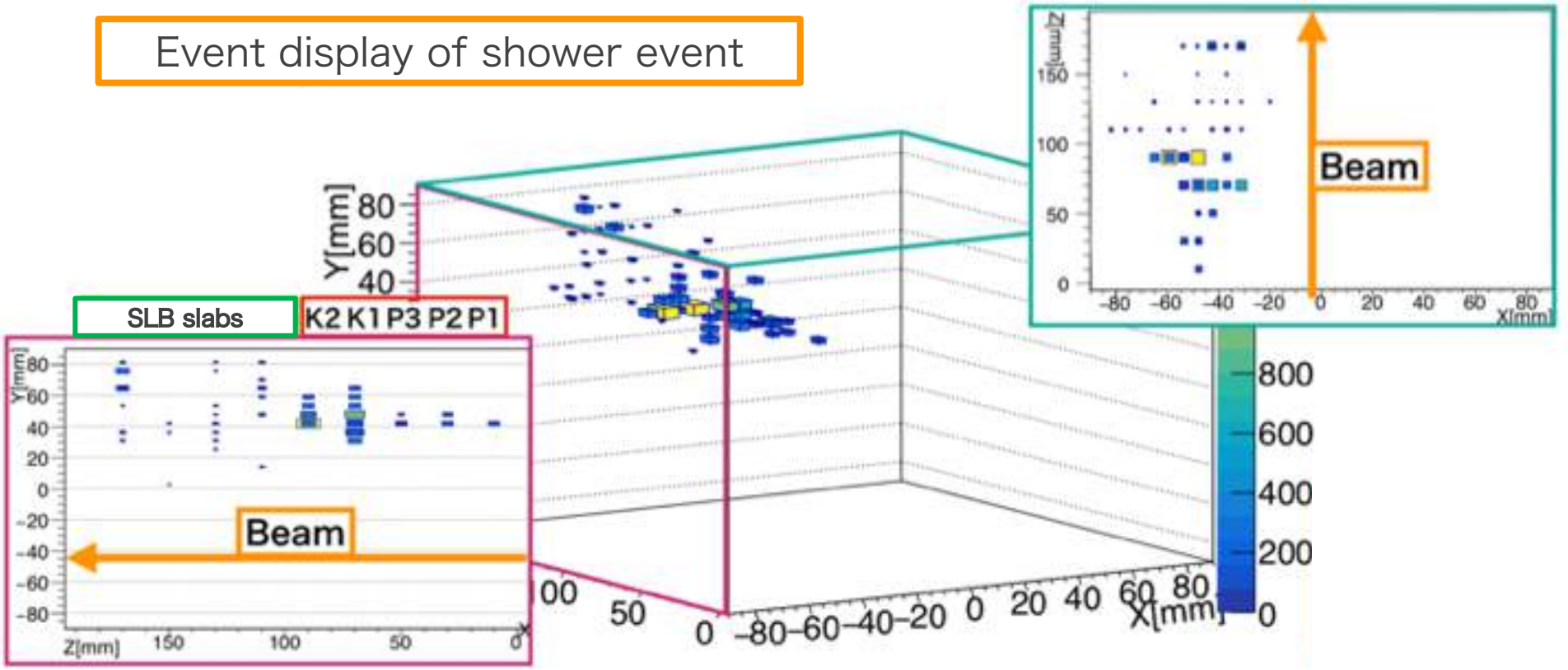
- MPV maps:



Shower event

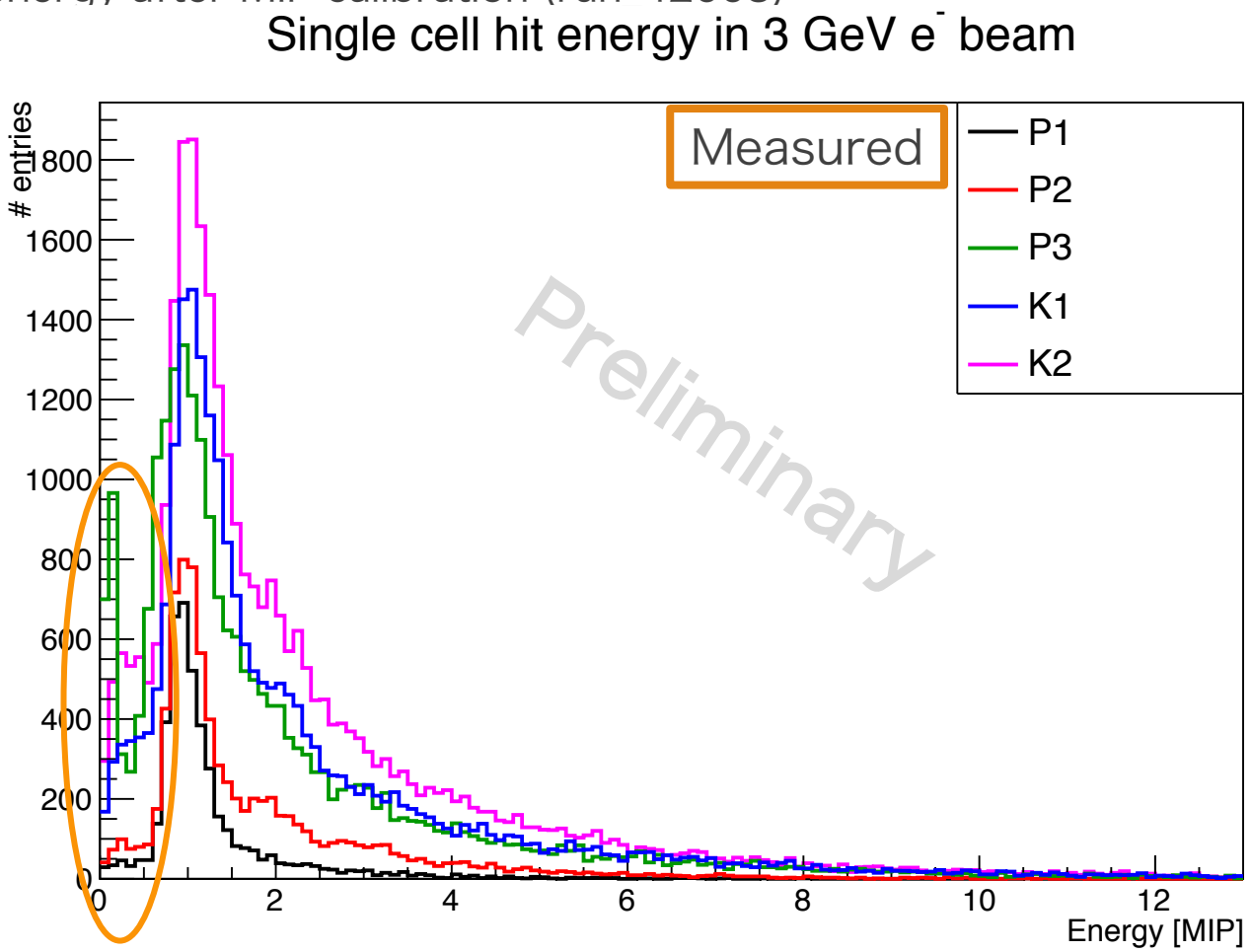
- Using the preceding results, we can finally build events.
  - BCID offsets between SLB-based and DIF-based are corrected.
- A typical event is checked with event display.
  - In this picture, color scale is not converted to energy, still ADC output.

Event display of shower event



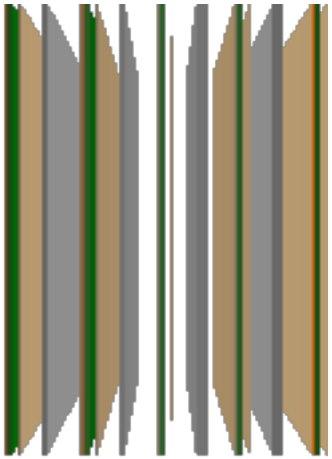
Shower Analysis: Hit Energy

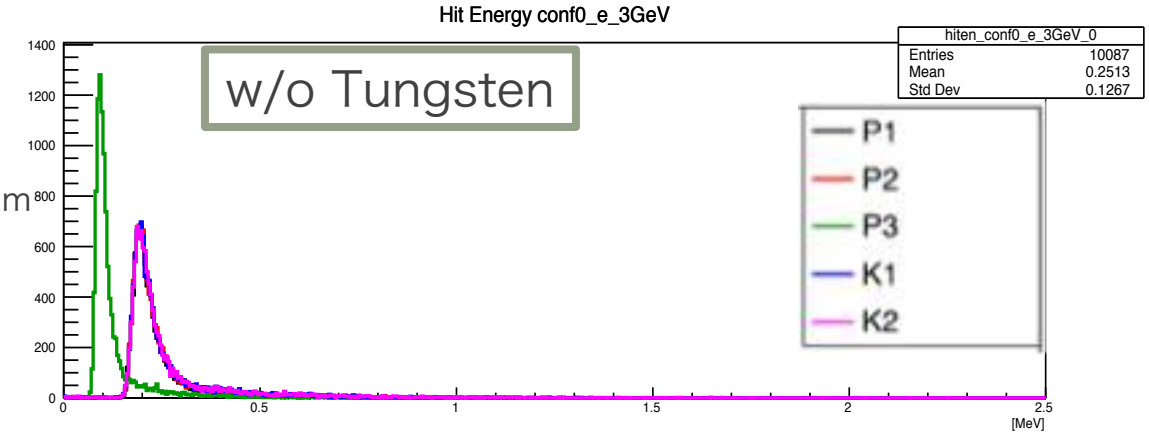
- Hit energy after MIP calibration (run 42003)

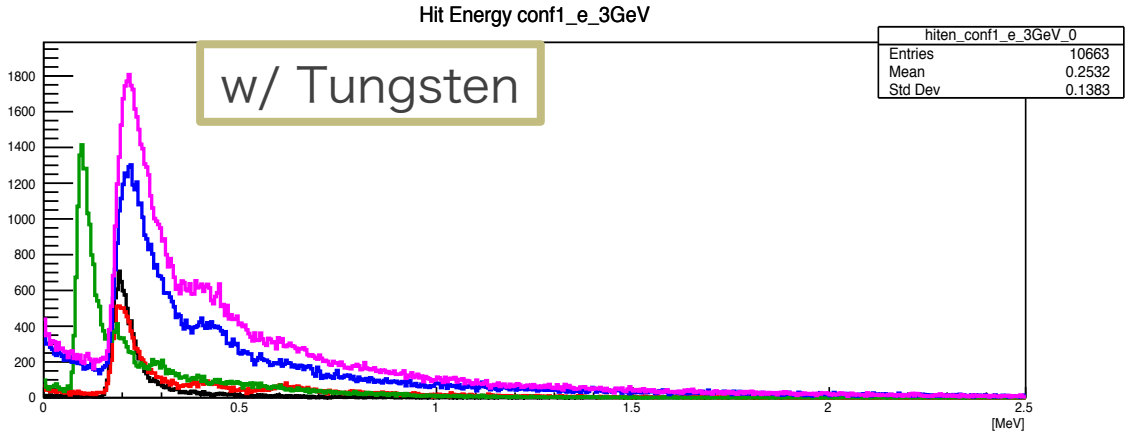


Simulation

- We performed detector simulation for this beam test.
- Simulator: DDSim in iLCSoft
- Structure of FEV13-Jp:
  - CF: 0.6mm
  - Electronics(Air)
  - PCB: K1: 1.6mm, others: 1.8mm
  - Glue(Air): 0.08mm
  - Si: 0.32mm or 0.65mm
  - Glue(Air): 0.08mm
  - Kapton(Cu): 0.06mm
  - CF: 0.6mm
  - Plastic(polyethylene): 5mm

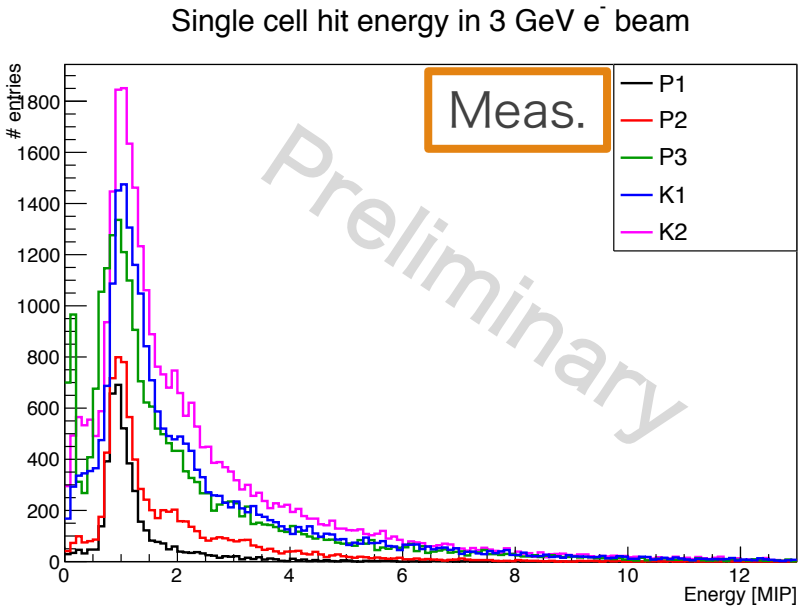


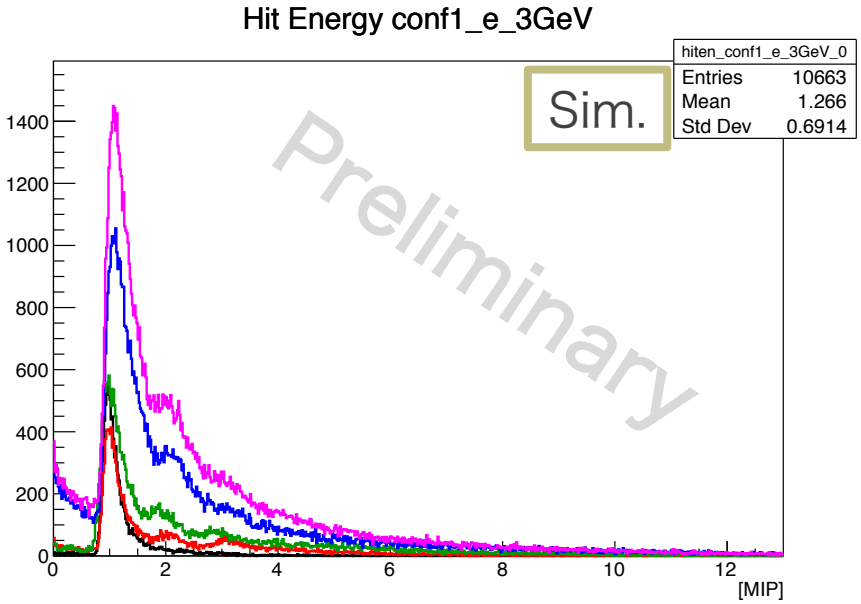




Comparison of Measured and Simulated.

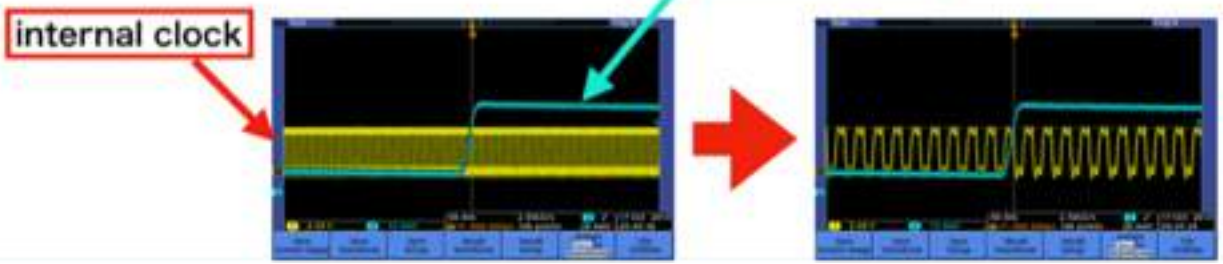
- Simulated results are converted to MIP units and compared to measured ones.
- Work in progress.

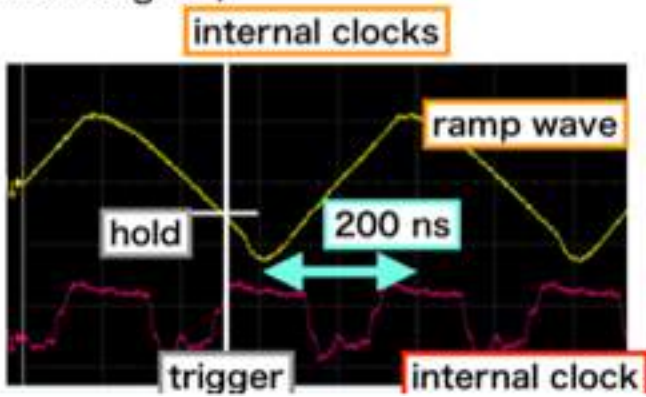




TDC Analysis

- TDC mode operation test
- SKIROC2/2A has the ramp wave as one of the internal clocks
  - I measured this ramp waveform for calculating from TDC to real time factor
- The ramp wave can be measured with
  - synchronization of internal and external clock (injection signal)
  - change the phase of injection signal

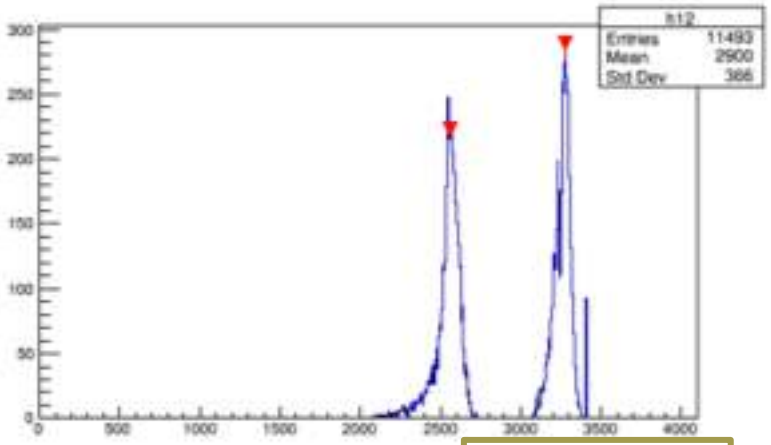




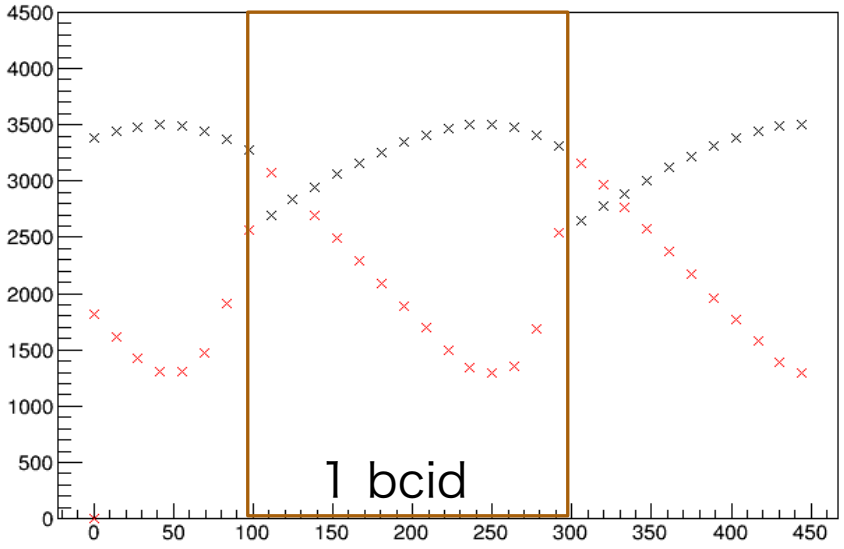
TDC Calibration

- peak search version
  - bcid is not used
- saturation
- phase should be shifted

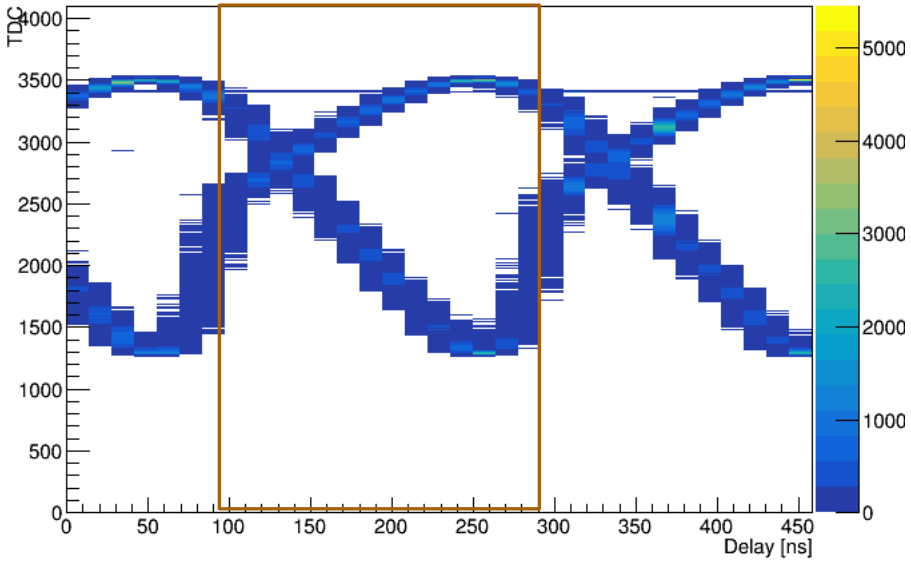
- TDC to real time calibration factors
  - 0.127 ns / TDC count (up)
  - 0.066 ns / TDC count (down)



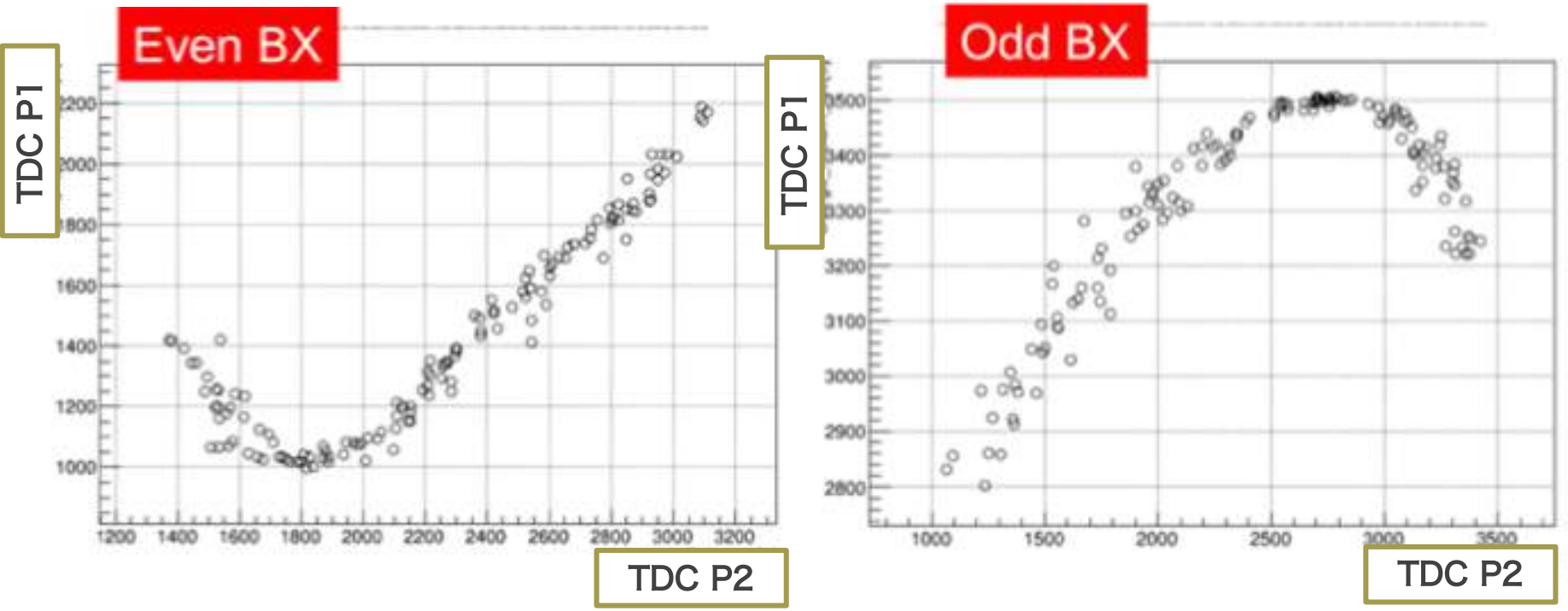
TDC output



test_191021_1_tdc_P1_ch13_3Hz_200kHz, chip12



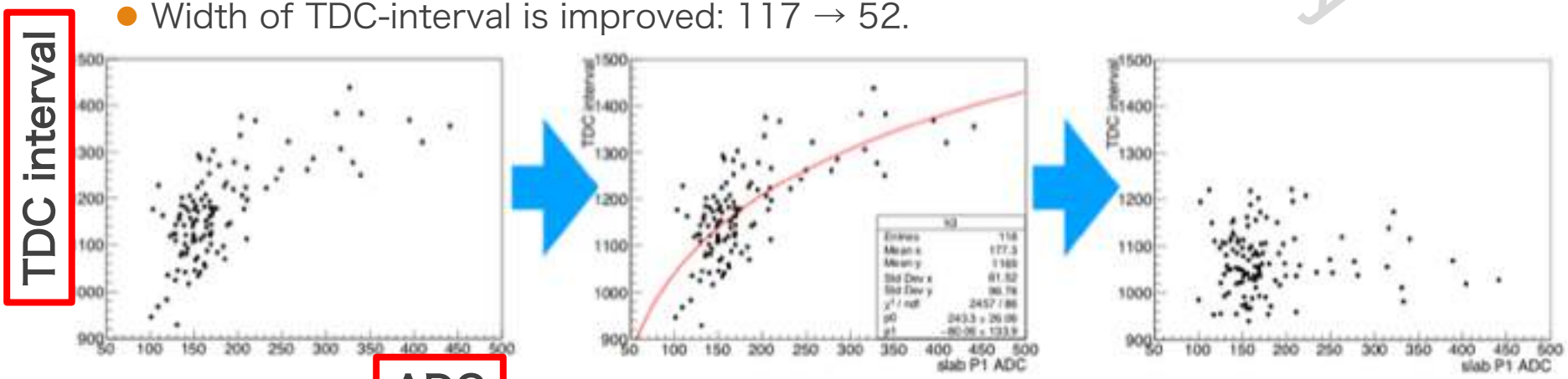
TDC Correlation with MIP

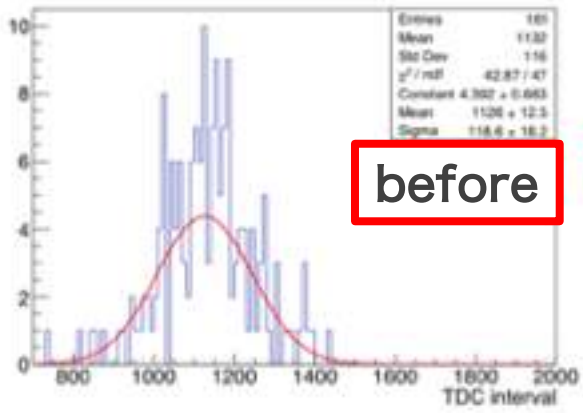


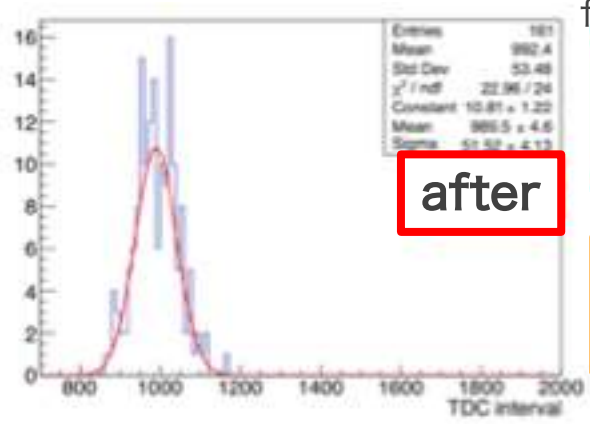
- Correlation of TDC between slab P1 and P2
- Select 1 ch (at the center of the beam), 450 < ADC < 500 (to avoid time-walk)
- ~10 / 1 ns at the normal slope: timing resolution ~ a few ns?
- TDC calibration in progress.

Correction of Time Walk

- Time Walk: TDC dependence on ADC
- TDC-interval vs ADC are fitted by Log function.
- Width of TDC-interval is improved: 117 → 52.







from previous talk,

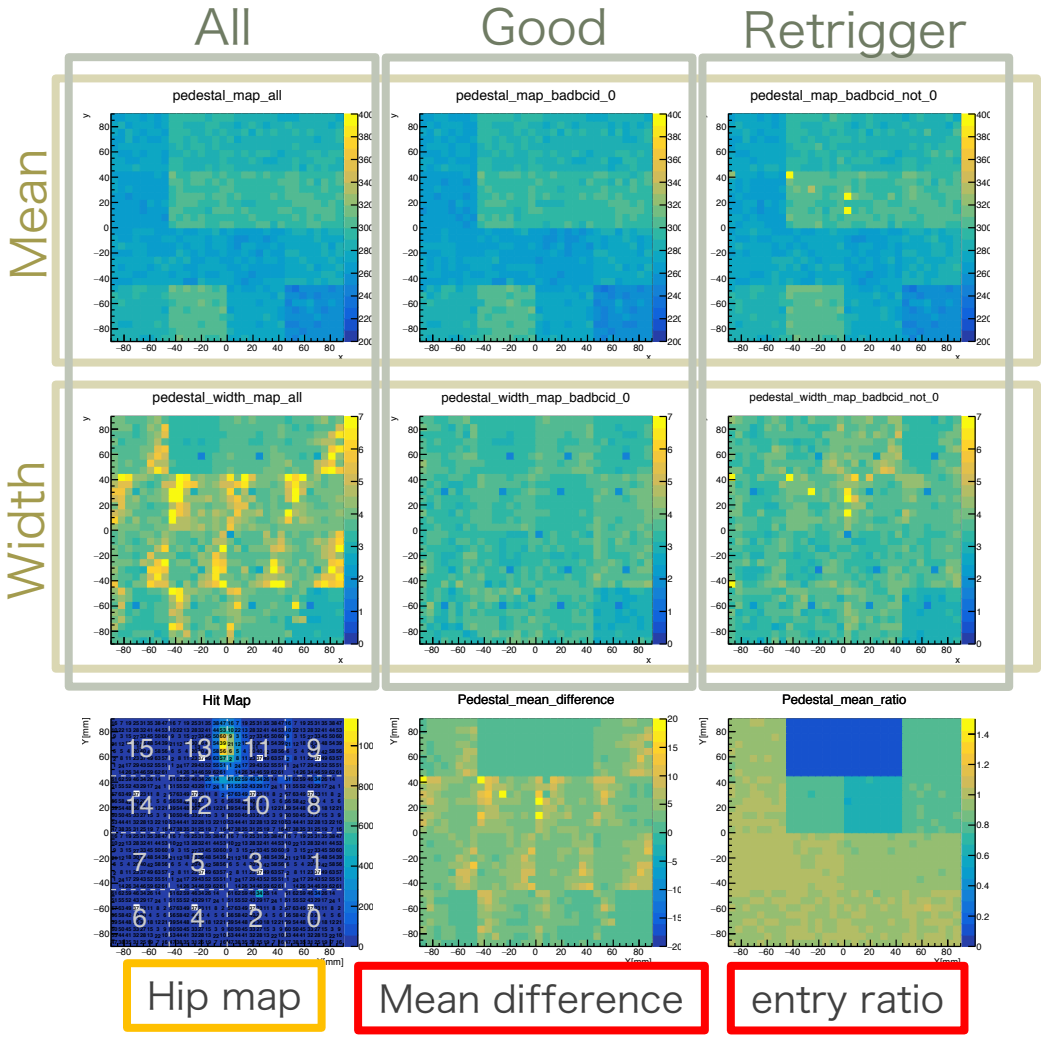
- TDC to real time calibration factors
  - 0.127 ns / TDC count (up)
  - 0.066 ns / TDC count (down)

timing resolution: 5.2 ± 1.6 ns

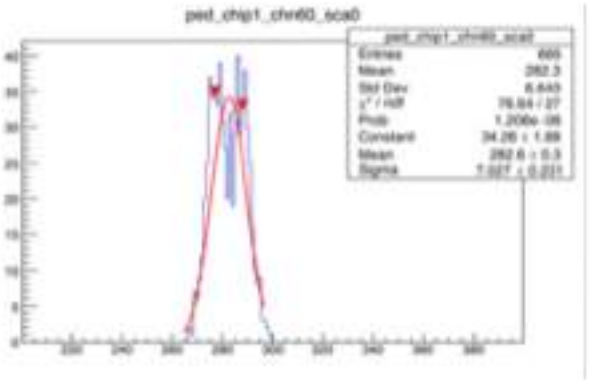
Remaining Issues

Double pedestal / Retrigger

- run 32015, slab P1



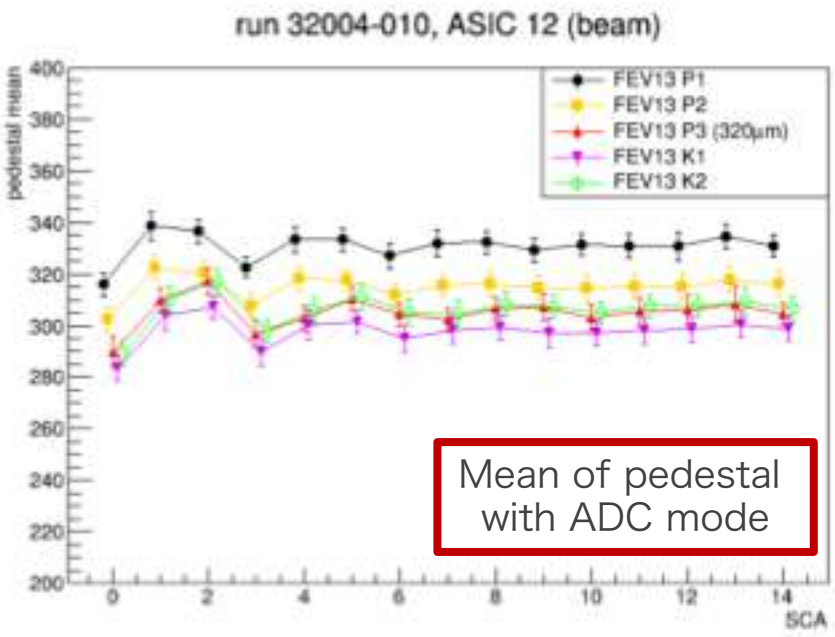
Retrigger event:
BCID is consecutive.

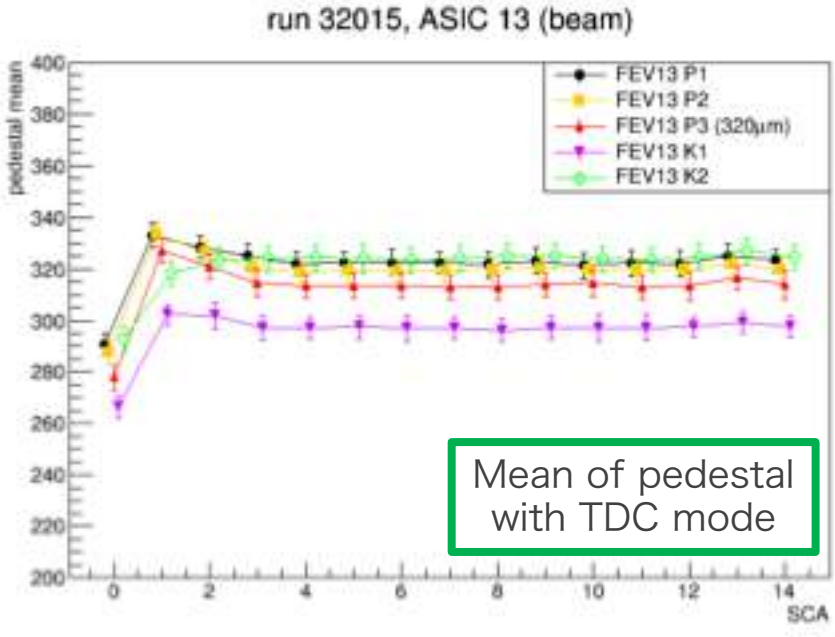


Double pedestal
by retrigger

Pedestal difference between ADC/TDC mode

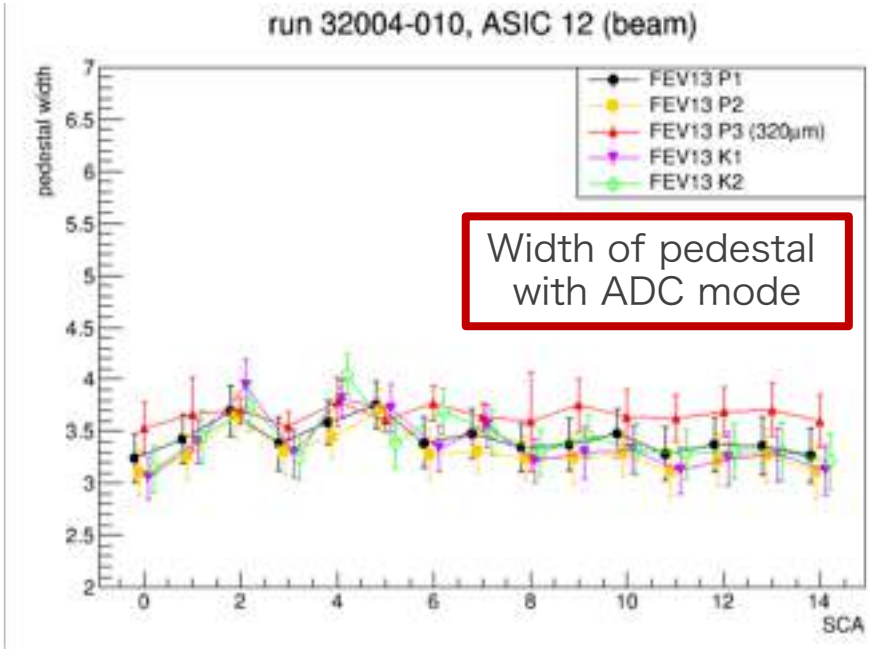
- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In the first memory cell, the difference of typical Ped_mean is ~15.

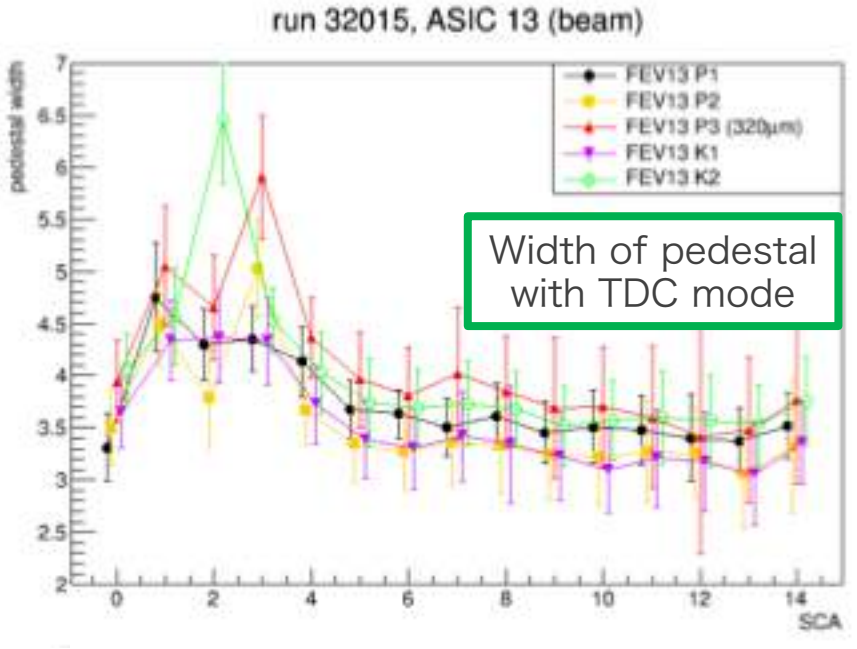




Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In TDC mode, SCA~2 is worse.





Pedestal difference between ADC/TDC mode

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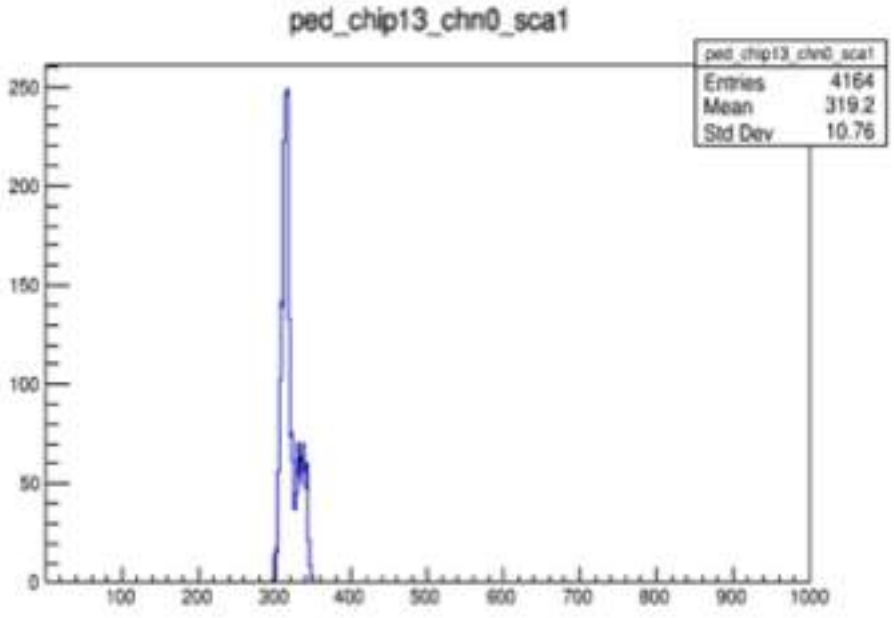
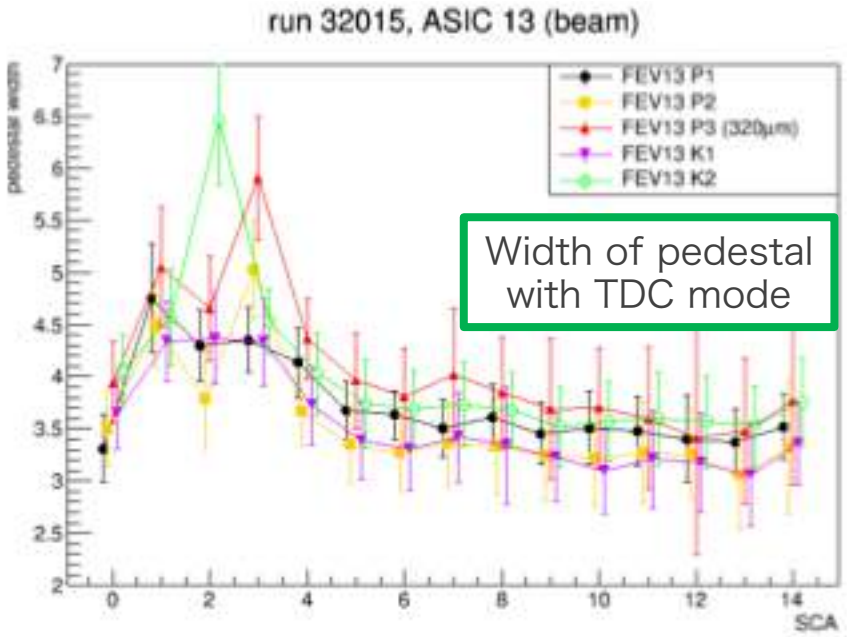




- There are double pedestal even after bcid selection in TDC mode.
- The criteria for identification of double pedestal is not optimized.

Work in progress.

Summary

- FEV13-Jp: 5 slabs from Kyushu U.
- BT 2019 DESY: **All the slabs worked consistently.**
- Pedestal study
  - Uniformity and Stability is verified.
- MIP calibration
  - MIP calibration is almost completed.
  - S/N is obtained for 5 slabs:

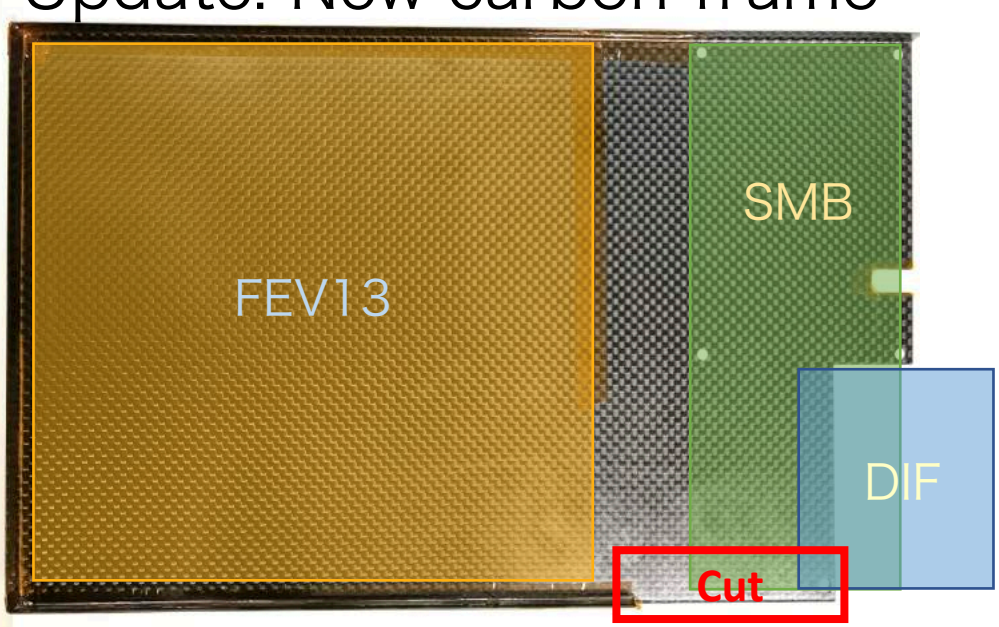
slab	P1	P2	P3	K1	K2
thickness	650μm	650μm	320μm	650μm	650μm
S/N_{ADC}	49.0	48.9	21.7	50.2	47.5

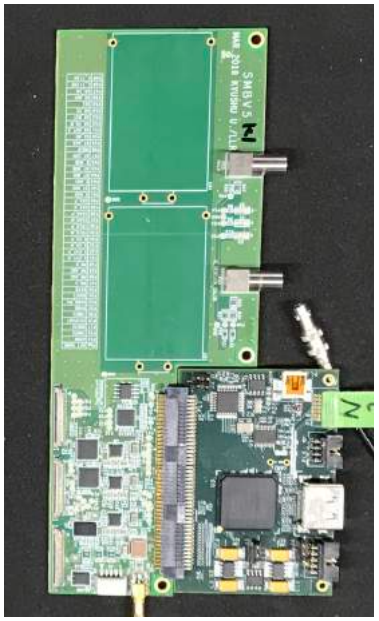
- Shower analysis
  - Event building has done and shower event is seen in event display.
  - We take a look at hit energy which is consistent with simulation result.
  - Work in progress.
- TDC test
  - Time walk is corrected, but very preliminary.
  - Timing resolution is obtained, however we need more detail study using injection.
- Several issues remain:
  - Retriggered events are removed practically although the cause is still unknown.
  - In TDC mode, pedestals become worse because of retriggers.

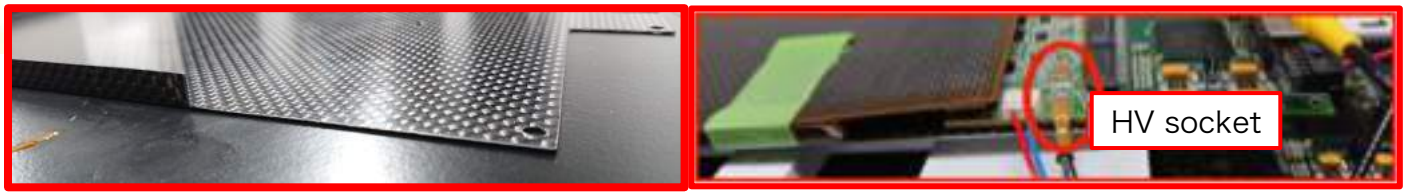
backup

Hardware update

- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.
- Update: New carbon frame

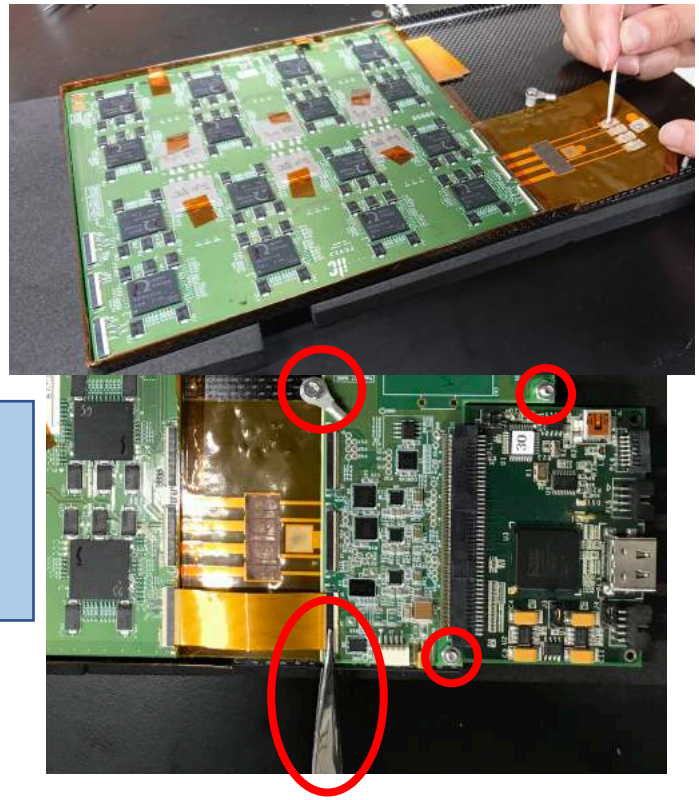






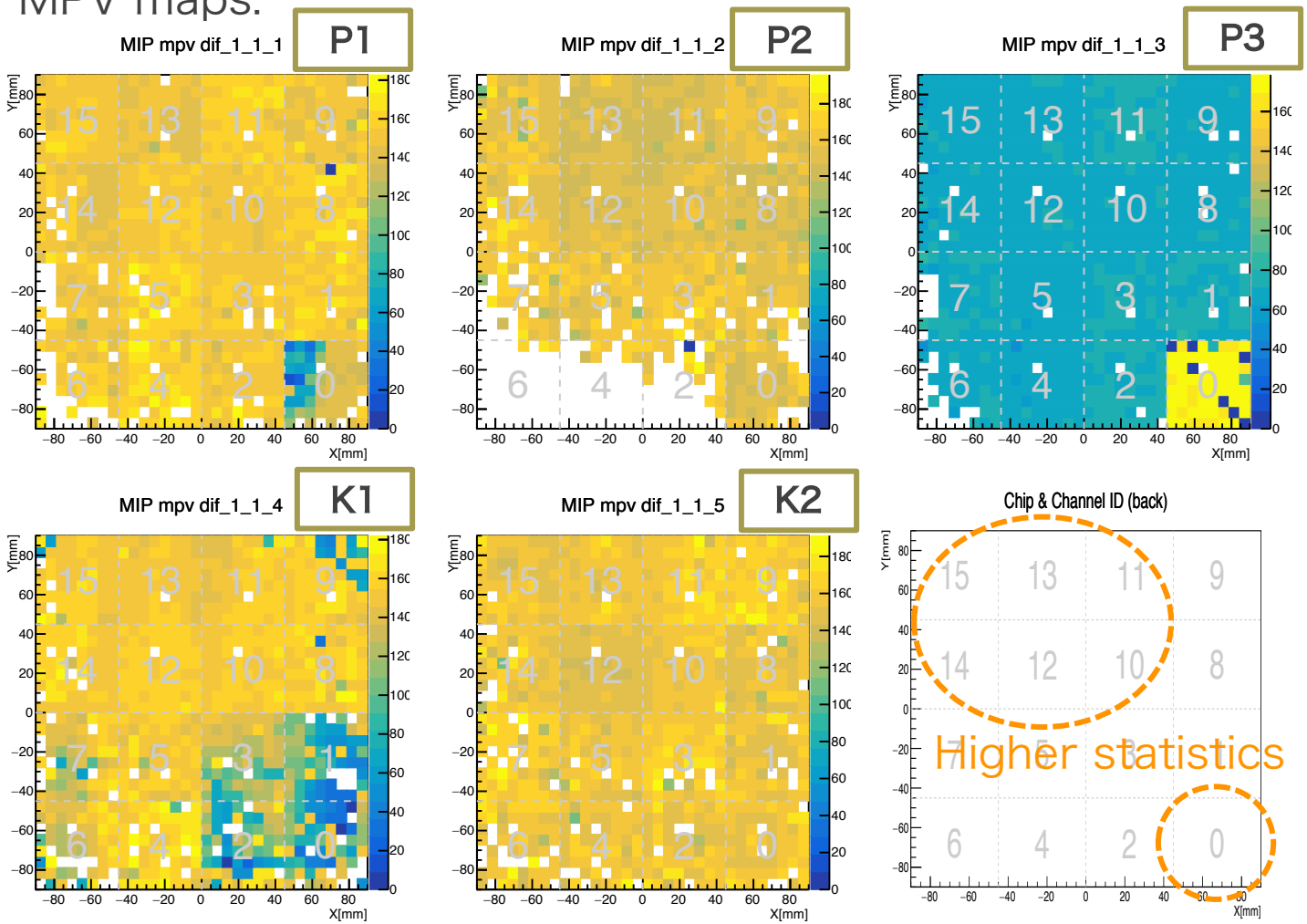
Hardware update

- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.
- Update: Conductive adhesion



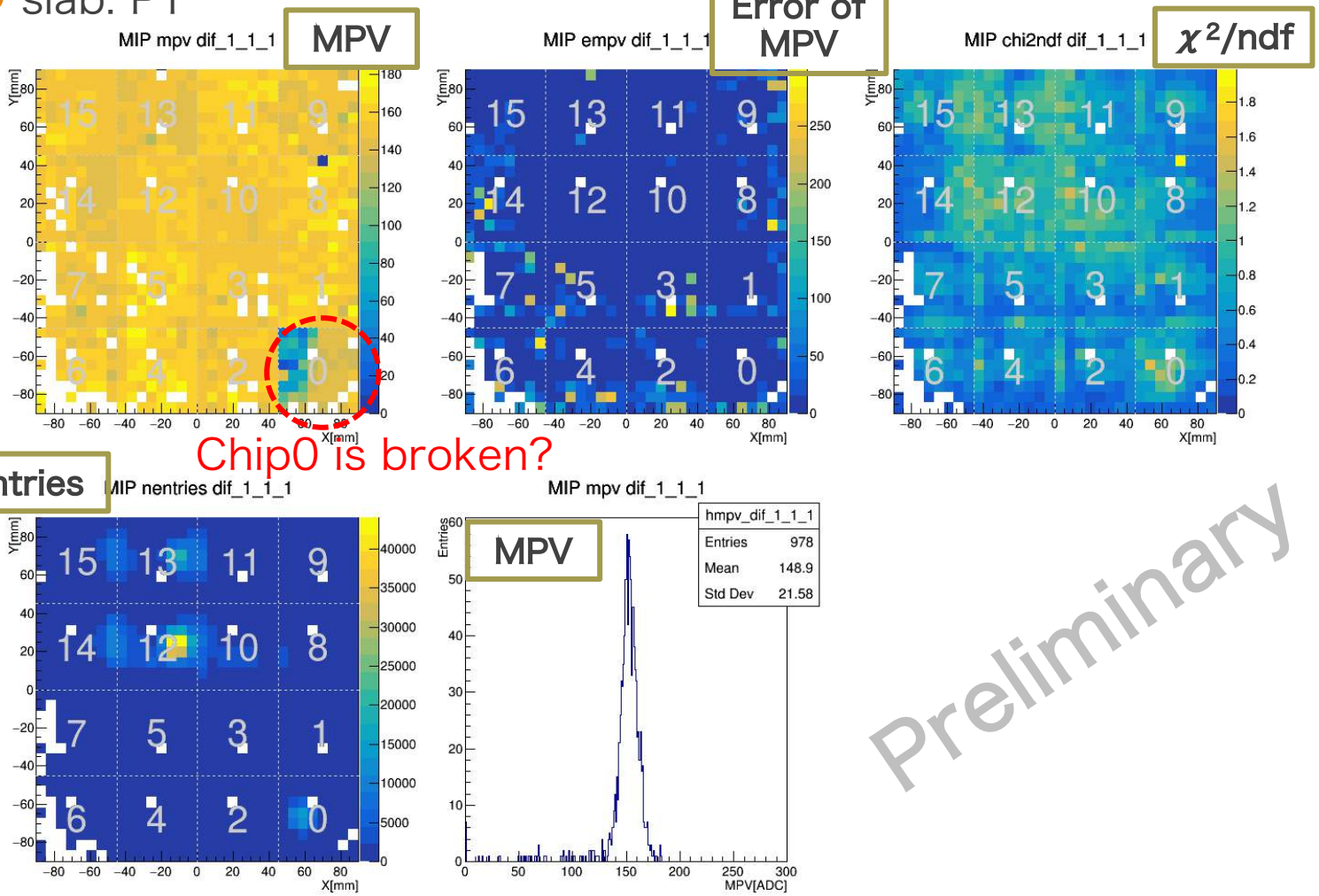
MIP calibration

- MPV maps:



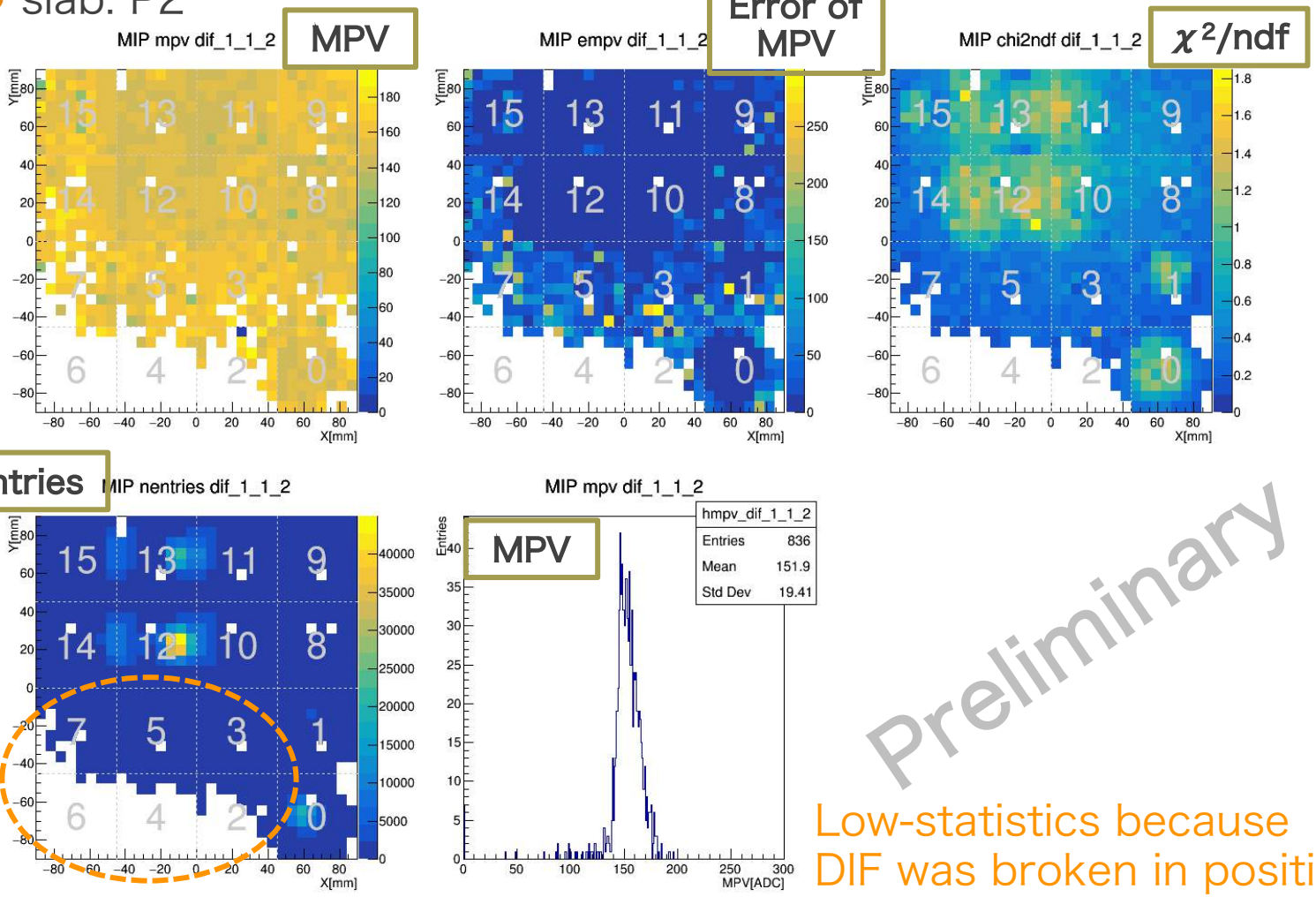
MIP calibration

- slab: P1



MIP calibration

- slab: P2

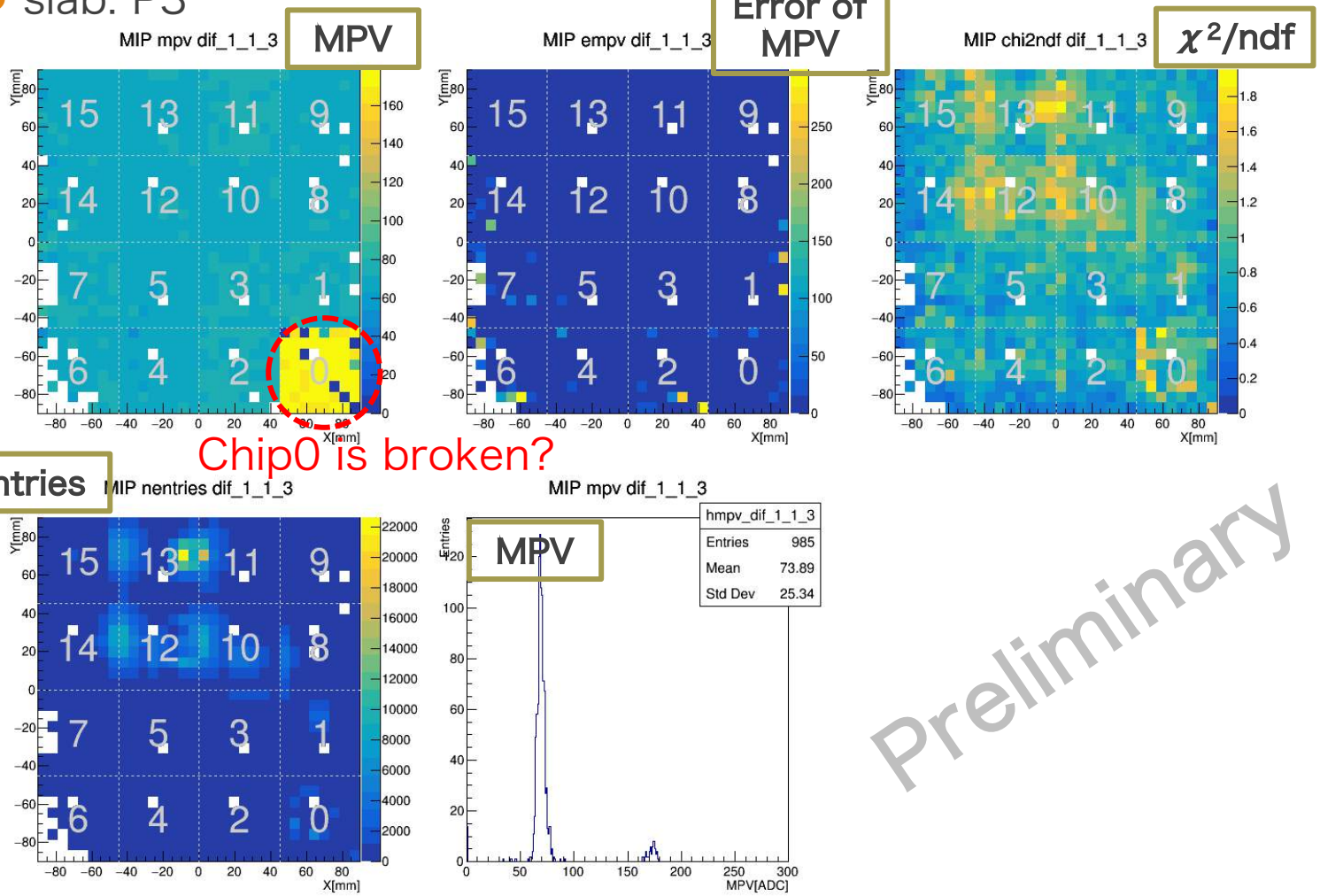


Preliminary

Low-statistics because
DIF was broken in position scan

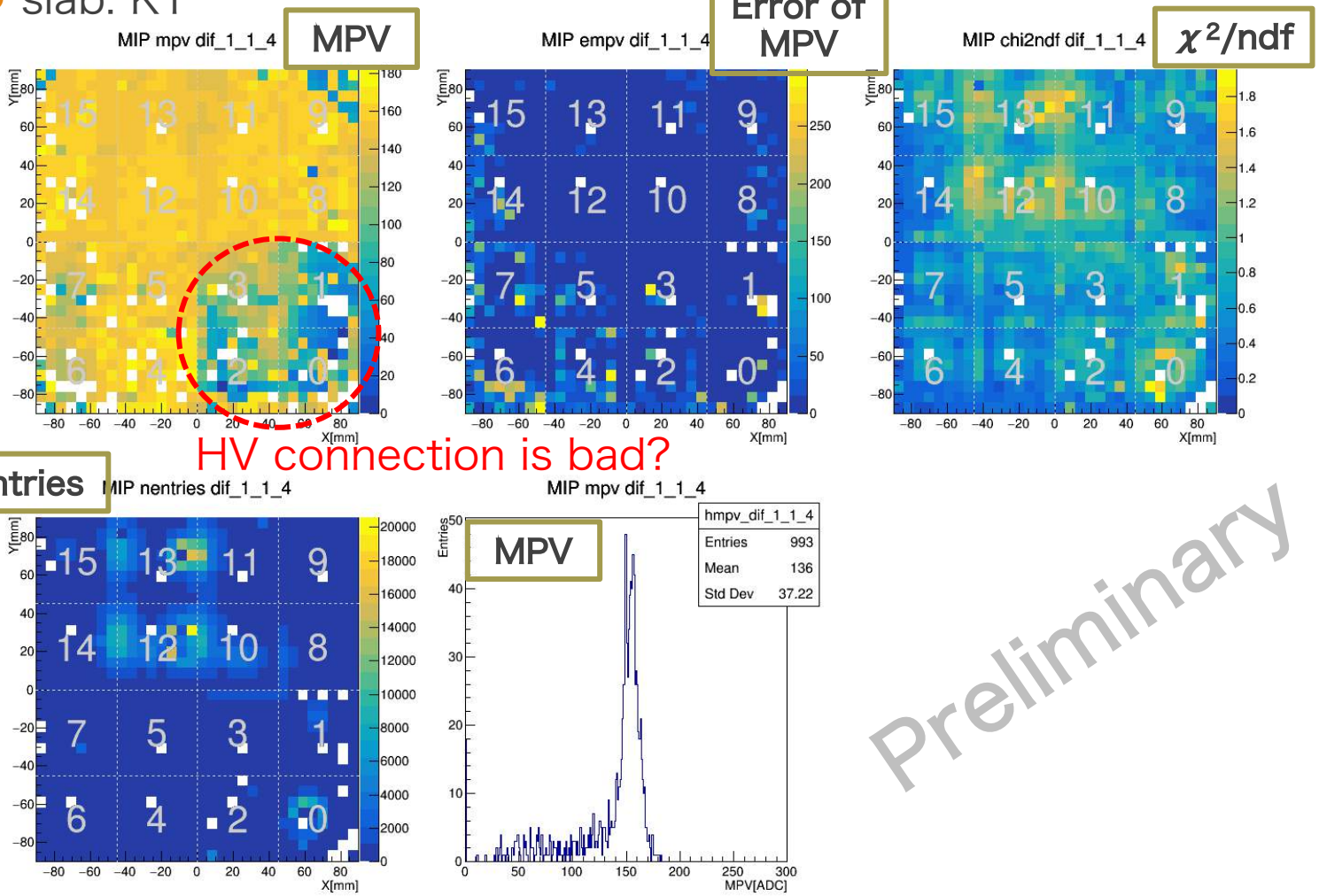
MIP calibration

- slab: P3



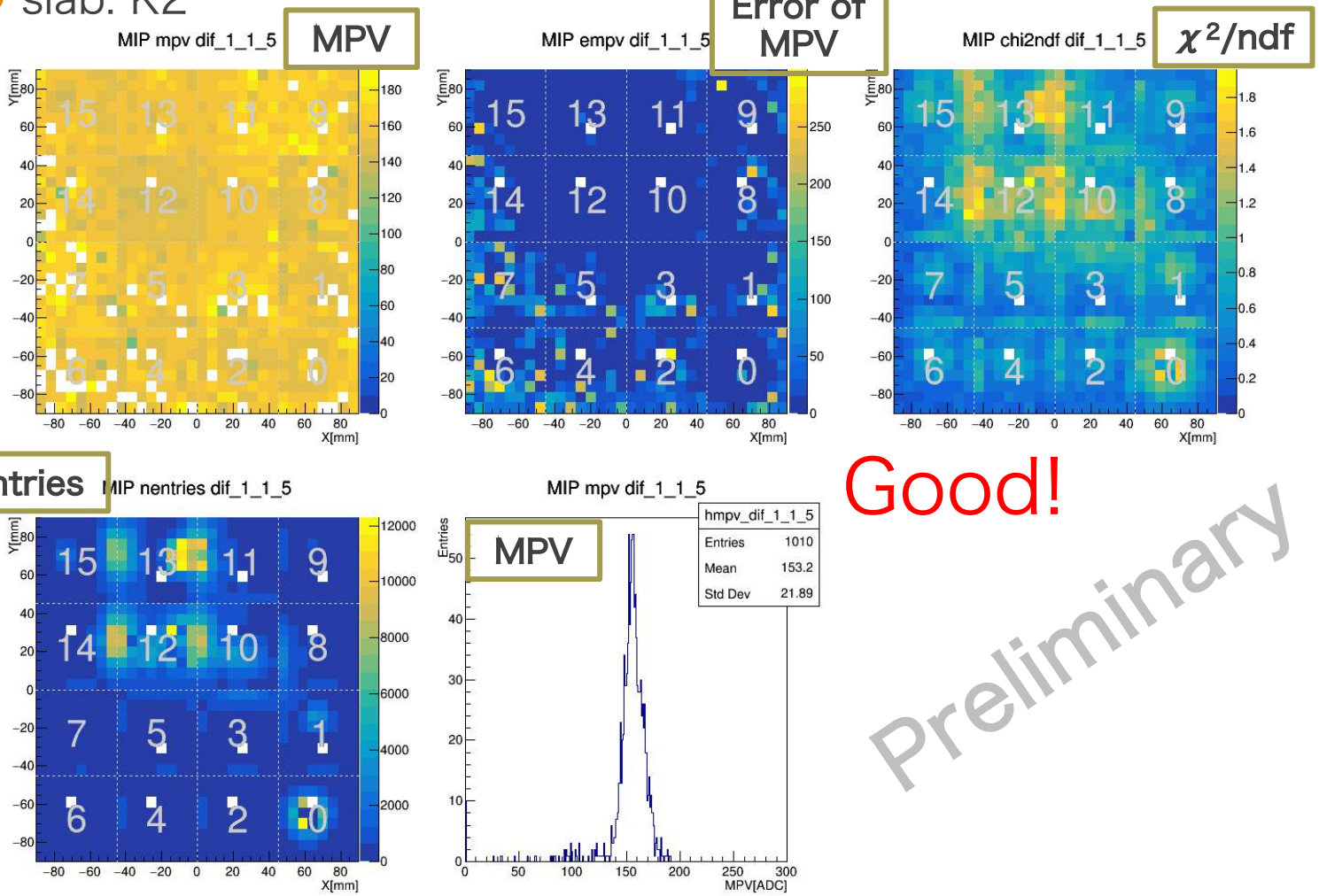
MIP calibration

- slab: K1



MIP calibration

- slab: K2

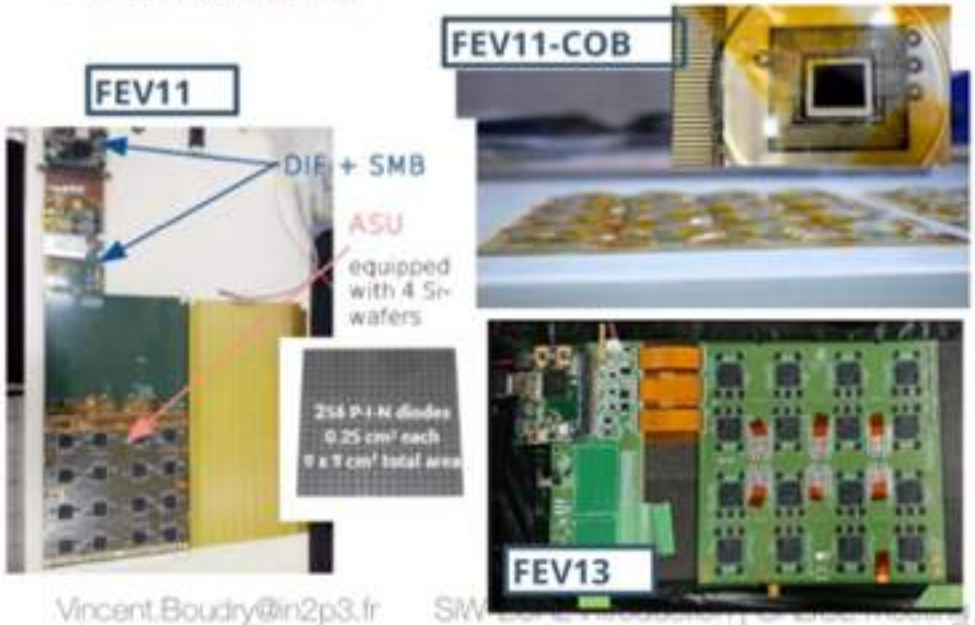


R&D of SiW-ECAL technological prototypes

ASU: 12 years of R&D

Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints



Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	7 units	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 (12)$_{\text{Trig}}$ 6–8 % masked
1st technological ECAL	2018	SLABvFEV11 & FEV13 SK2a+ Compact stack	SK2 & SK2a (>timing)	Improved S/N Timing...

R&D of SiW-ECAL technological prototypes

Beam-test 2015-2018

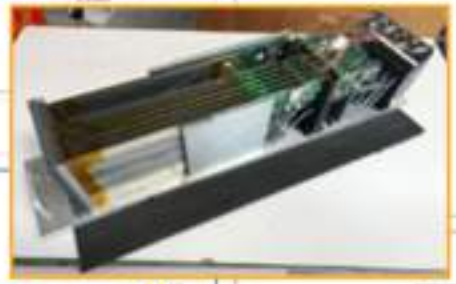
CERN 2015

"Naked FEV11"

S/N_{ADC} = 16–17

$(MIP - ped) / \sigma_{ped}$

Defaults cataract :
- Negative signals
- re-triggers
- ~ high thr.
- sq events / 10



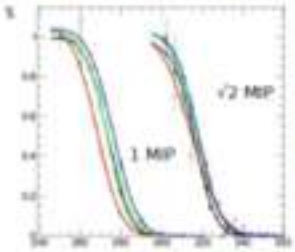
DESY 2018

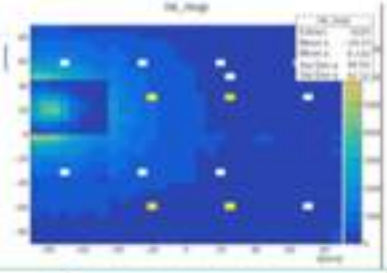
7 FEV11 + 1 FEV13(650µm)

S/N_{trig} ~ 11.6±0.7

Trigger → ~1/3 mip (est.)

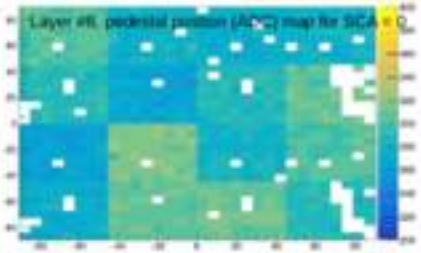
First comm. of FEV13





DESY 2017

7 FEV11



S/N_{ADC} = 20.3,

$\sigma_{S/N}$ = 1.5 (7.4 %)

masked ch. ~ 8 %

Hit eff. ~ 99.95 %

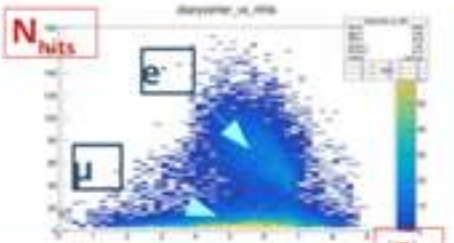
0°, 45° ✔

1T operation ✔

CERN 2018

Masked ch (FEV11) ~ 4 %

6 FEV11 + 1(4) FEV13(320 & 650µm) + 24X_0 W



Vinc… ECAL introduction | CALICE meeting | Utrecht uni, 10/04/2019

Taikan

11/35