R&D Projects of LCTPC
In the next 2 years

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for LCTPC

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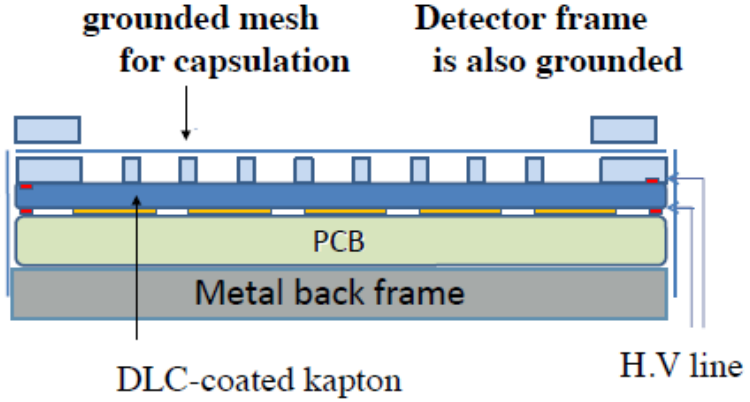
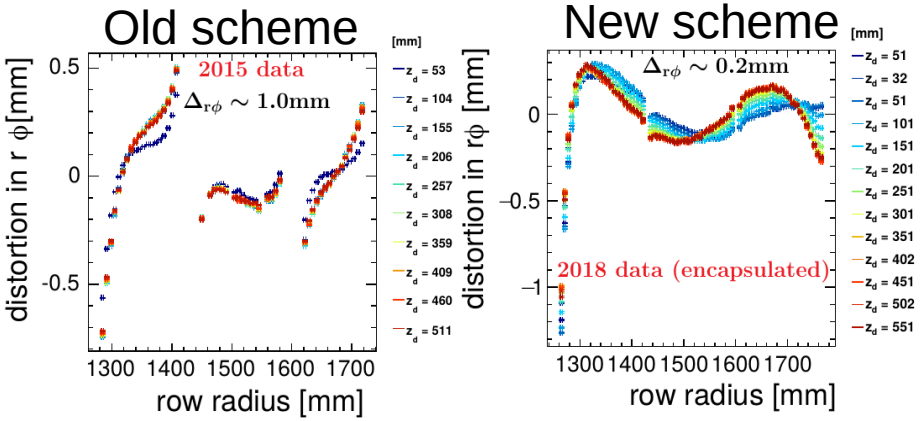
Optimization of Modules

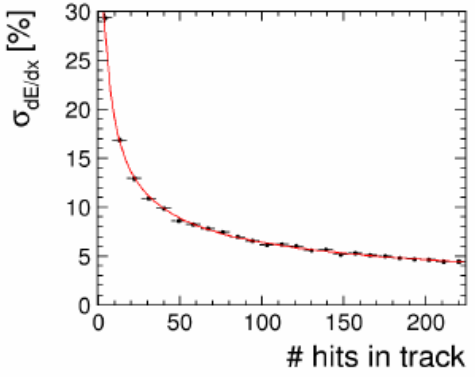
Recent progress was presented in several talks at the LCWS. Here, only 2 examples should be given:

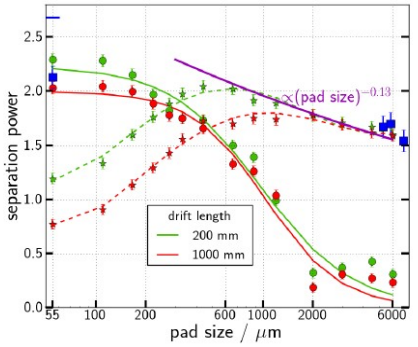
1.) Micromegas: New HV scheme of the module places grid on ground potential and reduces field distortions significantly





2.) GEM modules: dE/dx performance is scrutinized. Also, in dependence on the pad sizes.





Detector Modules

GEM and Micromegas groups have finished analysis of test beam data with previous set of detector modules. Both groups want to implement improvements in a new generation of modules. They are discussing new common modules with

- a more final design and
- a more comparable design.

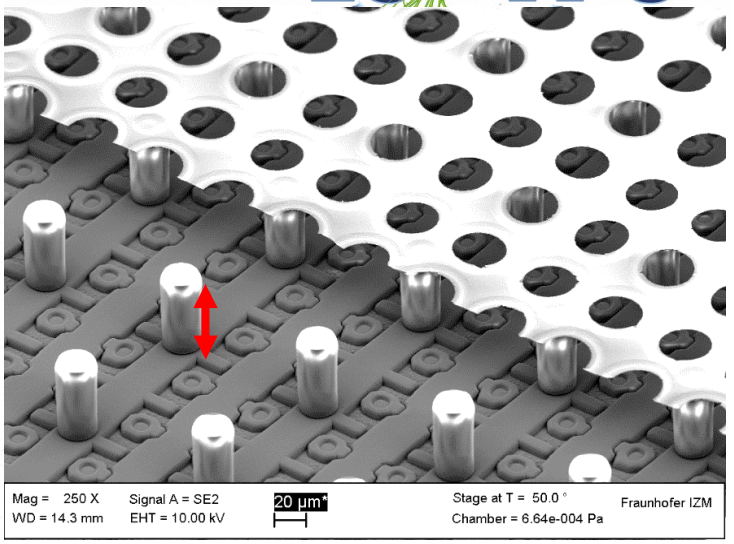
These common modules should have a

- common readout electronics (sALTRO),
- an identical gating device (gating GEM) and
- possibly a common pad plane

→ Only the gas amplification stage differs => better comparison of performance for a technology decision.

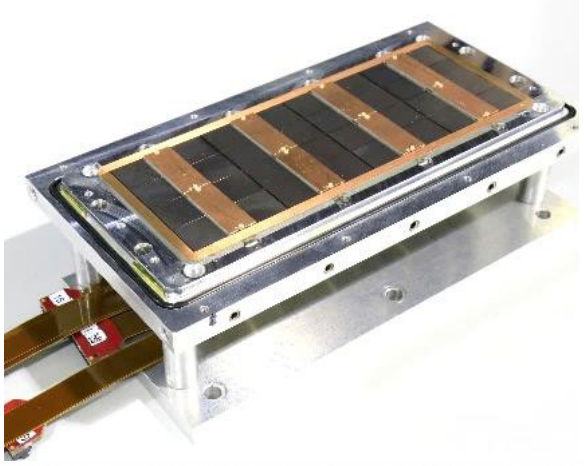
GridPix Detectors

GridPix detector have moved from Timepix to Timepix3 ASICs.
Tests with single and quad devices have been successful.



Currently a first module with 32 GridPixes is being constructed and will be tested in a test beam next year. Also tests in a magnetic field are foreseen.

Finally, a complete LCTPC module with about 100 GridPixes should be built.



Also the resistive protection layer will have to be optimized and the resistivity reduced.

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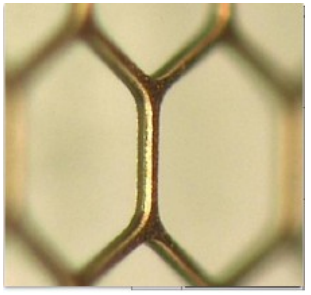
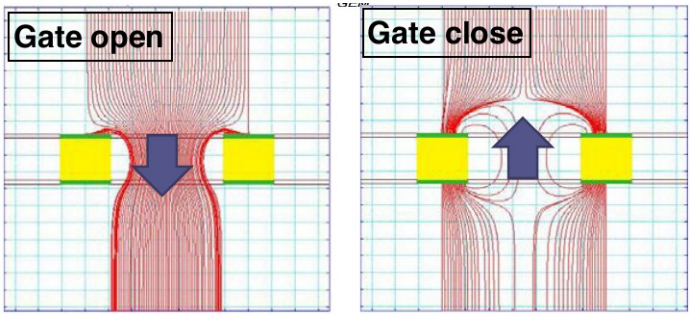
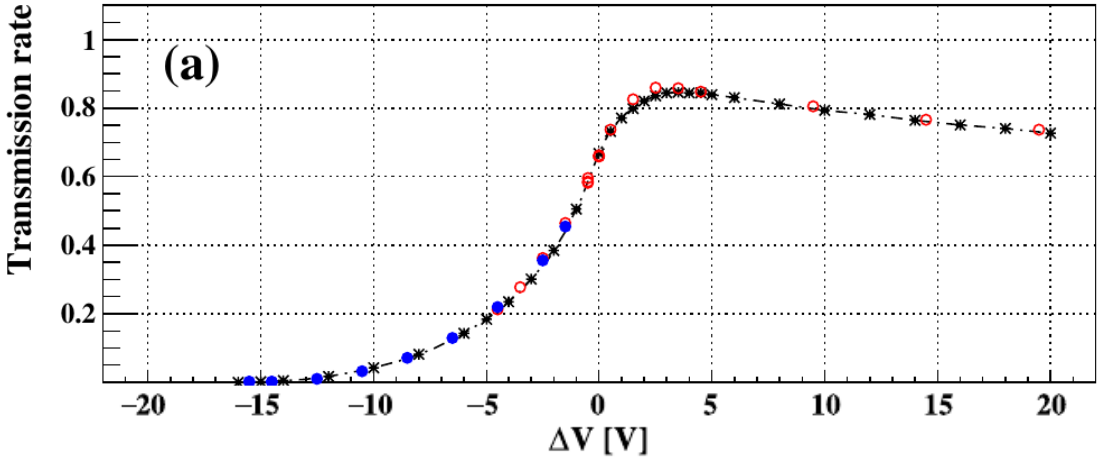
Gating GEM

As a gating device the gating GEM is a favorite, which has large holes (Ø 300 µm) and thin strips inbetween (30 µm).





The electron transparency has been determined with different measurements and corresponds to 82 % as expected from simulations.

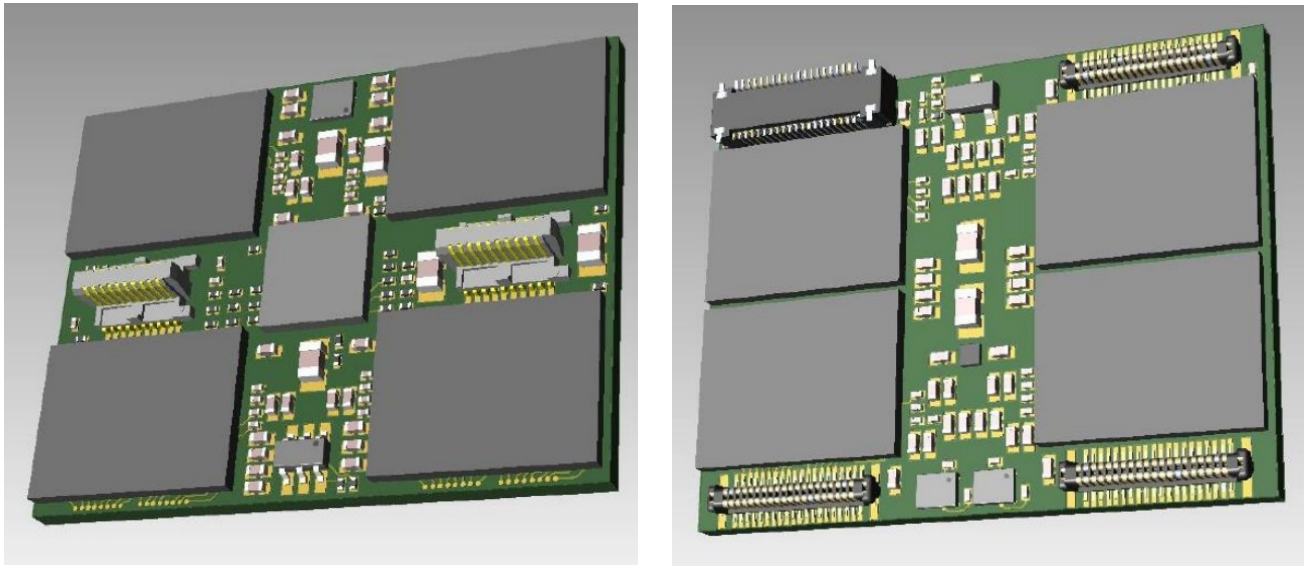


The ion blocking power still has to be determined and quantified.
First measurements have been initiated for this, but no results yet.
Also a fast HV switching circuit has to be developed.
The gate should also be tested in B = 3.5-4 T.

Electronics

A new electronics for R&D purposes is being developed.
It is based on the sALTRO ASICs.

- All ASICs are packaged and are being tested now.
- Additional boards have been designed and first (test) boards have been assembled. Tests show a full functionality
- The final layout is being designed.
- Still looking for an FPGA programmer to finalize the firmware.



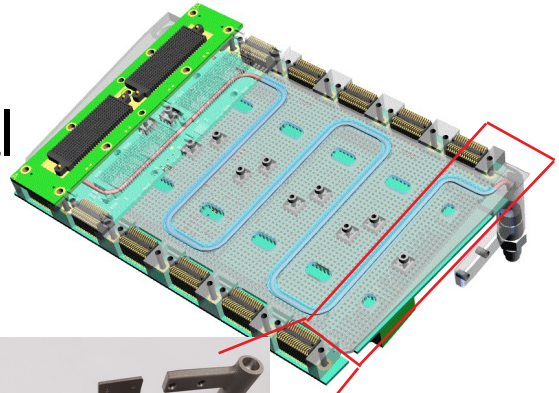
MCM-board from top and bottom

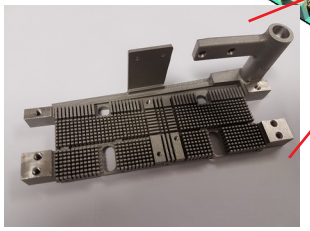
Determine design parameters for final ASIC.

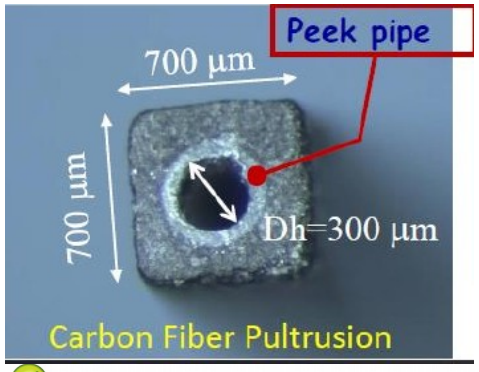
Cooling

Despite the power pulsing, the readout electronics may require a cooling system.
2-phase CO2 cooling is a very interesting candidate for the cooling. A fully integrated AFTER-based solution has been tested on 7 Micromegas modules during a test beam before.

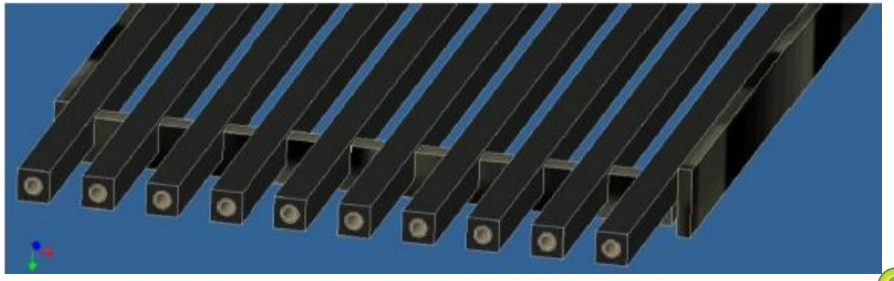
To optimize the cooling performance and the material budget, 3D-printing is an attractive possibility for producing the complex structures required. A proto-type of 1/8 module is already available at CEA, Saclay. It will be increased to 4 modules until 2021.







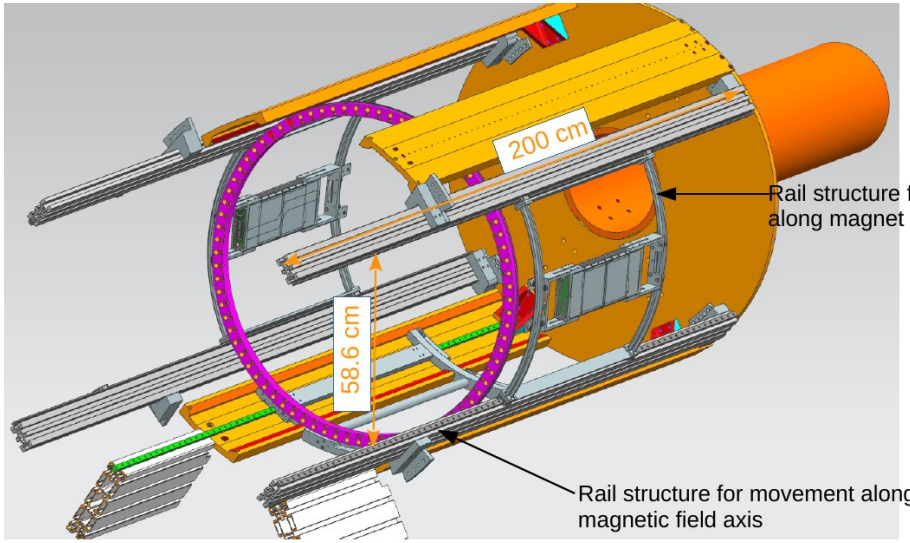
Alternatively, Lund is exploring micro channel cooling together with Pisa.
These consists of pipes with Ø 300 µm in carbon fiber tubes.



Setup at DESY

Further improvements of the test beam setup at DESY are in progress or planned:

- An external silicon tracker for the Large Prototype (LP) is advanced and first test beams have been performed. But there is still work to integrate everything.
  All groups will redo measure-ments with newest module types to study distortions



- Current field cage shows misalign-ments of the axis to the endcaps.
  → Construction of an improved field cage for the LP.
  → Also important for learning to build the final detector.

Open Issues

There is still a long list of open issues, which is very difficult to address, because a lot of manpower is missing.
Most of the issues are connected to simulating the TPC in detail:

Simulation (somewhat older list from 2017 – has to be revised, but probably true in many points)

(a1) Implementation of the response of the resistive anode in our simulation, and, test of one module with a resistive anode in the ILC events with beam backgrounds conditions.

(a2) Test of our current dE/dX code for the LP events, and provide it to the physics simulation.

(a3) Study of the pad size/length in the two hit separation, the occupancy, and the spatial resolutions (in the comparison to the current condition used in the physics analysis)

(b1) Studies of the dependencies of TPC and ILD tracker performances on TPC size and configurations in cooperation with the optimization group.

(b2) Pinpoint performance requirements based on various physics analysis for the technology choice, i.e. looking at different physics channels and charting distributions and requirements (single point, double track resolution, momentum and dE/dx resolution, reliability in performance), which allow the CB later to define the technology choice. Also, suggestions for the test procedure need to be studied.

(b3) Physics simulation to study the benefit of a TPC (vs. Si detectors): dE/dx, continuous tracking, non-pointing tracks. Find appropriate channels and show what a TPC can do better.
→ mostly done by ILD optimization group, but need input and some work from LCTPC

(c1) Study of benefit of pad/pixel readout: This may be partially included in the (b2). For the pixel readout optimized reconstruction algorithms are needed.

(c2) Simulation of physics events to understand requirements on two track/hits separation: This may be studied partially in (a3) for the pad readout.

Software – partially covered and large overlap with simulation tasks

- Further development of MarlinTPC and better understanding of the data already taken.
- Develop correction procedure for local field distortions → give 'final' result for single point resolution in PCMAG and 3.5 T.
- Develop simulation and reconstruction tools for 2 hit/2track reconstruction.

Summary

- Continue GEM, Micromegas and pixel tests at the LP in preparation for the preliminary design of the LCTPC after the green light.

- A gate should be included in the next-generation GEM, Micromegas and pixel modules.

- Continue electronics, cooling and powerpulsing development.

- Many simulations are still necessary to understand the detailed requirements of the final detector (e.g. number of ADC bits, pad sizes, etc.)

- Detailed plans will be discussed at our next collaboration meeting in January.