Asian Module

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No news from the last meeting(same as the last year)
except minor update of beam test result and some R&D

typical performance meets ILD requirement 100um σrphi, 5% dE/dx
Beam test result
some behavior are still not explained well
diffusion constant are not stable in each pad row
but Y.A. is trying to finalize result
A study of two track separation is on going by A.S. (not me)
using two event overlaid beam data at raw data level
R&D
In order to increase stability of GEM(100um thick GEM)
The system to investigate GEM thickness will be built
and may try larger hole GEM (sim. By T.O.)

Asian module

concept : minimize dead region with Gate device

Frame less @ module side -> effect is unclear
we may have dead area even without frame
due to gap btw module (1mm clearance in design)
GEM hole cannot be allocate the edge

Double GEM stack : to reduce mech. complication
Single GEM is better if charge can spread enough
wider induction gap

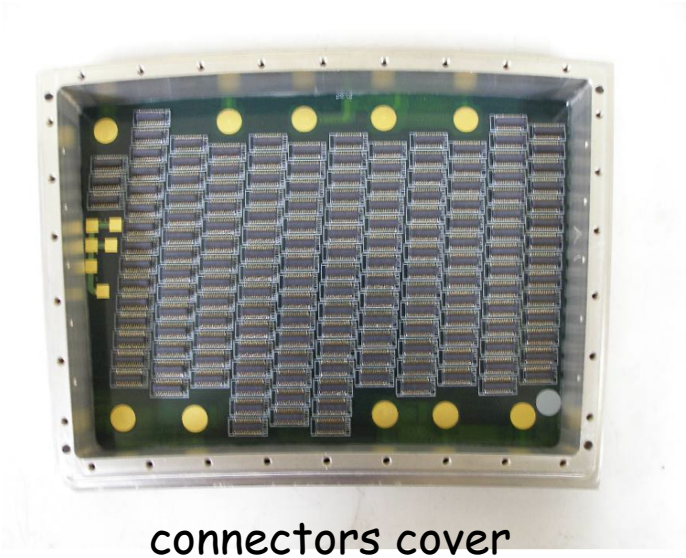
Module does has not been updated more than 10 years
(except minor modification of GEM)

Concept of Asian GEM module LP1

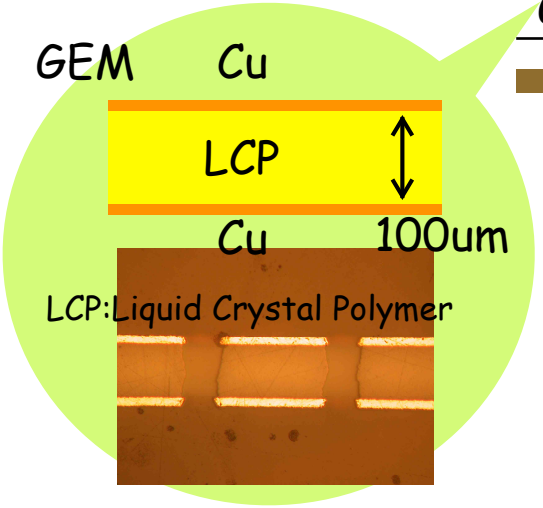
Pad plane (w/ Tsinghua U.)

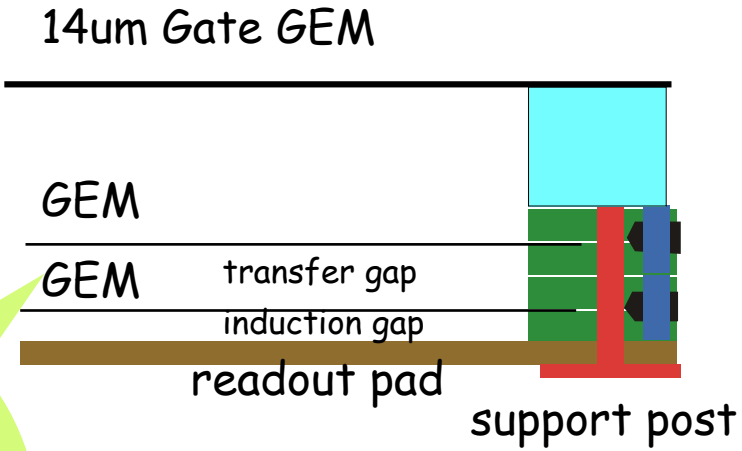
pad pitch ~1.1mm
pad height ~5.5mm
by ~300um diff.@amp.GEM

~5000 pads/module



connectors cover
most of the area in backside

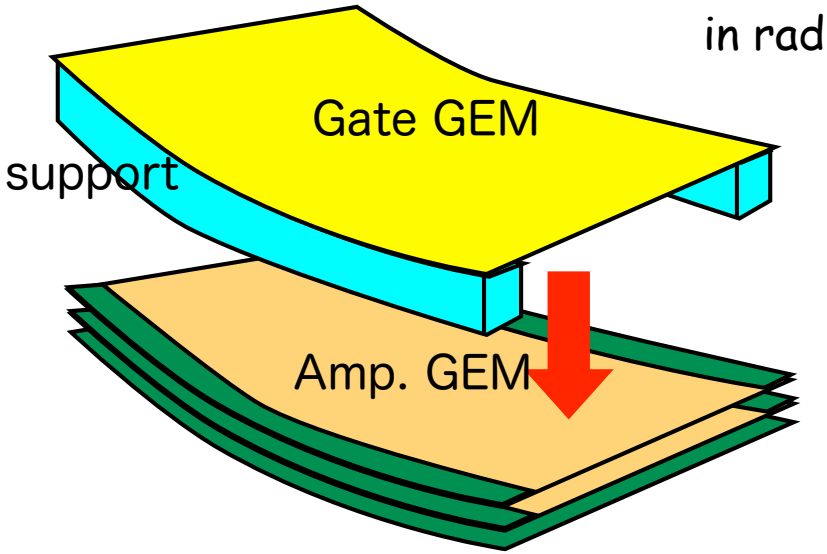




Amp. structure

Double 100um thick GEM

GEM stretched by support post
to minimize dead(support) area
in radial direction



GEM gate

14um thick GEM

Upper structure of module (Amp. GEM + Gate)

Which kind of GEM is the best for ILC ?

we have been waiting ideal GEM coming but ???????

std GEM, LCP GEM, teflon GEM, ... these need frame to stretch

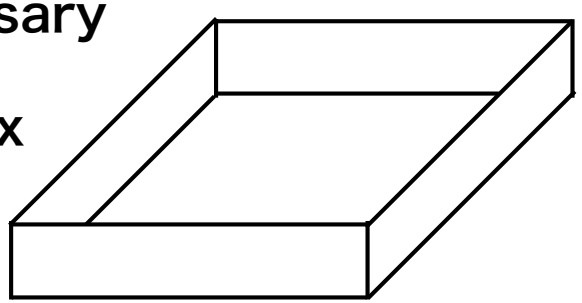
glass GEM (by HOYA, simulation study is begun by K.Yumino)

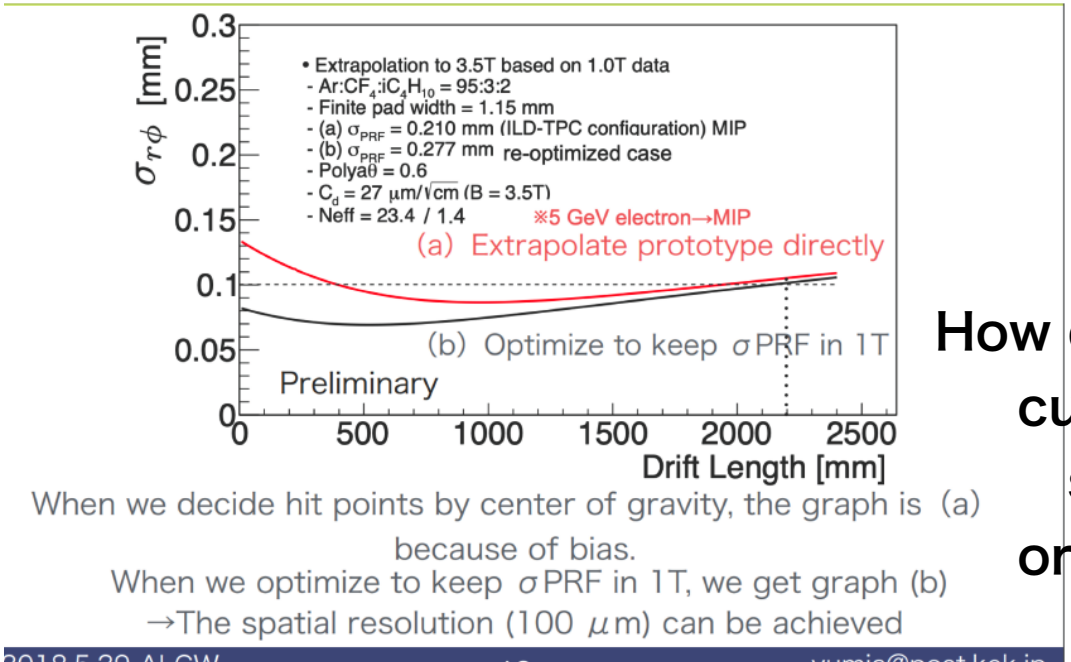
ceramic GEM (has been test by Kato)

these are rigid, no frame is necessary (?)

but GATE must be thin, so frame is necessary

rigid box





When we decide hit points by center of gravity, the graph is (a) because of bias.

When we optimize to keep σPRF in 1T, we get graph (b)

→The spatial resolution (100 μm) can be achieved

How do we enlarge diffusion at amp. region

current 6mm(4mm trans. + 2mm indu.)

should be 8mm??

or other ? method

Gate: this is not a specific issue of Asian module

We don't order Gate for a while

I don't know how long they can maintain technique to produce it.

Gate R&D with FUJIKURA

type0 -> type3 (current final model for 10x10cm size)

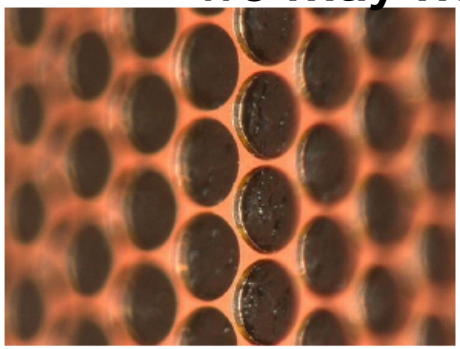
type4 is module size

type4 is produced @2015

some production@2016 for beam test

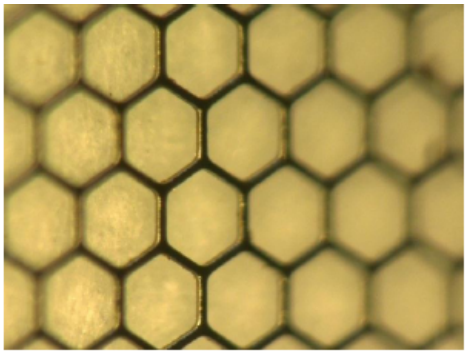
but no further production is done.

we may need to make sure their technology still alive someday



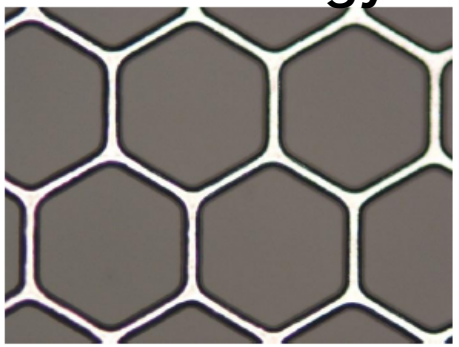
Gate GEM Type 0

形状:丸穴
穴径:300μm
リム幅:top 15μm, bottom 30μm
開口率:75%
size : 10 x10 mm
Process : Lazer direct



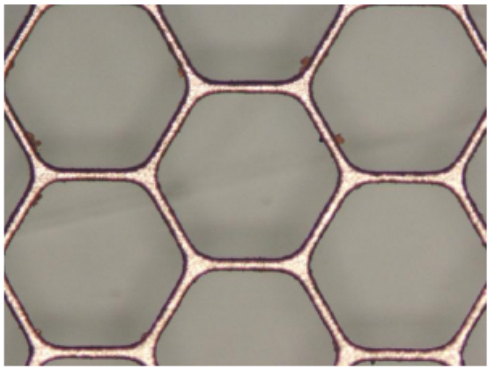
Gate GEM Type 1

形状:ハニカム
穴径:295μm
リム幅:top 25μm, bottom 35μm
開口率:80%
size : 30 x30 mm
Process : Ni -Plating



Gate GEM Type 2

形状:ハニカム
穴径:275μm
リム幅:top 35μm, bottom 40μm
開口率:76%
size : 90 x90 mm
Process : Ni-Plating



Gate GEM Type 3

穴径:295μm
リム幅:top 10μm, bottom25 μm
開口率:85%
size : 30 x30 mm
Process : Ni -less-Process

Electron transmission has been measured

by using test chamber with std 10x10cm GEM

with 3GEM, with 2GEM and ? with MM ? using Fe

by LP1 module w/ Asian module using 55Fe, Laser and Beam

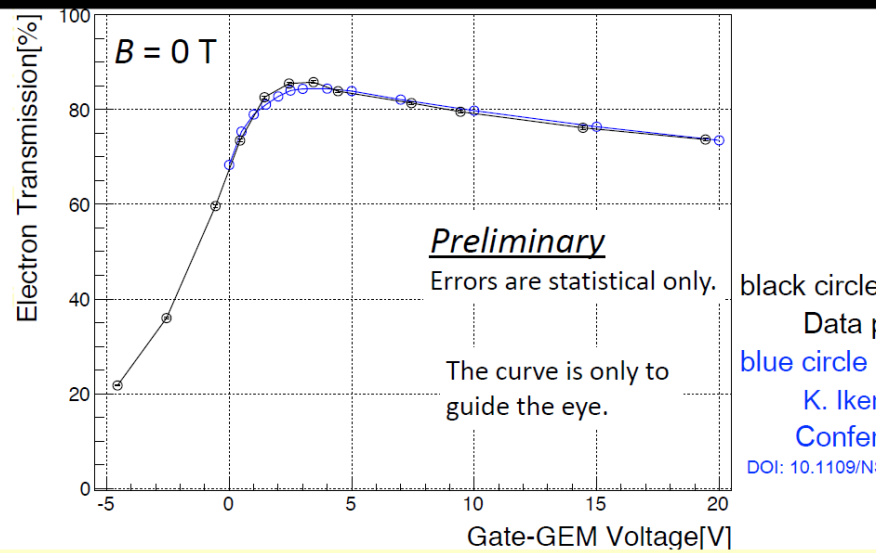
Transmission are obtained by different methods

but obtained results agree well each other (within error)

from charge ratio, position resolution and dE/dx

Quality Gate seem to be same for different samples

Electron transmission rate vs. ΔV measured with ^{55}F



black circle
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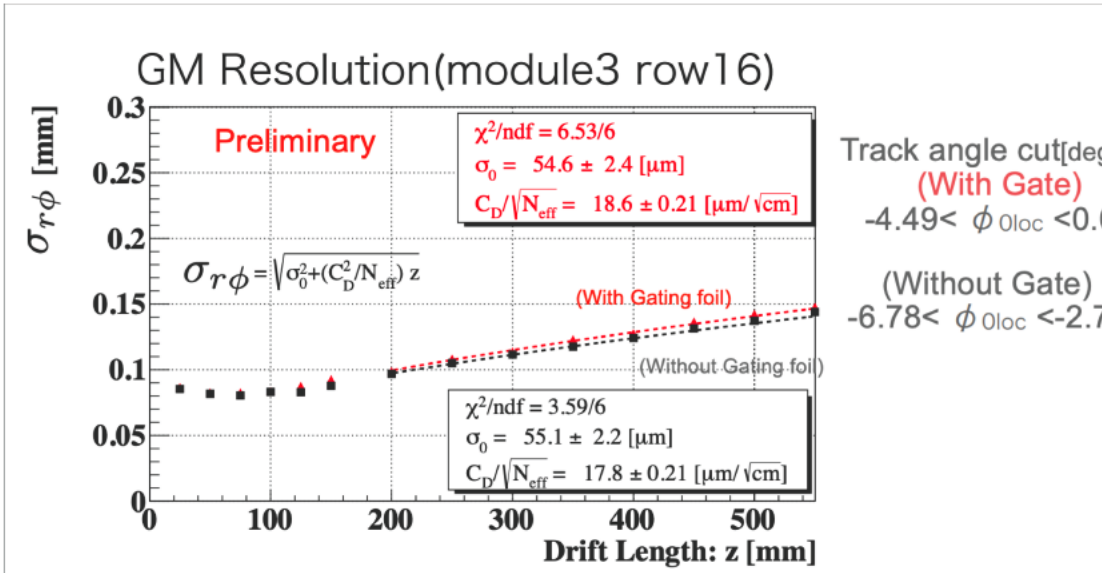
- The maximum transmission rate is about 86% at around ΔV = +3.5 V.
- The transmission rate decreases slowly above +3.5 V.
- It decreases rapidly with increasing negative ΔV.
- The measurement is difficult below ΔV = -4.5 V because of small signals.

Spatial resolution



Track angle cut[deg
(With Gate)
-4.49< ϕ 0loc <0.

(Without Gate)
-6.78< ϕ 0loc <-2.7

Transmission is also measured by CERN with P. Colas

show similar results with different gas Ar/CO2 with 3GEM

they also measure ion back flow using 55Fe under low pressure

we don't see any problem yet (because we don't study further?)

The remaining thing to be done for Gate

Ion back flow measurement under realistic condition

by using wire chamber to produce more ions

with precise current meter

HV to open/close Gate

Middle structure of module (PCB)

front side

Pad plane : 1mm width? for GEM

routing

rear side

connectors

current connector

X-talk btw neighbor channel >10%

not necessary to be high pitch like we used at LP1

-> Saclay's connector

can we make it 3 times more dense ?

RO chip can be mounted 5000ch on one side?

how to cooperate w/ sAltro16 effort

Back structure (electronics+cooling) of module is more unclear

Electronics

sAltro64 like chip ?

How we mount 80 chips on BP

surface mount? or MCM scheme ?

Connector

Cooling system is largely depend on chip layout/scheme

How/where we cool ?

Chip only ? Pad electrode ? Connector?

It's not easy to expect further progress of module R&D without budget and clear direction

Summary

We have to consider what will we do
after Green(yellow? orange?) light on

After this meeting
We hope to recognize which direction we would go