Status of the SALTRO16 readout system.

13.1.2020

Leif Jönsson
Lund Univerisity
(on behalf of the Lund group)

The Lund group:

Björn Lundberg:	previous electronics engineer at the division. He moved to a private company in 2010 but has recently started his own private enterprise.
Ulf Mjörnmark:	previous research engineer at the division. Since mid 2018 retired.
Anders Oskarsson:	since the end of 2018 retired.
Lennart Österman:	electronics engineer at the division. Is instructed to work mostly on the ATLAS experiment.
Leif Jönsson:	since the end of 2010 retired.

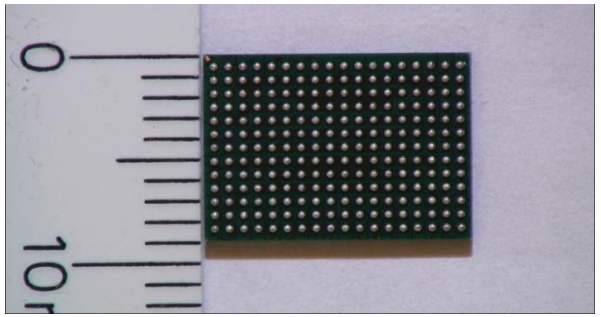
Flashback:

The packaging of the SALTRO-dies was started at the end of 2017.

Top side ← 12 mm →

9 mm

Bottom side with soldering balls in BGA pattern



- Prior to the full production two pre-samples including in total 89 chips were produced and tested.

- The packaging of the full number of dies was completed at the end of 2018 after careful tests of the pre-samples. Out of the initial number of 794 dies sent to the company, 748 were successfully packaged and delivered to Lund.

Prototype MCM

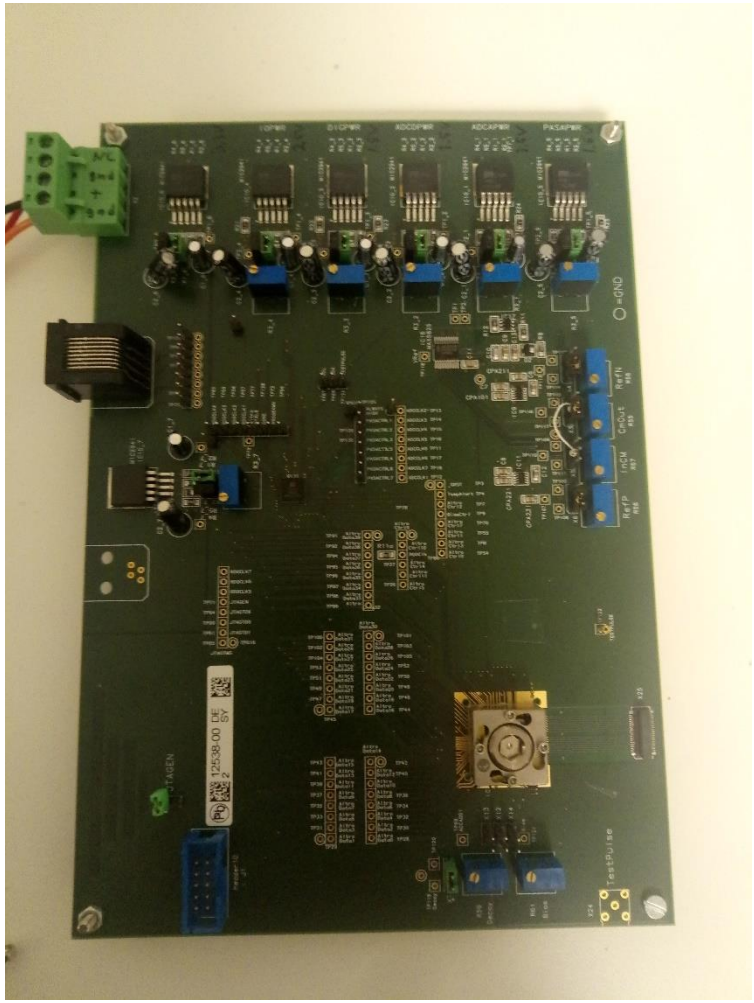
- In order to test the functionality of the chips we have produced a test board.

- The test board is read out via an SRU (Scalable Readout Unit).

- The FPGA firmware on the SRU is using the ALICE and TOTEM systems. However, this firmware has to be modified for full functionality in our application.

- The firmware for the CPLD is adopted from the ALICE exp.

This test system was used to test the 89 chips from the pre-samples with the result that 66 passed the test requirements.



Problems:

- With the present DAQ-system we are limited to perform a full readout of 2 channels out of 16, alternatively to read out all channels but limited to 180 samples.

- The SRU: re-arrangement of the memory management is necessary for full readout of al 16 channels.

- A bug which causes the system to hang has to be solved.

All this needs an FPGA programmer.

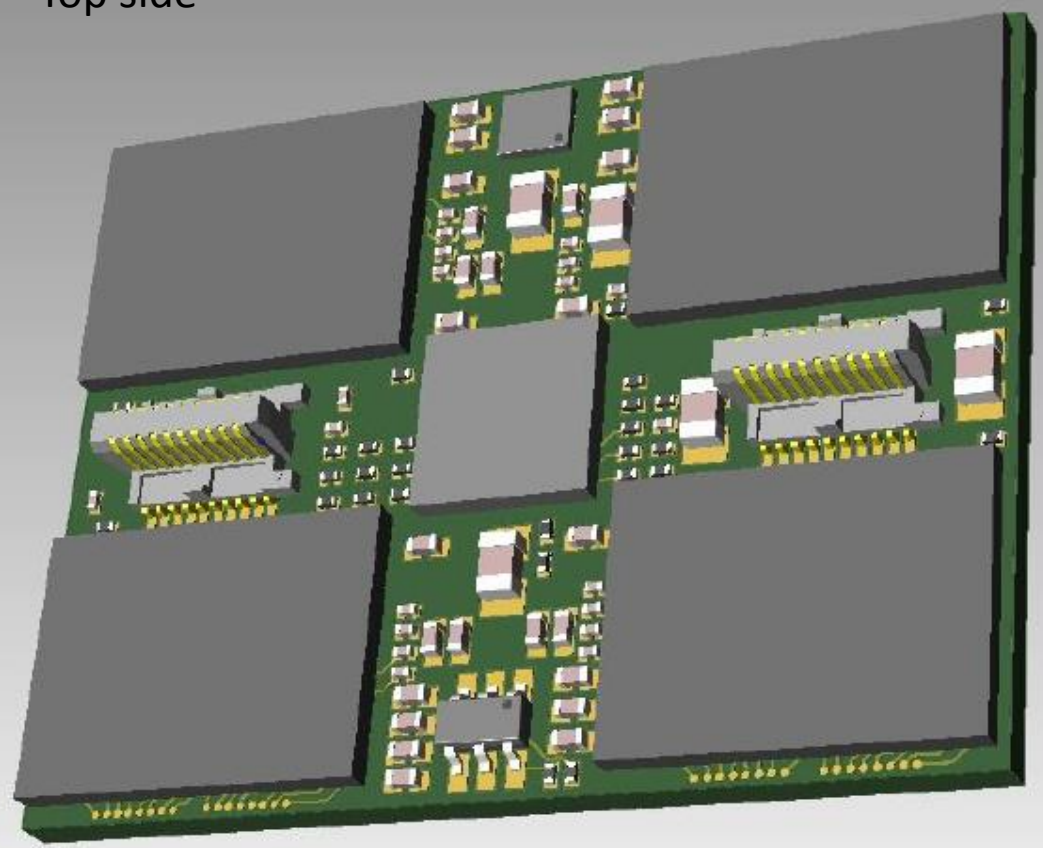
Until this has been solved no further chips will be tested. Presently we have 66 tested chips which is more than enough to produce one fully functional MCM-board.

The PC: the software exists but has to be further developed.

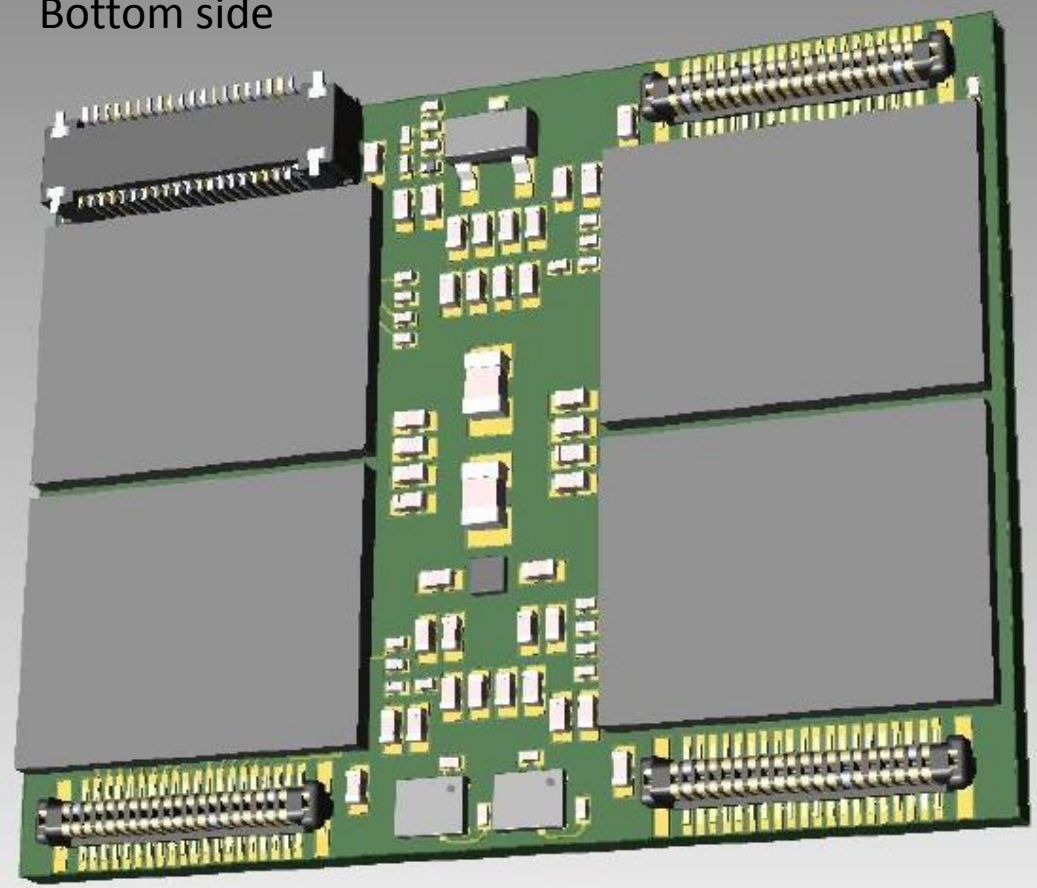
What has happened in 2019?

The design of the 16 layer MCM-board in HDI-technology was completed.

Top side

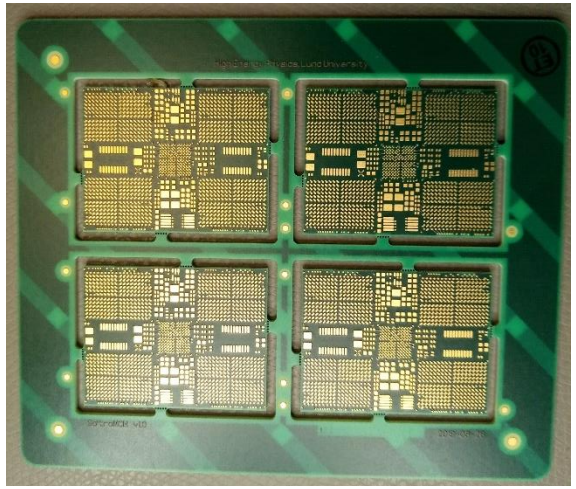


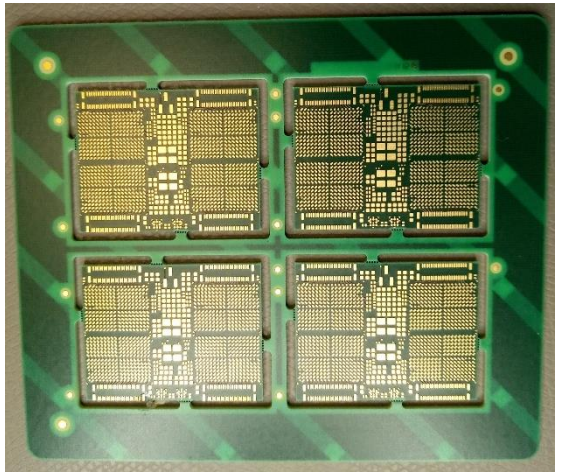
Bottom side



PCB-panel

One PCB panel contains 4 MCM-boards. The positioning of this panel in the pick-and-place machine and the solder mask is given by three reference points (3 in order to resolve right-left ambiguity).
Further reference points for each MCM-board are there for the specification of the coordinates of the various components.
The chips are positioned with respect to small angles in the corners of each chip.
Due to the small size of the soldering pads, the solder mask has to be positioned very accurately.
The soldering balls of the chips are 0.3 mm in diameter.
The design of the 4 board MCM panel was approved by the DESY electronics group in August 2019.



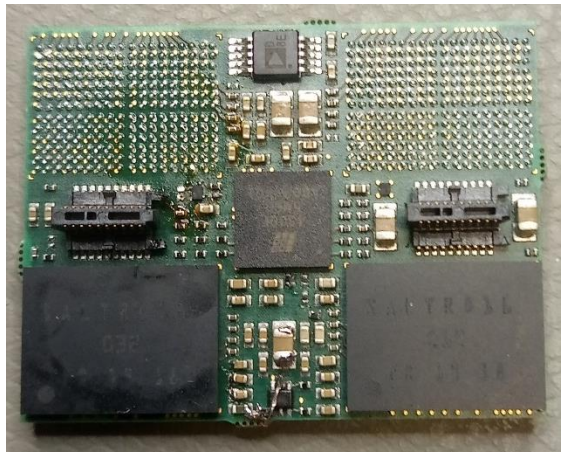
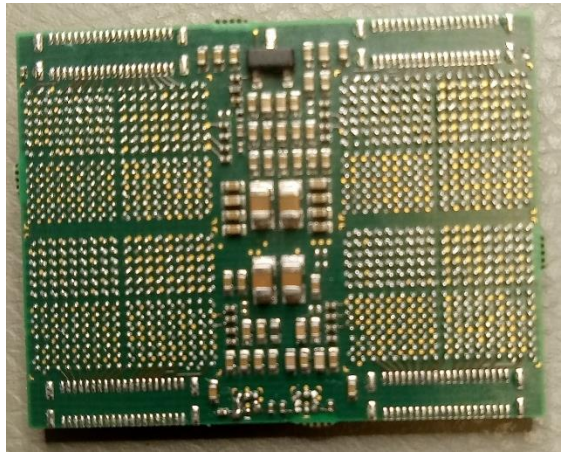
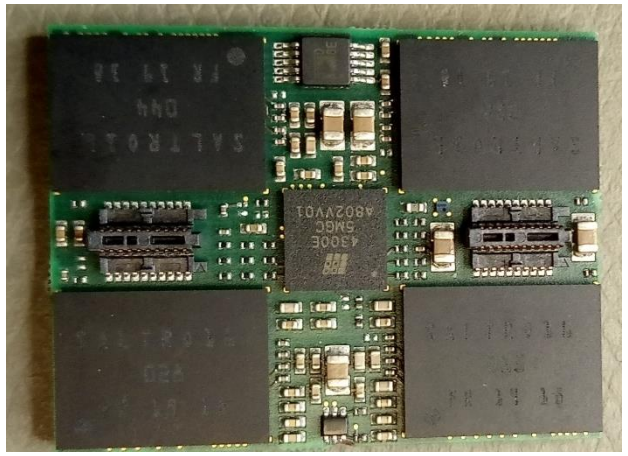
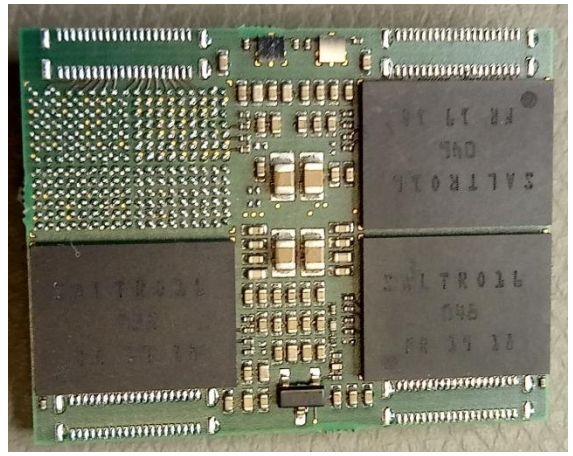


Two quotes for this 16 layer board was obtained, one through DESY and one through Lund. The quote obtained by Lund was almost a factor of two less than the other one.

25 panels were ordered in the middle of September 2019 and they were delivered at the end of October.

Mounting

Mounting of two boards was performed by the DESY electronics workshop at the end of November 2019, one with two chips and one with seven chips

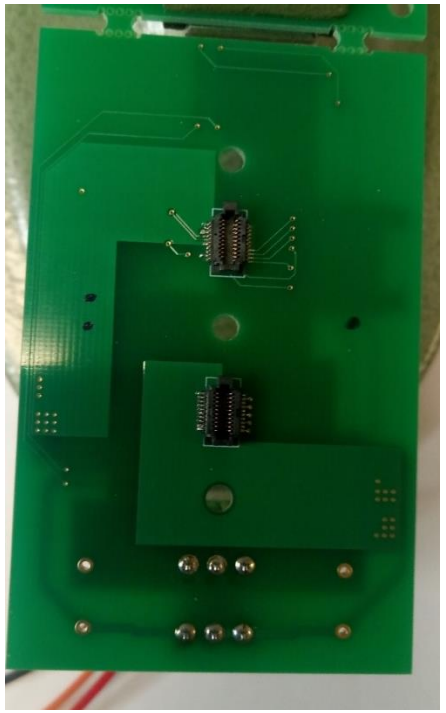





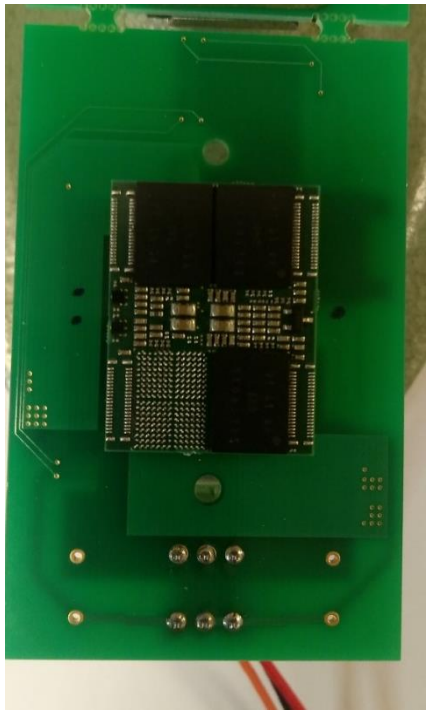
Problems:

Due to some confusion in the internal communication, within the DESY electronics group, an old version of the pick-and-place file was used, which didn't include all the components.
The part number of the Panasonic connectors was incorrectly specified by Lund (female instead of male).
There was also some confusion about the reference marks for positioning the solder mask.
First test in Lund in November-December showed some bugs in the design. Some bugs have been fixed and others not, either because their function is not critical for the tests or that it was impossible to fix them.

The LV prototype board

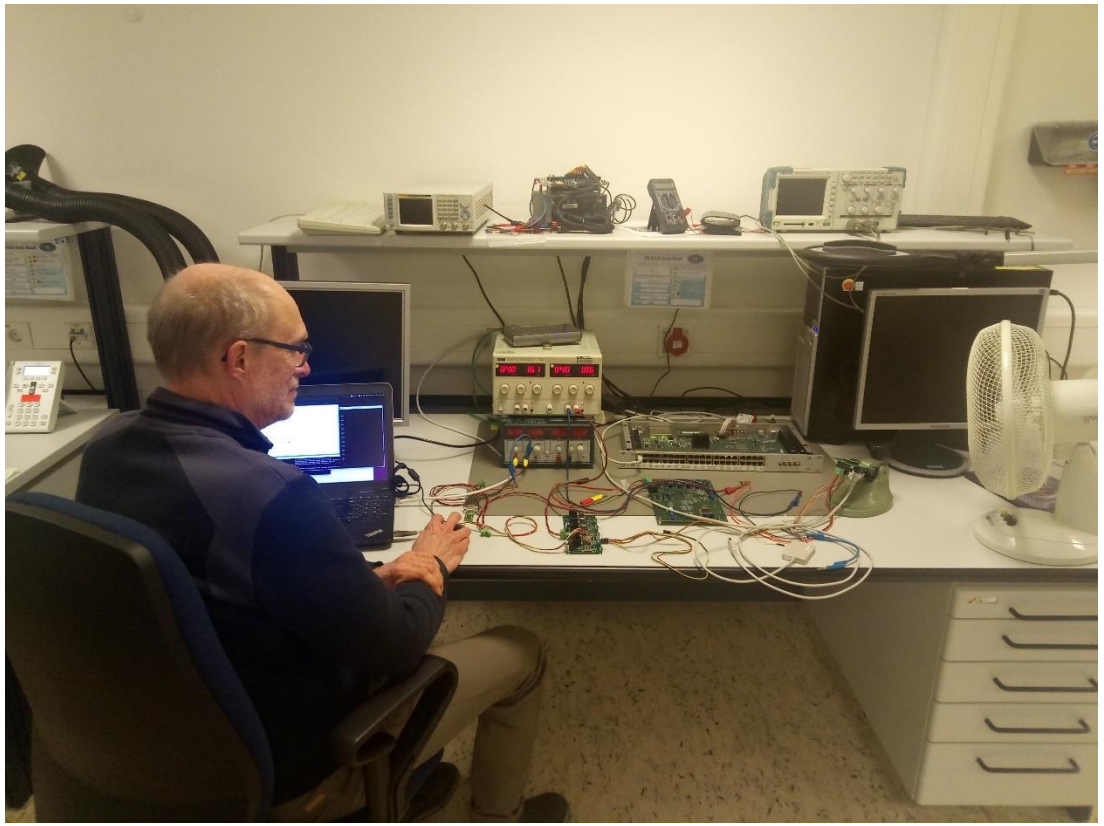
For the tests of single MCM-boards a prototype LV-board was designed. The final LV-board will supply voltages for 5 MCM-boards.
Due to the small size of the MCM-board the voltage regulators have to be placed on the LV-board.
Improvements: previously we had 7 voltage levels, now this is reduced to two, 1.5 V and 2.5 V.
Possibly the number of voltage regulators can be less than two per MCM-board, depending on how much current they draw.





Tests at DESY week 2, 2020

Due to the PCB bugs we can not test everything. What have been able to test (after bug fixes on the PCB) is:



1) The two chip MCM

- I2C communication: OK
- control communication DAQ-SRU-MCM: OK

2) The seven chip MCM

- control communication DAQ-SRU-MCM-SALTRO: 2 of 3 expected are OK.
- data communication DAQ-SRU-MCM-SALTRO: OK on the 2 accessible SALTRO
- data structure: OK on the 2 accessible SALTRO
- simple data bit test: OK on the 2 accessible SALTRO

Further tests need more bug fixing of PCB.

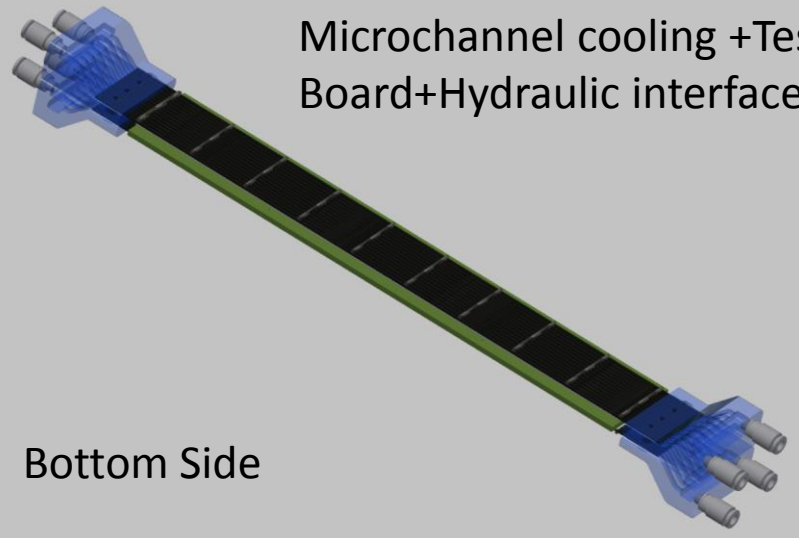
Cooling

The PISA-group within the AIDA-project, has designed a cooling support structure, which will be produced shortly and tested in PISA with the mockup board provided by Takahiro Fusayasu.

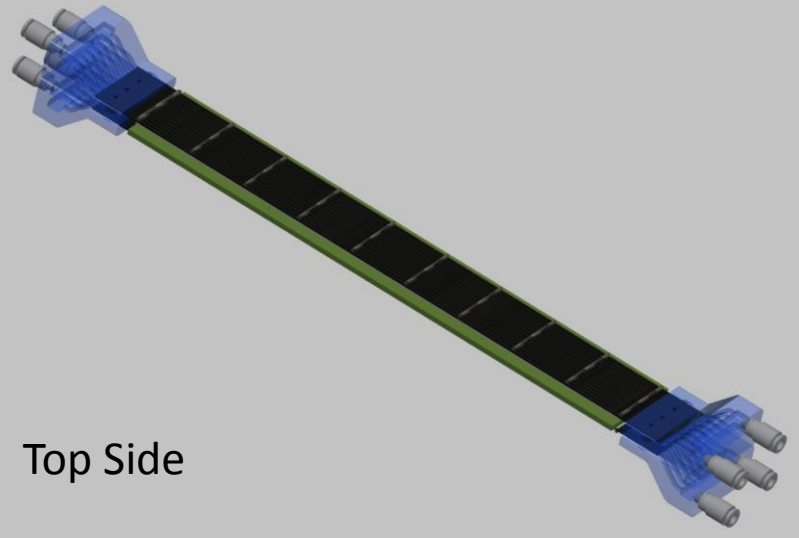
This board simulates one ladder of 5 MCM-boards, providing a realistic simulation of the power dissipation.

Microchannel Cooling with opposite flux

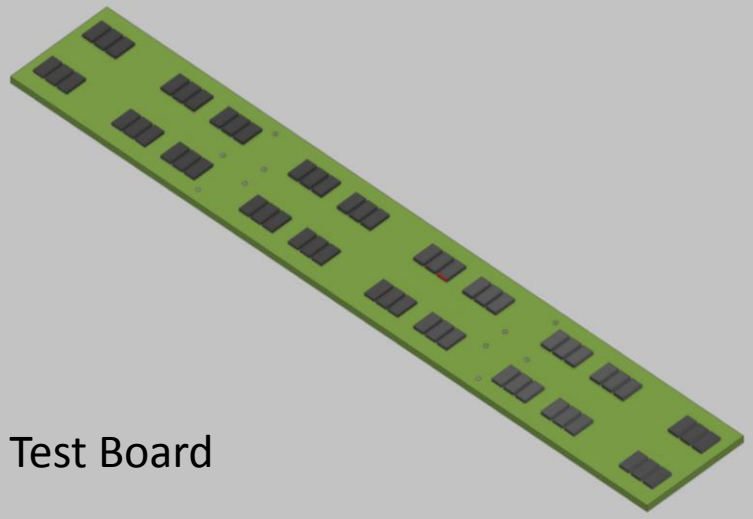
Microchannel cooling +Test Board+Hydraulic interface



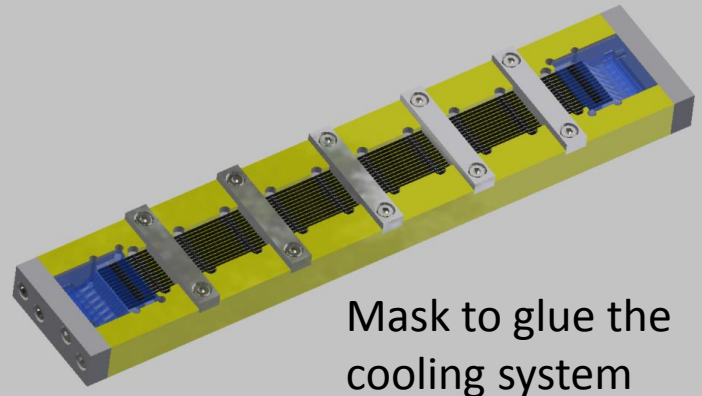
Bottom Side



Top Side

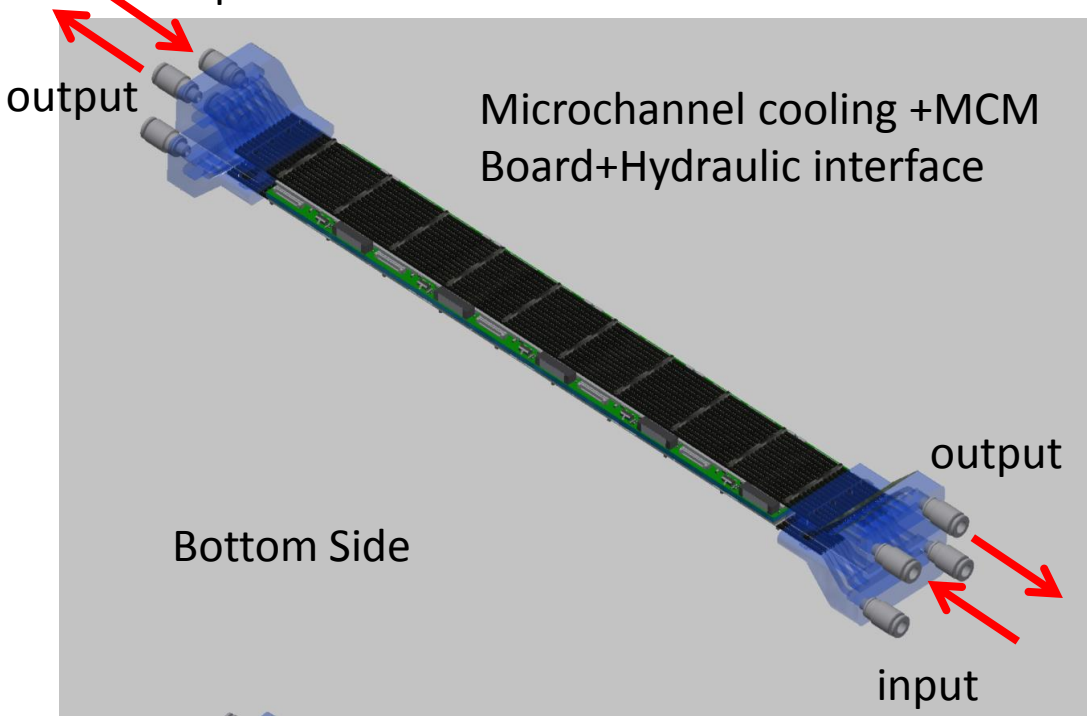


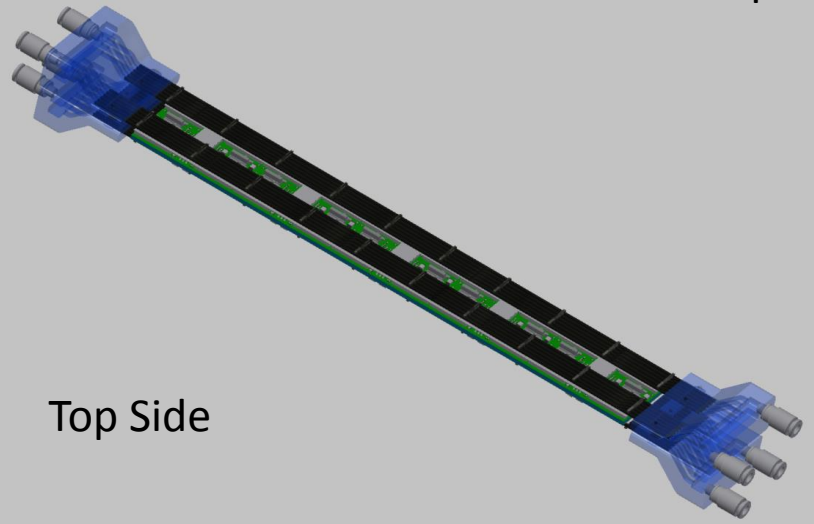
Test Board

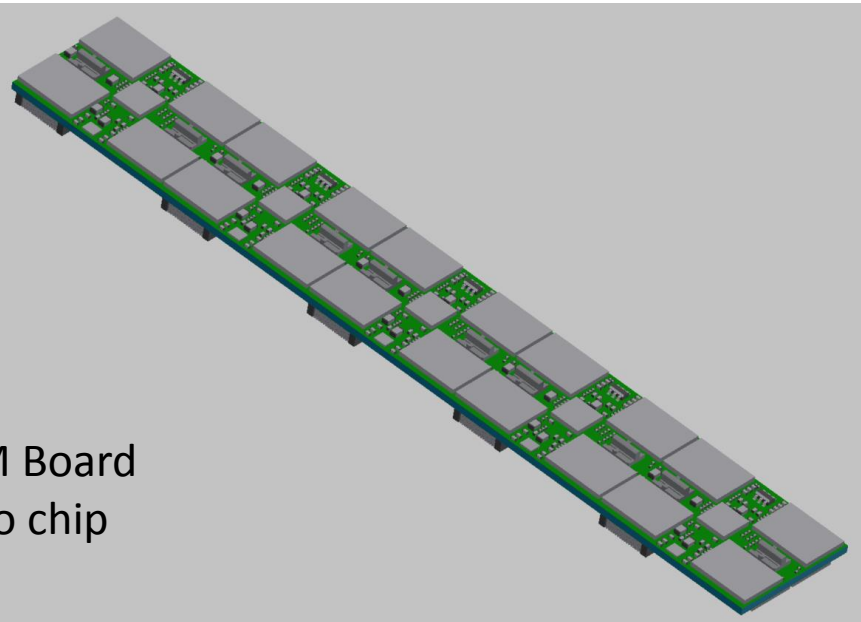


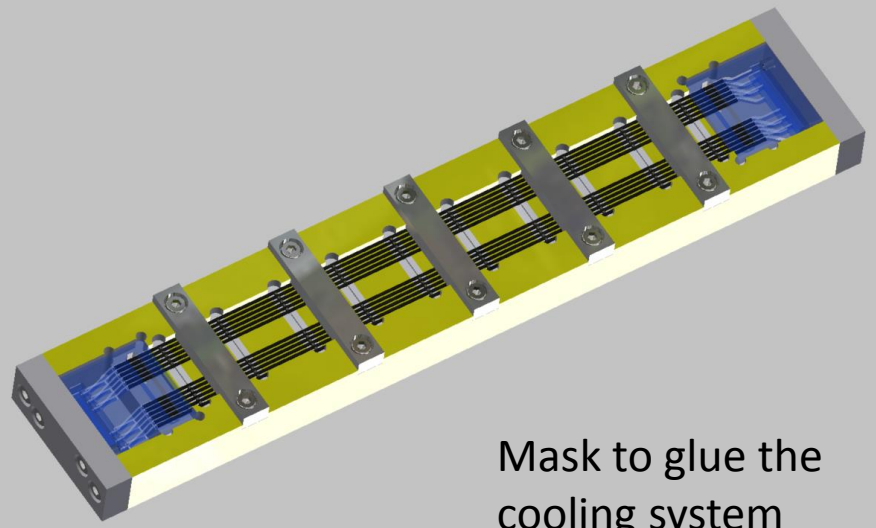
Mask to glue the cooling system (Top and Bottom Side)

Microchannel Cooling with opposite flux









Next steps

- Another assembly of the existing PCB is foreseen where attempts will be made, to correct known errors, where possible.

- Tests of the full functionality of the MCM-board (if possible)

- In the meantime all known hardware errors will be corrected in the PCB design.

- Once the prototype has been verified and no more hardware issues have been identified, a production version of the MCM PCB will be ordered.

- When the prototype MCMs have been verified, a final version of the LV-card will be designed, which will include power, slow control and read-out connectors for 5 MCMS.