

TPC Overview

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LCTPC

Status of LCTPC

Baseline

Pixel

Process towards tech. Choice

TPC in Japan

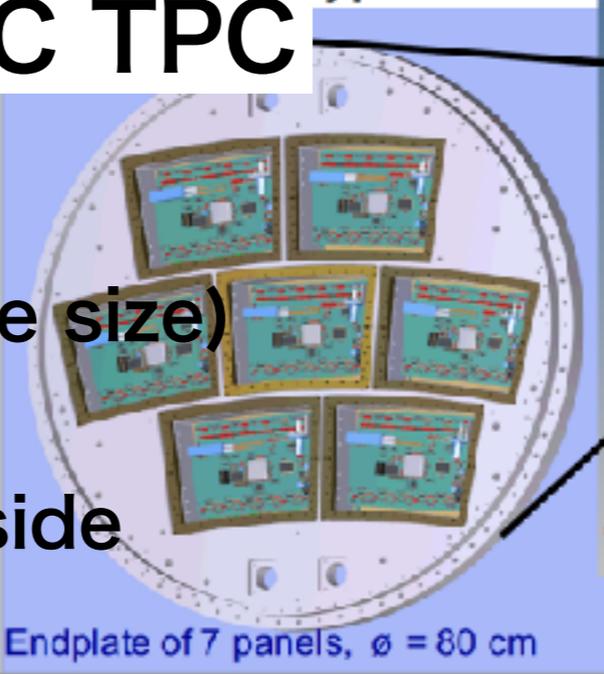
Recent study

beam test result update Aoki

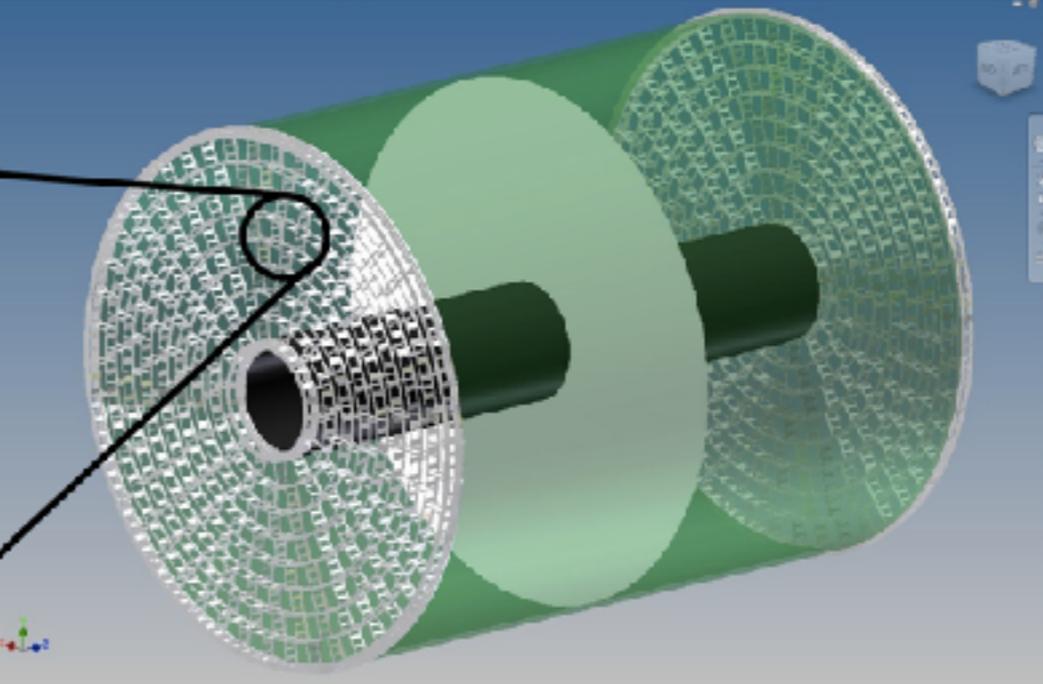
2-track separation Shoji

Basic concept of ILC TPC

Fan shape module (middle size)
 Amp./gate on front side
 RO electronics on back side



Endplate of 7 panels, $\phi = 80$ cm



ILD TPC: 240 modules

Module can cover drift volume with minimum dead space

GEM module

- Asian (double thick GEM + Gate
- DESY (triple std GEM

- RO electronics
- Altro base
- 1mm pitch pad

Micromegas module

- Saclay (MM on resistive anode

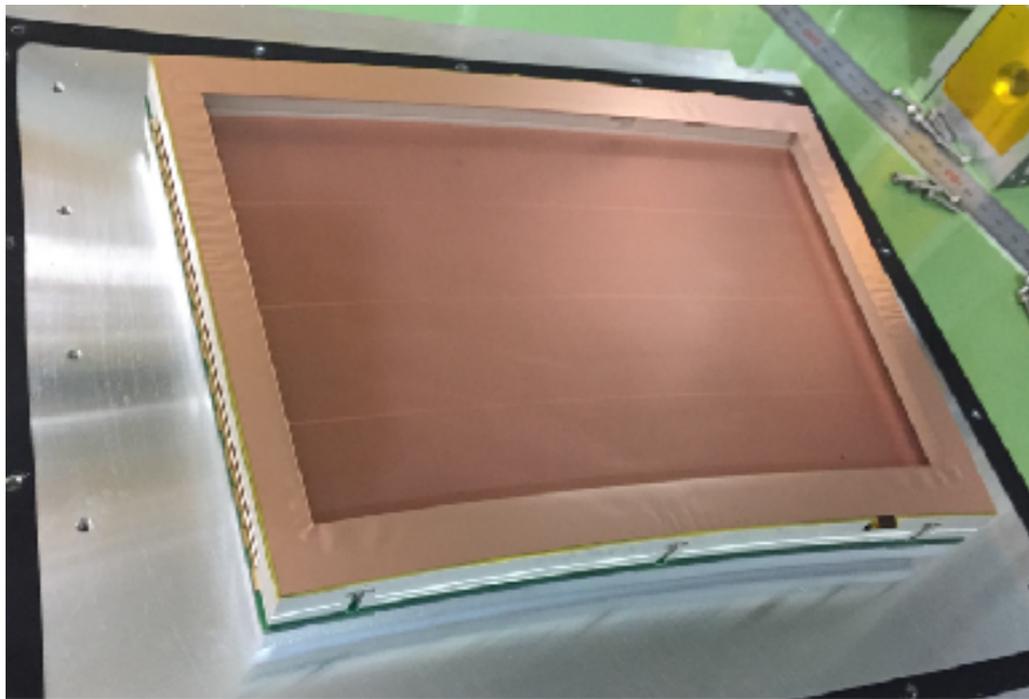
- After electronics (T2K)
- 2~3mm pitch pad

Common RO electronics (sAltro16) is not ready yet

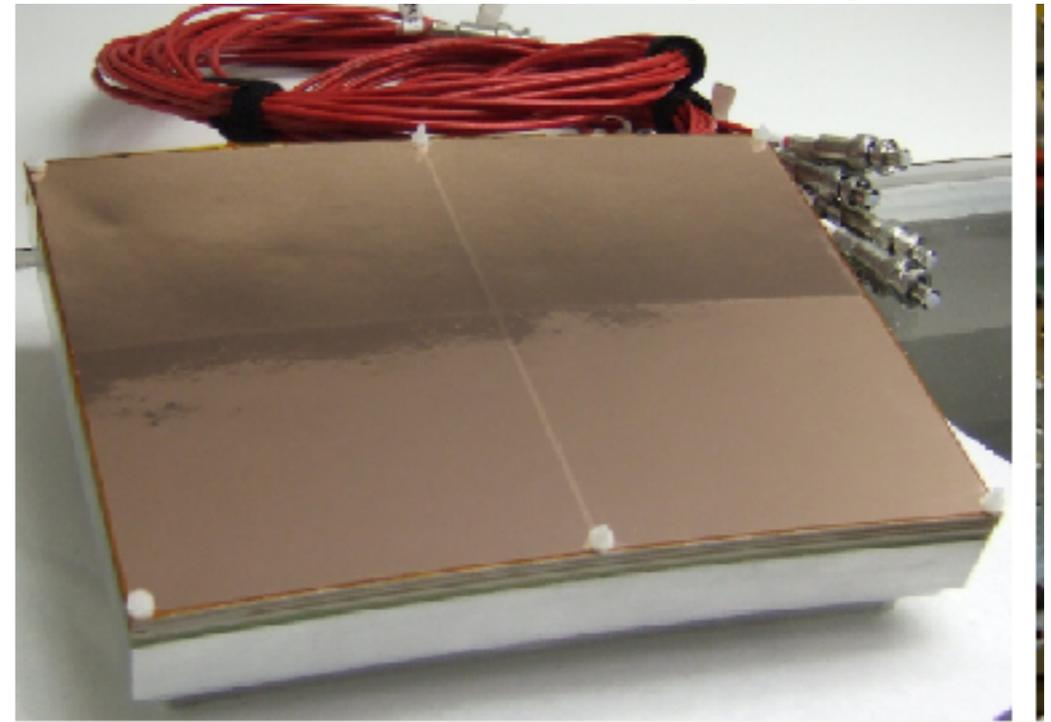
But these modules are tested under same LP1 test facility
 and provide almost similar result as expected

though there are some issue to be solved

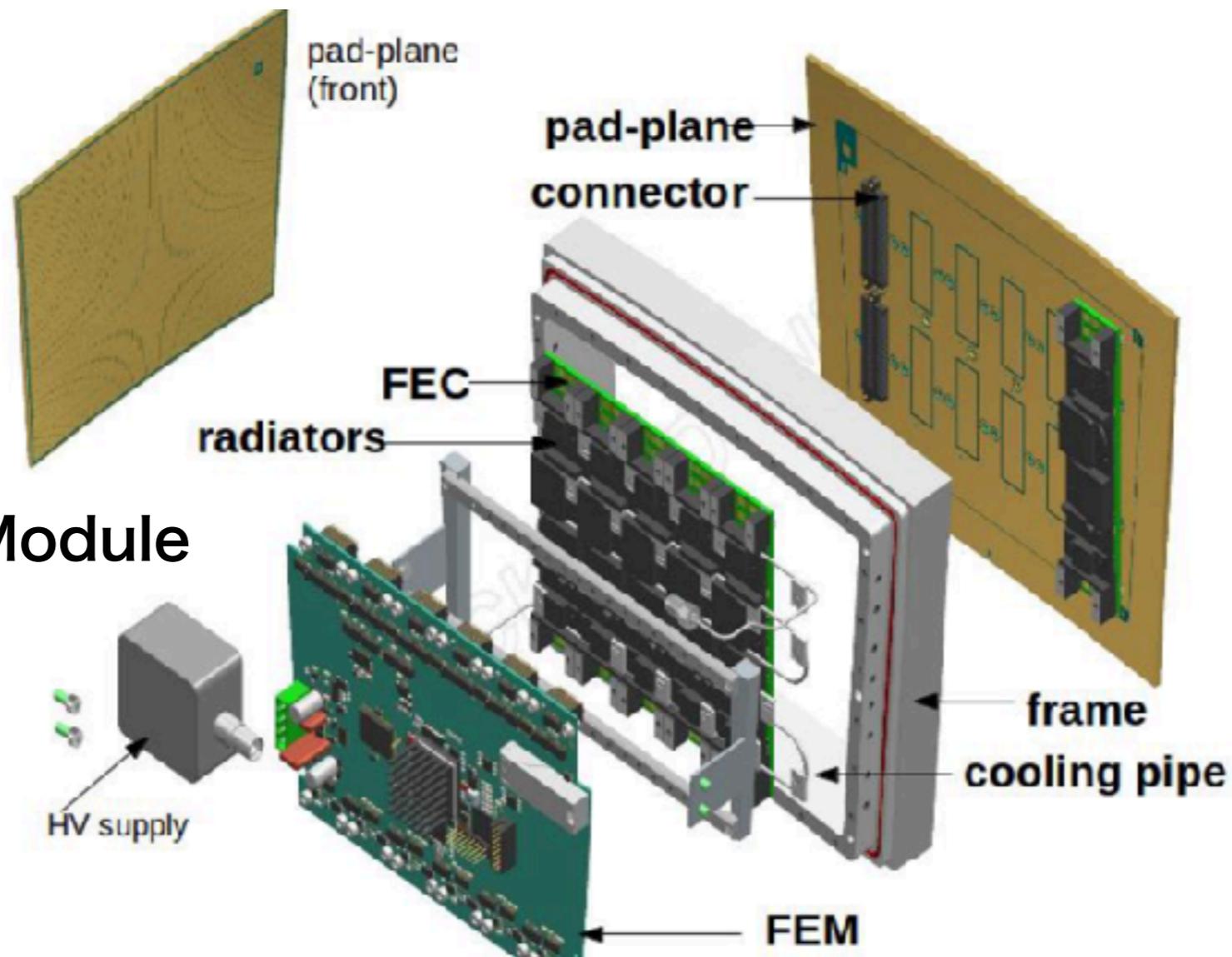
Asian GEM module



DESY GEM module



Saclay Micromegas Module



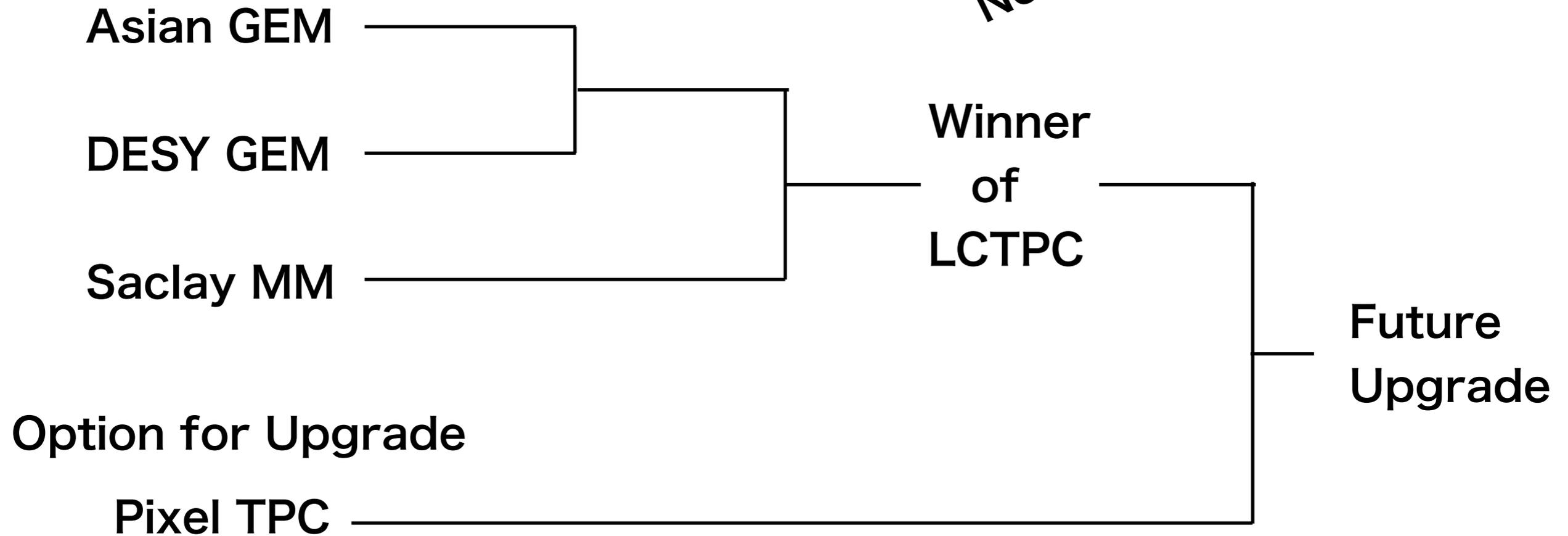
Realistic integration
(compact RO+
2PCO2 cooling)
was tested only at
Micromegas

	Gas amp.	RO pad	RO electronics	electron Gate int.	Possible problem	
Asian	GEM Double thick	1mm pitch	Altro base	Done	Upper structure frame/holding GEM GEM stability Realistic integration	New GEM? Mech. Engineering dev.
DESY	GEM Std. 50um triple	1mm pitch	Altro base	Not yet	HV distribution Realistic integration	
Micromegas	MM ~100um gap	2~3mm Pitch w/ resistive anode (DLC)	After w/ 2PCO2 cooling	Not yet	Stability of resistive anode Charge collection	

before 2020

Technology championship tournament

Not official procedure



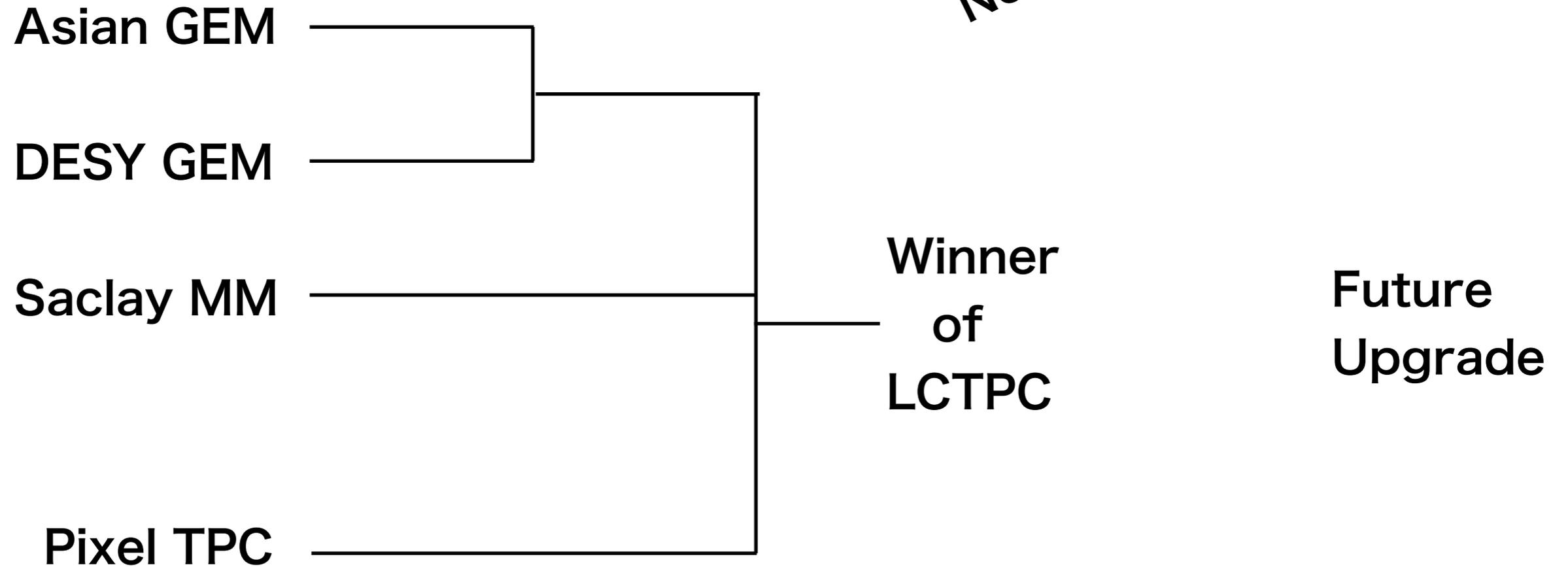
However, recent progress of Pixel module threaten above scheme.

Initial R&D grow fast, but pixel group continuously bring progress
Step by step

Now at 2020

Technology championship tournament

Not official procedure



Pixel module became one of tech. option (proposed at LCTPC mtg)
Not future upgrade anymore

Today, I would introduce how is pixel module now

What is merit of pixel

Digitization of position information by size

No ADC in electronics

= reduction of power consumption

Single electron counting

= no effect of gas gain fluctuation

Handling of too many channel

2k x #pad channel(2M)

Assembly of Si at large scale

New concept for tracking ?

Normal Pad

Position info.

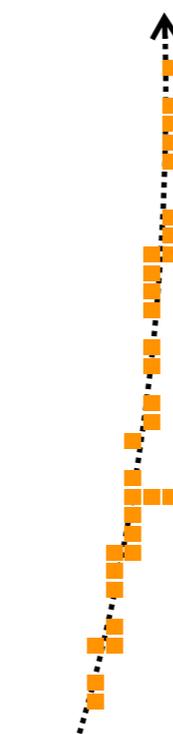
C.O.G with charge(ADC)

need multi. pad hits

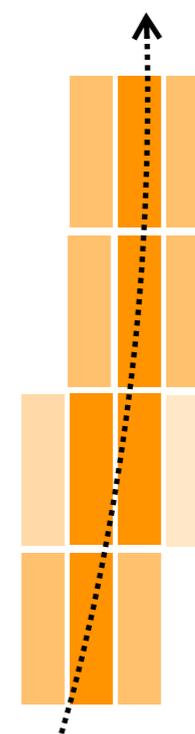
ADC (pipeline SAR)

Waveform record

~50 electrons/ row
gain fluctuation



Pixel

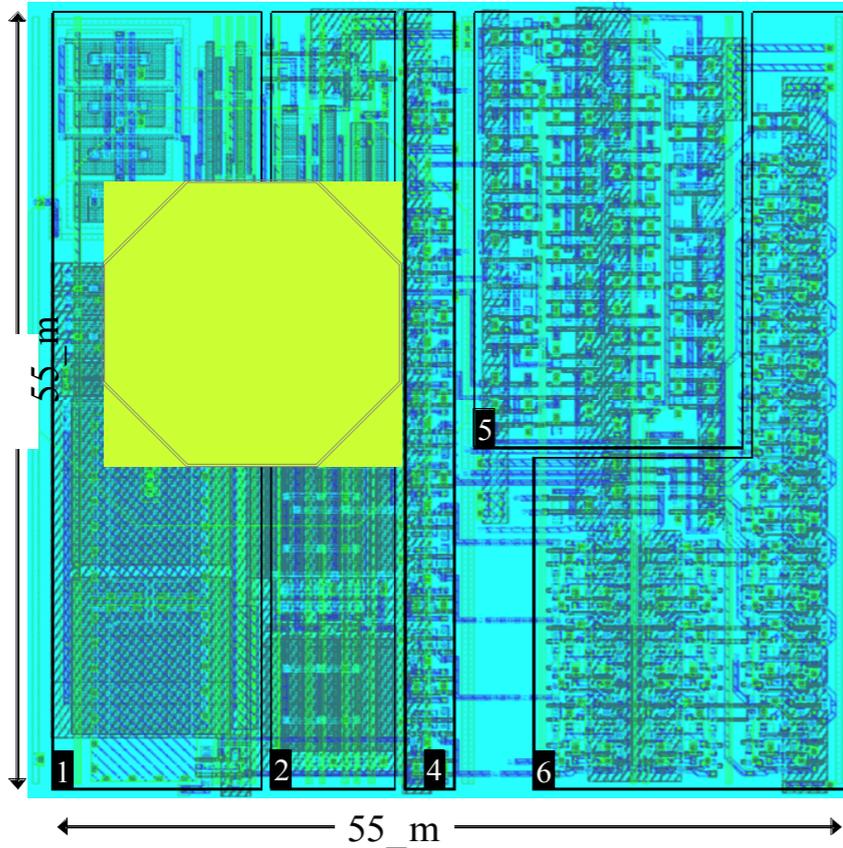


Normal Pad

This must be the beginning of pixel TPC



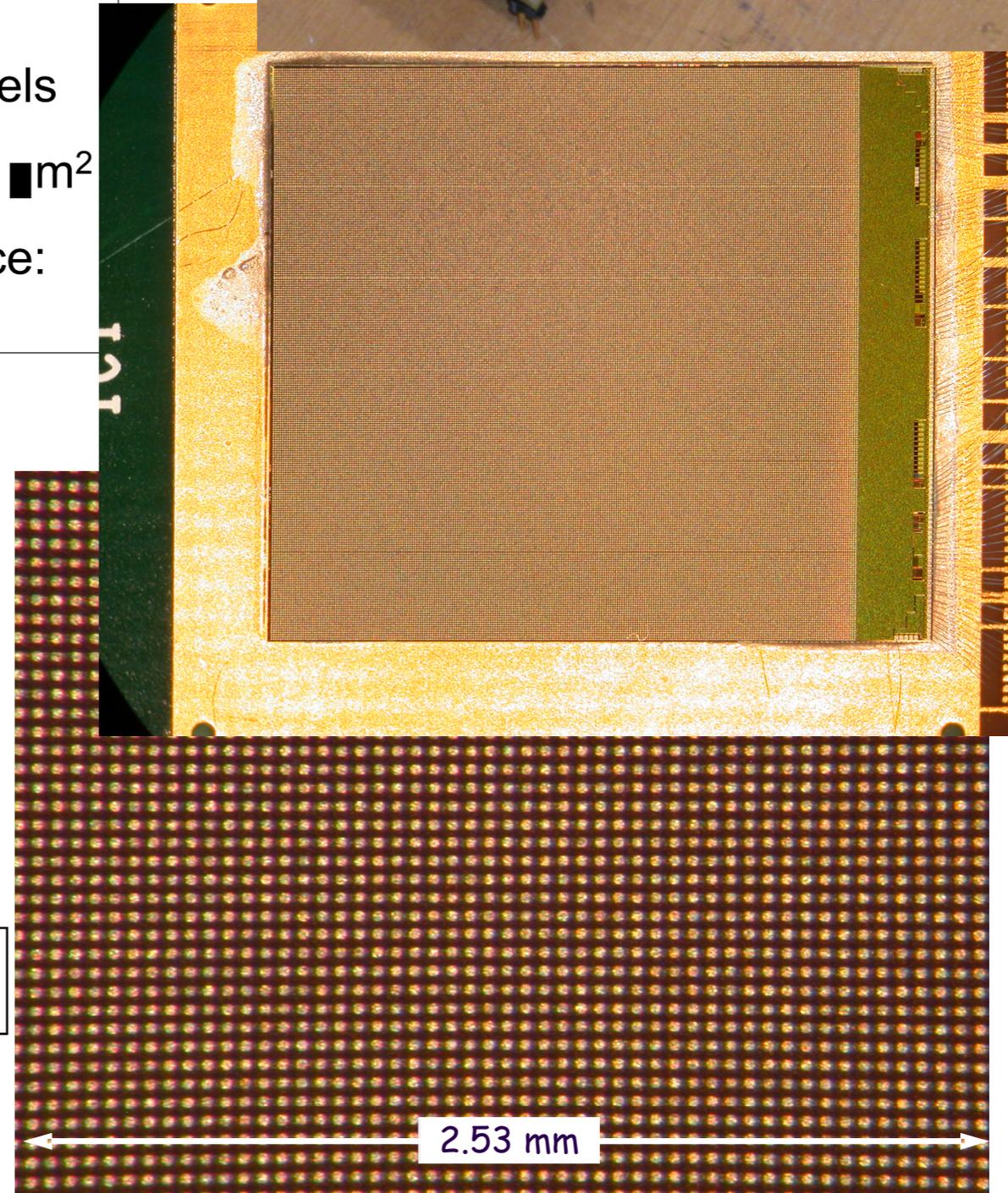
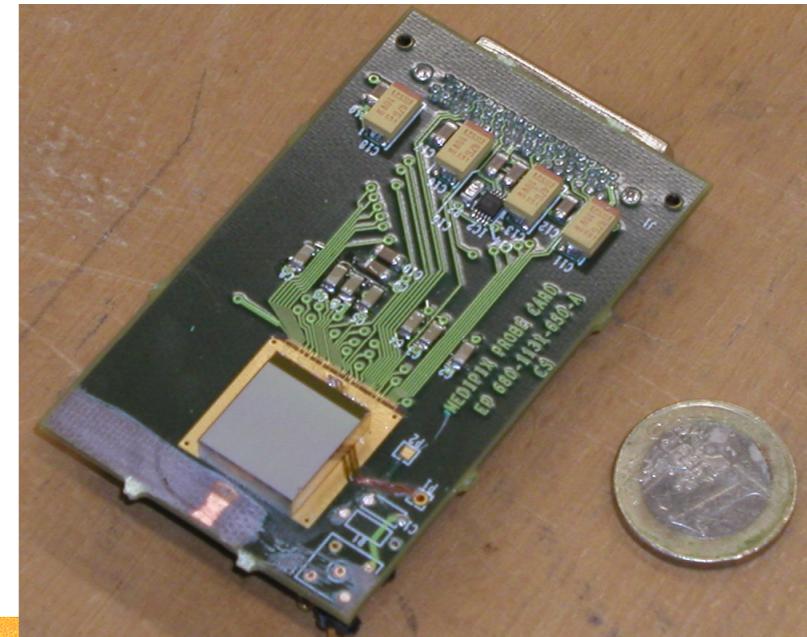
Timepix pixel



CERN

Timepix chip:

- 256x256 pixels
- pixel: 55x55 μm^2
- active surface: 14x14 mm^2



Timepix chip (1st version) produced Sept. 2006

Available for use in detectors since Nov. 2006

1: Preamplifier; 2/3: Threshold discriminator; 4: 8-bit configuration latches
5: Disc., 6: 14-bit Counter and overflow control

TimePIX + MEURO

TimePix project exist from the beginning of LCTPC collaboration
By NIKHEF, Bonn, Saclay,

TimePix originated from Medipix chip(medical use mounting sensor)
developed for LHC pixel detector

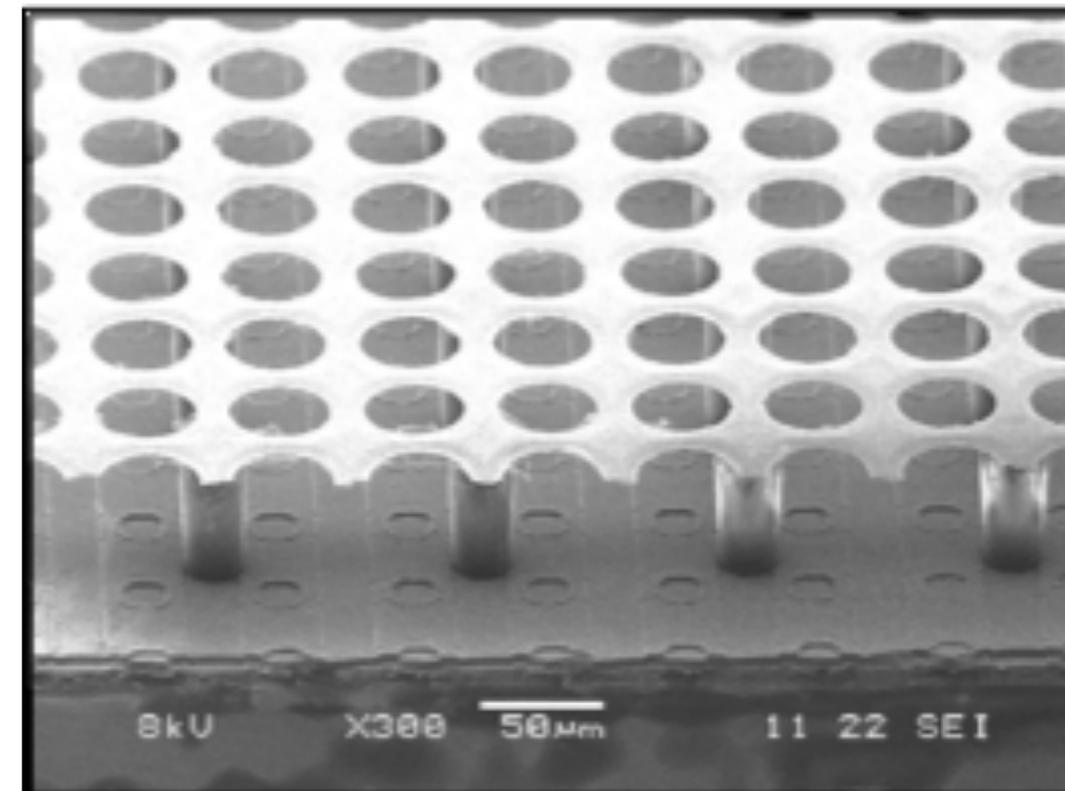
Micromegas structure is build on the CMOS chip by post process
Typical diffusion @amp. gap is less than 20um

Timepix 1 Single electron signal is covered by one pixel

TimePix chip (pixel size $55 \times 55 \text{ um}^2$, 256×256 pixels on $14 \times 14 \text{ mm}^2$)

Each pixel has one function
out of 3(hit counting, ToT, TOF)
You can choose function for each pixel

Discharge destroy chip !
Protection layer is introduced
Si-nitride, amorphous Si



But at those days,

Timepix has

One function for each pixel

TOF for TPC use , then no other information is available

Time resolution (by clock 100MHz -> 10nsec.) not so good

meas. time restricted by counter 14bit (cannot cover 1msec)

No multi hit capability (though pixel is small, 1msec coll. time)

dead space for wire bonding

integration with less insensitive area

Pixel looks good but ... for future upgrade

But Now Timepix became 1 -> 3

Timepix has

Two functions for each pixel

TOF for TPC use ,

ToT is also available: ToT ~ PulseHeight -> time walk corn.

much improved Time resolution

Data is transferred to Control board

you can measure next hit after some processing time

dead space for wire bonding -> It might be reduced after Timepix4

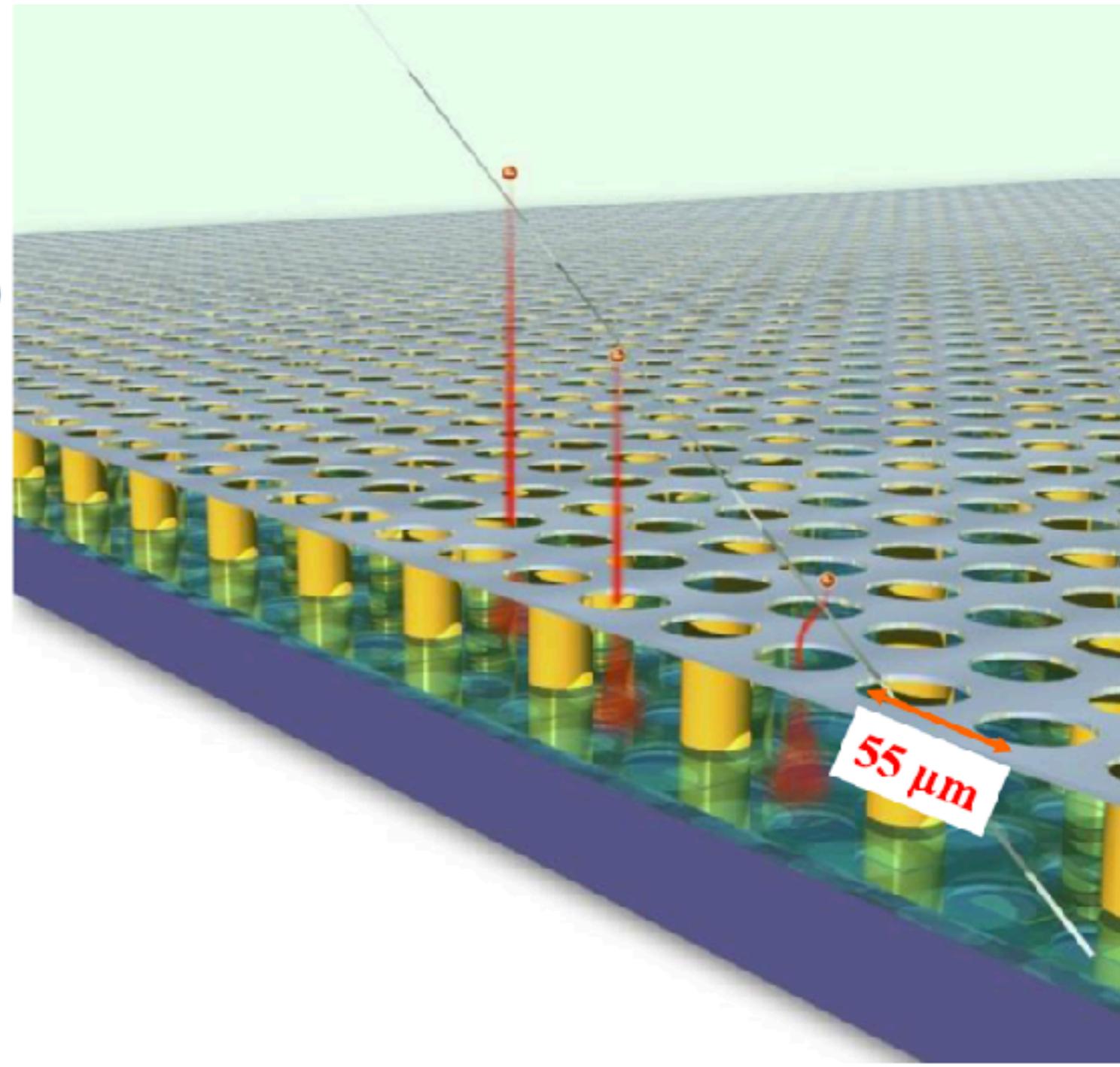
Si through hole may improve

integration with less insensitive area

GridPix technology

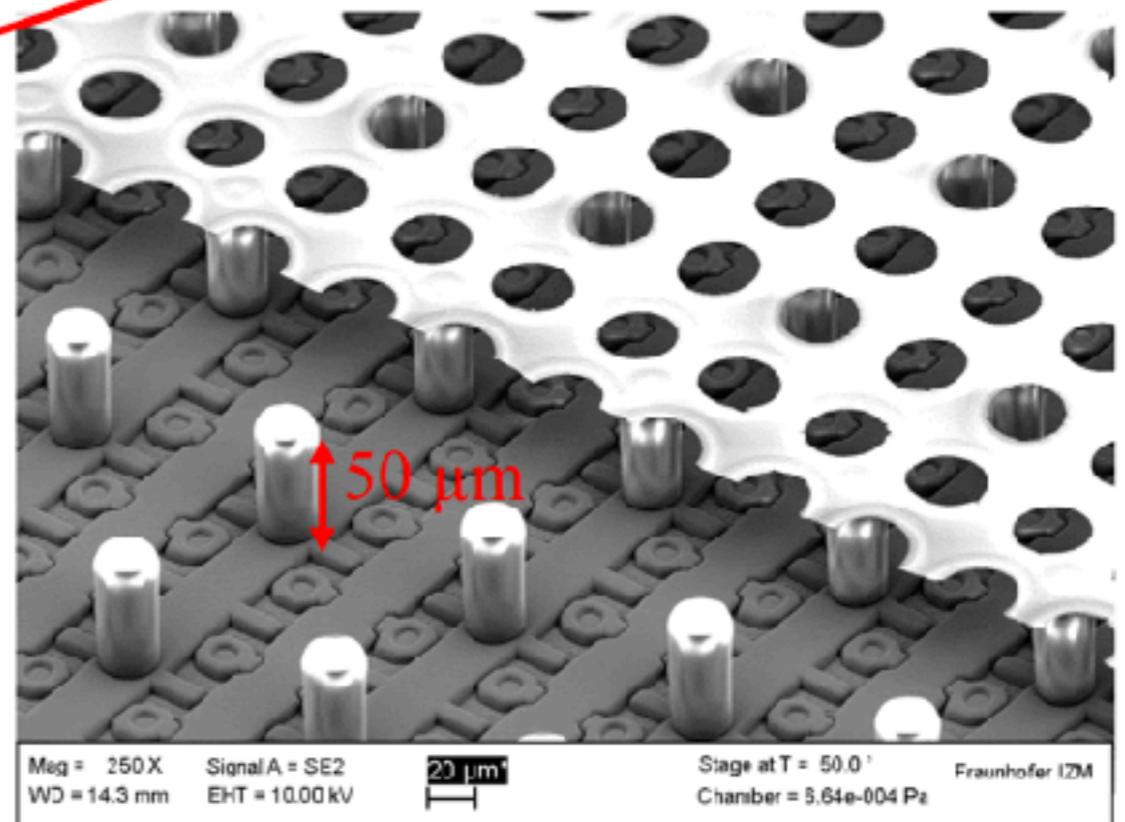
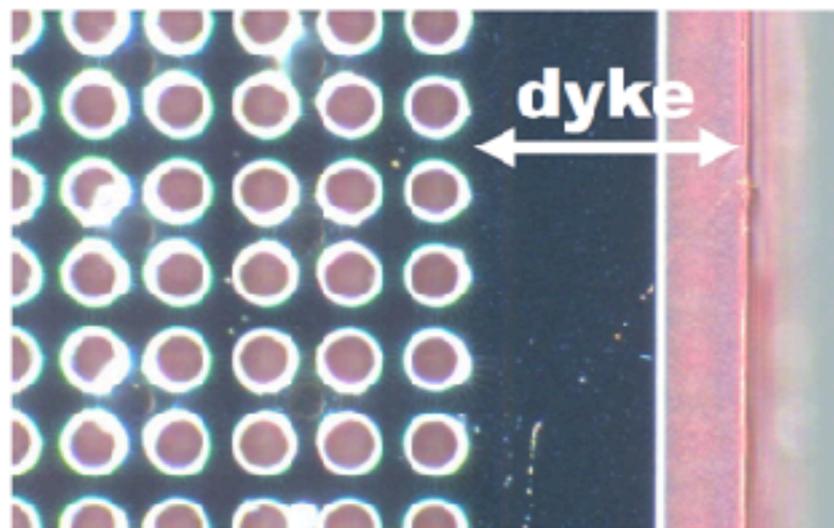
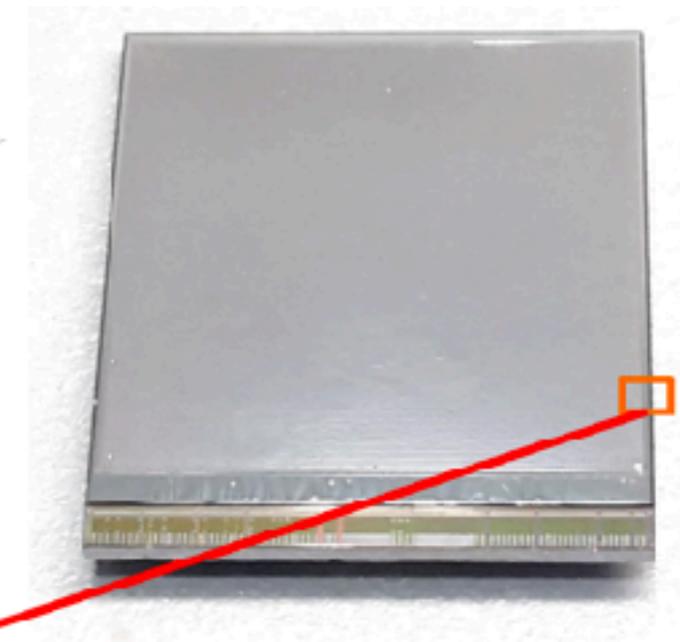
- Pixel chip with integrated Micromegas
- => **InGrid**
- Grid set at negative voltage (300 – 600 V) to provide gas amplification
- High granularity (55 x 55 μm)
- => mostly detecting **single electrons**

GridPix chip

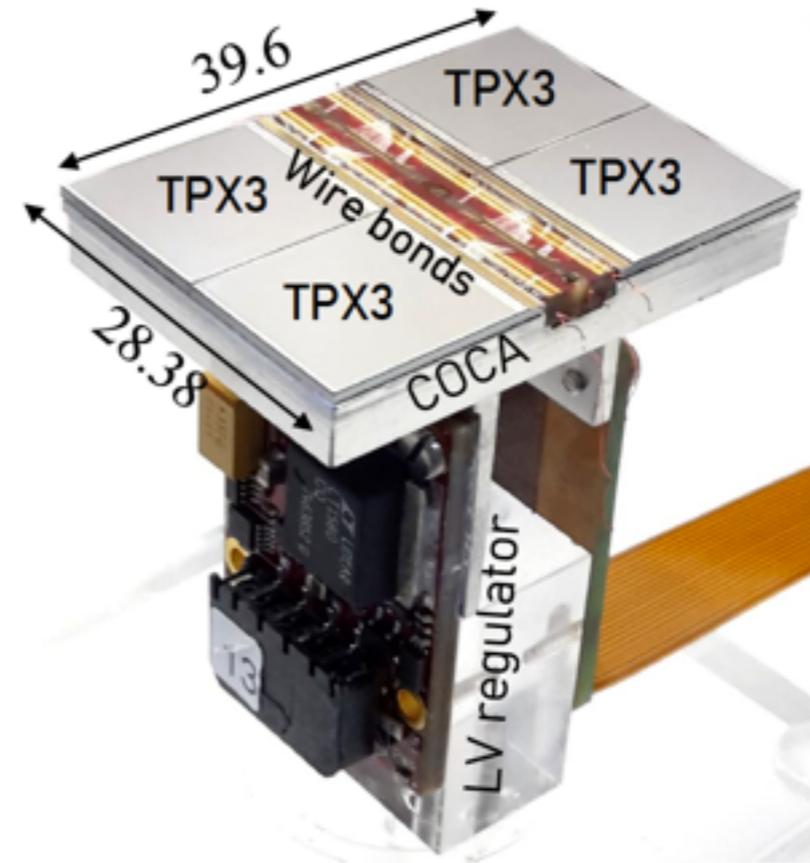
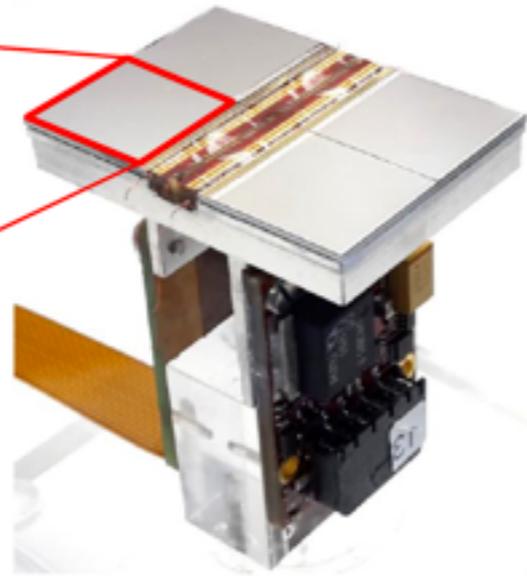
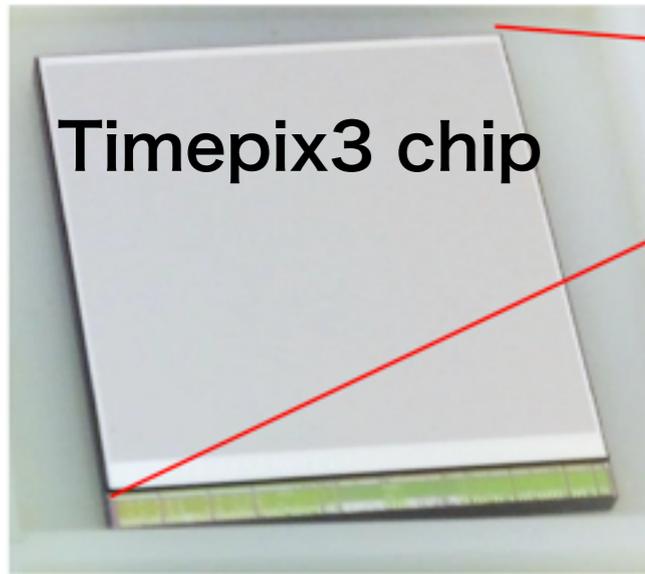


TimePix3 equipped with InGrid

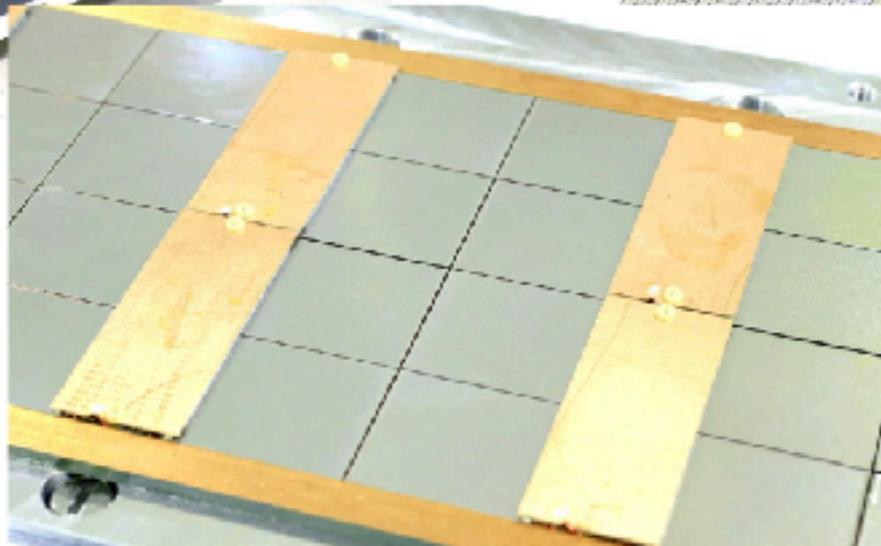
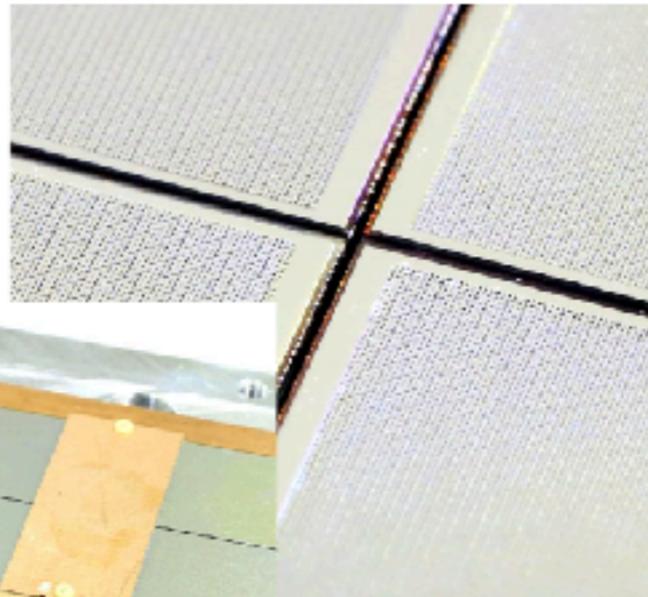
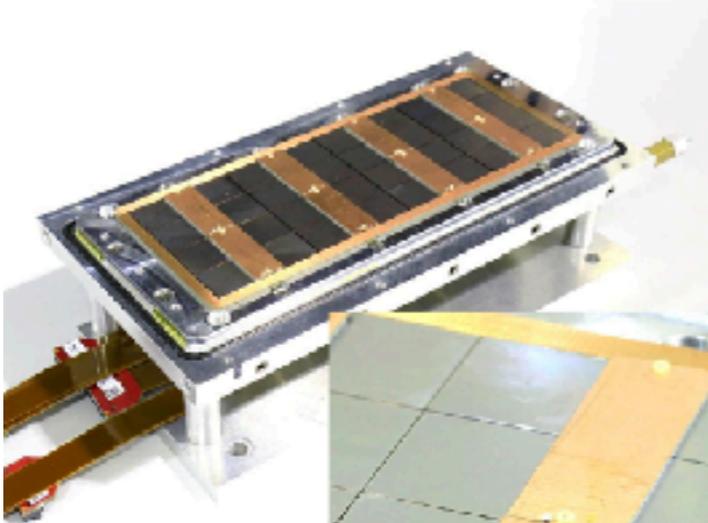
- Aluminium grid (1 μm thick)
- MEMS technology at IZM Berlin
- 35 μm wide holes, 55 μm pitch
- Supported by SU8 pillars 50 μm high
- Grid surrounded by SU8 dyke (150 μm wide solid strip) for mechanical and HV stability



Quad module



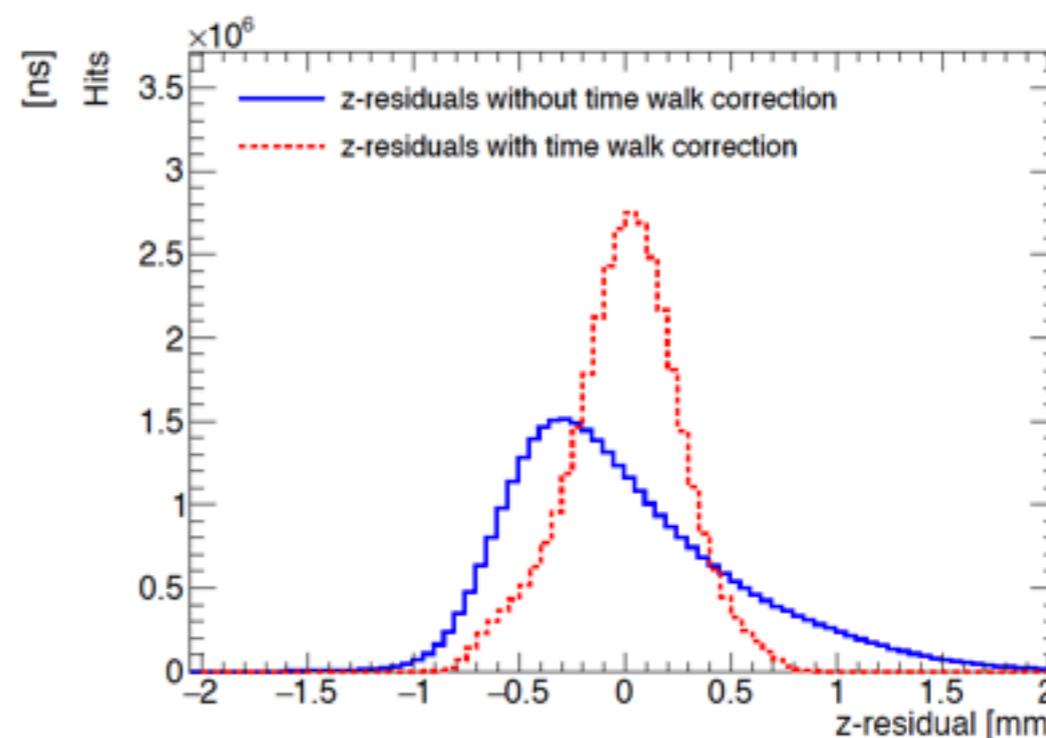
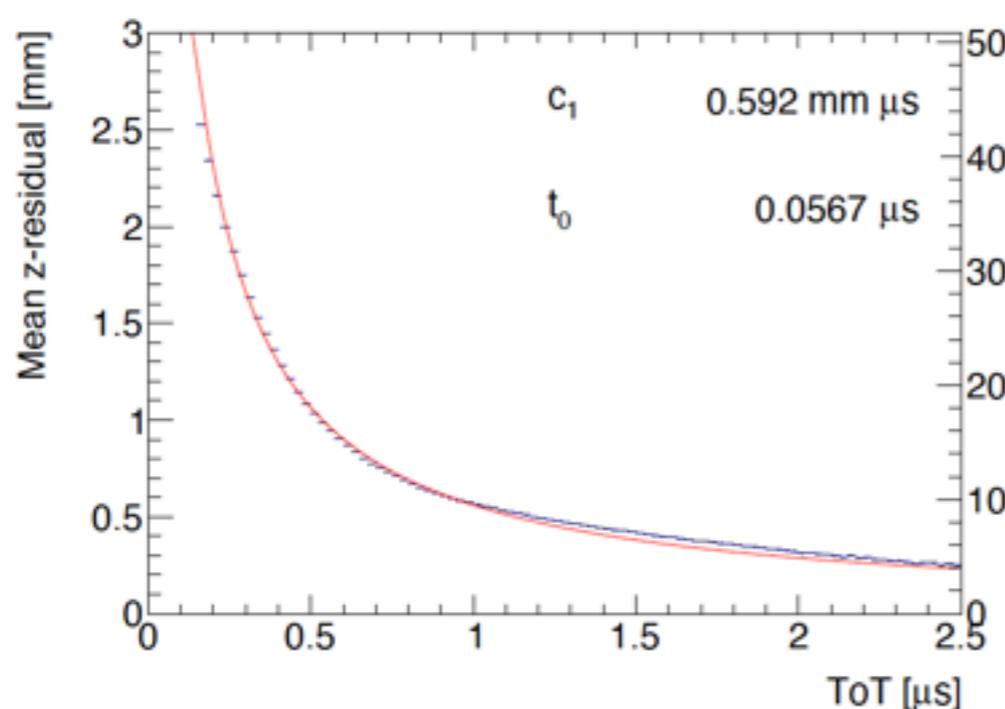
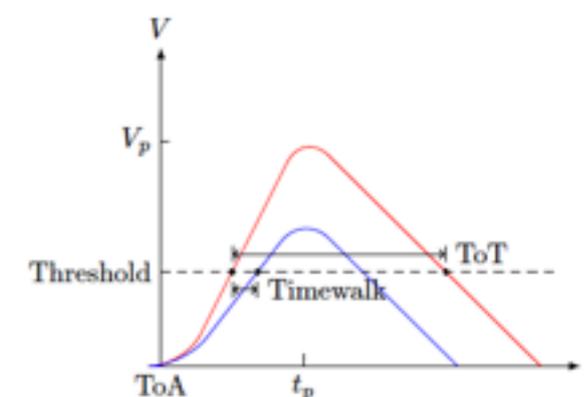
Eight-quad module has been realized



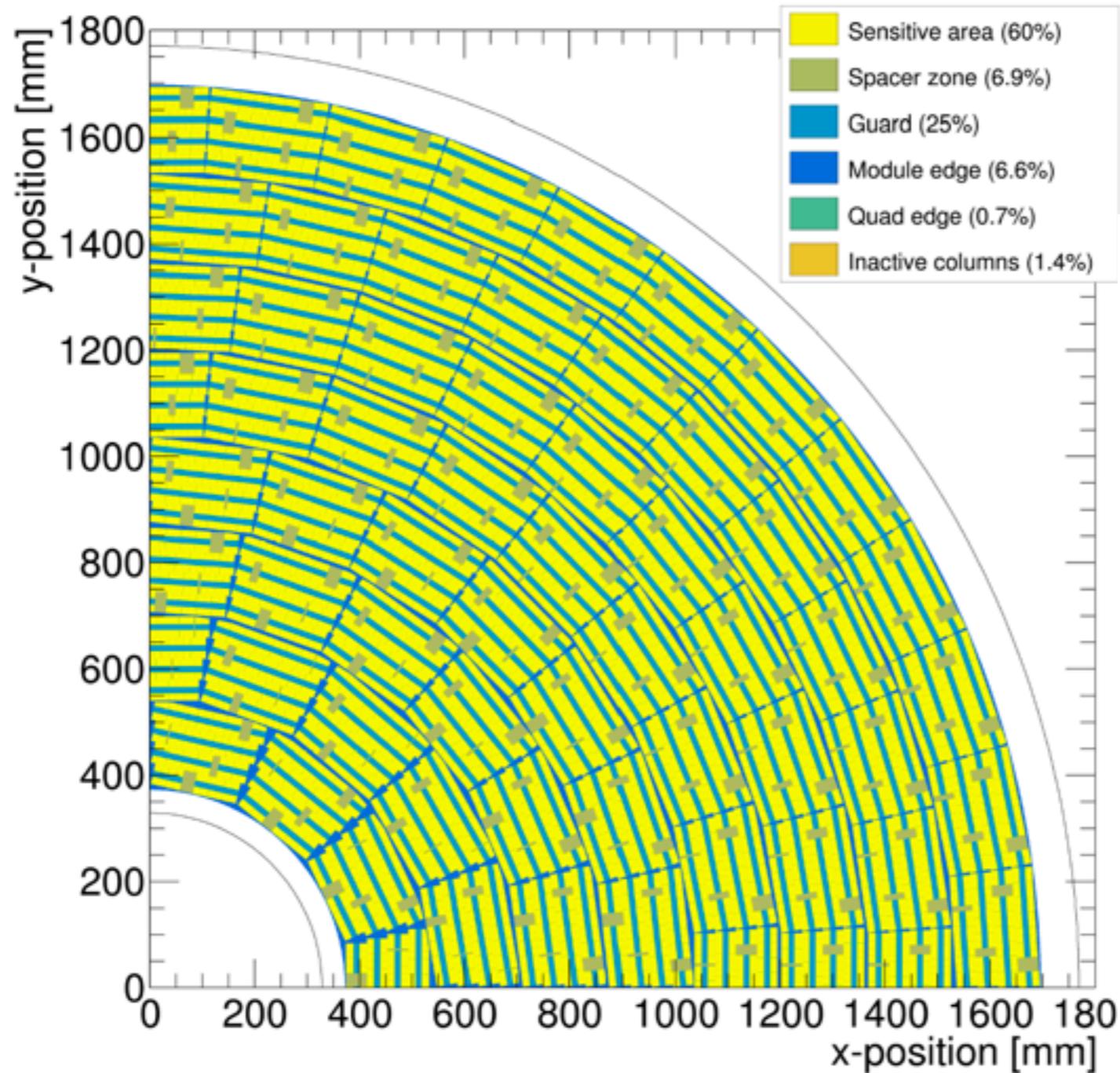
Time corrections

- Time walk occurs when the apparent time of arrival depends on the signal amplitude
- The time walk can be corrected using the Time over Threshold (ToT) as measure of signal strength:

$$\delta Z_{\text{timewalk}} = \frac{c_1}{t_{\text{ToT}} + t_0} + Z_0$$



Tiling of ILD end plate with GridPix quads



Quads module are tiled in fan shape LP1 module (trapezoid)

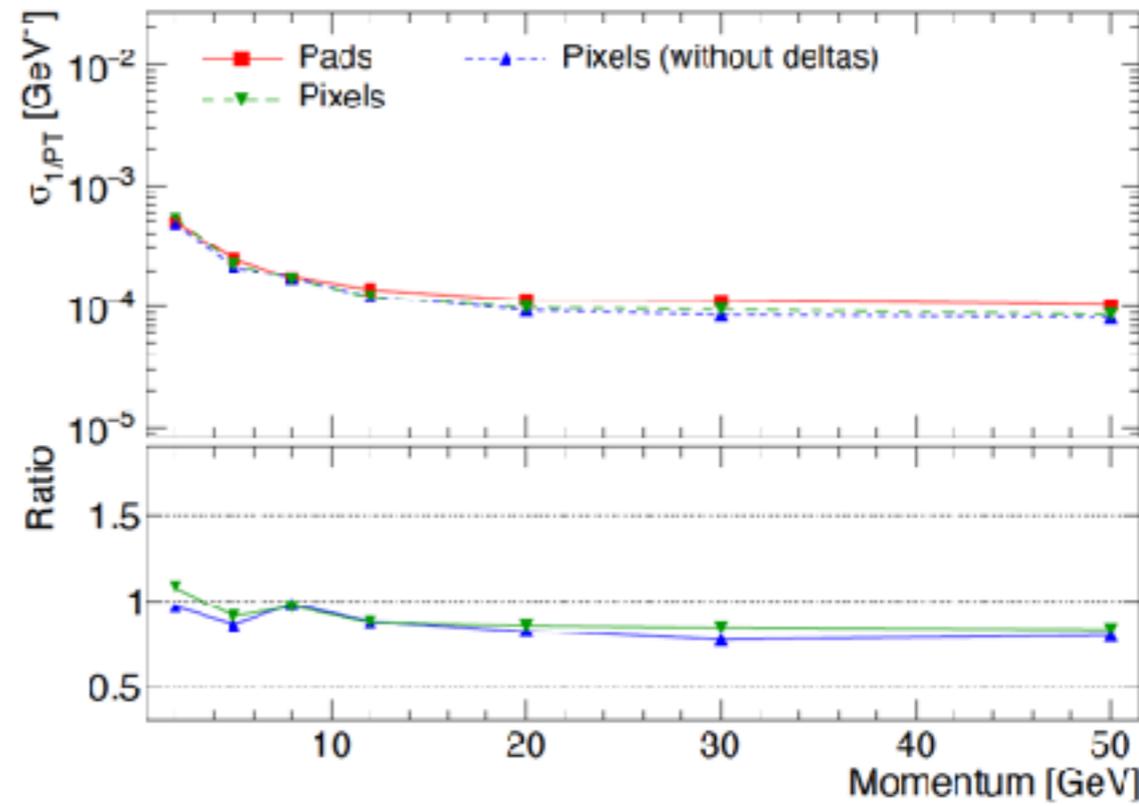
LP1 module shape is originated from pad shape

same dE/dx in each pad at same pad row

all Pixel is identical square shape module must be optimum for pixel

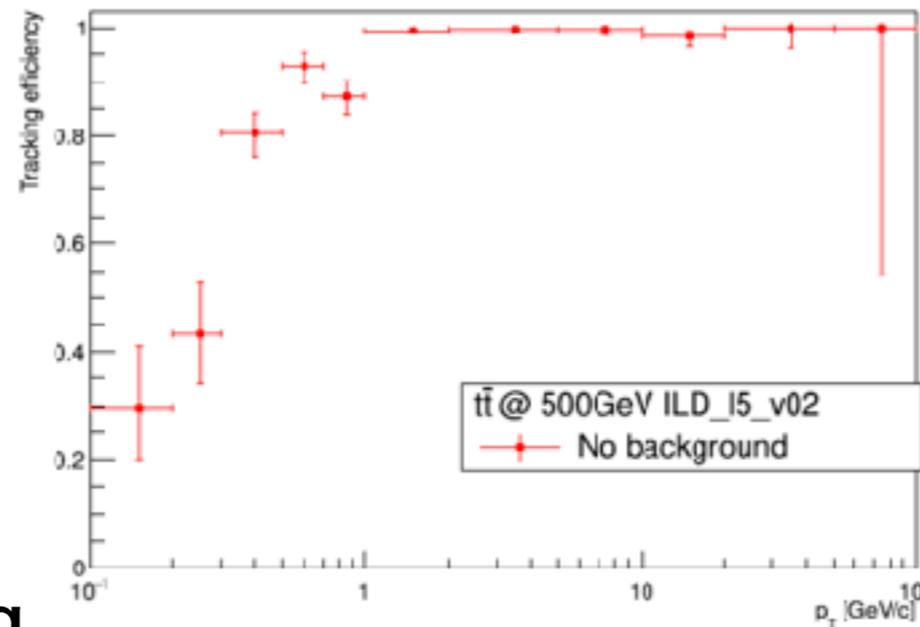
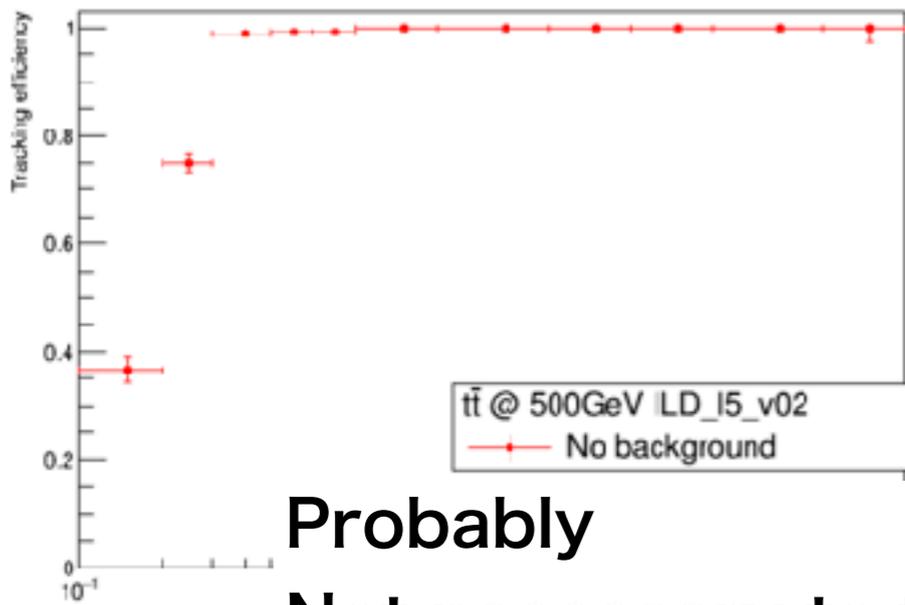
Pt resolution

Pixel provides better than pad



Simulated muons at $\phi = 0.01$ and $\theta = 85^\circ$ with coverage mask

Tracking eff. for tt events



Probably
Not necessary to tiling
Quads in LP1 scheme

Basic performance of Timepix3 Quad module

is quite good

same level with pad module or better

Reconstruction(track finding method) must be renewed

Many room for improvement exist

Many things are waiting for study

Now they are thinking to make Timepix4

enlarge chips -> more sensitive area

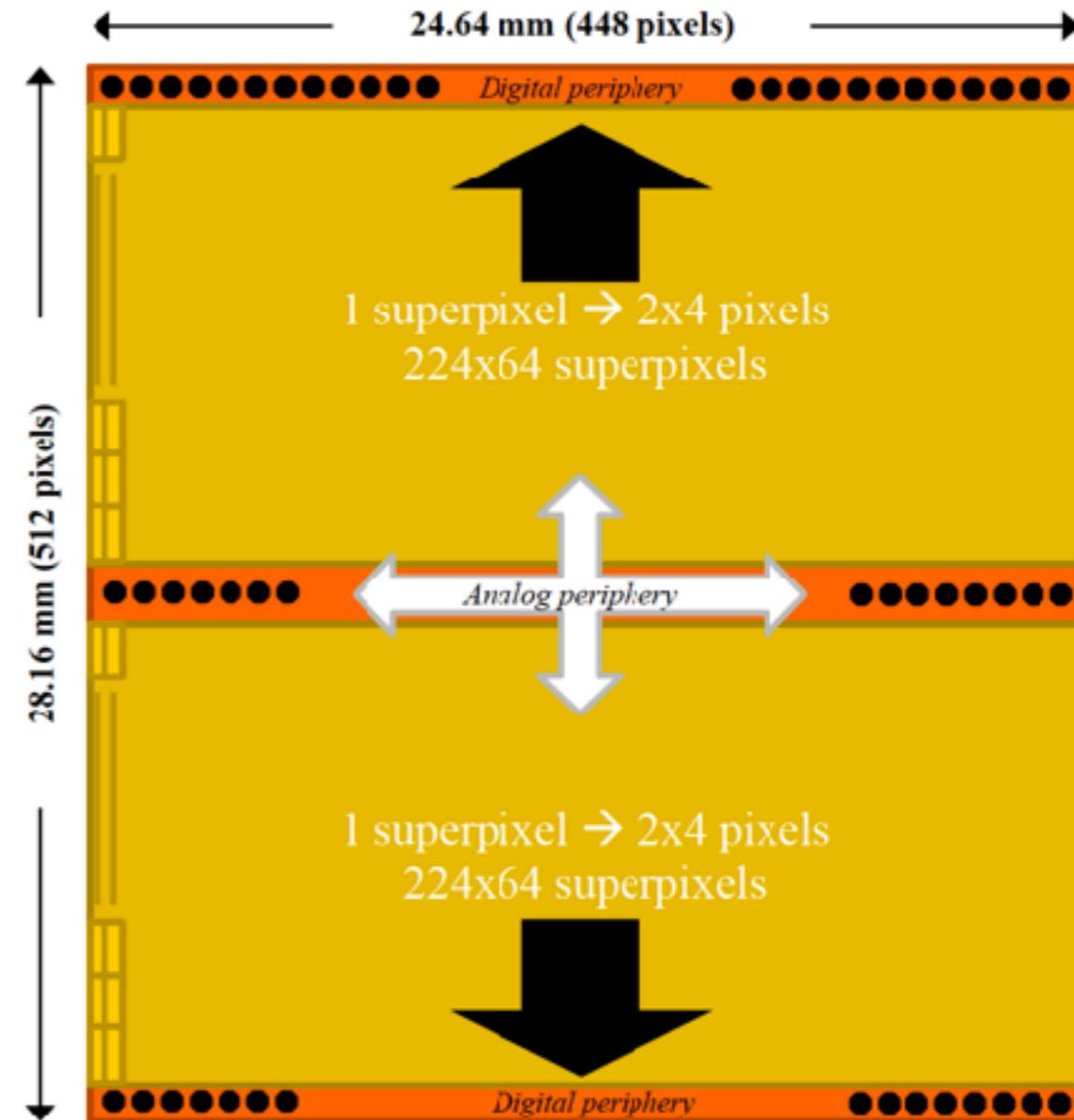
RO speed

but R&D of Si chip cost a lot

tech. is progressing fast

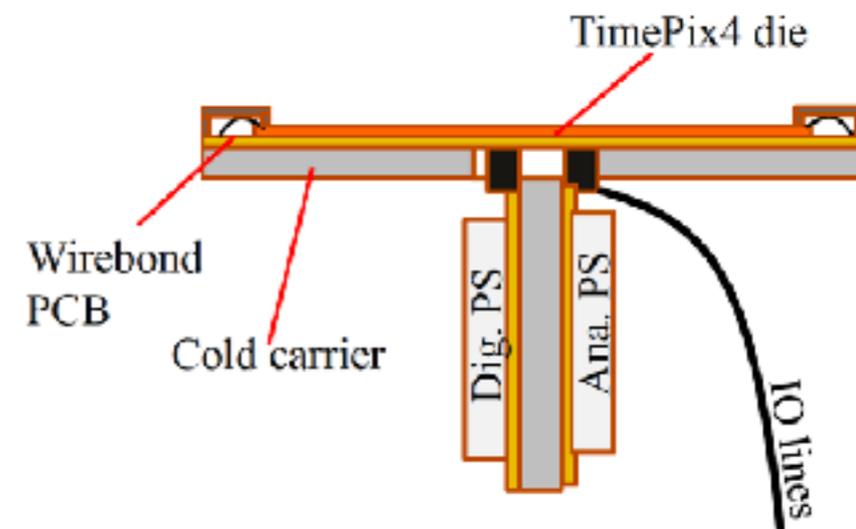
Future development: TimePix4

- Much larger die => 3.5 x active surface of TimePix3
- Same pixel pitch as TPX3 (55 x 55 μm)
- Electronic peripheries also covered with active pixels
- 8 x higher RO speed than TPX3
 - 357.7 vs 45 Mhits/cm²
- Power consumption 0.55 W/cm²
 - (TPX3: 0.7 W/cm²)
- Straight forward DAQ
 - Data driven, sparse RO
 - 64 data word per hit
 - Up to 160 Gbps => 10.8 kHz/pixel
- Just submitted, first (diced) chips expected end January 2020



Fred Hartjes

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Summary

It's difficult conclude

This is rather personal comments but

Pixel TPC seems to be realistic now
conventional technology (GEM, Micromegas) is better ??
has any advantages ??

ADC-> Pwr consumption -> cooling

Pads need new electronics(cost ?)

Pixel is just beginning of realization stage

real difficulties may appear later ... ??

Pixelized gas detector -> innovation,

Gate is necessary for any case at ILC.