Vertex Detector

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ILC Summer Camp 2020

Belle II / KEK

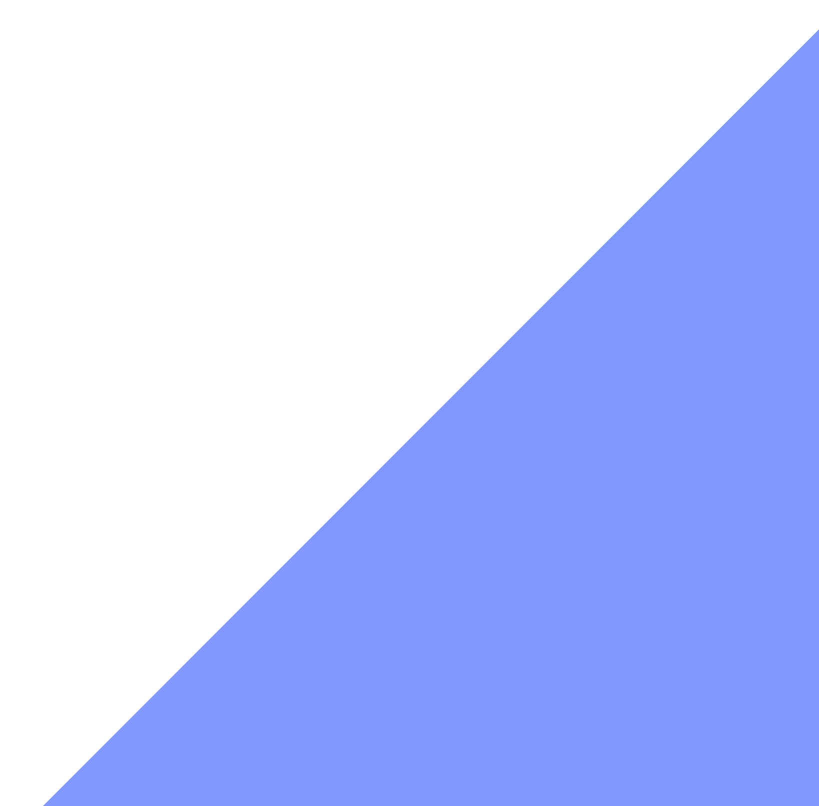
Outline

0. Objective
1. Introduction
   1. What is vertex detector?
   2. Why vertex detector? Flavour tagging
   3. Matters to be considered
2. Working principle
   1. Position measurement
   2. Semiconductor
      1. Energy band in a crystal
      2. Building blocks for high functionality (diode, sensor ,transistor)
      3. Several semiconductor processes to add new structures
3. Candidates for ILD vertex detector
   1. ILC specific requirements
   2. MAPS
   3. FPCCD
   4. DEPFET
   5. SOFIST
4. Summary

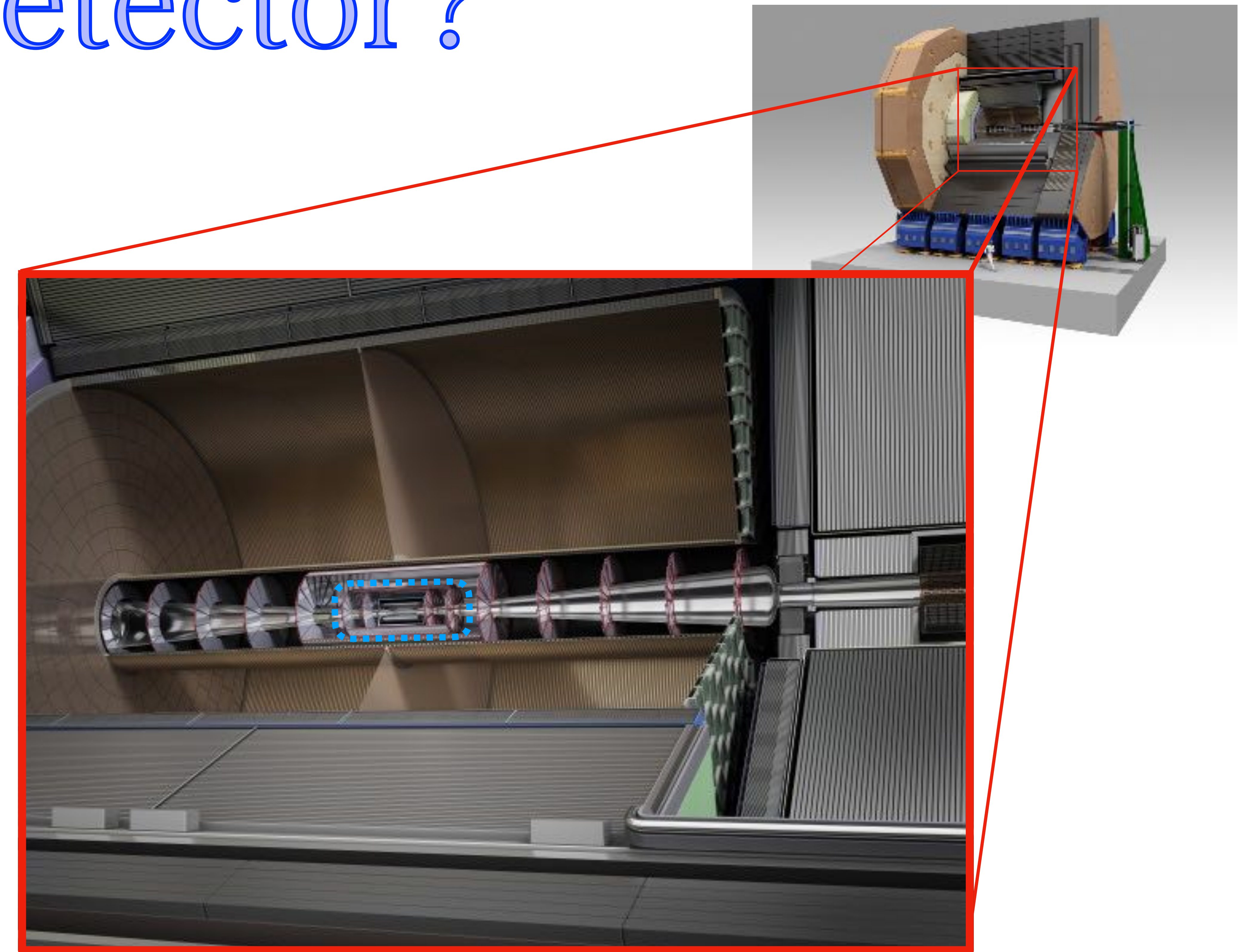
Objective

1. Develop a basic understanding of vertex (semiconductor) detectors
2. Introduce further readings

Introduction



What is vertex detector?



Innermost detectors :
Designed to identify track origins

Key role :
Flavour tagging (b-quark, c-quark tagging)

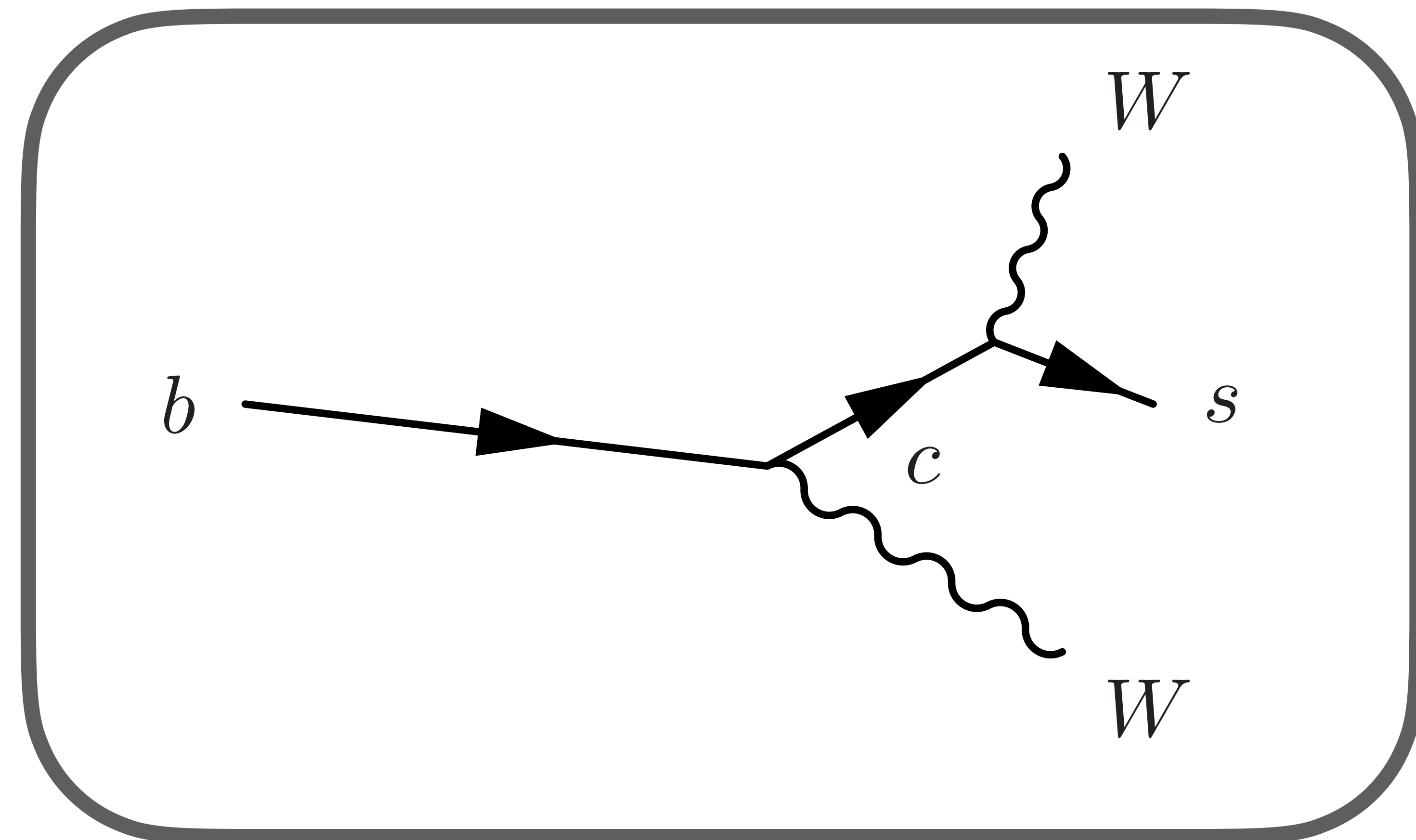
Why flavour tagging is important?

Heavy flavour quark tagging (Quark pair production, Higgs branching ratios)
Higgs tagging (ZHH, ttH, …)

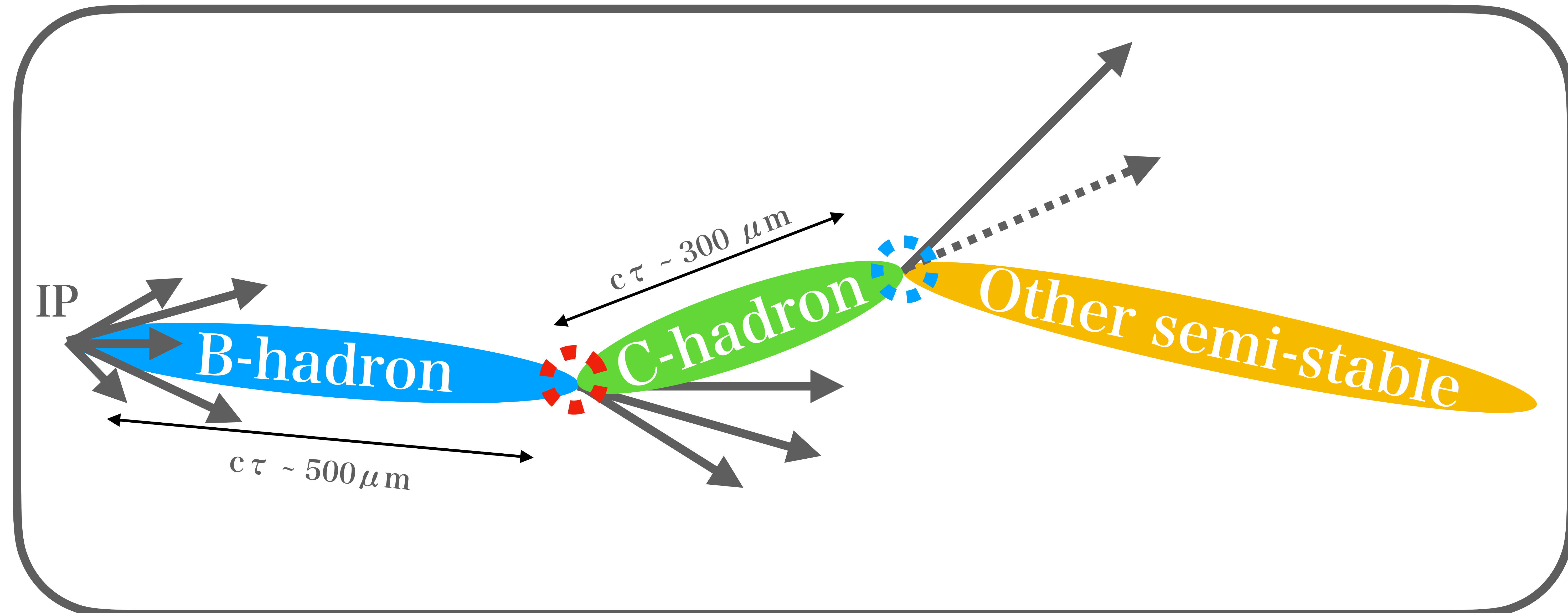
Vertex detector : position measurements closest to IP

Principle of flavour tagging

b-quark decay diagram

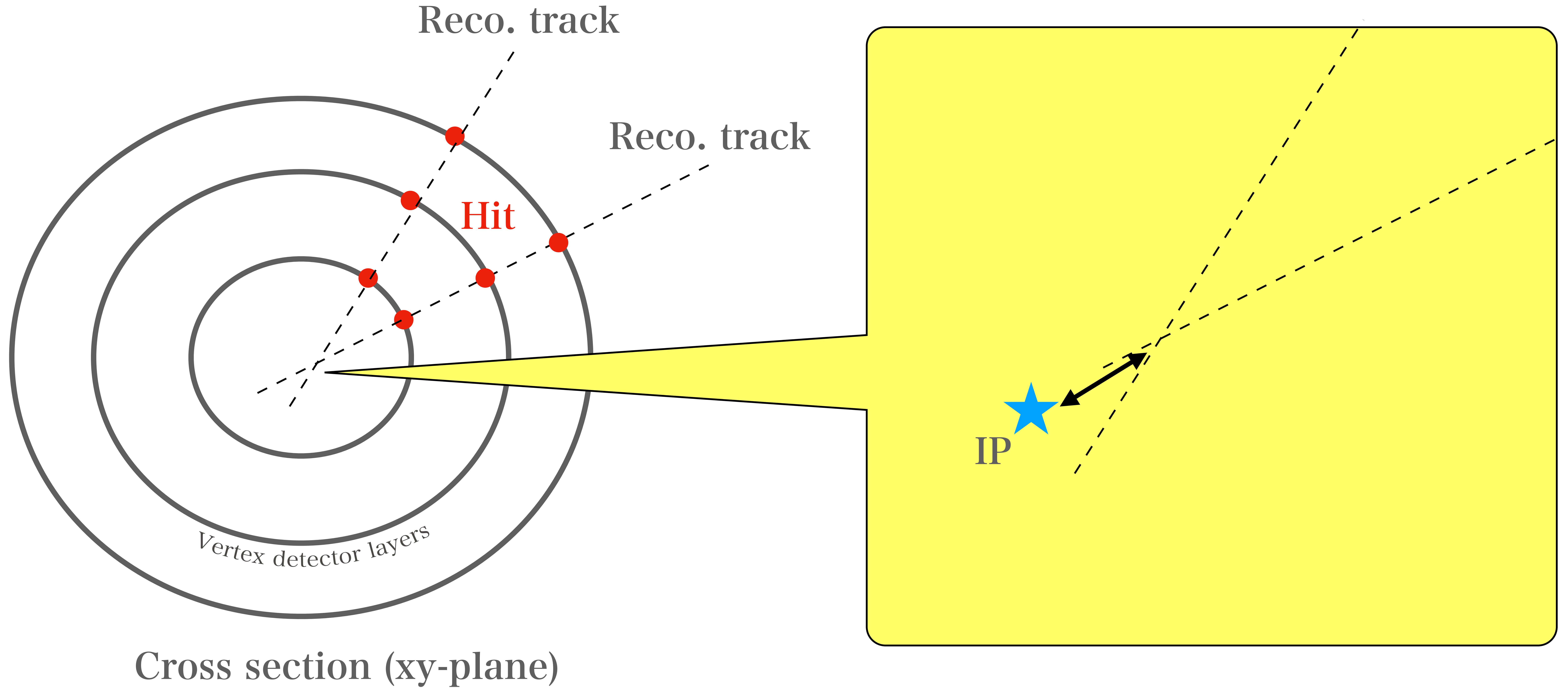


schematic event signature



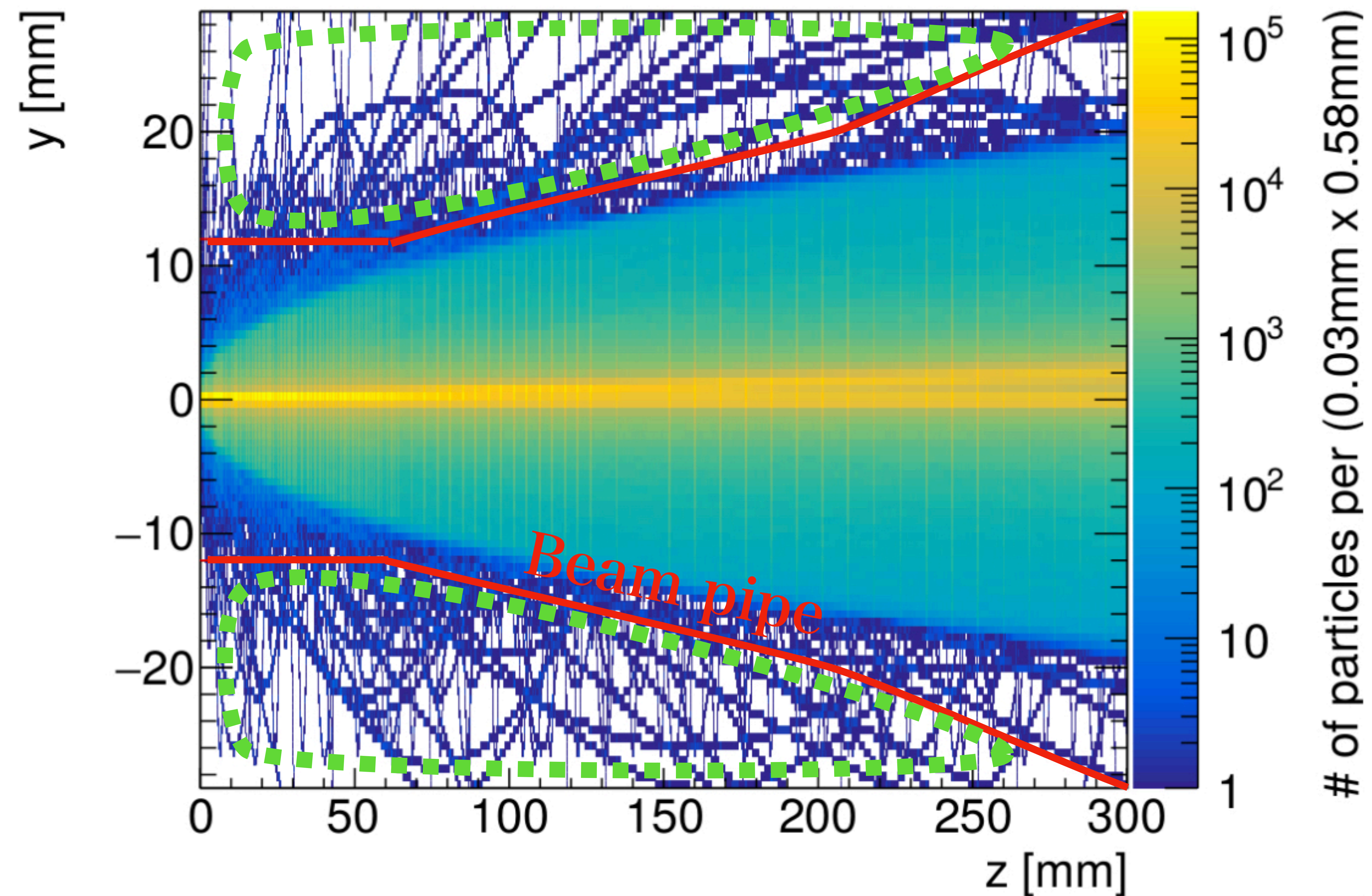
Key: Find vertices away from IP (secondary-, tertiary- vertices)

Schematic View of Vertexing



Higher point resolution and smaller radius are preferred for vertexing

Beam background



Trajectories of the pair background particles

MC simulation (GuineaPig)
500 GeV beam parameter
5T (SiD), 1 bunch crossing

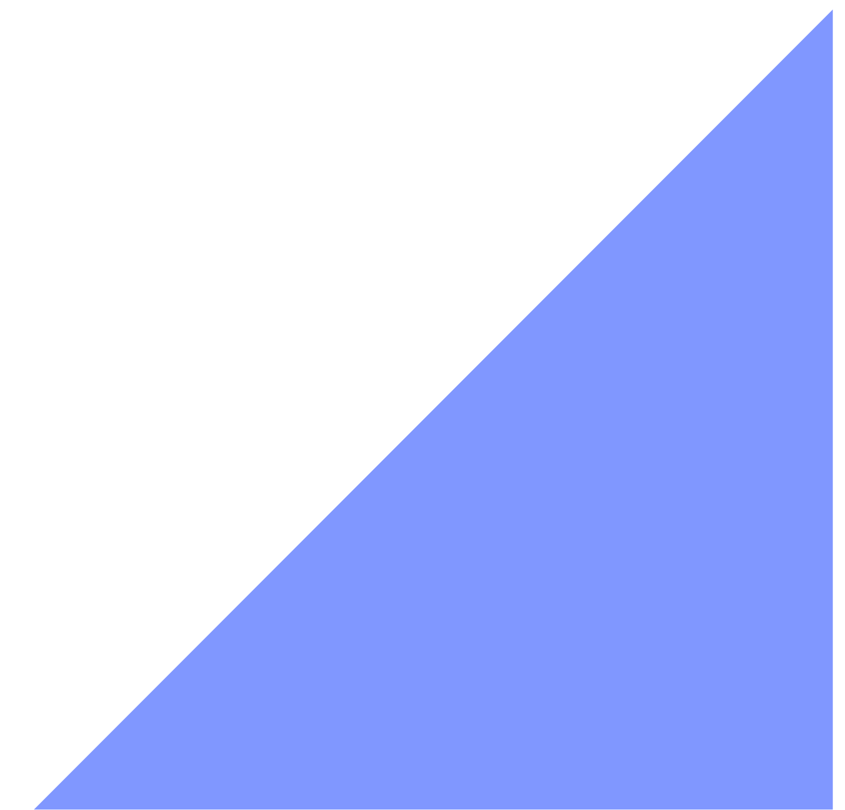
Smaller radius —> Larger beam background

Matters to be considered for vertex detectors

In general

- Spatial resolution,
- Time resolution (time stamping for assigning a particular bunch crossing—>This reduces background),
- Readout speed
- Material budget (minimize multiple Coulomb scattering),
- Radiation tolerance,
- Occupancy (most sensitive to beam-induced background, readout speed)
- Power consumption and cooling
- SN

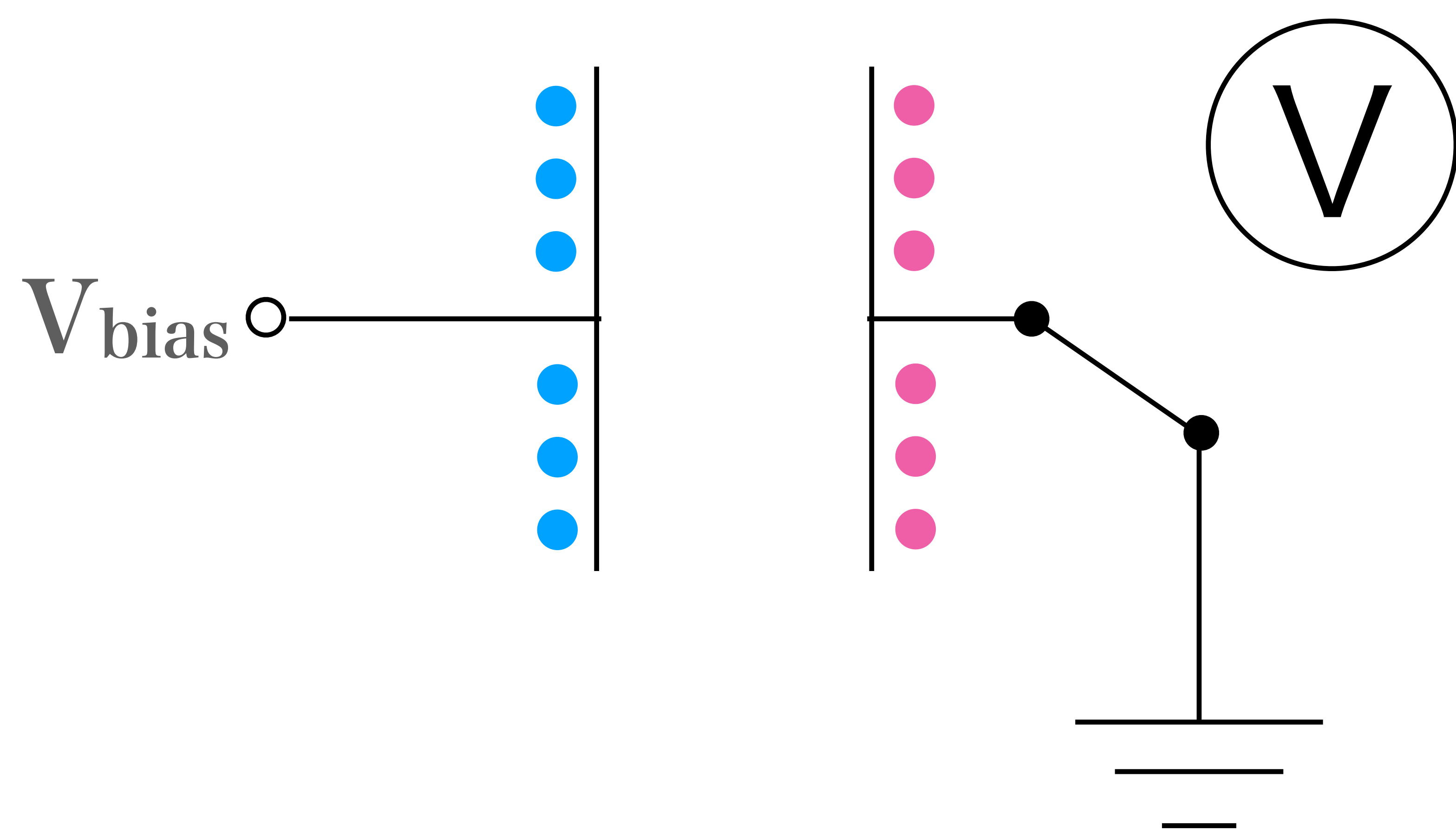
Working principle



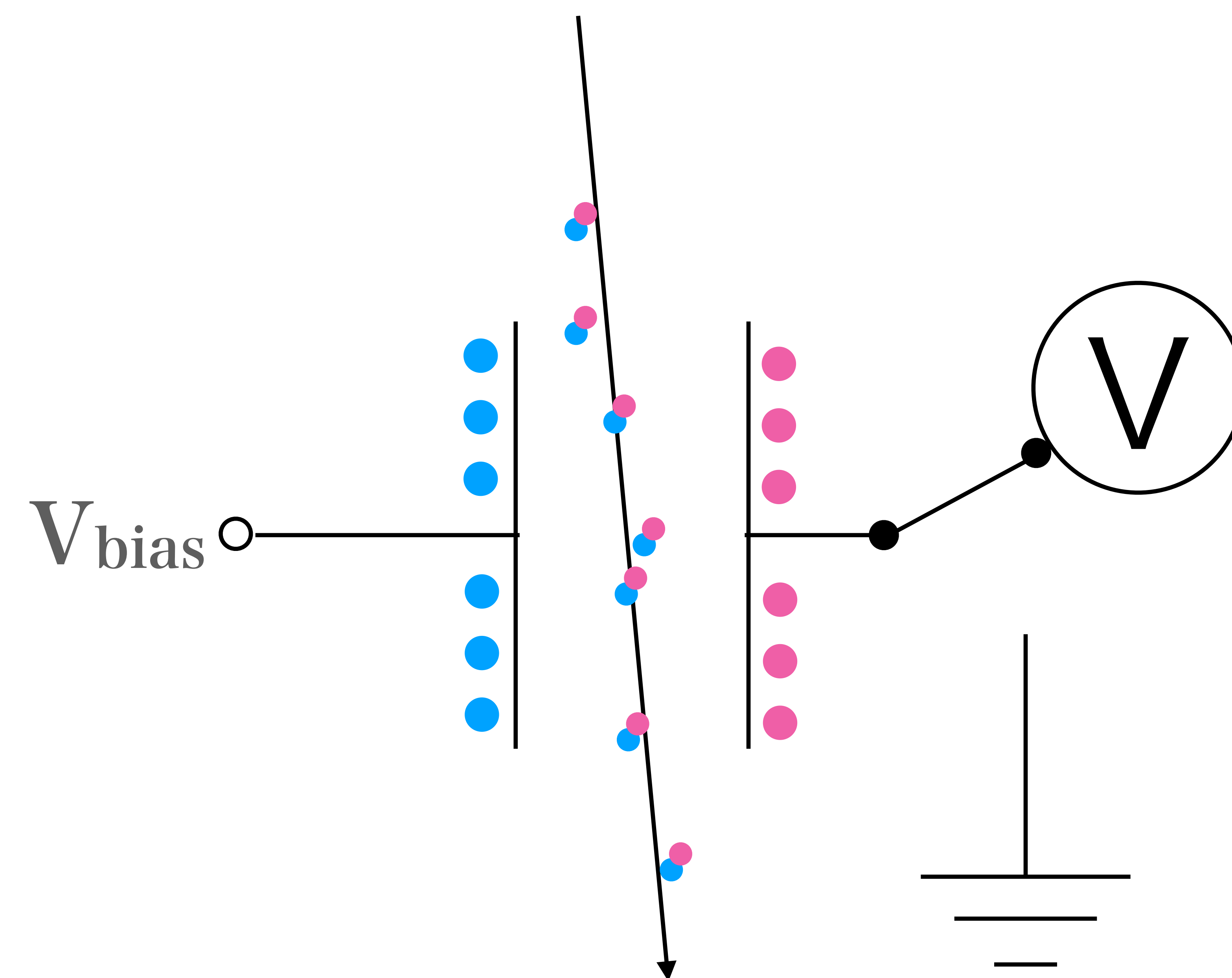
Detection Principle

Basic idea : Ionization chamber (or capacitor)

Apply electric field

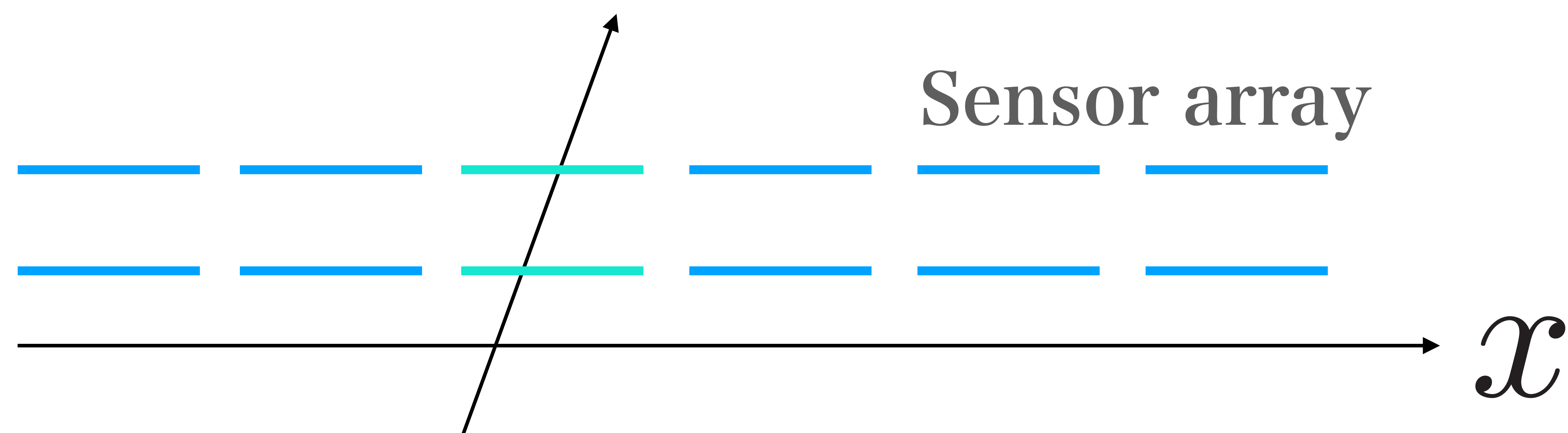


Read slight changes of charges



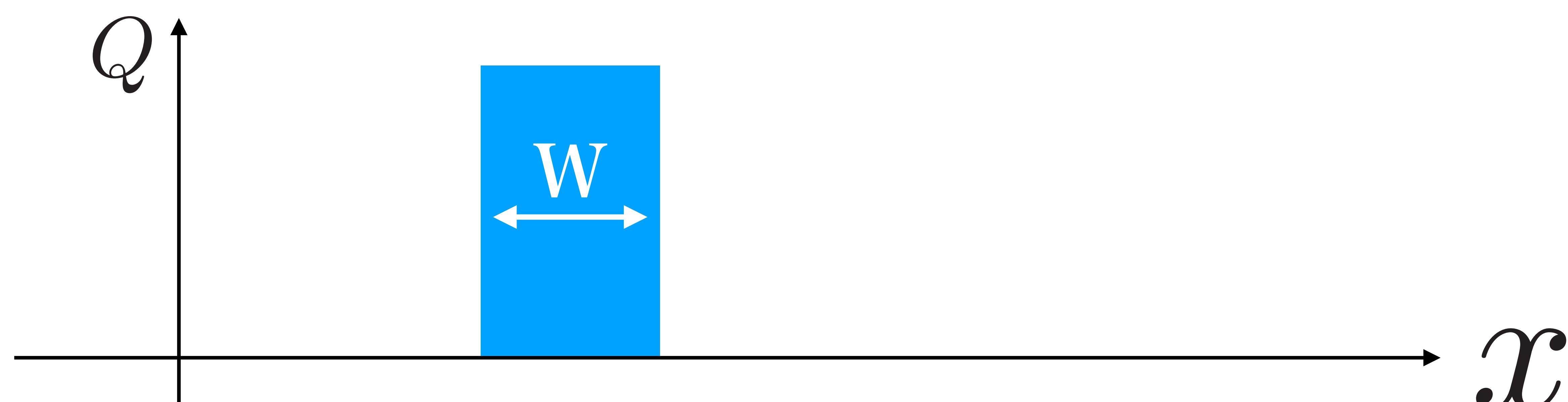
Sensor <—> Capacitor

Position Measurement



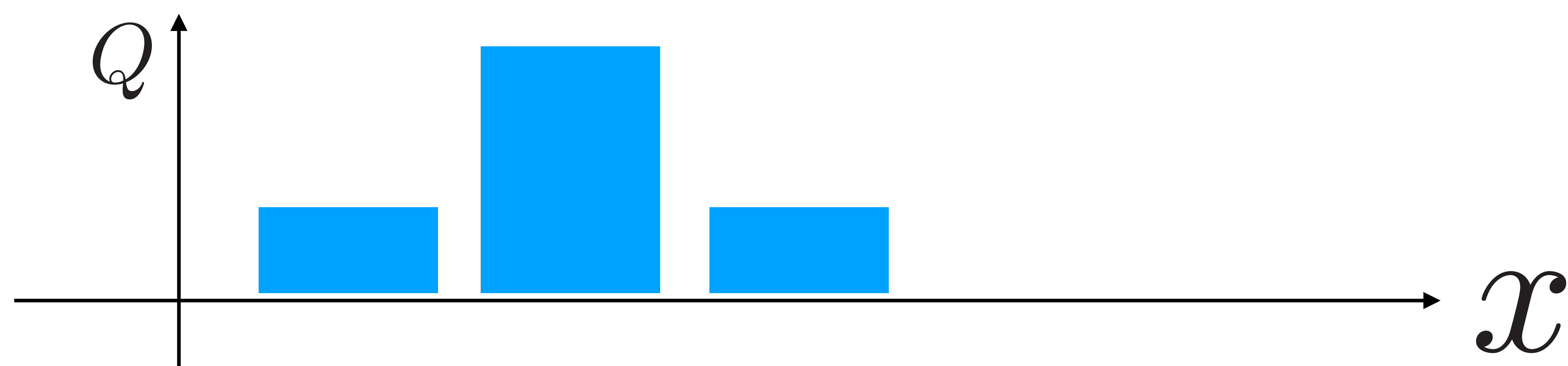
Position measurement from hit sensor ID

(Alignment and calibration are crucial)



Spacial resolution for single hit

$\sigma = W/\sqrt{12}$



Spacial resolution for multiple hits

Charge centroid method

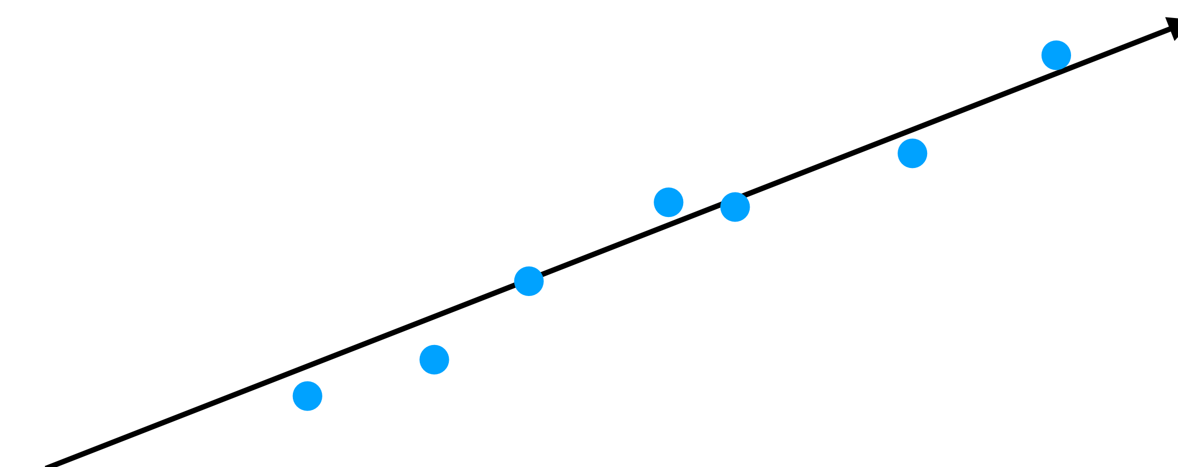
—> Much better resolution than "$W/\sqrt{12}$"

Sensor width does not always limit spatial resolution

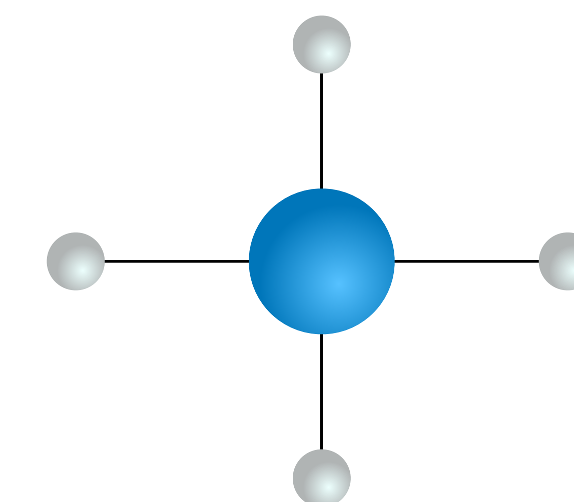
Semiconductor

Low ionization potential

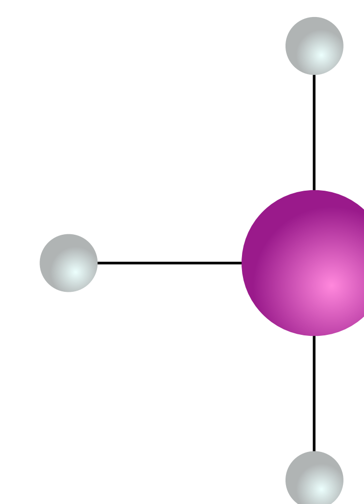
Typical energy to create an electron-ion pair in Ar gas ~ 30 eV
Semiconductor lowers down to a few eV —> Efficiently create e-h pairs

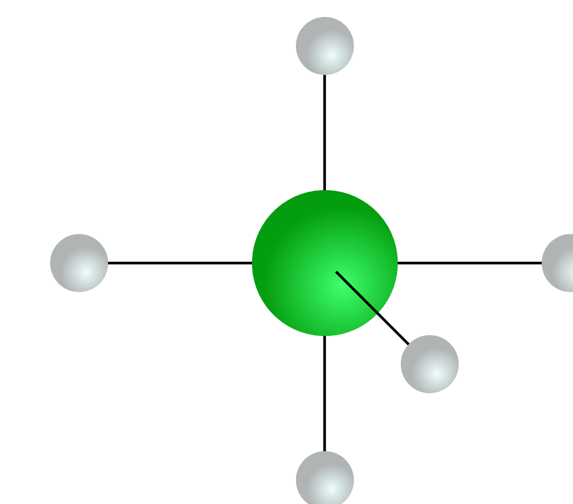


Semiconductor is based on single-crystal quadrivalent atoms e.g. Ge, Si, C



Conductivity can be controlled by doping trivalent(P-type) or pentavalent(N-type) atoms

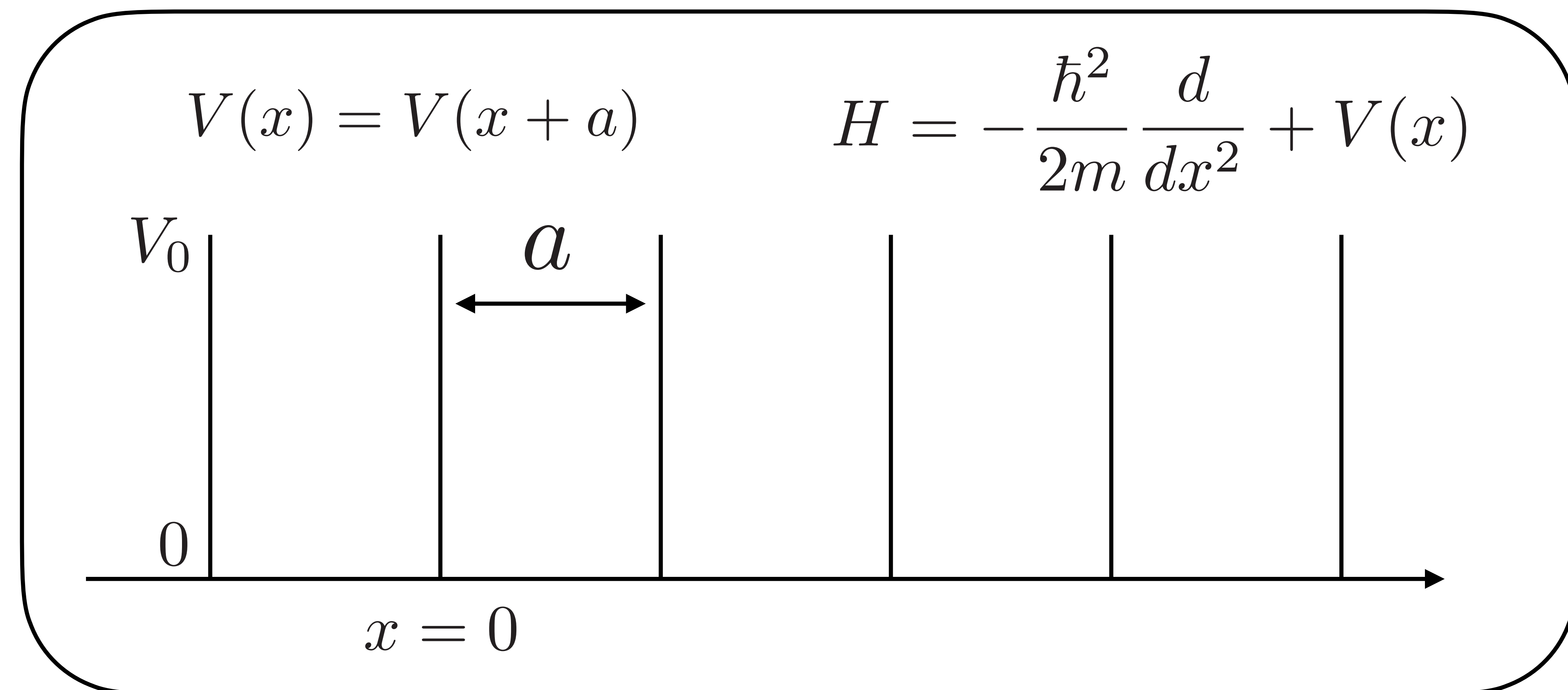




Why is the ionization potential in semiconductor low?

Periodic δ-function potential (Kronig-Penney model)

Reference:「半導体の物理」西澤潤一編　御子柴宣夫著



If a function $u(x)$ satisfies $Hu(x) = Eu(x)$,
then $u(x+a)$ is also another solution
Considering a phase factor, it can be written as:

$$u(x+a) = e^{i\theta}u(x)$$

General solution in:

1) $0 < x < a$

$$u(x) = Ae^{ikx} + Be^{-ikx}$$

, where $k := \frac{\sqrt{2mE}}{\hbar}$

2) $-a < x < 0$

$$u(x) = e^{-i\theta}u(x+a) = e^{-i\theta}\left(Ae^{ik(x+a)} + Be^{-ik(x+a)}\right)$$

3) The solution at $x = 0$ can be derived from the two solution above:

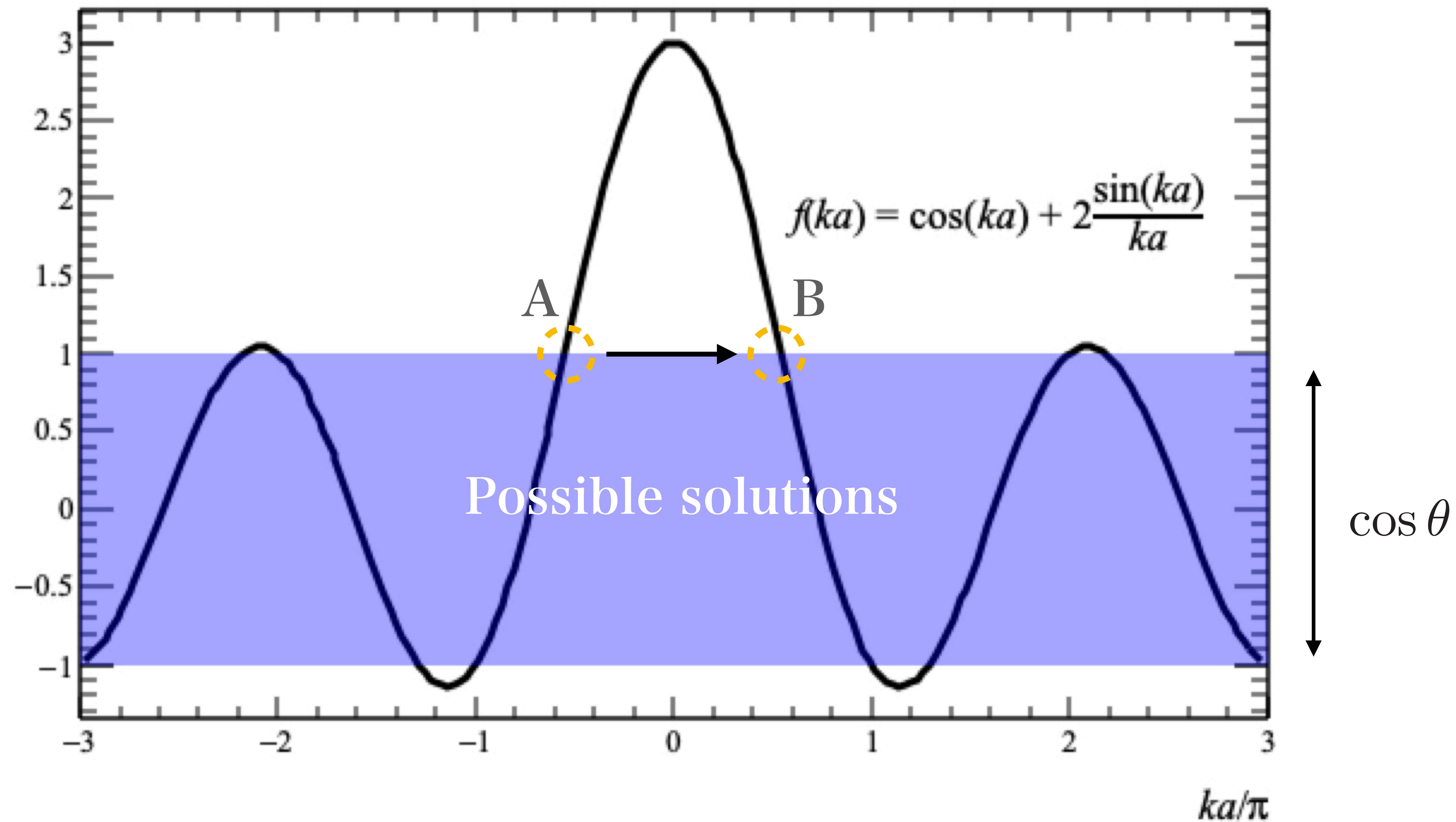
Integrate both sides of $Hu(x) = Eu(x)$ from $-\epsilon$ to ϵ

$$\int_{-\epsilon}^{\epsilon} dx \left[-\frac{\hbar^2}{2m}\frac{du(x)}{dx^2} + V_0\delta(x)u(x)\right] = -\frac{\hbar^2}{2m}\left(\left.\frac{du}{dx}\right|_{x=+\epsilon} - \left.\frac{du}{dx}\right|_{x=-\epsilon}\right) + V_0 u(0) = 0$$

These solution must be continuous around $x = 0$ —> $\cos\theta = \cos ka + \frac{mV_0}{\hbar^2 k}\sin ka$

Note that there may be no solution for certain θ

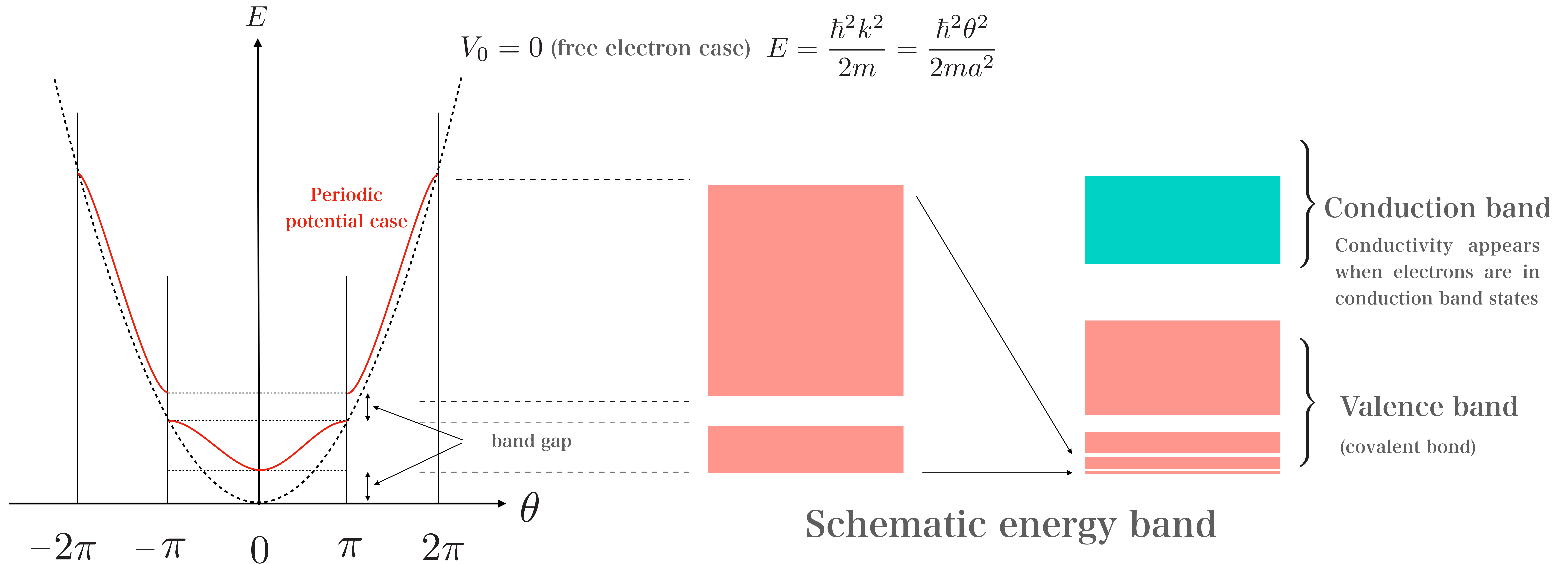
Energy band and band gap



Transition from A to B corresponds to a jump from the view point of energy

$$\left(E = \frac{\hbar^2 k^2}{2m} \right)$$

Valence band and conduction band



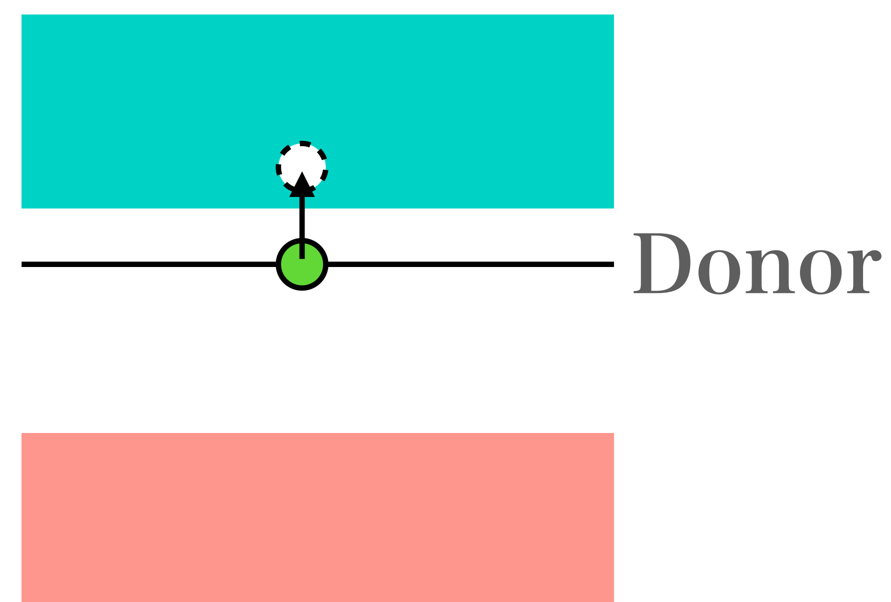
Pursuing "Ideal" energy band is important for good semiconductors

Tidy crystal structure is important (radiation may affect crystal)

Too small band gap between valence and conduction band causes a noise excited by thermal energy

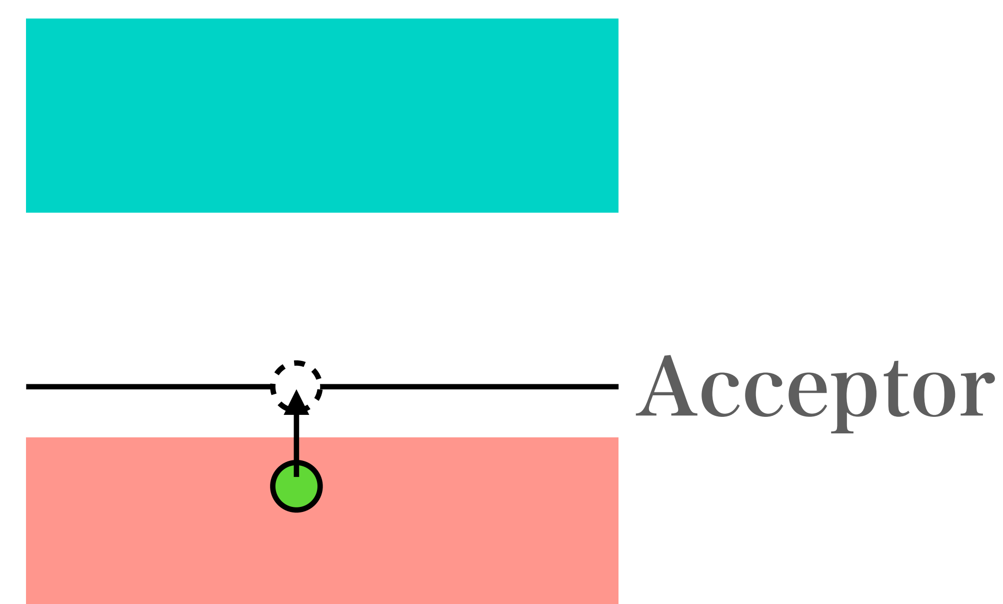
Some impurity (dopant) leads to electrons in conduction band or holes in valence band —> conductivity

N-type and P-type semiconductors



Dopant : Pentavalent atoms

Supplying electrons (charge carrier : electron)

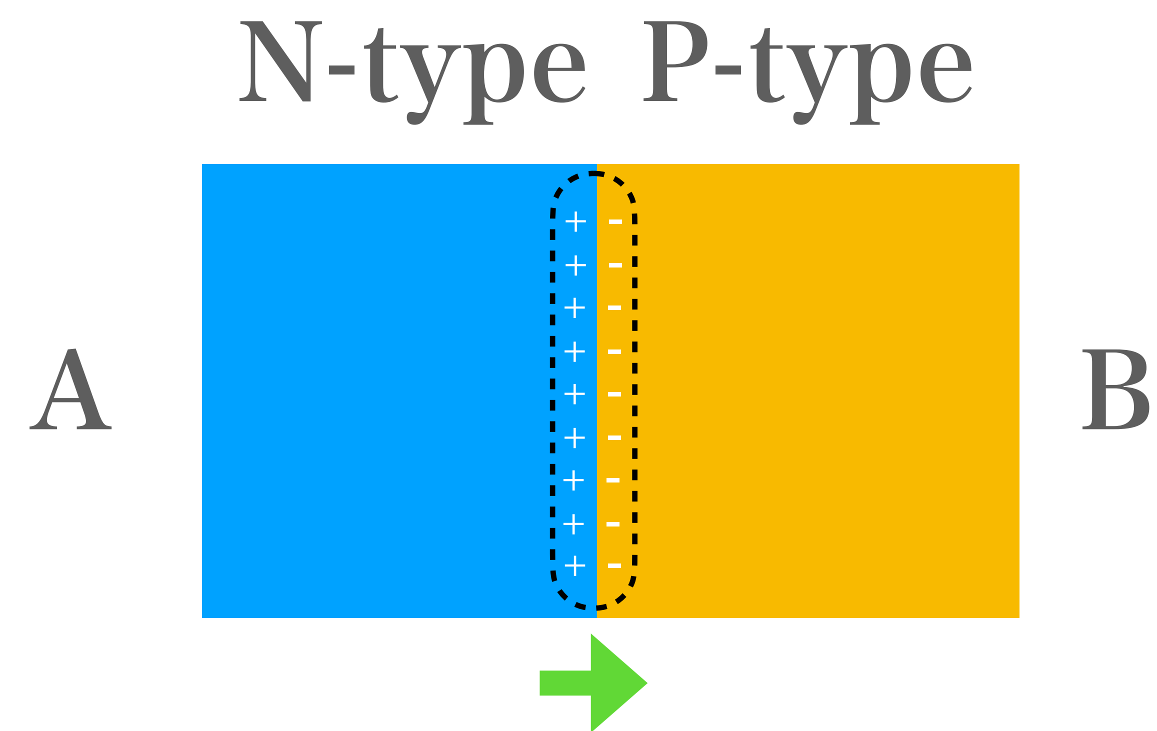


Dopant : Trivalent atoms

Demanding electrons (charge carrier : hole)

Two type semiconductors are essential for many applications

PN junction



Diode as a circuit element

Around the boundary, carriers move and annihilate

—> a region without carriers (=depletion layer)

Depleted P-type semiconductor gets negatively charged
Depleted N-type semiconductor gets positively charged
—> Automatically the move of carriers stops by the self-created electric field

Why is it a diode?

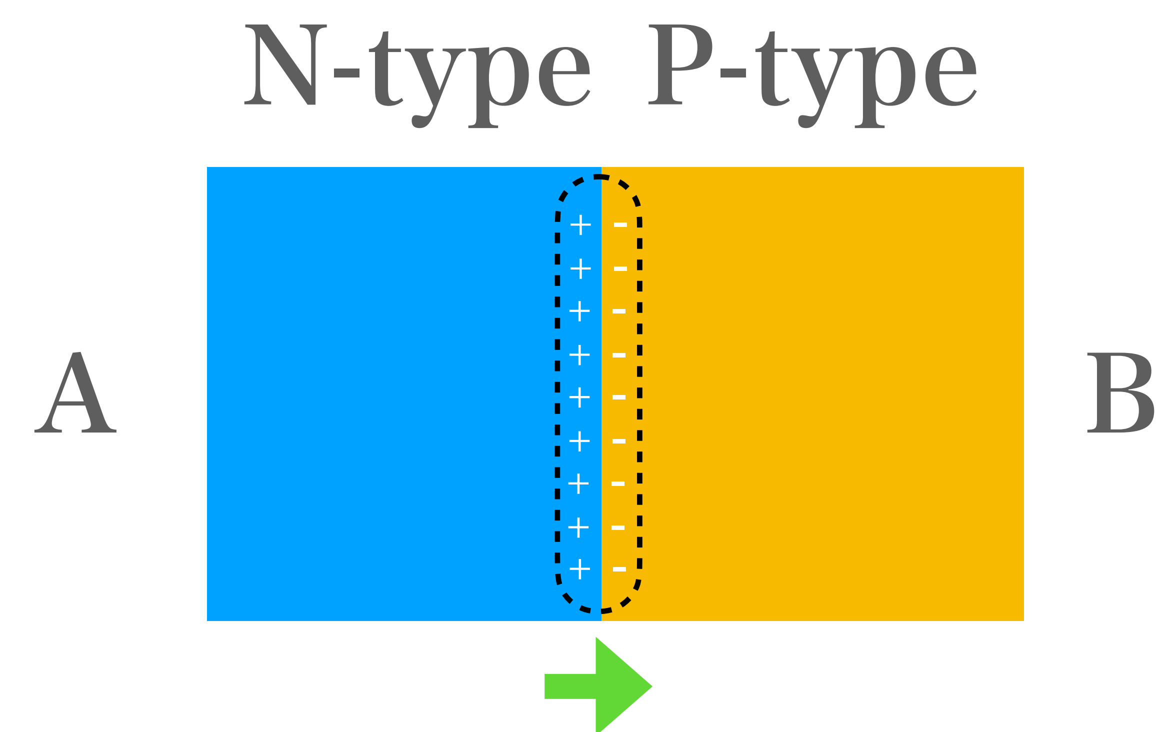
What happens if apply a voltage with A < B (reverse bias)?

—> Electrons move to B, holes move to A
—> Depletion layer enlarges (nonconductive)

What happens if apply a voltage with A > B (forward bias)?

—> Electrons move to A、holes move to B
—> Depletion layer disappear (conductive)

Depletion layer = sensitive volume



Depletion layer forms a capacitor

Deposited energy in depletion layer by incident particles,
carriers can be easily created due to a small band gap

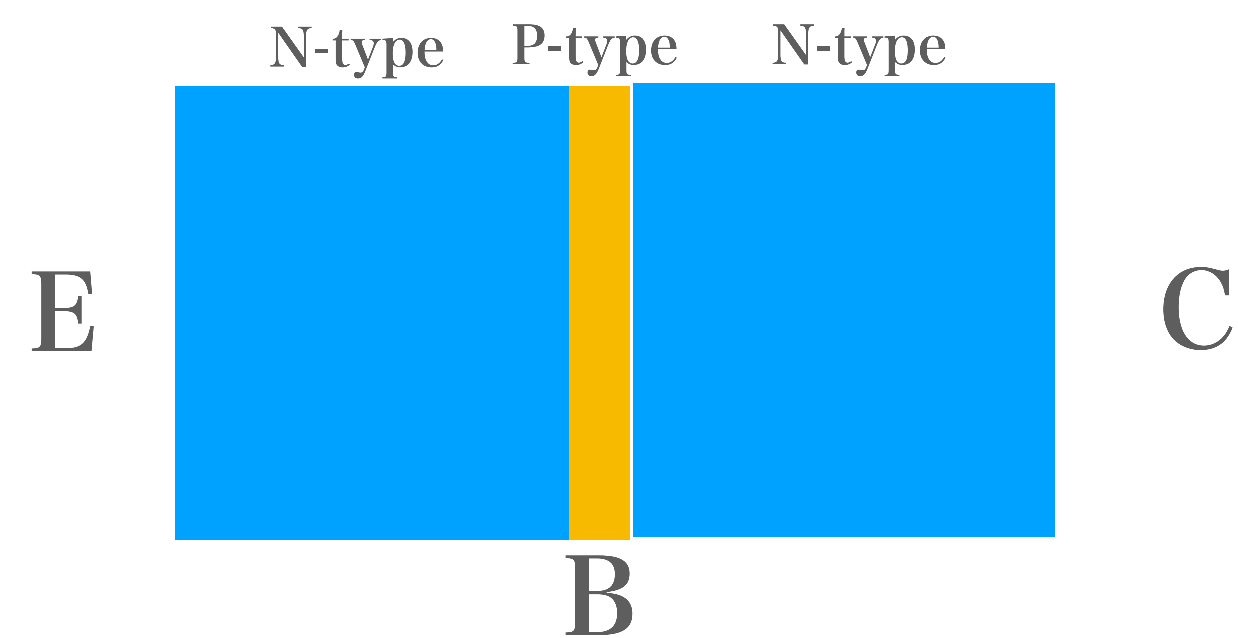
Larger depletion layer enable to create more carriers

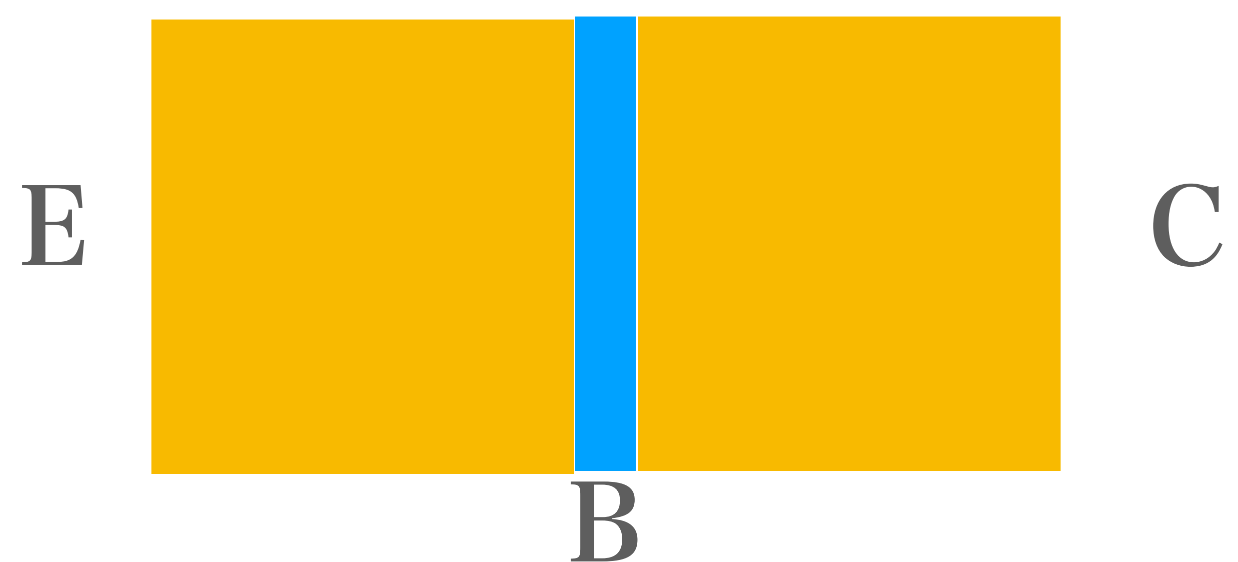
PN junction = Sensor

PNP, NPN junction (Transistor)

Transistor { Bipolar transistor / MOS transistor }

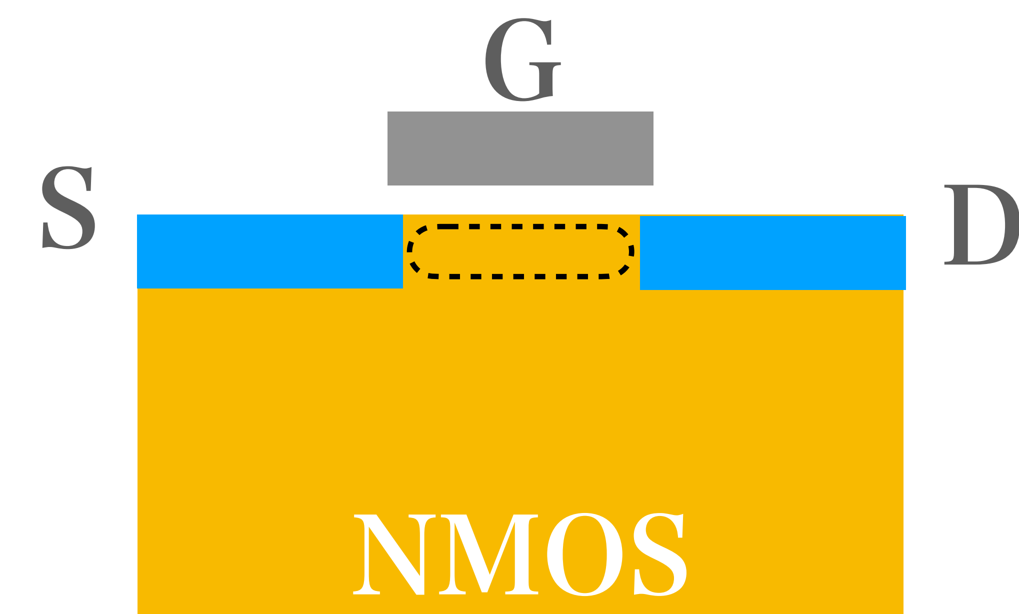
Bipolar transistor

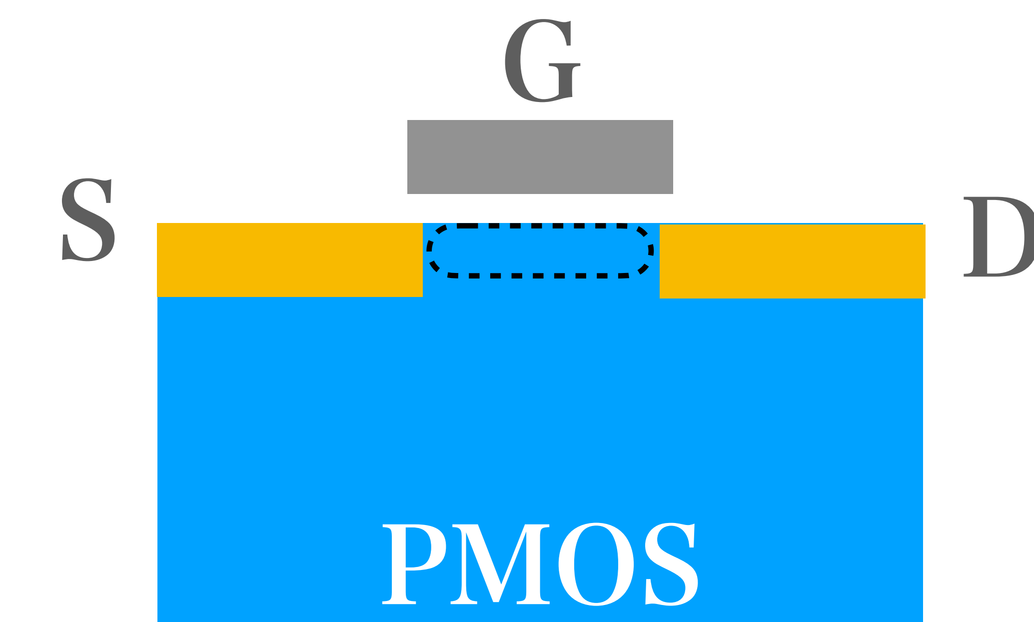




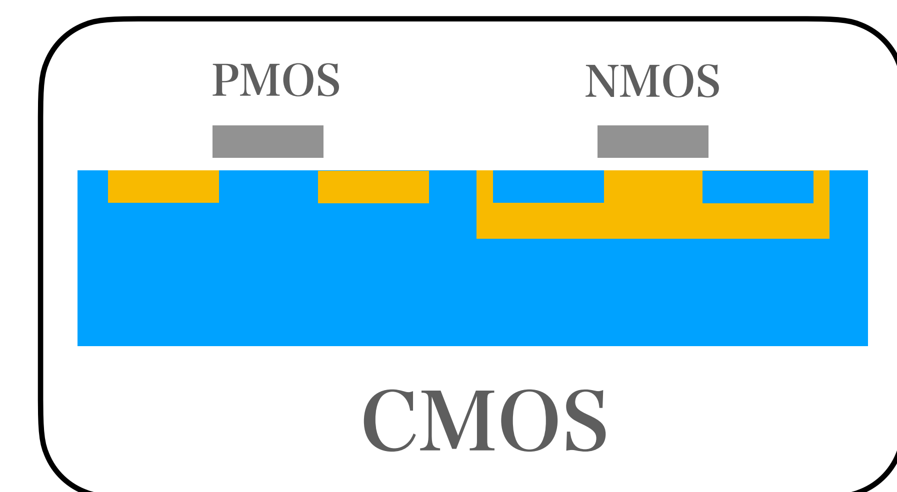
Control E-C conductivity
by a current between B and C

MOS transistor (MOS FET)





Control S-D conductivity
by a voltage of G



CMOS

Transistor = Conductivity controller

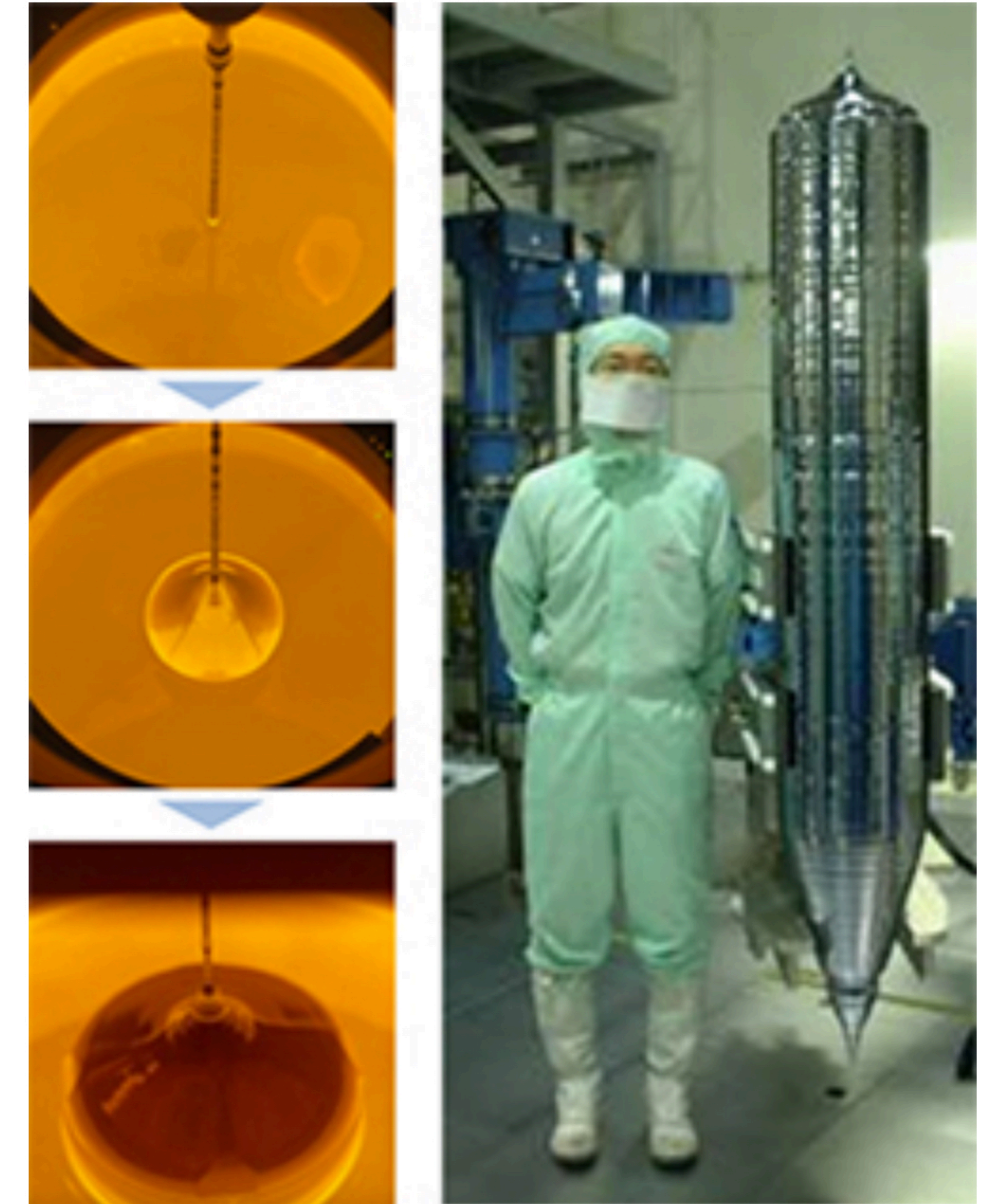
Semiconductor processes (some)

1) Prepare high purity single-crystal substrate (slice : **wafer**)

2) **Ion implantation** : Implant dopants by accelerated ions
   B (P-type), P (N-type), O (insulator)

3) **Photolithography** : A micro-fabrication method using photoresist, of which etch resistance is changed by a light exposure, and printing technology, which realize a reduced-size copy

4) **Deposition** : Methods to produce thin films and coatings
   Evaporation: Evaporating a metal or an oxide and attaching vapor to a substrate
   Sputtering : Colliding accelerated ions with a target metal and attaching ejected metal to a substrate
   Epitaxial growth : Forming additional crystal layers with a well-defined orientation w.r.t a substrate
   Stacking layers enable us to make 3-dimensional structures



https://yab.yomiuri.co.jp/adv/wol/opinion/science_180903.html

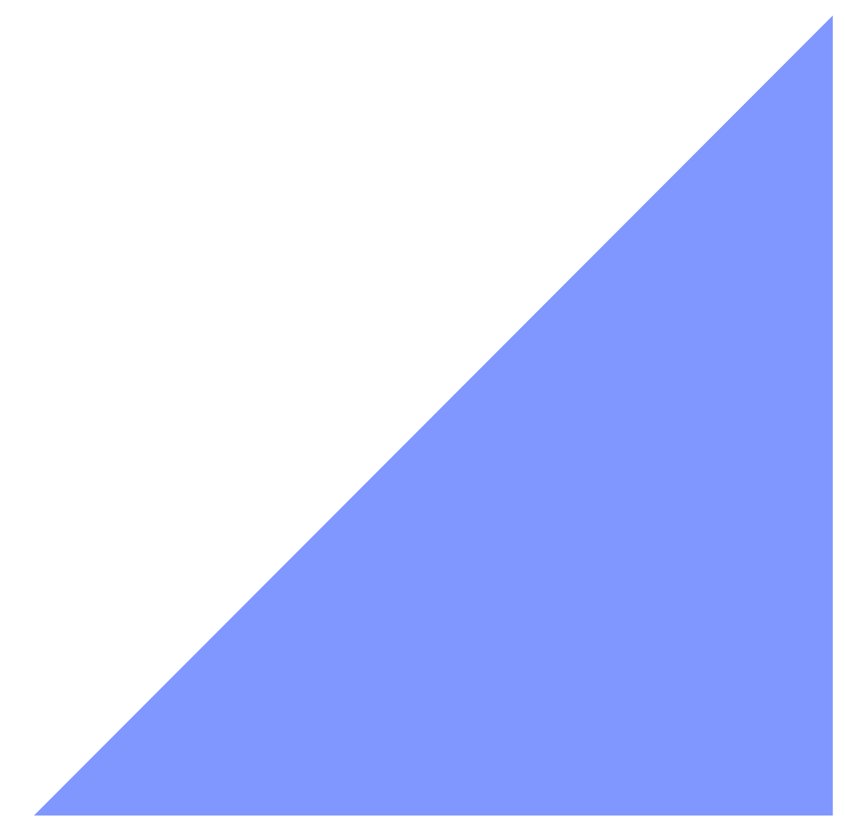
These techniques realize to design your circuits as you like

Candidates for ILD vertex detector

Reference : "Status and Perspectives of an ILC Vertex Detector", M. Winter et. al.

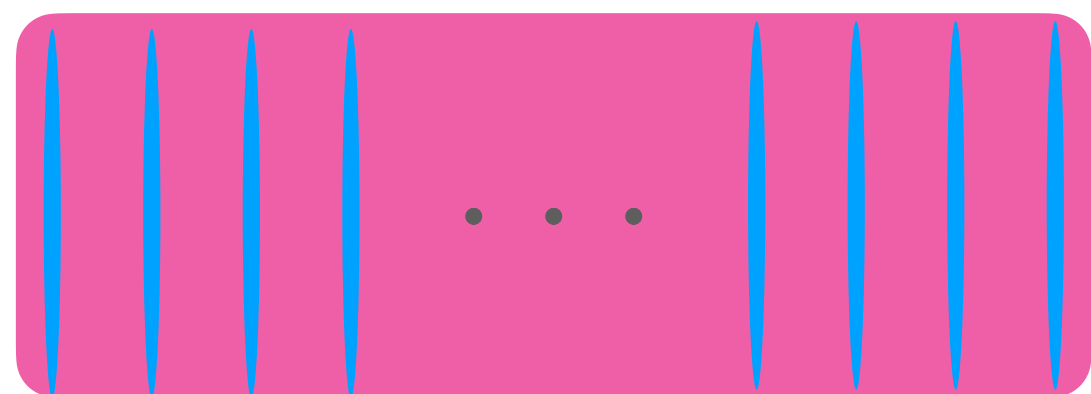
http://www.iphc.cnrs.fr/IMG/pdf/ilc-vd-mwinter-final.pdf

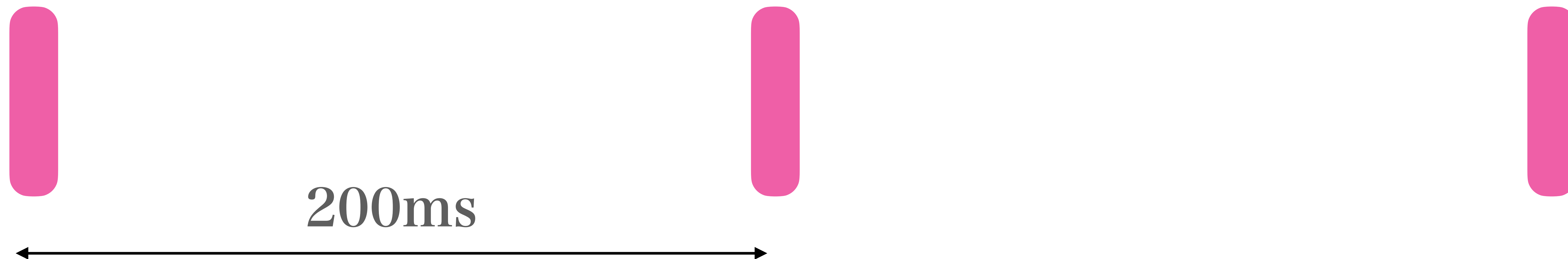
We can proceed the development until a few years before the start of ILC



ILC beam structure

Electrons or positrons in beams=bunch





When do we read out signals?

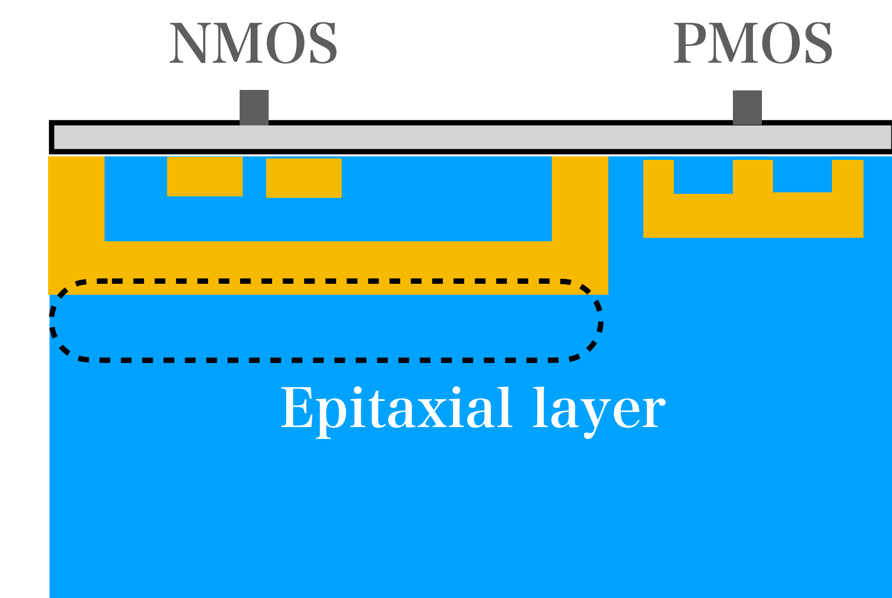
- Every bunch?
- Every several bunches?
- Every train?

ILC specific requirements

ILD vertex detector goal

- Spatial resolution < 3 μm (~ 10μm pitch for binary readout)
- Material budget < 0.15% X_0 / layer (~ 140μm thick for pure Si)
- Innermost radious ~ 16mm ~ 200 hits/mm2 from pair background per train (1312 bunches)
- Pixel occupancy < a few % (~ 7μm pitch for one readout per train)

CPS (also named MAPS)



- CMOS Pixel Sensor
- Monolithic Active Pixel Sensors: Thin, radiation-hard monolithic pixel detector based on CMOS technology

- The first use at STAR, further developments for LHC upgrade and new experiments
- Use epitaxial layer for sensitive area (~10~30 μm) and build readout circuit above
- No bias voltage for depletion layers
- Industrial standard CMOS process (cost effective)
- Innermost doublet : one for spatial resolution, the other for time stamping (enlongated pixels)
- Time resolution 1-4 μs
- 20 μm*20 μm ~ 2500 pixel /mm2 (Estimated occupancy 200/2500 ~ 8% for 1 train)
- Readout frequency 20 times —> Occupancy ~ 0.4 %

Critical aspects under study : Readout speed (single bunch tagging) with low power consumption, material budget

References

overview https://arxiv.org/abs/1007.2634

recent activities https://agenda.linearcollider.org/event/8217/contributions/44630/attachments/34965/54045/CMOS_Besson_LCWS2019.pdf

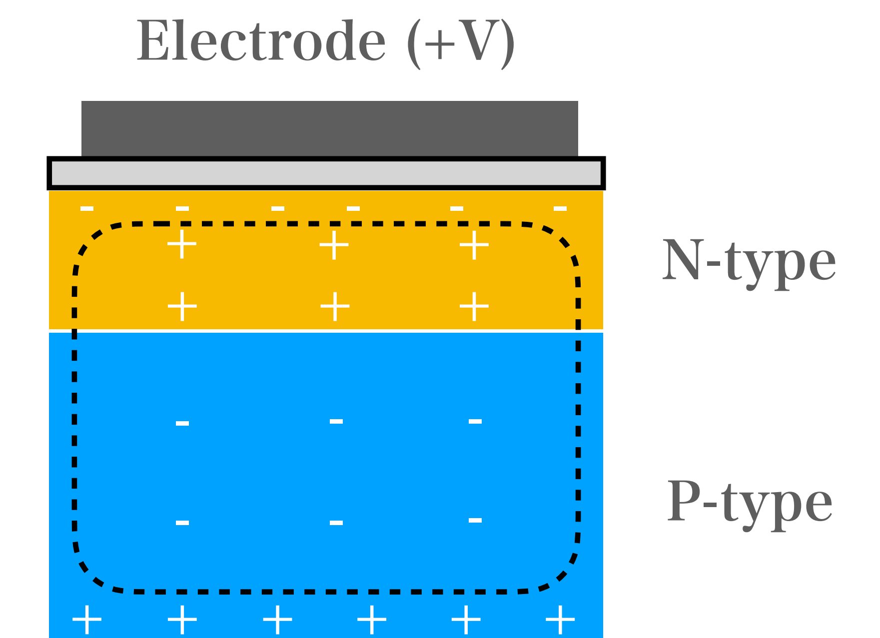
FPCCD

CCD :

- Charge coupled device, which contains arrays of linked MOS capacitors
- Proven technology for vertex detector at SLD

(~10μm spatial resolution, pixel size : 22μm*22μm ~ 2025 pixel / mm²)

If we use the same CCD, the occupancy would be 200/2000 ~ 10%.



Fine Pixel CCD :

5μm*5μm = 40000 pixel /mm² (Estimated occupancy ~ 0.5%)
~1μm point resolution (one of most precise of all the other options)

Readout signals all at once after train passing (No EMI noise, which was problematic at SLD)
Low power consumption due to relatively slow readout

Readout circuit must be built separately (readout electronics at ladder end)
To suppress the radiation damage, the detector should be cooled down to -40℃

Critical aspects under study : Resistance to radiation (especially e+e- pair background)

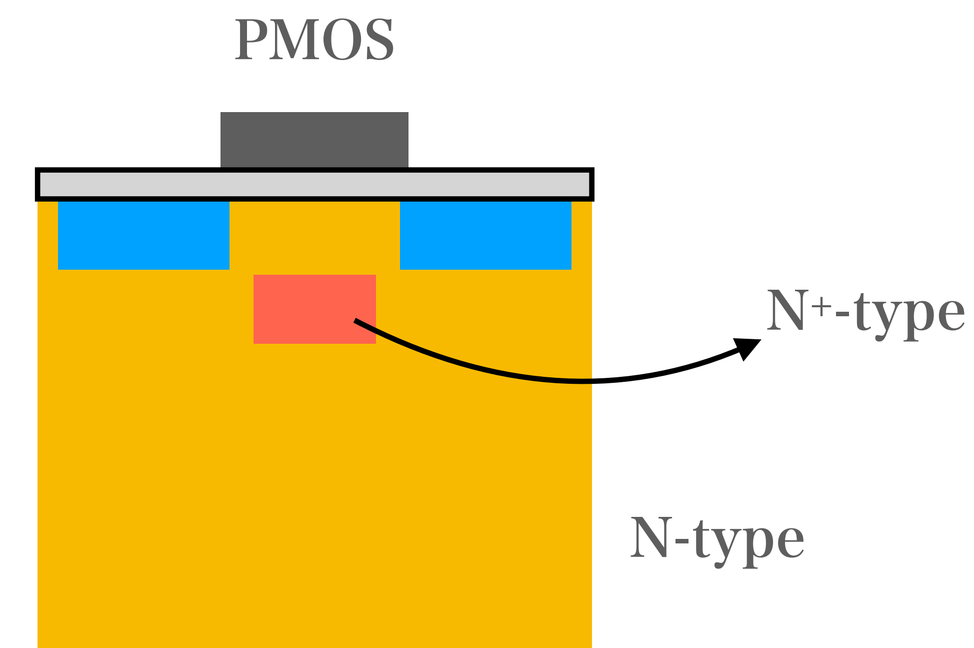
Radiation damage test plan @ ATF https://agenda.linearcollider.org/event/8613/contributions/46087/attachments/35742/55473/RadDamTest_ATF.pdf

References

overview https://www.slac.stanford.edu/econf/C050318/papers/0804.PDF
cosmic ray tests http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2020_Mthesis_yanagawa.pdf
readout electronics http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2012_Mthesis_kato.pdf
neutron radiation tests http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2017_Mthesis_murai.pdf
neutron radiation tests http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2015_Mthesis_ito.pdf
simulation study http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2014_Mthesis_mori_ver2.pdf

DEPFET

- DEPleted Field Effect Transistor
- The first use in HEP at Belle II
- (Semi-) Monolithic IC sensor (Readout circuit located at the ladder end)



Internal gate

Charges created by incident particles are collected here and the S-D current at gate open is modulated depending on the amount of the collected charges

Design for ILC:

-20 μm*20 μm ~ 2500 pixel /mm2 (Estimated occupancy 200/2500 ~ 8% for 1 train)

-Readout frequency 20 times —> Occupancy ~ 0.4 %

Critical aspects under study : Industrialization of the fabrication process (can be only processed in MPI)

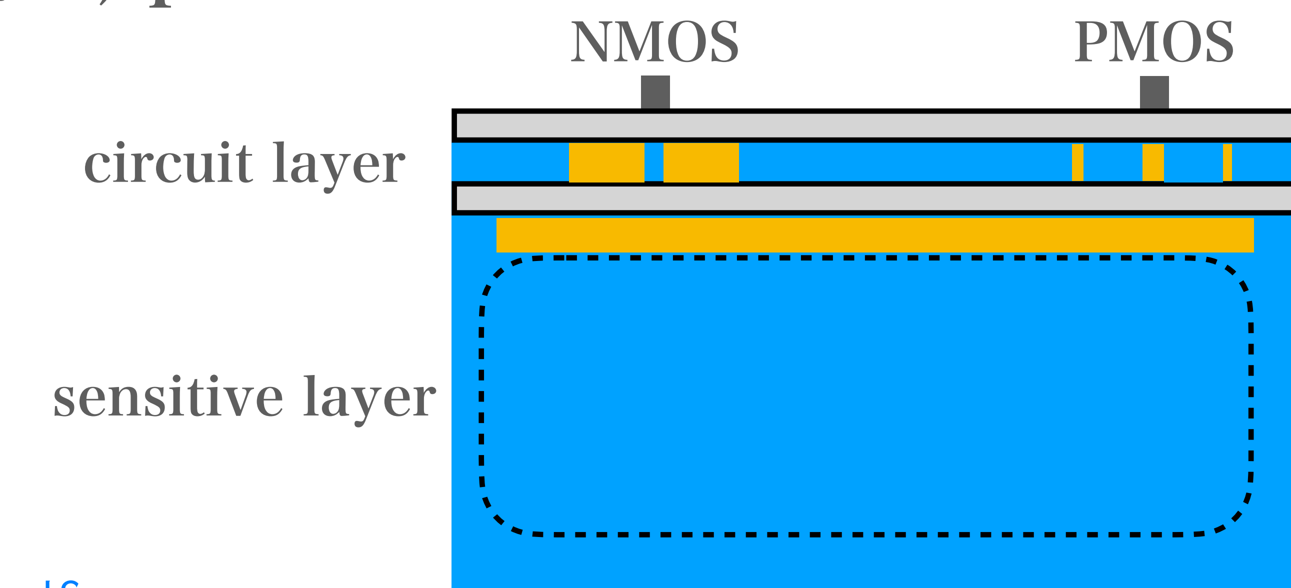
Charge sharing is not enough for 50 μm thick sensors (beam test result σ ~ 3.5 μm)

Reference

overview https://doi.org/10.1016/j.nuclphysbps.2015.09.154
https://ieeexplore.ieee.org/document/6484214
https://doi.org/10.1016/S0168-9002(03)01802-3

SOFIST

- SOi sensor for FIne measuremnt of Space and Time
- SOI (Silicon on Insulator) technology was developed aiming for improving circuit performance by reducing parasitic capacitance and leak current
- Form oxide layer inside by depositing oxygen ions and build circuit on the oxide layer
- High density in-pixel circuitry (Preamplifier, Comparator, Memories (Analog singal/Time stamp))
- Possibility to stack and interconnect two chips on top of each other (3D stacking)
- The position and timing informations of the full ILC train are stored in the pixel array and readout inbetween the trains
- 20μm*20μm
- ~1μm point resolution (one of most precise of all the other options), timestamp at O(1μs) precision



Critical aspects under study : Power consumption

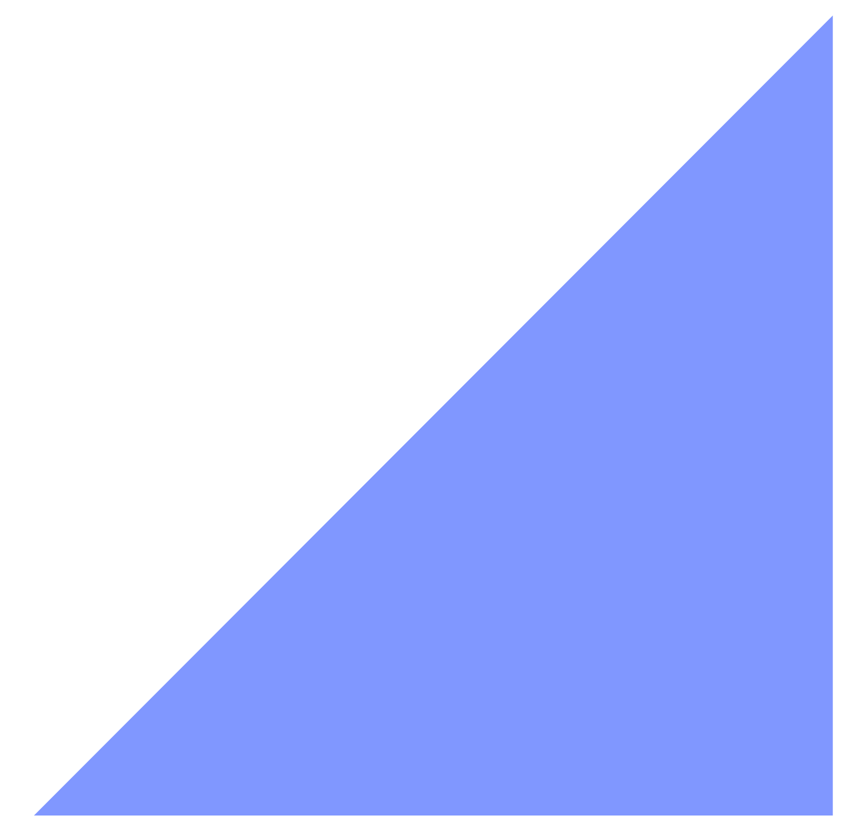
3D stacking https://agenda.linearcollider.org/event/8613/contributions/46089/attachments/35737/55467/ILC2020seasonal_SOI.pdf

References

overview https://doi.org/10.1016/j.nima.2018.06.075

PIXOR http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2012_Mthesis_ono.pdf
SOFIST https://rd.kek.jp/project/soi/thesis/1903taohan_Mthesis.pdf
beam test http://epx.phys.tohoku.ac.jp/eeweb/jp/paper/2012_Mthesis_katsurayama.pdf

Wrap-up



Other useful references

Previous ILC summer camps

- 2012 http://epx.phys.tohoku.ac.jp/eeweb/meeting/201207_ILCschool_kato.pdf
- 2015 https://agenda.linearcollider.org/event/6772/contributions/33303/attachments/27414/41657/20150720ILCSummerCamp.pdf
- 2018 https://agenda.linearcollider.org/event/7980/contributions/42140/attachments/33527/51378/ILCSC2018MYamada.pdf
- 2019 https://agenda.linearcollider.org/event/8237/contributions/44026/attachments/34704/53560/20190905-ILC.pdf

TDR Volume4: Detectors https://arxiv.org/abs/1306.6329

ILD IDR https://arxiv.org/pdf/2003.01116.pdf

Machine-related backgrounds in ILD, D. Jeans

https://confluence.desy.de/display/ILD/ILD+notes?preview=/42357928/159752429/machine_backgrounds_final.pdf

What are presented in this talk :

- Basics on vertex (semiconductor) detectors
- References for more details

Semiconductor technologies are being rapidly developed.
We should stay tuned for further updates!

Backup

Baseline design

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100