SiW Ecal Compact Digital Readout Electronics

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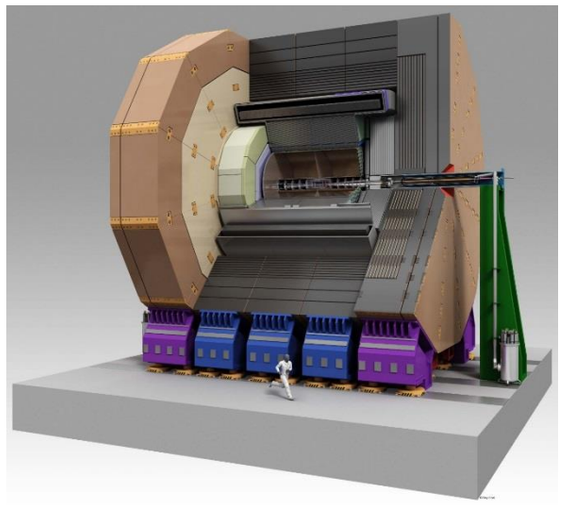
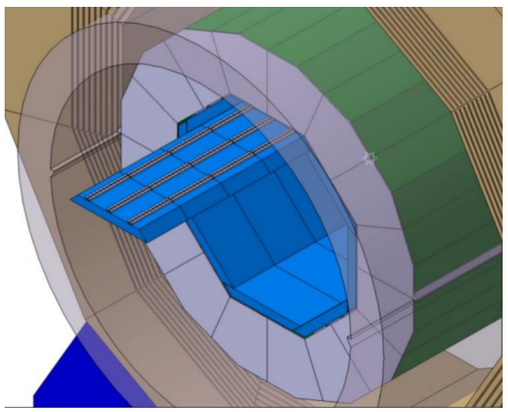
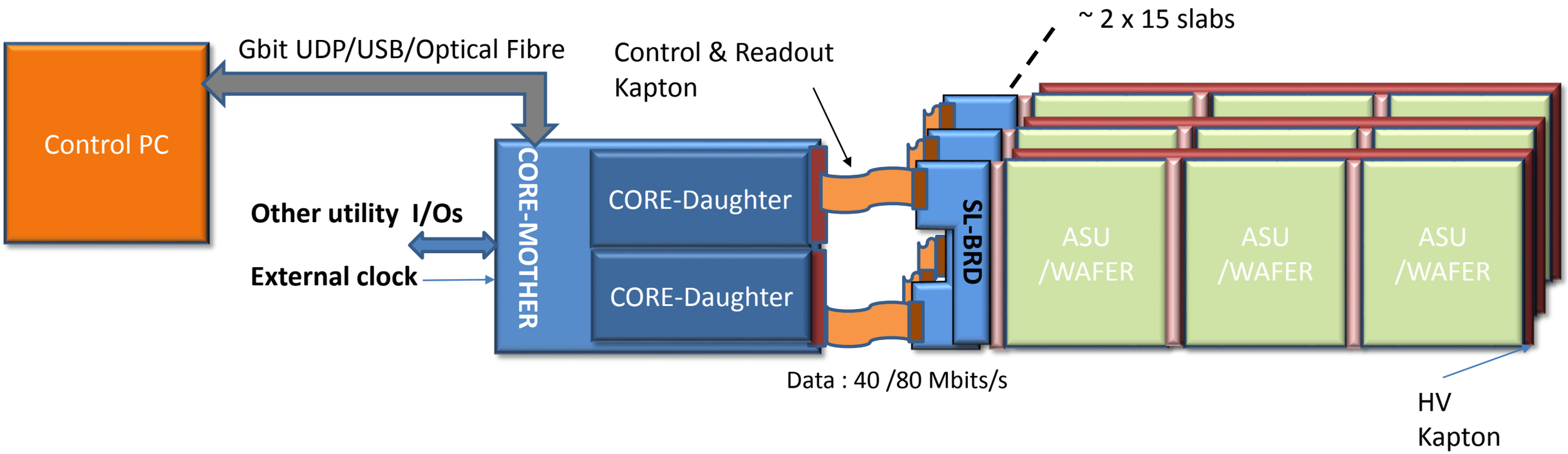
Introduction





- Status of the SiW Ecal compact digital electronics
- Preparation for next test beam: 30 Nov- 6 Dec
- Next steps

Global Architecture Scheme

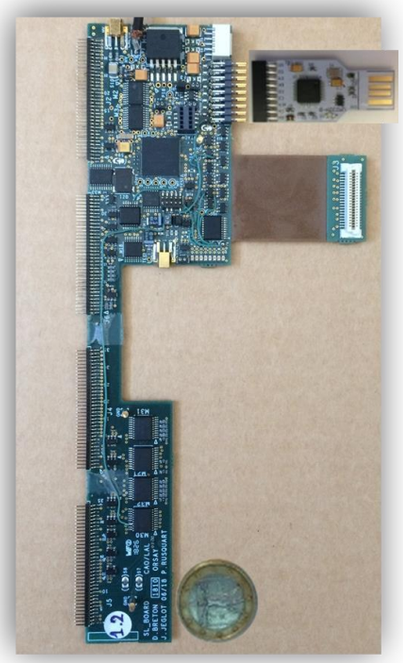


CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab

External clock and Utility I/Os : possibility to be synchronised with other systems!

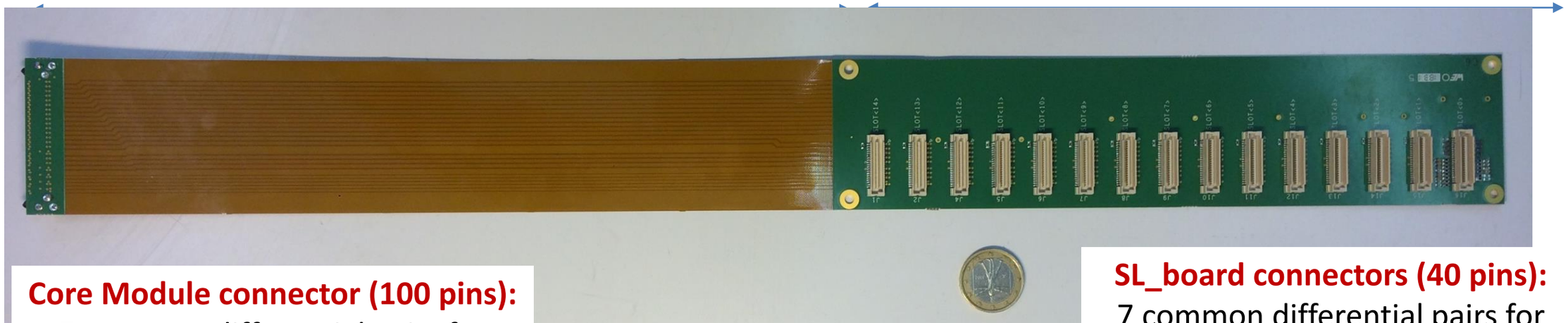
The SL-Board

The **SL-Board** is the sole interface for the **~10,000 channels of a slab :**



- It delivers the **regulated power supplies,** including **High Voltage**, **controls** the SKIROC ASICs, and **perfoms the full data readout**.
- It is connected to the CORE-Kapton via an internal **kapton layer** and a 40-pin connector.
- It is based on a **MAX10 from ALTERA**, which is a mix of CPLD and FPGA.
- It includes an **ADC** which will be used to **monitor** the **pulsed power supply** and the **temperature.**
- Very size **limited:** 18 cm in width, 10 to 42 mm in length.
- Its **own power** consumption is **< 1W**
- It can also be an **autonomous system** with direct computer access for testing and characterization purposes (using the **FTDI USB module**).

The SL Board Core-Link (Core-kapton)



Core Module connector (100 pins):
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

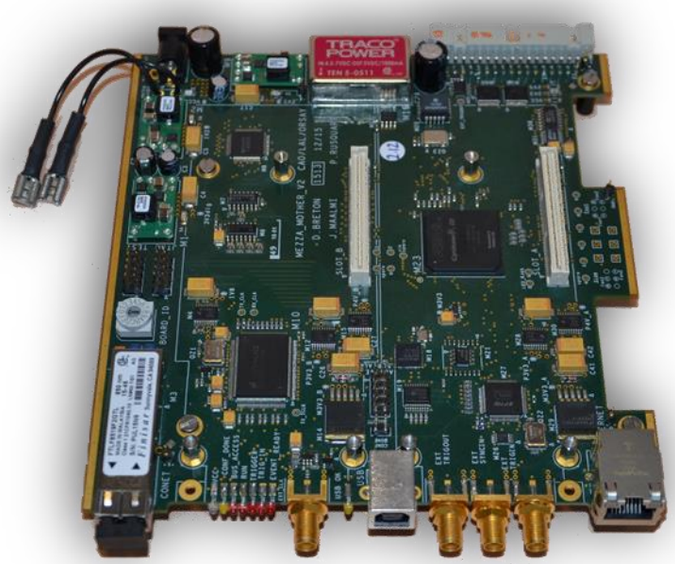
SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

- The **CORE kapton** measures 40 cm. It is the **interface** between the CORE Daughter and the SL-Board. It permits driving and reading out **up to 15 slabs**.
- It transmits all the **clocks and fast signals**, and houses the control and readout links.
- It handles the **synchronisation** of the **15 slabs**.
- The Kapton Interface makes use of **asynchronous serial transmissions** in order to greatly simplify the synchronization of the numerous control and data links.
- The speed of the slow control and the individual readout links is : **40 Mbits/s**
- Reminder : readout link of the ASUs **: 2 x 5 MBits/s**

The CORE Module

The CORE Mother:

- The **Control and Readout Motherboard** have been developed for housing up to 2 **Mezzanines**: it permits separating the **acquisition** part from the specific front end part.
- **External** input and output signals permit **synchronising** or interfacing the module with other systems.
- The CORE mother sends **common clocks and fast signals** to the Core Daughters to keep the **system synchronised**
- The control and readout is possible through **USB(2.0)**, Ethernet (secured UDP) over copper **or Optical link**
- The CORE module **power consumption** is **5 W**

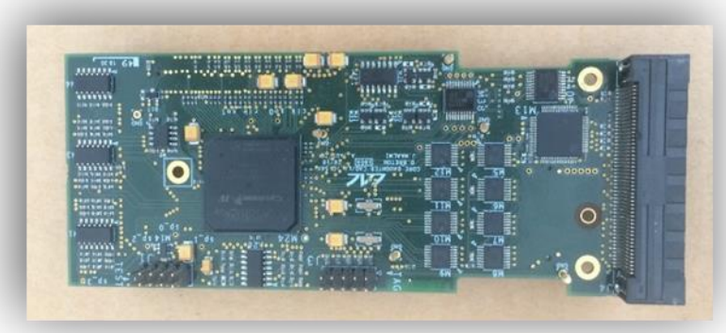


The CORE mother

The CORE module

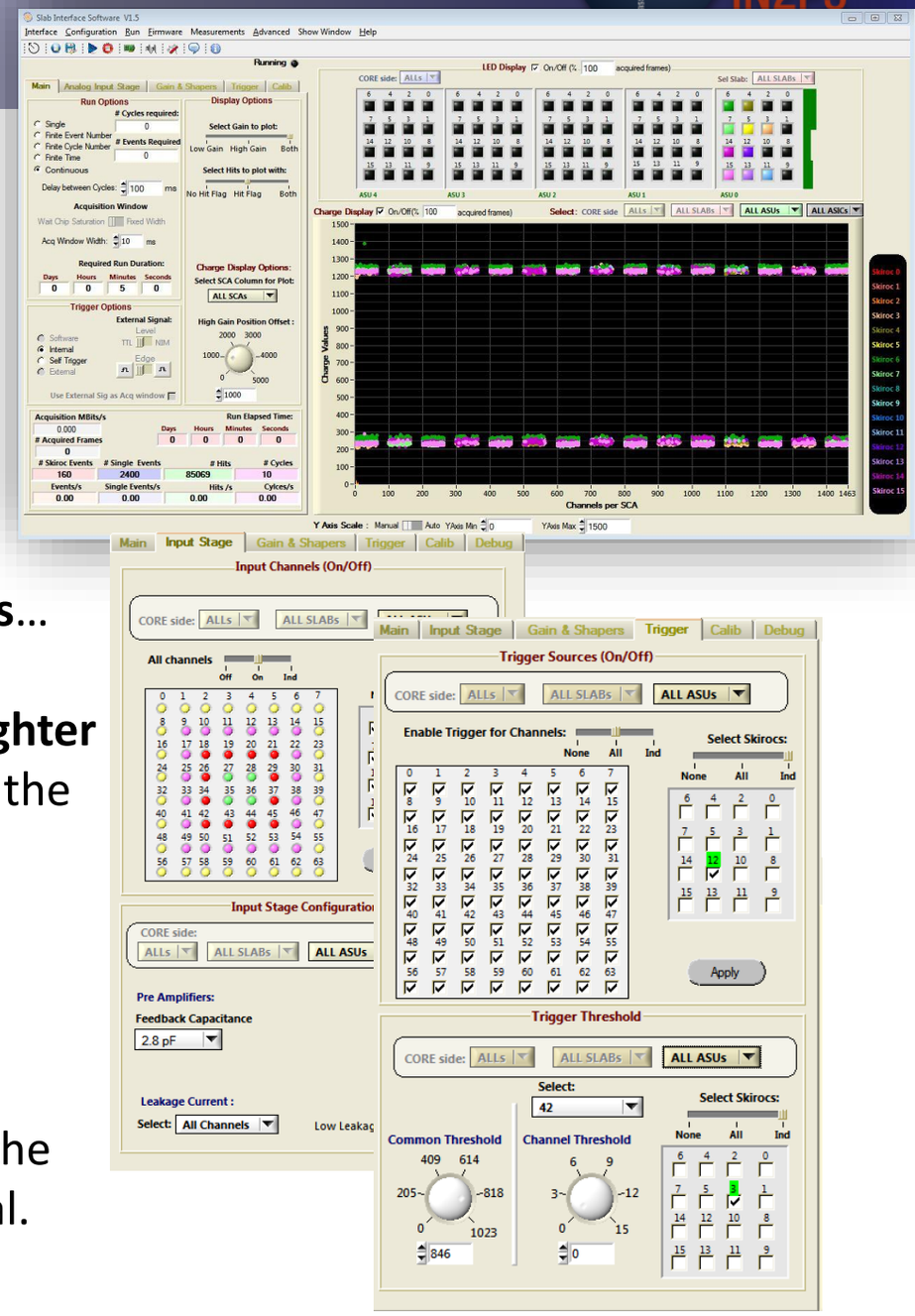
The CORE Daughter:

- The **CORE Daughter** is based on a Cyclone IV FPGA. It is the interface between the CORE motherboard and the Kapton which permits driving and reading out **up to 15 slabs**.
- It buffers all the clocks and fast signals, and deals with the control and readout links through the Kapton Interface.
- It houses the second level of **event buffers** (derandomizers)**.**
- Ctrl & Readout link between CORE Daughter and CORE Mother **: 60 MBytes/s** if USB**, and 125 Mbytes/s** if UDP**.**



The CORE daughter

Acquisition Software



- The Software can handle the communication through FTDI connector **or** through **CORE Module**.
- It handles the **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**

- Advanced measurements can be performed Online such as **Threshold scans**…

- All the hardware components are detected automatically : **Number of daughter boards**, **number of SL Boards** connected to each daughter board, and also the **number of ASUs** on each slab using **slow control readout**.

- All necessary **Slow Control parameters** can be programmed through the Software

- Slow control configuration is checked by writing twice the same values to the SKIROC shift regiser and reading back the pushed value on the SROUT signal.

- Control and data Readout with **direct connection** to the SL Board via FTDI module or through the **CORE module**.

- The C-functions that handles the communication (readout and configuration) can be used as a a library with any other program that handles C-langage.

Hardware Improvements

Going from SL_Board V1 to V2

Experience from beam test permitted **upgrading the design** of the SL_Board:

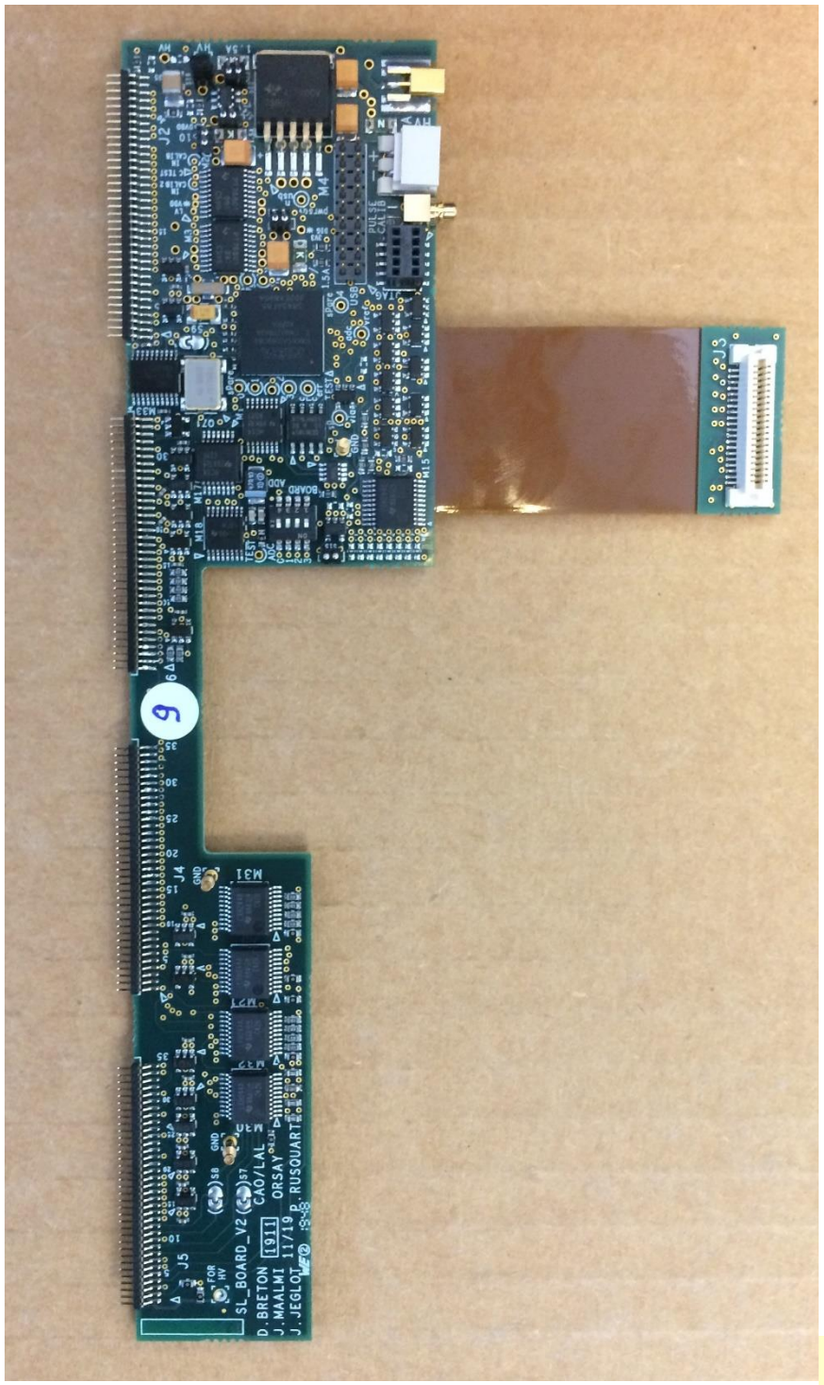
- All useless circuitry has been removed and the rest optimized
- Kapton length has been raised from **40** to **48 mm** (this will **ease the plugging to the kapton**)
- The main input plugs are moved next to the kapton (HV and calibration pulse in MMCX)
- The connector for the FTDI USB module is changed and moved => takes less space, easier to handle
- A more robust LV connector has been mounted which permits using thicker wires (we had a large voltage drop with the old ones)
- A **switch** has been added to encode the **slot number**

- We added:
  - a **DAC for SKIROC ADC calibration**
  - a **flash EEPROM** for permanent information storage: Serial Number

- The FPGA can produce **pulses** for **autonomous functional calibration of both gains**

- The **HV will be made available on the SL_Board** to ASU connectors (both sides)

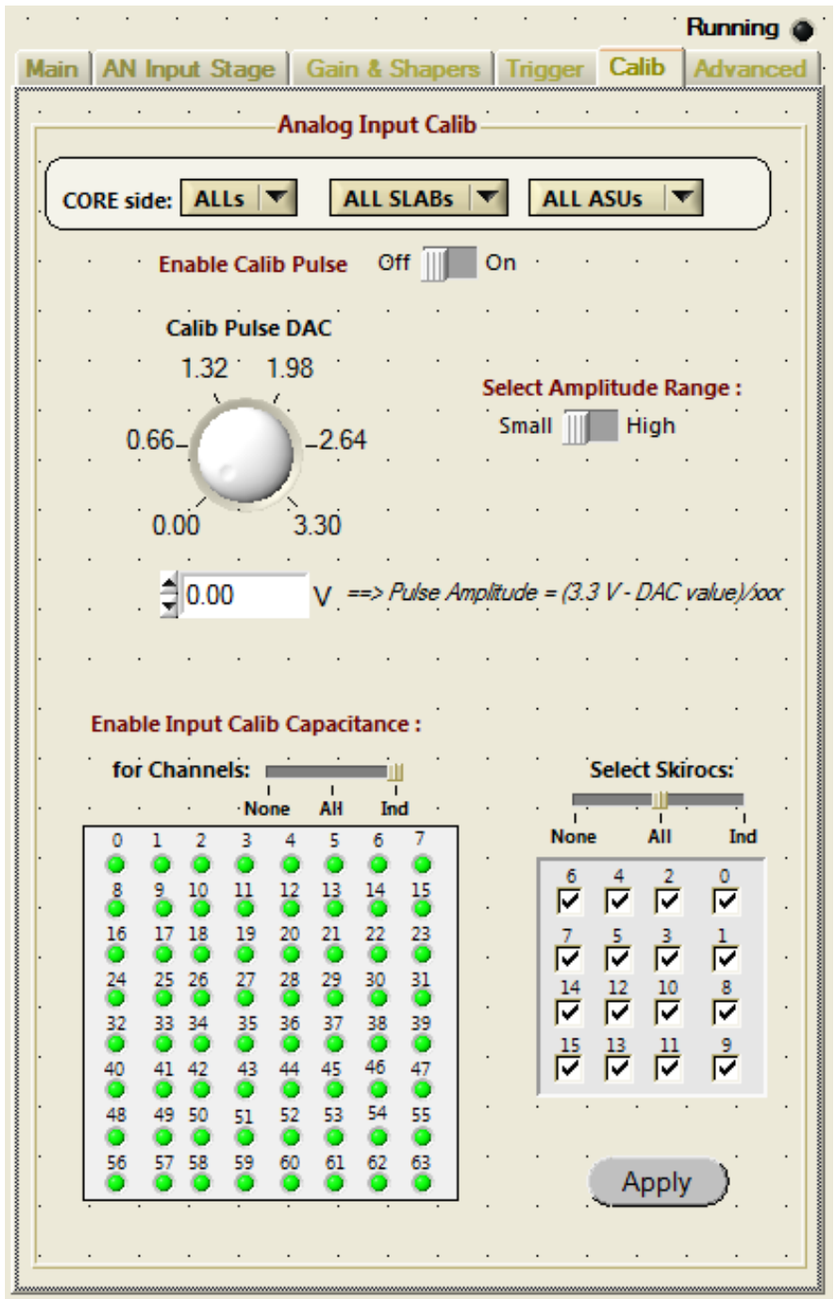
SL Board V2



- 20 boards have been produced and equiped.
- Almost all the functionalities have been tested and validated:
  - Communication through FTDI and CORE KAPTON
  - Firmware programmation trhough CORE KAPTON.
  - Calibration pulses (see next slide)
- Still need to be tested:
  - FLASH eeprom
  - Power pulsing mode using the current limiter.

15 SL Boards already tested and successfully validated !

Calibration Pulses



- We have two ranges of amplitudes: in order to test High and Low Gain.
- Thanks to the DAC on the SL Board, we can send Pulses with Amplitude from ~few mV to ~150 mV.
- The FPGA can generate equidistant pulses with known distance:
  - Permits testings the synchronization between multiple layers
  - we can study the Re-triggers…

➔ Thanks to this feature we can adjust the Common Threshold/ ASIC and the individual thresholds for each channel to trigger on ~0.5 p.e

Calibration Pulses : High Range

Slab Interface Software V2.14

Interface Configuration Run Firmware Measurements Advanced Show Window Help

Running

Main | AN Input Stage | Gain & Shapers | Trigger | Calib | Advanced

Analog Input Calib

CORE side: Left | ALL Slabs | ALL ASUs

Enable Calib Pulse Off On

Calib Pulse DAC

1.32 1.98 0.66 2.64 0.00 3.30

Select Amplitude Range : Small High

0.00 V ==> Pulse Amplitude = (3.3 V - DAC value)/xxx

Enable Input Calib Capacitance :

for Channels: None All Ind

0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63

Select Skirocs: None All Ind

6 4 2 0
7 5 3 1
14 12 10 8
15 13 11 9

Apply

LED Display On/Off (% 100 acquired frames)

CORE side: Left Sel Slab: ALL Slabs

ASU 4 | ASU 3 | ASU 2 | ASU 1 | ASU 0

Charge Display On/Off(% 100 acquired frames) Select: CORE side ALLs ALL Slabs ALL ASUs ALL ASICs

Charge Value + Gain Offset

2063 1900 1800 1700 1600 1500 1400 1300 1200 1100 1000 900 800 700 600 500 400 300 144

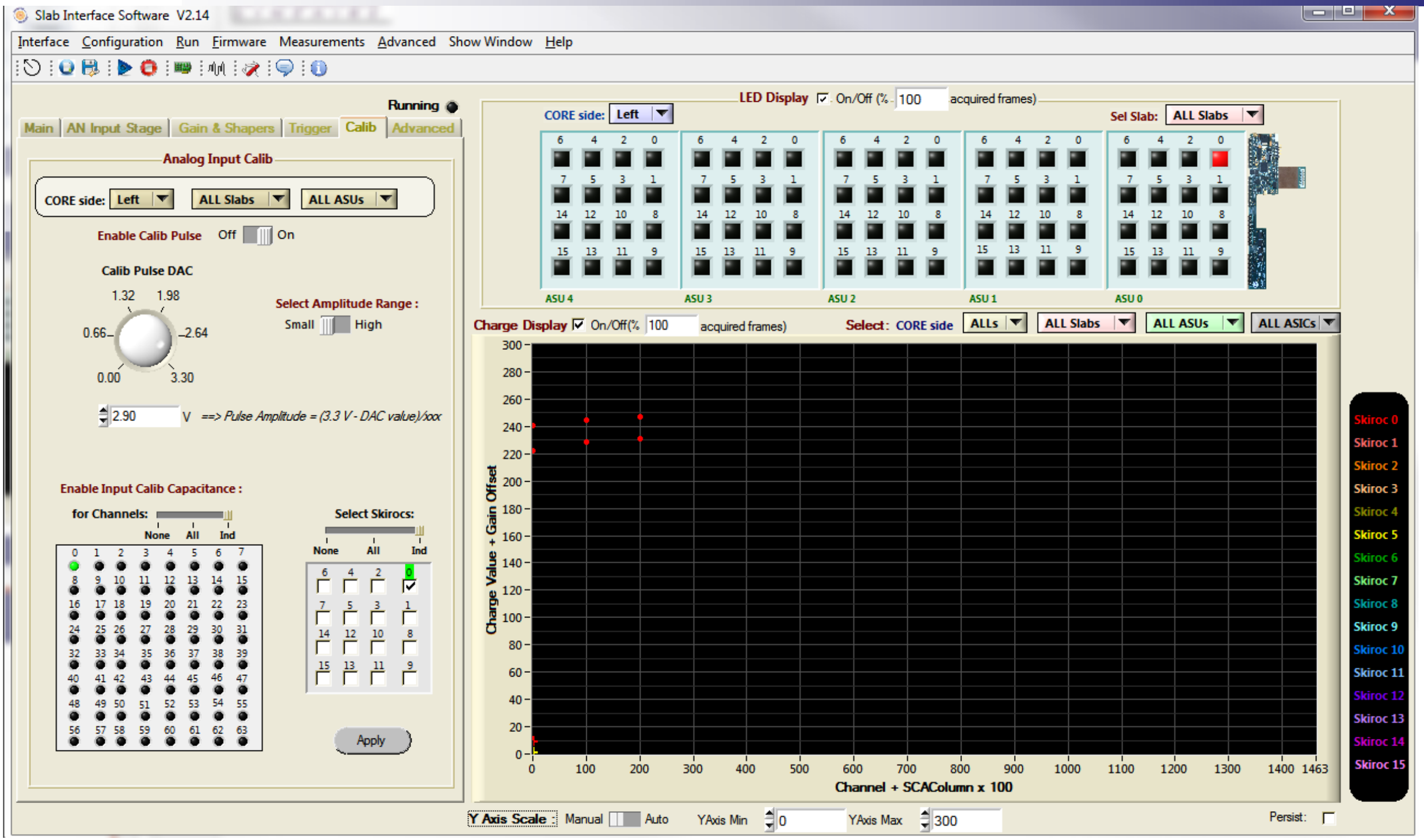
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1463

Channel + SCAColumn x 100

Skiroc 0 Skiroc 1 Skiroc 2 Skiroc 3 Skiroc 4 Skiroc 5 Skiroc 6 Skiroc 7 Skiroc 8 Skiroc 9 Skiroc 10 Skiroc 11 Skiroc 12 Skiroc 13 Skiroc 14 Skiroc 15

Y Axis Scale : Manual Auto YAxis Min 0 YAxis Max 4000 Persist:

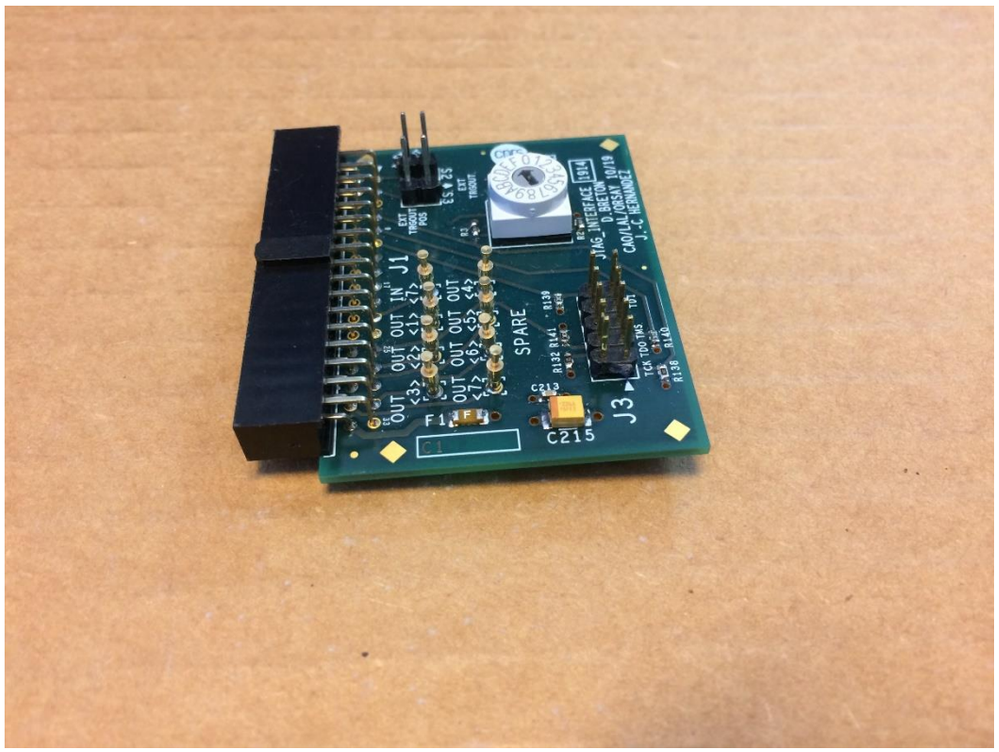
Calibration Pulses : Low Range

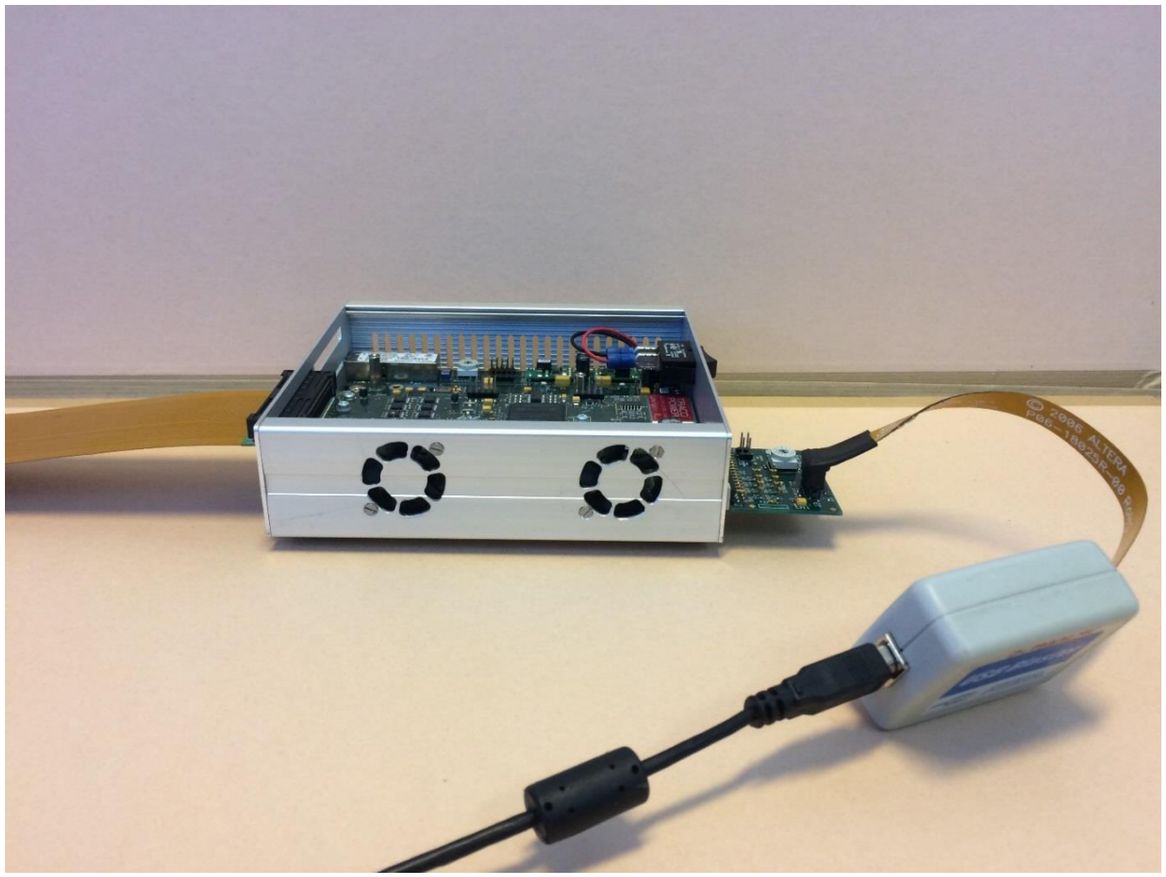


Programming Firmware through CORE module: The JTAG Interface Board

- We designed this board in order to program the SL Boards Firmware through the CORE Module via the Core Kapton.
- We can program each SL Board using the encoder wheel.

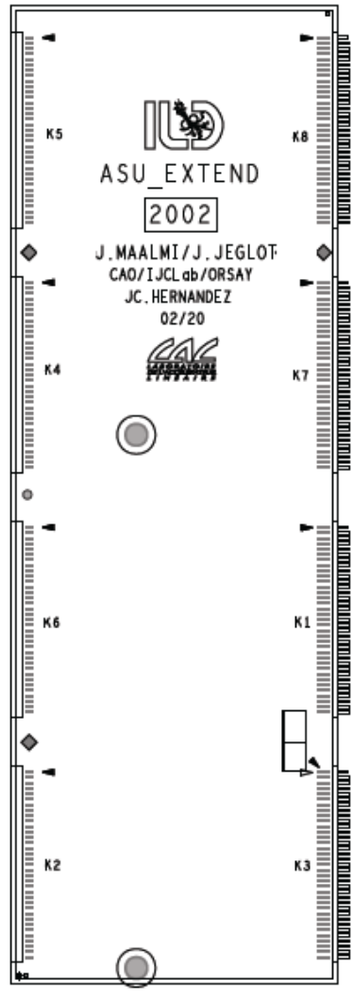
(unfortunately it is not possible to program all SL Boards in parallel because of a conflict on the returned data)





Interfacing SL_Board to FEV13:
design of the SL-ADAPT board

The new **SL-ADAPT interface** board permits the **control** and **readout** of a **FEV13** by a SL_Board. A **hole below the 3 kapton** cables permits connecting the high voltage for the wafers.

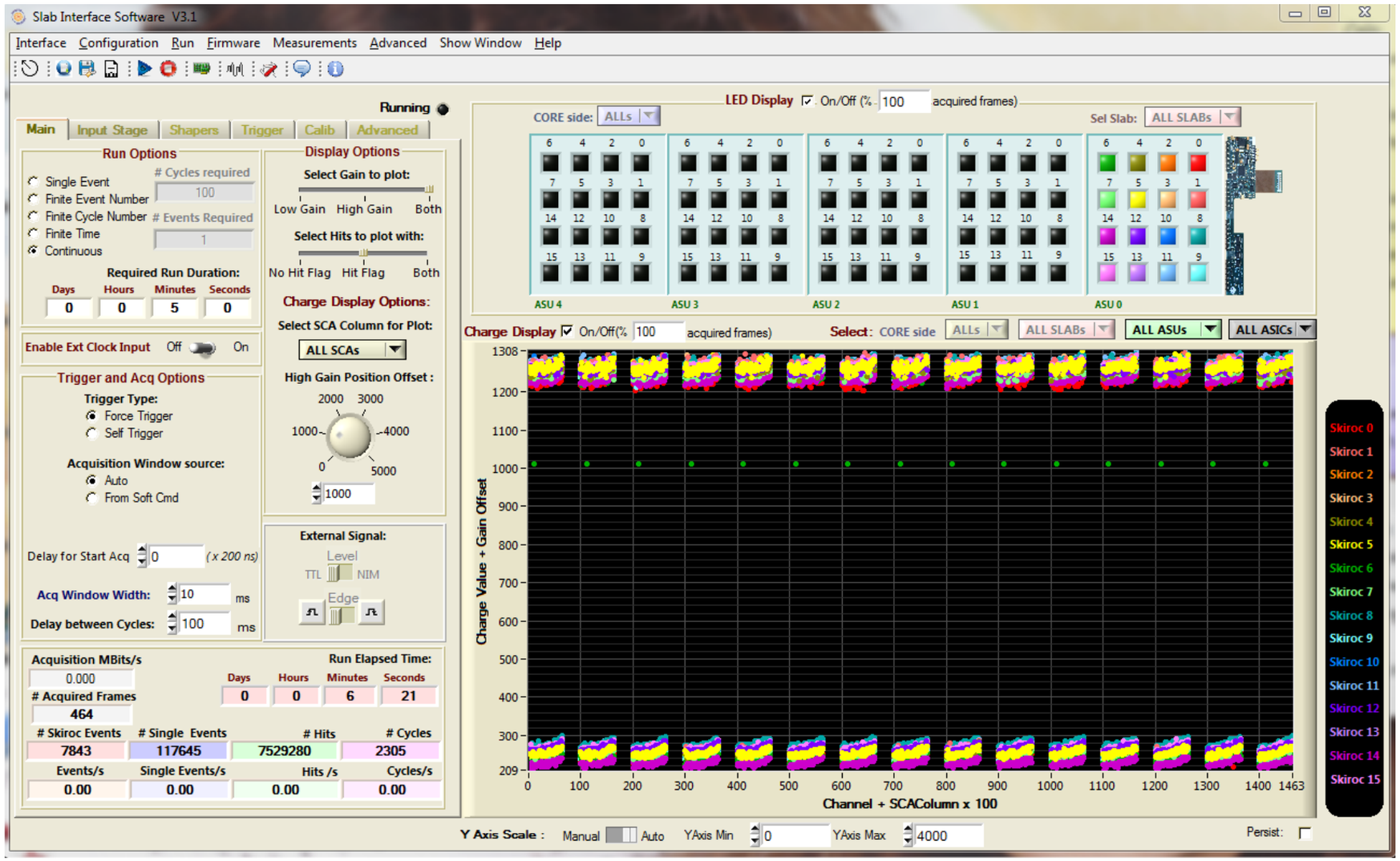


ASU_EXTEND Board

➔ To align all the FEVs11/12 with the FEV13

Readout of FEV13 through SL-Adapt/SL-Board

- SL Board interfaced with the FEV13 with **same Firmware** as for a FEV12 or older : thanks to straps and re-routings of signals **diretctly on the SL-Adapt board**.
- The Software **detects automatically** if the board is a FEV13 or FEV12 and « adresses » it according to it.
- We can **mix** on the same Core-Kapton SL-Boards connected to FEV13 boards and FEV12 (or older).



First image of the Software reading out a FEV13 through SL-Adapt and SL Board!

15-Layers working prototype!

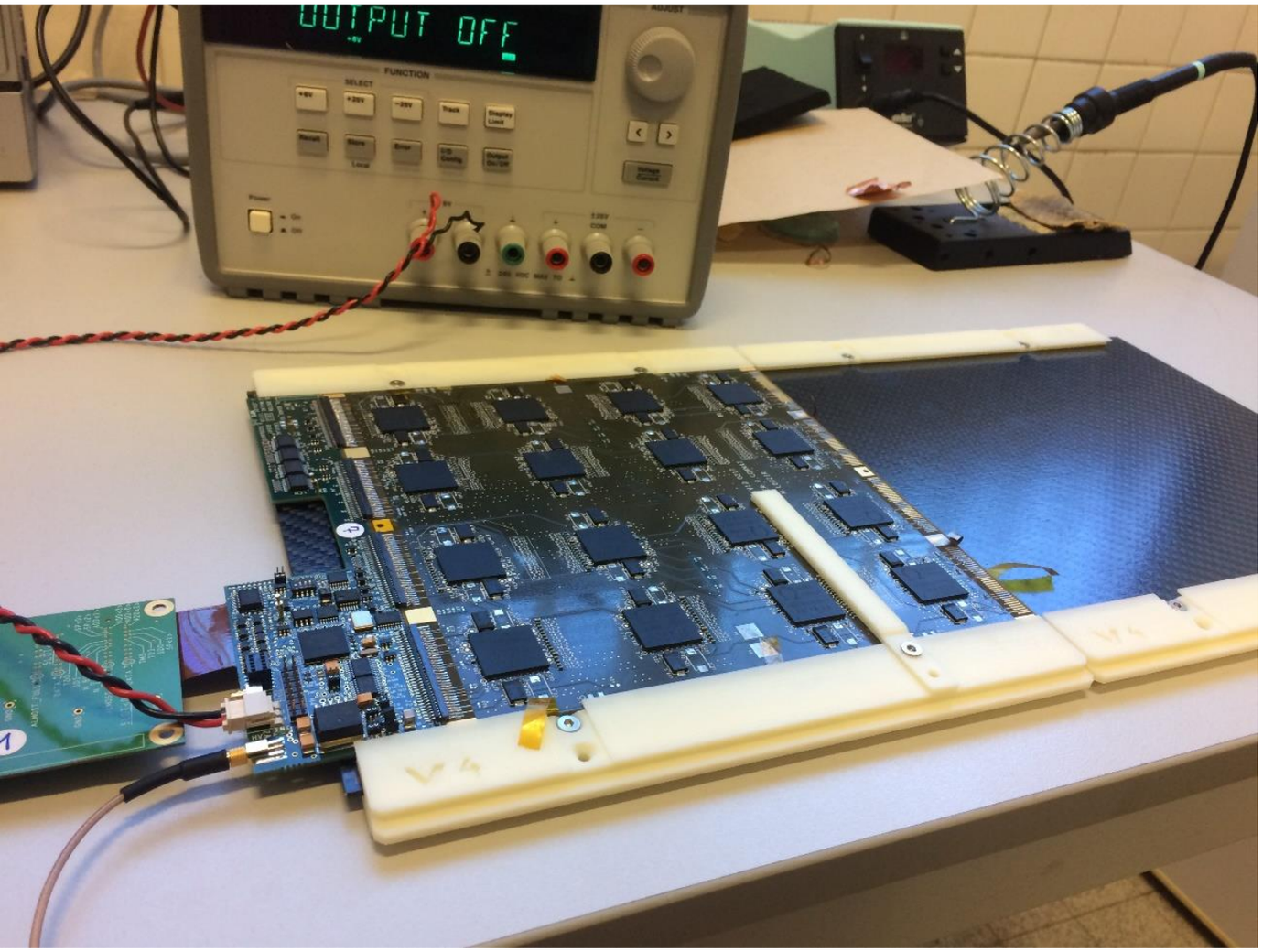
~15 000 channels

Preparing Test Beam in DESY (30 nov- 6 Dec)

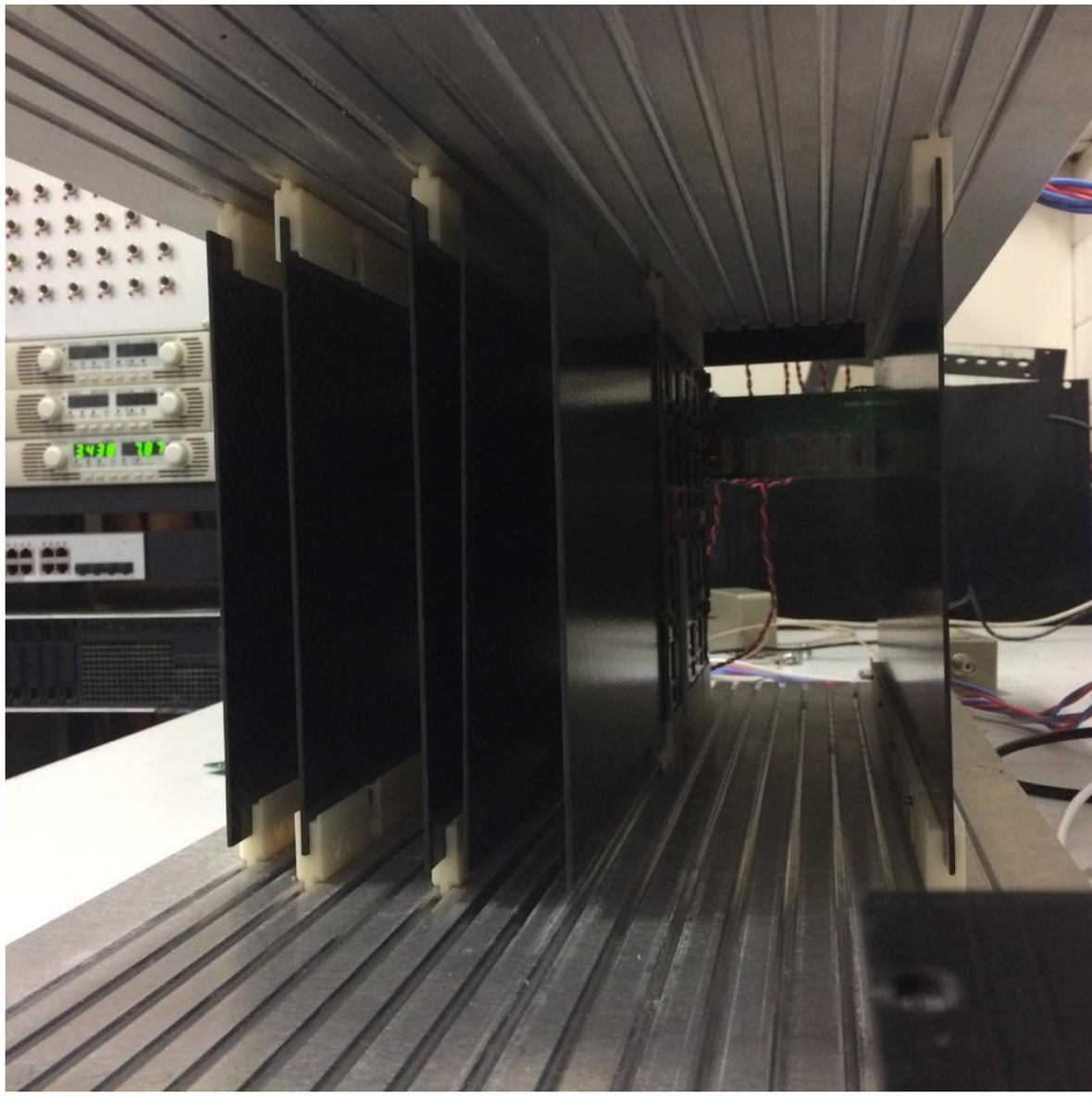
We were « almost » ready in March … we should be fully ready this time!

Improved Integration (1)

The SL_Board V2 is coupled to the FEV which holds the wafer on its bottom side. They are then pushed together into the **plastic slides** screwed on the new **carbon frame**. The **tungsten plate** will be fixed on the back of the carbon frame.

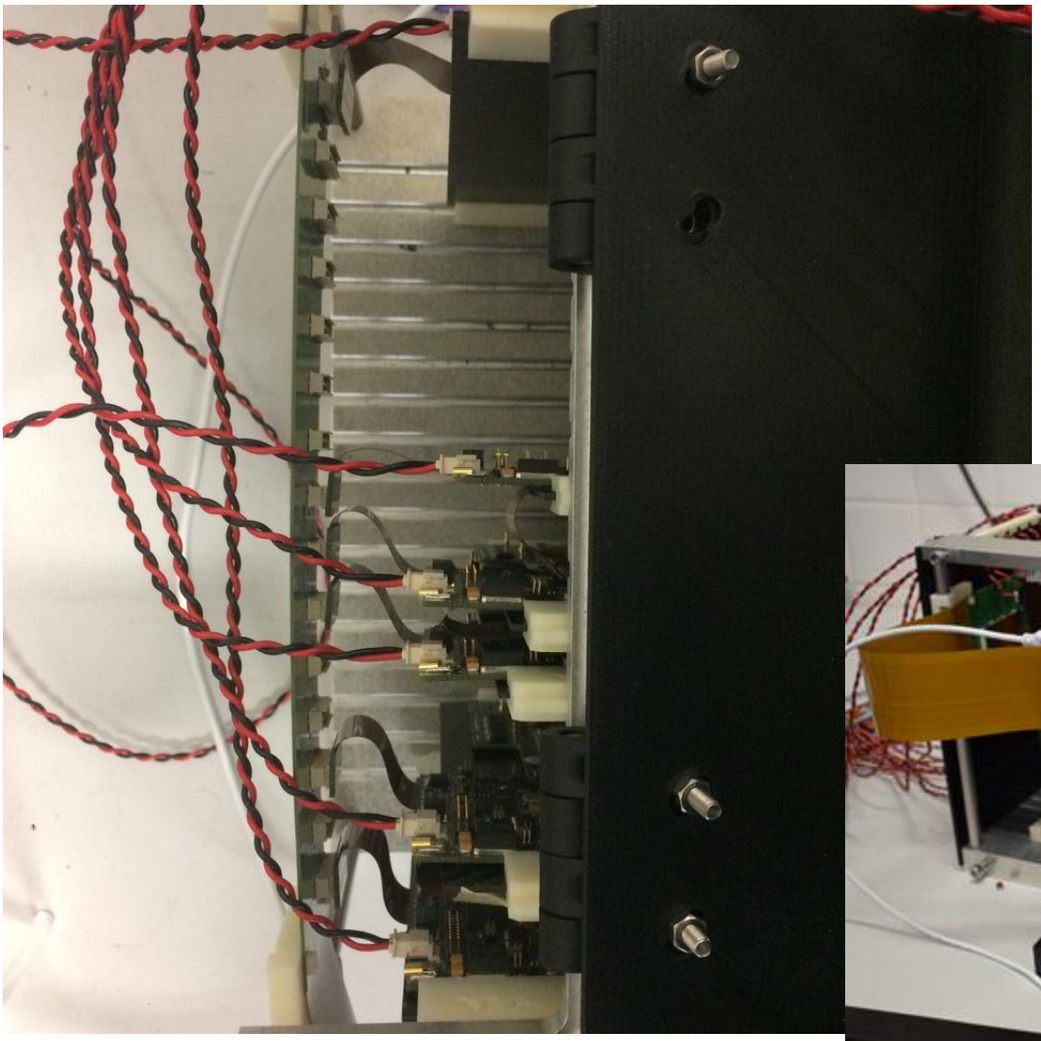


The full slab is then pushed into the rails of the metallic box, which can house **up to 15 slabs**.

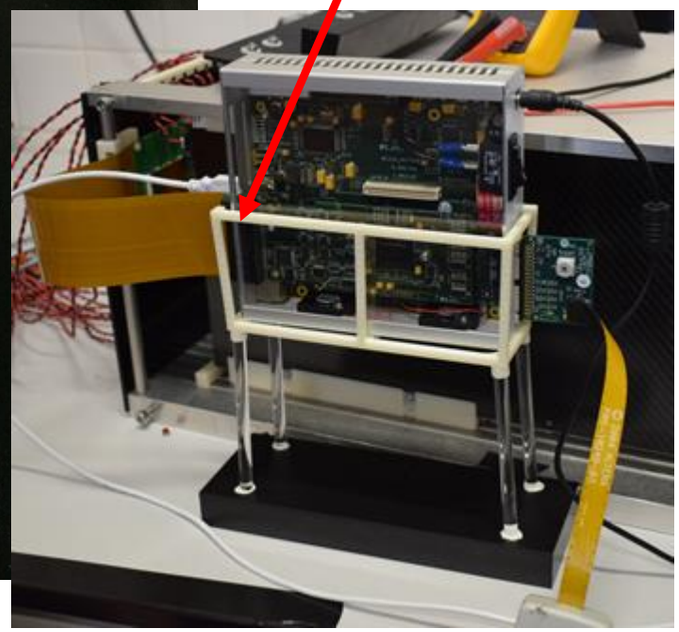


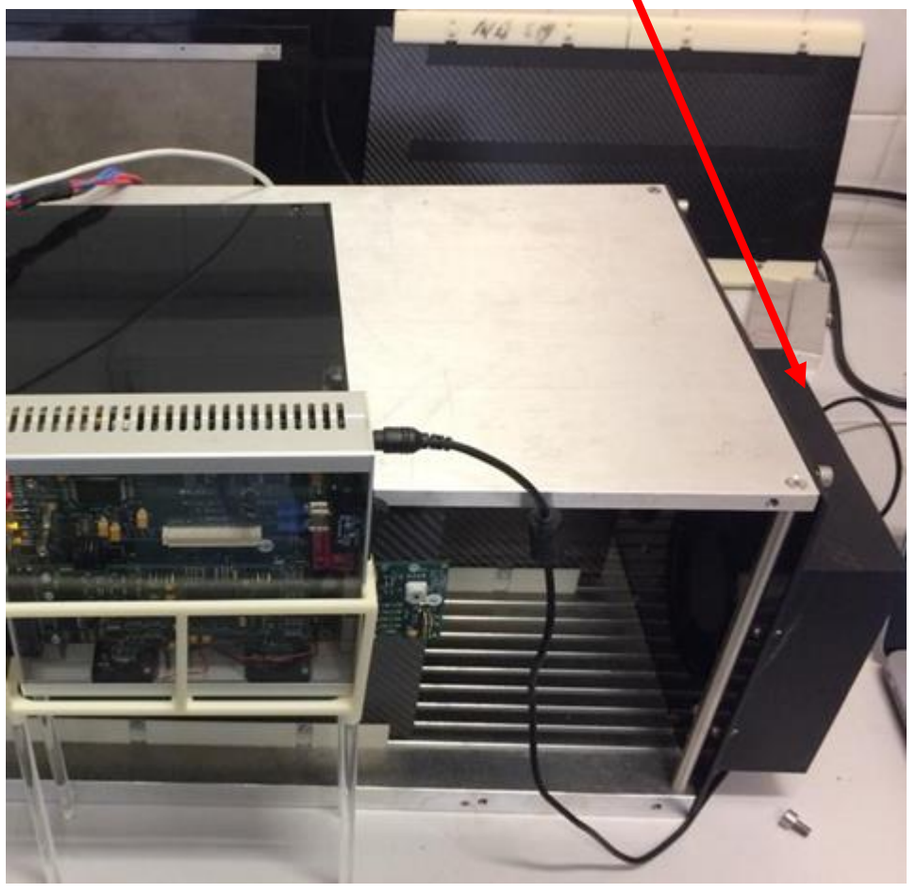
Improved Integration (2)

Once the slabs are inserted, the Kapton then the power supplies are connected (LV and HV). Total LV current will be of the order of **24A** with **no power pulsing**, producing **~90W** .



A **dedicated pedestal** has been designed for carrying **the CORE module** to which the CORE_Kapton is connected. Electronics inside the box **is cooled down by two fans**.

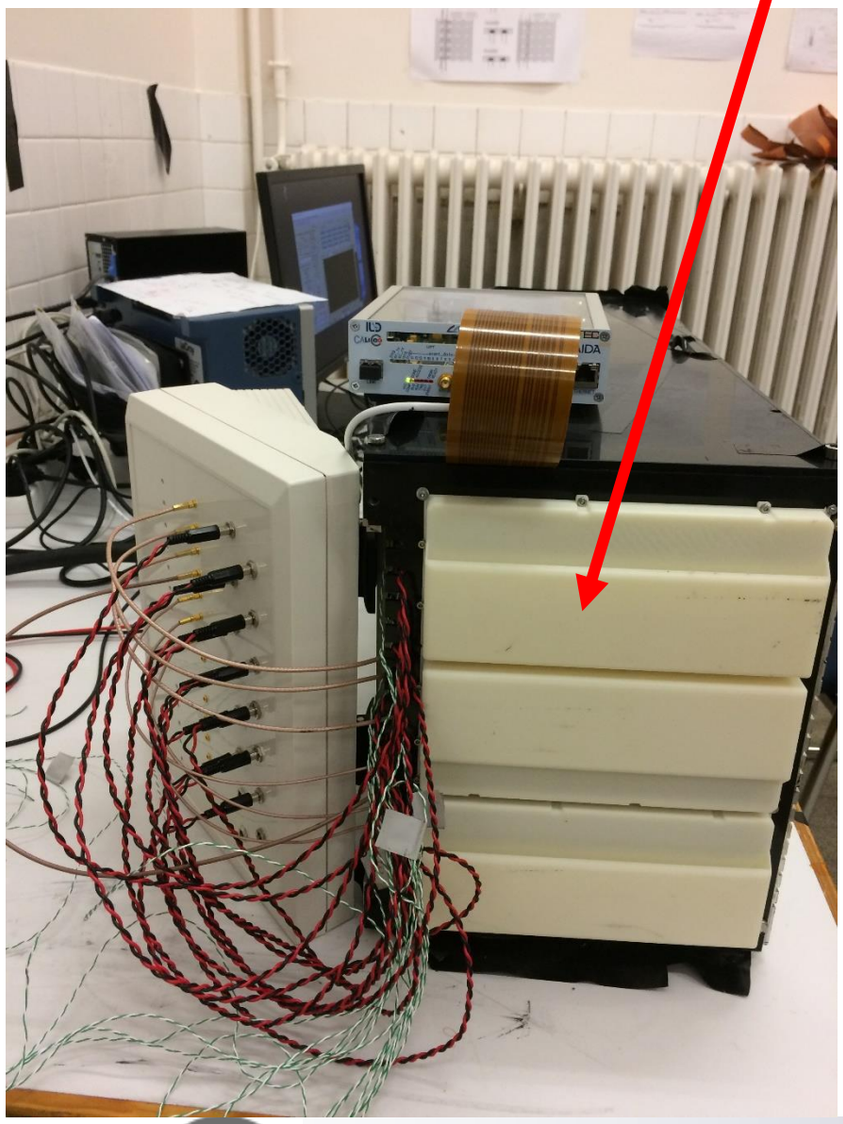




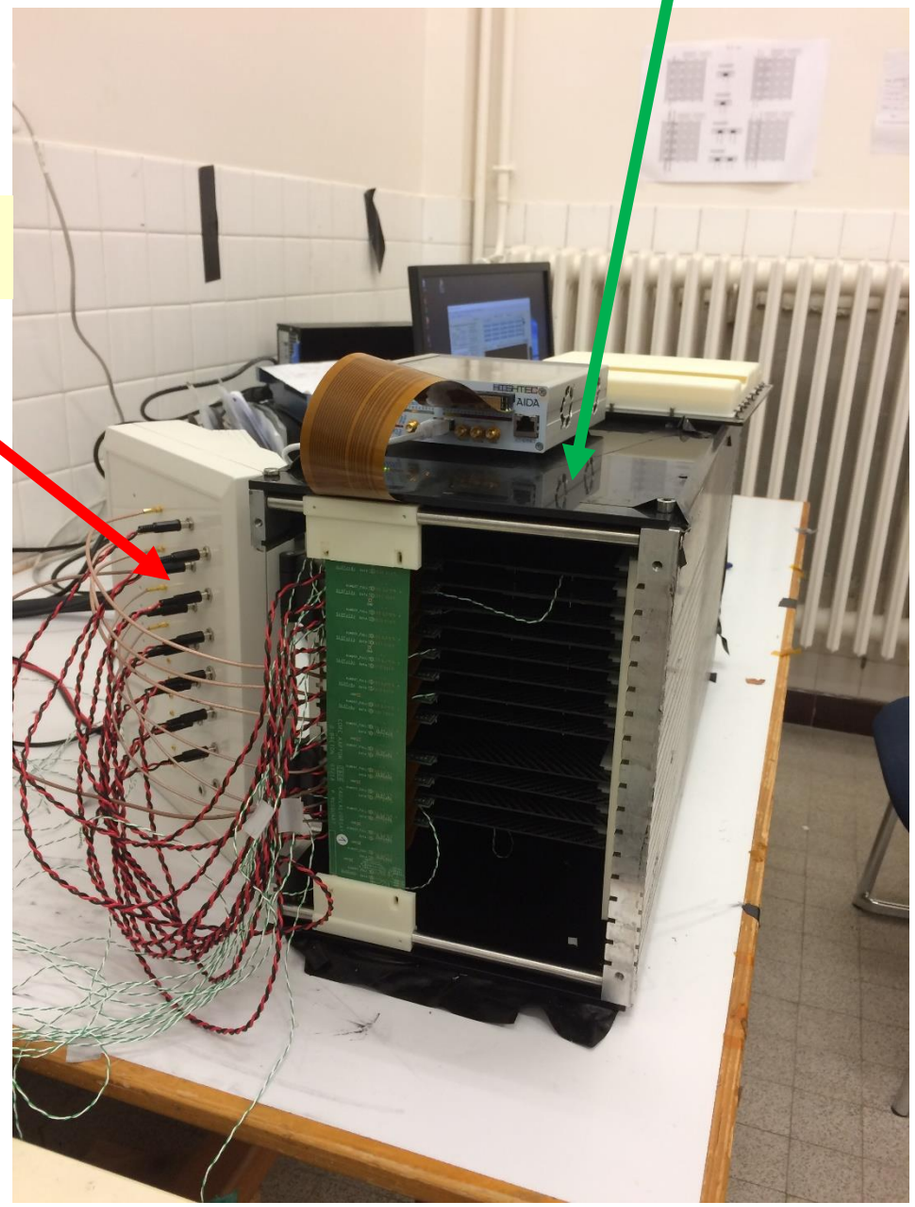
Improved Integration (3)

Slabs in horizontal position for Commissioning runs with Muons

Baffles for air cooling input



New Patch Panel!



Software Improvements…

- Load Configuration from ASCII file :
  - Easy configuration of Gain, Trigger Enable, Thresholds etc … per Slab Add

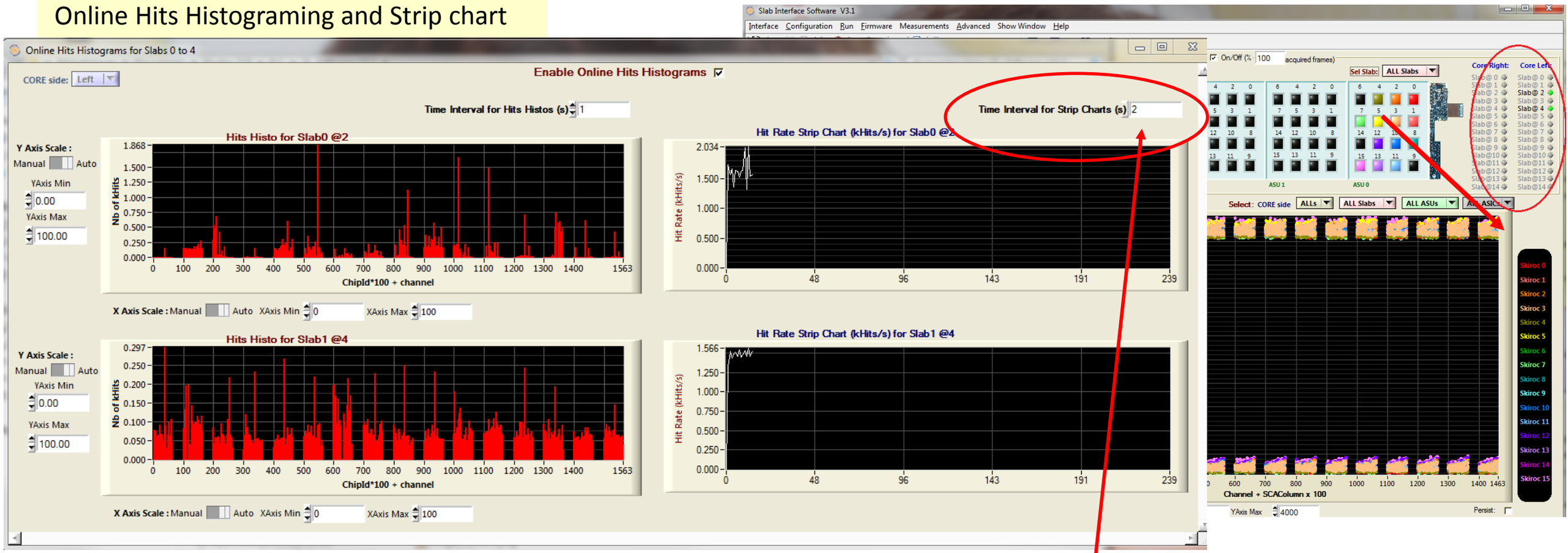
  ⇒ Works even if we change Slabs position, and also if Slab is missing.

```
# AcqParams TrigType ' SELF_TRIGGER ' AcqWindowSource ' AUTO ' ACQWindow 2 DelayBetweenCycles 100 DelayForStartAcq 0 ExtSigLvel ' TTL ' ExtSigEdge ' POS '
# SlabSerNum 1.3 SlabAdd 2 Asu 0
## ChipIndex -1 FeedbackCap 4 ThresholdDAC 250 HoldDelay 80 FSPeakTime 2 GainSelectionThreshold 500 DefaultChThreshold 10 DefaultTrigMask 0 DefaultPAMask 0
### Ch 55 TrigMask 1 ChThreshold 0 PAMask 1
```

- **Coming soon** : Online **Monitoring** of **Temperature** and **AVDD** at beginning and end of Acquisition Window=> ADC values stores with physics Data.

LEDs to visualise data coming from each slab.

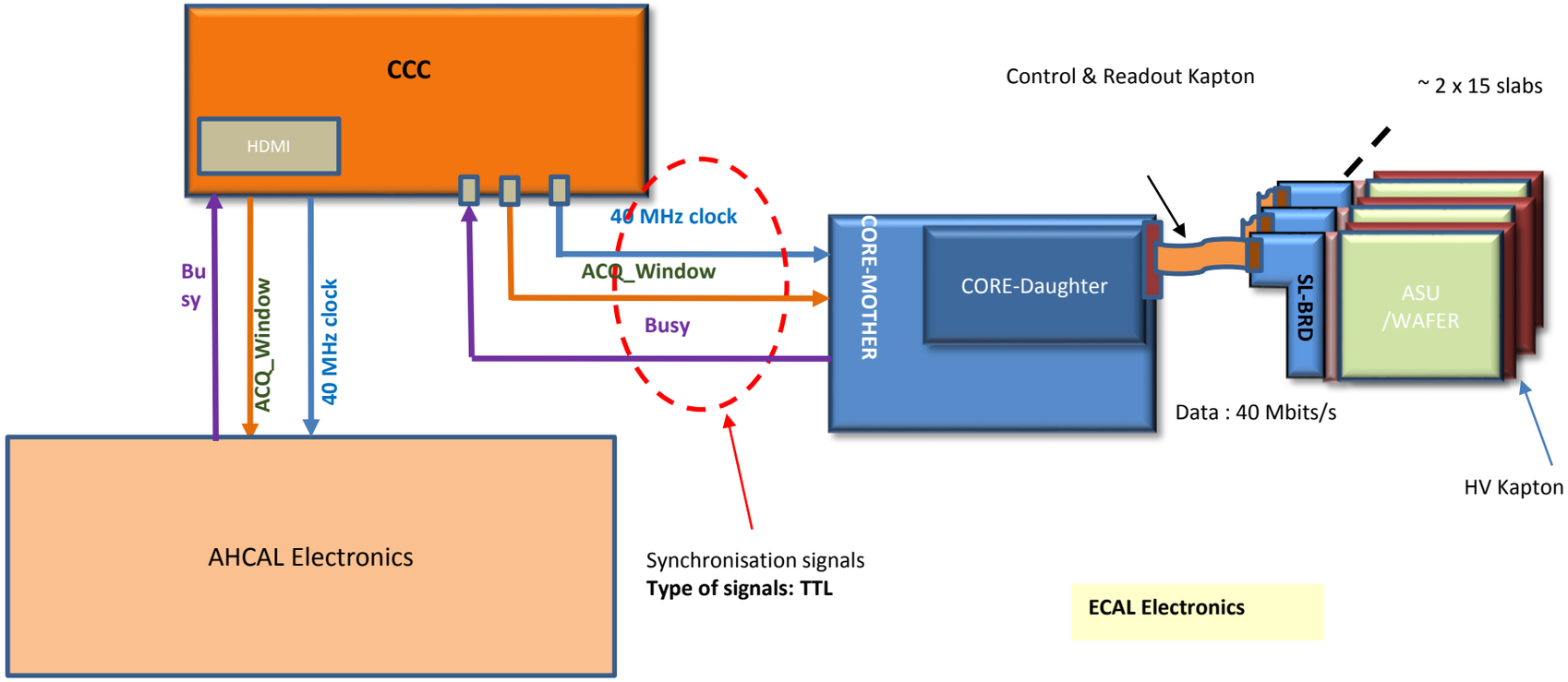
Online Hits Histograming and Strip chart

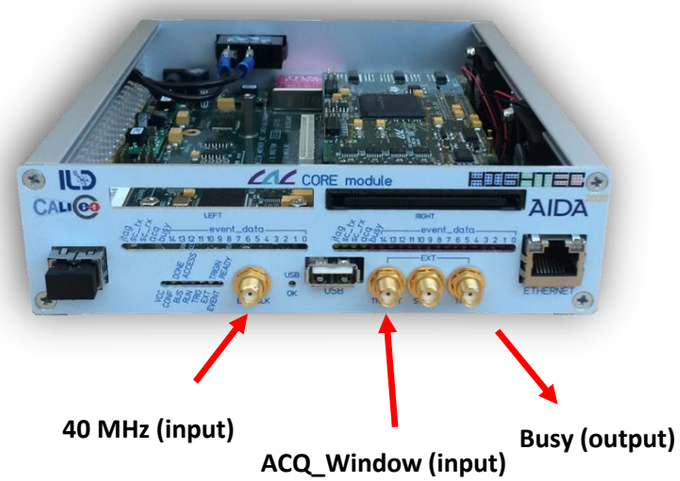


Xaxis is ‘ChipID * 100 + Channel’ =>
permits vislualsing immediatly Beam position in each ASIC!

Time Interval to refresh total Hit Rate (kHits/s)
=> Permits to **monitor Hit Rate/Slab** during Test Beam

Synchronising with AHCAL

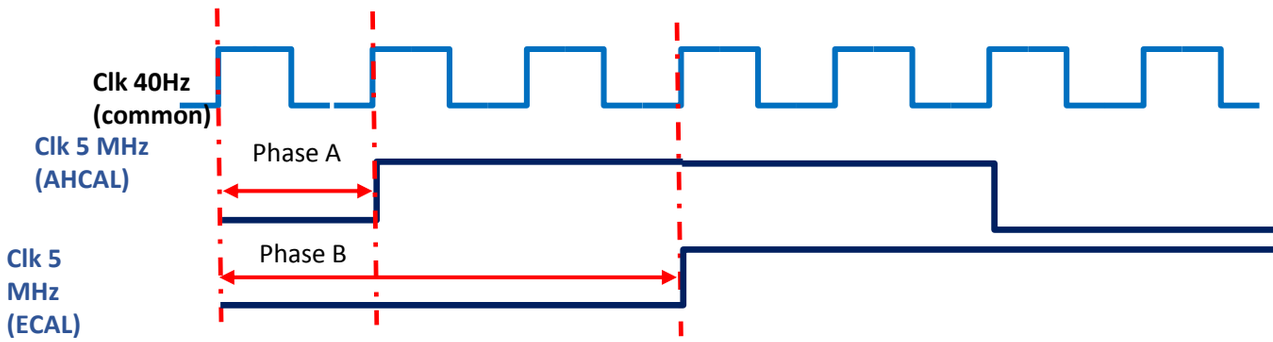




CORE Module inputs/outpus are **SMA female.**
➔ We will need **Lemo to SMA male adapters**

- We prepared synchronisation with AHCAL for testbeam in March:

- Common 40 MHz **Clock** and **AcqWindow** source.
- **Busy signal** (*corresponding to End of readout of All Skirocs AND buffers empty in SL-Board*) sent from CORE-Module to CCC
- FPGA timestamp is Reset with **first Start Acq**.



PhaseB – PhaseA = fixed Offset between AHCAL and ECAL at each power ON
Max = 200 ns (1 clock period of 5 MHz)

Ongoing integration tests

- Commissioning runs with muons with new patch panel: check noise, Grounding policy …
- Calibrate noisy channels etc…
- Intensive runs …

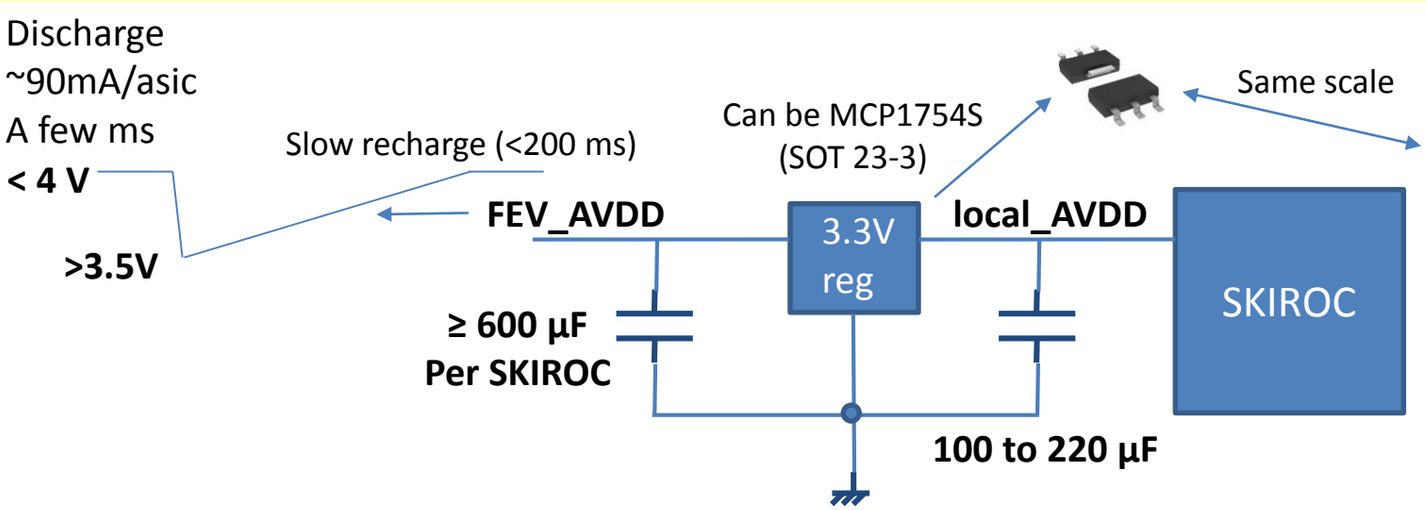
Under study: Power Pulsing

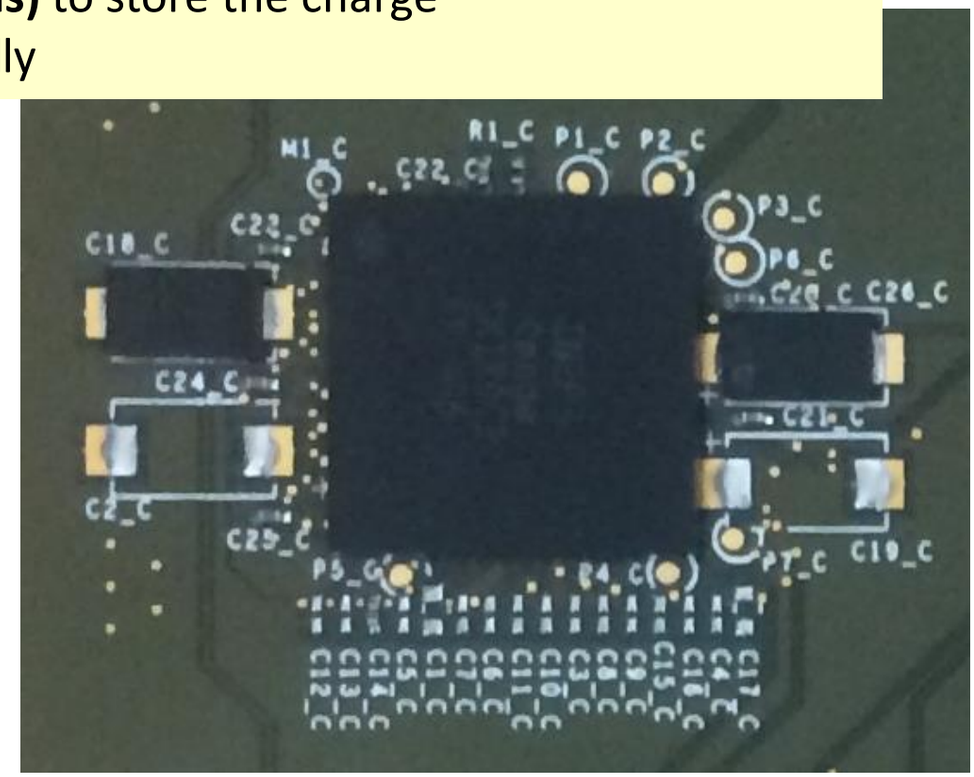
Two remarks:

1) High-value flat capacitors (**Murata**) actually have a poor **ESR** (**order of Ohms**) => not adapted to high currents
2) It is better that **the AVDD of the SKIROC chips does not vary** during the power pulsing

⇒ two actions:

1) Put **enough lower-value capacitors** with very **good ESR (~ tens of mOhms)** to store the charge
2) AND add an **individual regulator** for producing each SKIROC's AVDD locally





Example of Discharge/Recharge Cycle for one SKIROC block:

- Current of 90 mA during 2.5 ms in 600 µF => ΔV ~ 0.4V
- Total FEV capacitance ~ 15 000 µF
- Reload current can be as low as 15 mA/ASU

There are already 4 slots for decoupling capacitors around the SKIROC chips. More can be added if required (space is available).

There is **no more effect of the variations of AVDD on the SKIROC chips**
The only constraint is to **keep AVDD > 3.5 V.**
The higher the capacitance, the lower the variations => look for the optimum (~1000 µF ?)…

Next steps

Software

- Software Next steps:
  - Temperature and AVDD monitoring
  - EUDAQ interfacing
  - C library …

Power/Pulsing and long SLAB:

- We can test the functionality of the power pulsing with one ASU with the current hardware, but AVDD will not be constant on the Skirocs…

- For a long SLAB, we are studying an evolution of the FEV12 with:
  - distributed low value capacitors on the FEV and individual regulators.
  - Improved distribution of the Clocks along the long Slab

Conclusion

- A lot of experience learned from and since last test beam in DESY (July 2019)
- Improvements realized on mechanics, electronics (hardware/firmware) and software
  - We designed and produced a new version of the **SL-Board → V2**
  - We developed the **SL_ADAPT** board in order to permit **interfacing** between the existing **FEV13** boards and the SL-Board.
- **The 15-Layer compact prototype is now ready**: commissioning in progress …
  - Next test beam scheduled 30 nov-6 Dec 2020 in DESY
- Studies have started on Power Pulsing mode/ Long Slab: need of a **new version of the FEVs**

Backup Slides

Reminder:
Constraints on Readout Electronics

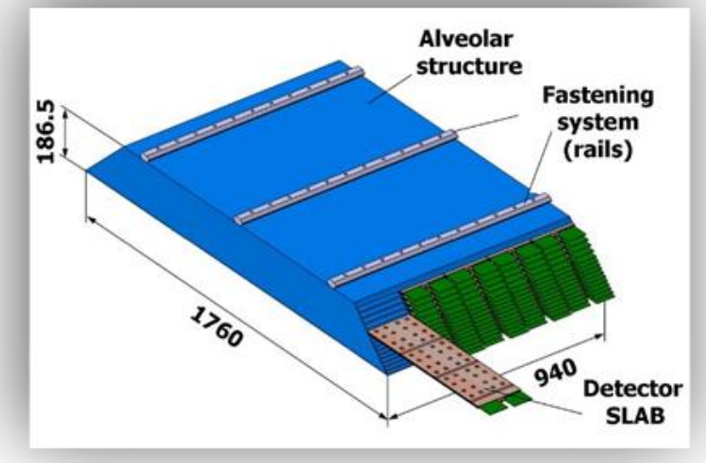
Spatial constraints for the Active Sensor Units (ASUs)

- Very limited space **between layers (depending on the total number of layers)**.

➢ Two protoype versions have been realized with different SKIROC packaging and thickness:

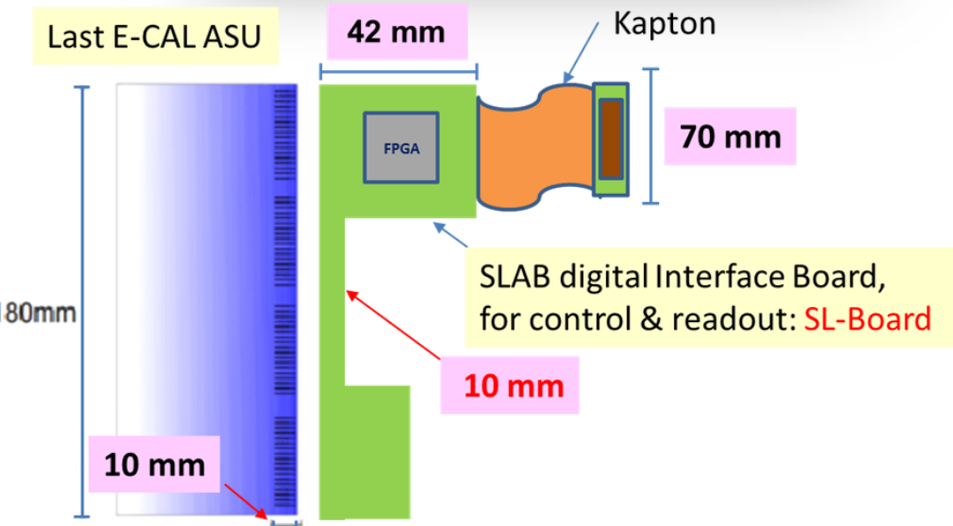
✓ BGA option : PCB + components*(1,2 mm)* + connectors = **~ 3,2 mm**

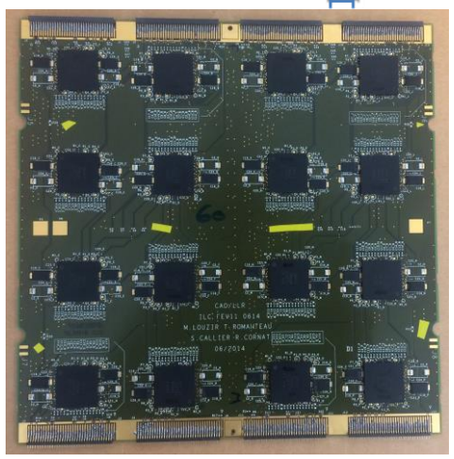
✓ COB (Chip On Board) option : PCB and ASICs **= 1,2 mm** + connectors = **~2,3 mm**



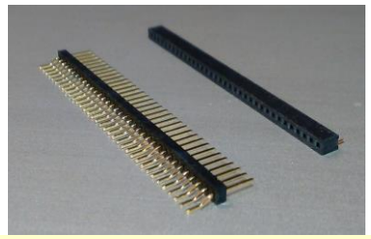
Constraints for the Slab Interface Board (SL-Board)

- The Sl-board will be installed between ECAL and HCAL, separated by only 67 mm
- L-shape because of the cooling system
- Maximum Height : **6 to 12 mm depending on the location**
- **Control & Readout electronics at the extremity of the Slab**
- Signal Integrity over a Slab : up to 15 interconnected ASUs
- Very low Power consumption (~ 150 mA/ Slab) : needs to run in **power pulsing mode**





ASU: FEV 11, with Skiroc BGA option, and the gradconn connectors



Gradconn connectors (1,5 mm high)